ECE2411: Logic Circuit II, Spring 2018

Lab6. Design and simulate a binary counter with overflow detection

Objective: Practice the modeling at behavioral level or high abstract level, and the handling of special condition such as overflow.

Write a behavioral model for a 16 bit binary up/down counter, with reset, parallel load and overflow detection. The overflow detection generate a single output bit that indicates overflow occurred by asserting 1 for one cycle. Write a testbench that can simulate and test the counter model in ModelSim. Show at least the following situations using waveform in the report. A) Counting up, until overflow occurred. B) Counting down, until overflow occurred. C) Reset the counter. D) Data loading and then counting. And discuss how you handles the long simulation of 2^{16} clock cycle needed until overflow.

Note, when modeling at behavioral level, the focal point is the functionality or the algorithm of the circuit. The details of the circuit implementation is no clearly spelled out, which can be done later or to be handled by the synthesize tools. Therefore the behavioral model is more abstract, for example, the key part of a counting up counter can simply be modeled as “C=C+1;” at behavioral level.