

Why and How to Use the Serial Peripheral Interface to Simplify Connections Between Multiple Devices

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Contributed By DigiKey's North American Editors

2019-02-14

Embedded systems use one or more processors or microcontrollers to execute specialized operations within a more complex system. These embedded controllers need to communicate with other system components, sensors, and even other controllers. While commonplace, complex serial interfaces and protocols can be overly difficult to program and troubleshoot, especially if the number of devices being communicated with is small.

Designers need microcontrollers, peripherals, and sensors with a simple device-to-device digital interface that can handle arbitrary length data at high speed and eliminate the complex protocol-related programming tasks.

The simple solution is to choose controllers with a serial peripheral interface (SPI), a solution to interfacing the controller to a few local peripheral ICs or sensors. It is a simple synchronous interface that uses hardware addressing and operates at a clock rate of up to 50 megahertz (MHz). The SPI does not use a complicated protocol requiring addressing and status checking. Instead, it is a basic interface for rapid data transfer without the programming overhead of a more sophisticated interface bus.

This article will cover the basics of the SPI interface including the many operating modes. It will then introduce microcontrollers and other devices that feature an SPI interface and show how to apply it.

What is SPI?

SPI was developed by Motorola (now part of NXP Semiconductors) around 1985. It is a synchronous serial interface intended for short distance, device to device communication. Since then, it has become a de facto standard employed by many semiconductor manufacturers, especially in microprocessors and microcontrollers.

The reason for SPI's popularity is its many advantages. The first is that it's a simple hardware addressed interface which offers complete flexibility for the number of bits transferred. It uses a master-slave model with a single master and can handle multiple slave devices using full duplex communications operating at clock speeds up to 50 MHz. It does not use a standard protocol and transfers only data packets, making it ideal for transferring long data streams.

SPI uses a maximum of four signal lines (Figure 1). The master device, usually a processor or controller, supplies and controls the clock (SCK) and chip select (CS) lines. Full multiplex operation is handled by the data lines Master Out Slave In (MOSI) and Master In Slave Out (MISO). In a simple single master, single slave configuration, the chip select line can be eliminated and the CS input to the slave forced to the enabled logical condition. If the slave device can only send data (half duplex communication), then the MOSI line can also be eliminated, reducing the signal count further. The data is clocked out by the clock signal in such a way that the data transfer resembles a shift register with one bit shifted out for each clock.

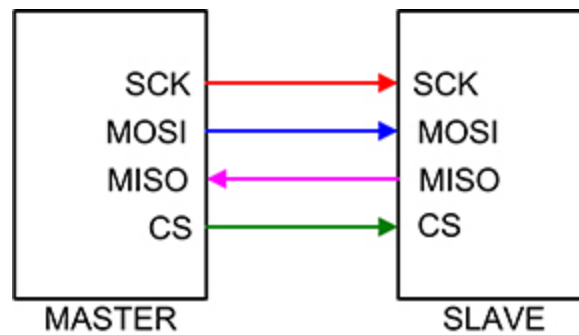


Figure 1: The basic SPI full duplex connection uses two data lines (MOSI, MISO), a clock line (SCK), and a chip select line (CS). MOSI on a slave is sometimes labelled slave data in (SDI). MISO may be labelled slave data out (SDO). (Image source: Digi-Key Electronics)

There are two approaches to handling multiple slave devices (Figure 2).

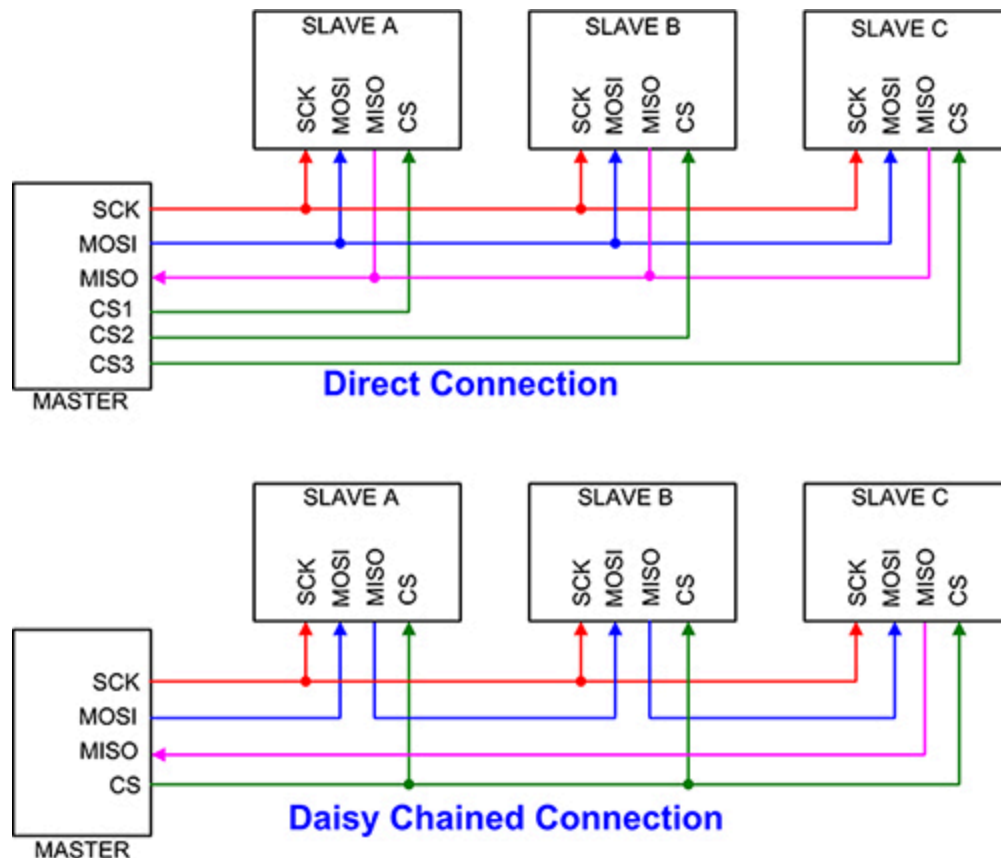


Figure 2: Two configurations for dealing with multi-slave interfacing. The direct connection requires a chip select for each slave. The daisy chained connection uses a single chip select and combines all the data on a single line. (Image source: Digi-Key Electronics)

The direct connection uses a chip select line for each slave device. Most microprocessors have three or four chip select lines. This limits the maximum number of slaves to the number of chip select lines. In most cases this is not a problem, but if a design requires more devices on the bus, some can be configured using the daisy chain approach. With a daisy chain, a common chip select is used for multiple slave devices and data is streamed out on a common data line. Again, using the model of the SPI slave devices as a shift register, the data from the slaves propagates in a serial multiplexed stream.

SPI clocking modes

The master controls and generates the clock. The two clock attributes are the clock polarity (CPOL) and clock phase (CPHA). These control the active clock edge where the slave device is clocked relative to the data. CPOL = 0 sets the clock to idle at logic 0. CPOL = 1 has the clock idling at logic 1. CPHA = 0 has the data clocked on leading edge, and CPHA = 1 has the data clocked on the trailing edge (Figure 3).

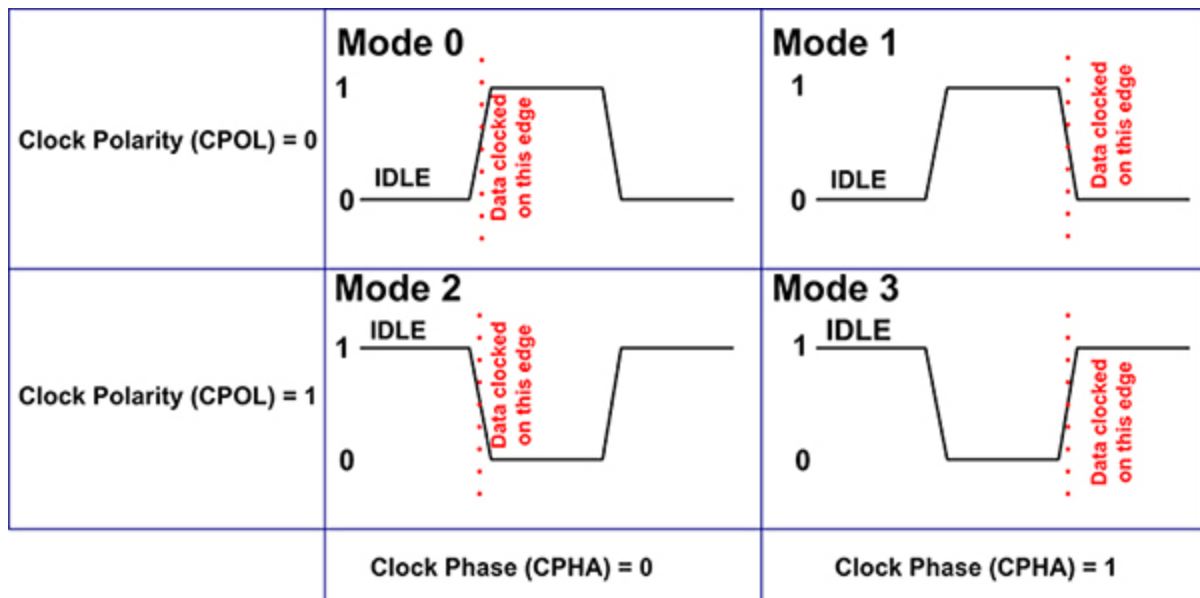


Figure 3: The SPI clocking mode selection fixes the active clock edge on which the data is sampled. (Image source: Digi-Key Electronics)

The settings of the CPOL and CPHA lines in the master determine the clock polarity and the active edge for clocking the data. Mode 1 is the most commonly used, but the other three modes are equally accessible to the designer.

The three signal components of an SPI transfer can be observed on an oscilloscope (Figure 4). In this example, eight-bit data packets are being transferred. [Teledyne LeCroy's HDO4104A](#) oscilloscope with its SPI serial decode option is used to observe the transfer.



Figure 4: Example of an SPI interchange as viewed on a Teledyne LeCroy HDO4104A oscilloscope with a serial decode option. The waveforms are as follows: the upper trace is the data line, the middle trace is the clock, and the bottom trace is the chip select. The blue overlay on the data trace shows the decoded content in hexadecimal. (Image source: Digi-Key Electronics)

The Mode 1 clock consists of groups of eight pulses with idle set to 0 (CPOL = 0), and data is clocked on the trailing or falling edge (CPHA = 1). The oscilloscope used in this example has a serial decode option which decodes the data content. The data content is read out in hexadecimal in the blue tinted overlay on the data trace. The decode is associated only with the data occurring while the chip select line is asserted (level 0). There are seventeen clock bursts in total, but only five of them correspond to active chip select states.

The table below the waveform display grids lists the active data content along with the time relative to the oscilloscope trigger for each packet and the measured clock rate, which is 100 kbits/s in this case. The number of clock cycles in each burst sets the number of data bits clocked out of the slave device.

Microprocessor I/O choices

The [Microchip Technology ATtiny816-MNR](#) is typical of many microcontrollers in that it supports multiple I/O interfaces (Figure 5). This particular controller uses the high-performance, low-power AVR® RISC architecture and can run at up to 20 MHz. It is supported by up to 4 or 8 Kbytes of flash, 256 or 512 bytes of SRAM and 128 bytes of EEPROM, all in a 20-pin package.

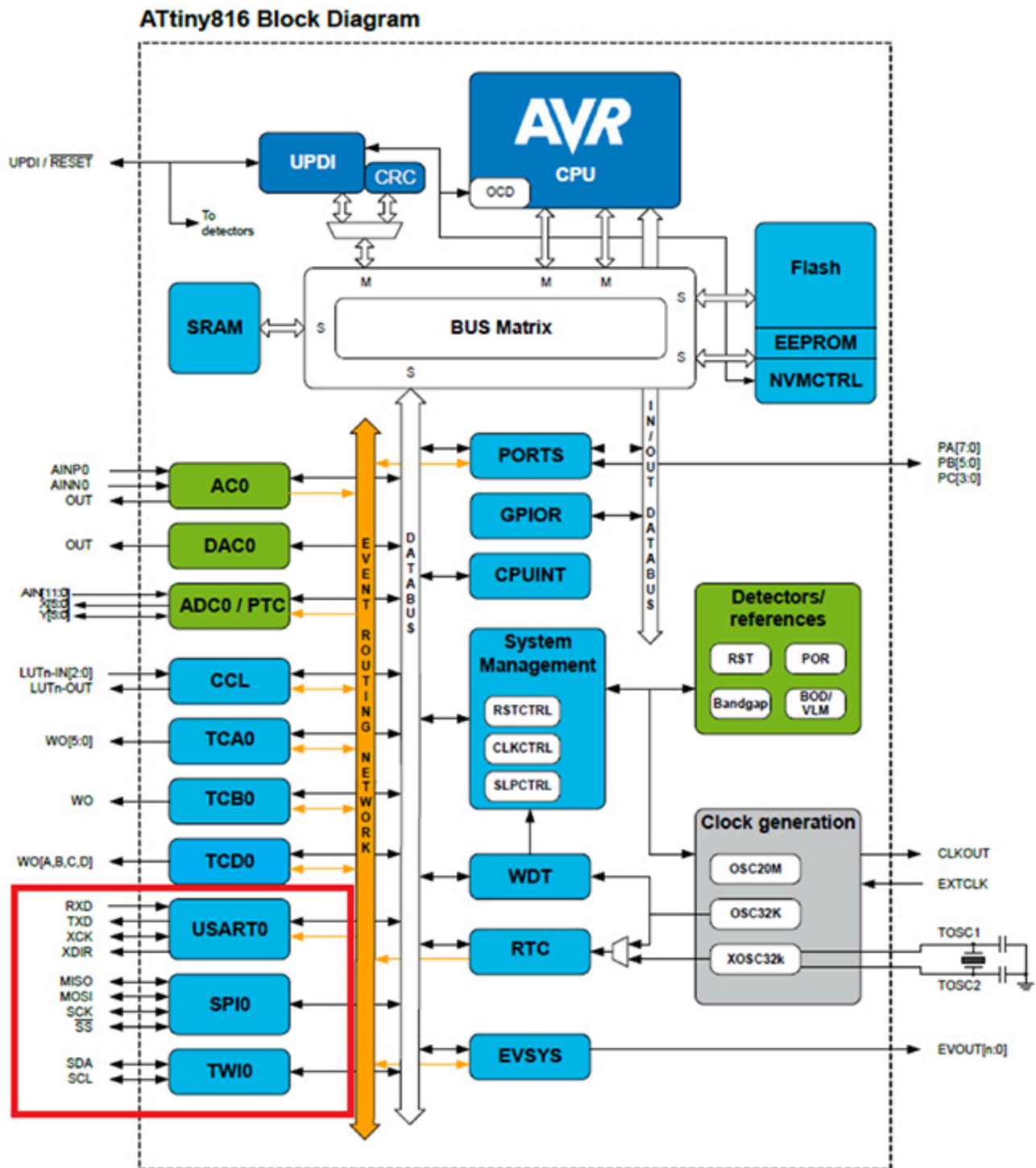


Figure 5: A block diagram of the Microchip Technology ATtiny816 microcontroller highlights the I/O ports. This controller includes both an SPI port as well as a USART port, the latter of which can be configured as a second SPI. (Image source: Microchip Technology)

On the interface side, the microcontroller includes a universal synchronous and asynchronous receiver transmitter (USART), an I²C compatible two-wire interface (TWI), and the SPI. The USART can be configured as a second SPI port.

The SPI allows full-duplex communication between an AVR device and peripheral devices or between several microcontrollers. The SPI peripheral can be configured as either master or slave, which enables the communication between microcontrollers.

SPI-based sensors

Complementing the large number of microprocessors and microcontrollers that incorporate SPI is a wide variety of sensors providing digital data via SPI. For example, Microchip Technology's [TC77-3.3MCTTR](#) digital temperature sensor is a serially accessible digital temperature sensor intended for small form factor, low-cost applications. The TC77 covers a temperature range of -55°C to +125°C. It runs off a 2.7 volt to 5.5 volt supply, draws 250 microamperes (μA) while in operation, and has an available low power shutdown mode that draws 1 μA .

In a typical application, the temperature sensor connects to the processor via a standard SPI connection. Its temperature data is formatted as a 13-bit digital word as shown in Figure 6.

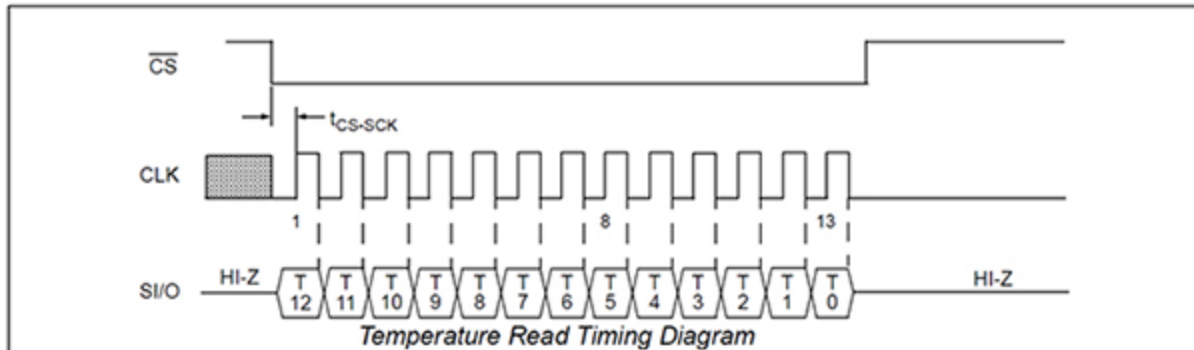


Figure 6: The TC77 from Microchip Technology is an easy to use temperature sensor that is both small and low-cost. It can be quickly connected to a controller or processor, transferring temperature readings as 13-bit digital words. As shown in the timing diagram, communication is initiated by asserting the CS line to a logic 0. (Image source: Microchip Technology)

The figure provides a timing diagram of a read operation of the T77's temperature register. Communication is initiated by asserting the CS line by bringing it to a logic 0. The sensor then transmits the first bit of data. The microcontroller reads the data in on the rising edge of SCK. The falling edge of SCK is then used to clock out the rest of the data from the sensor. This is a Mode 1 transfer like the previous example, but with a longer data word.

Extending SPI's reach

In addition to SPI's inclusion into many microprocessors and microcontrollers, several IC manufacturers have augmented the bus's functionality. A good example is Analog Devices' [LTC6820](#) isoSPI Isolated Communications Interface. This IC provides galvanic isolation between two SPI devices that communicate over a single twisted pair connection using differential signaling (Figure 7). This signaling mode extends the usable range of the LTC6820's SPI interface to up to 100 meters (m), albeit at a reduced clock rate from the nominal rate of 1 Mbit/s over a 10 m distance.

Microcontroller to SPI Slave Isolated Interface

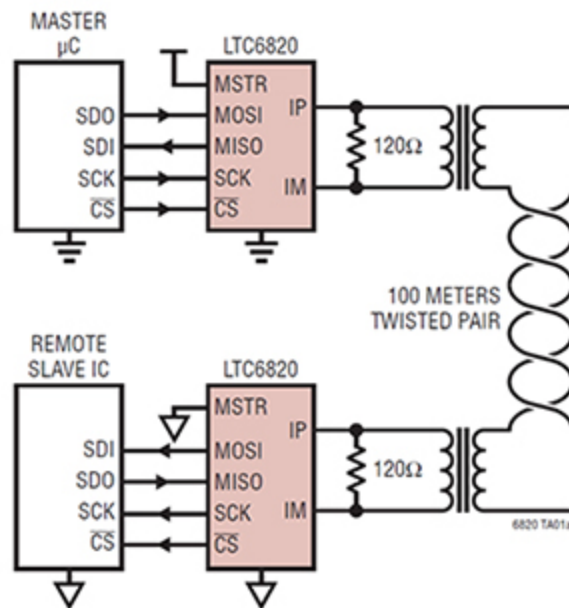


Figure 7: A pair of LTC6820 isolators provide galvanic isolation between two SPI devices. The IC supports data transfers at up to 1 Mbit/s at distances to 10 m, and at reduced clock rates for a distance up to 100 m. (Image source: Analog Devices)

Isolation is provided by pulse transformers, a technique often used in industrial networking applications and when reading remote sensors.

Conclusion

The SPI solves the need for a simple, low-cost, low overhead interface in applications where the source can be described as a data stream, as opposed to reading and writing data to address locations. This makes it ideal for handling device-to-device communications between microcontrollers and sensors, digitizers, digital signal processing devices, as well as other processors.

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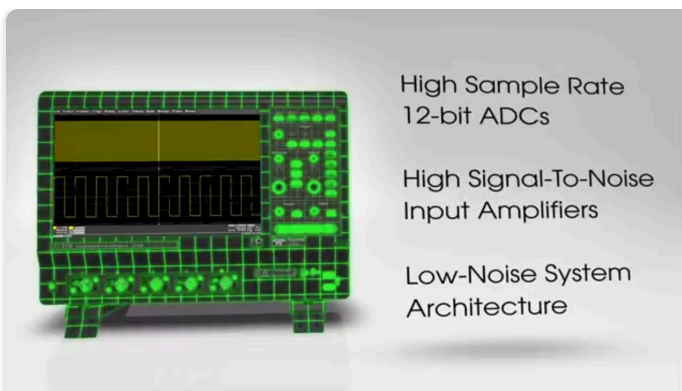
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Arthur (Art) Pini is a contributing author at DigiKey. He has a Bachelor of Electrical Engineering degree from City College of New York and a Master of Electrical Engineering degree from the City University of New York. He has over 50 years experience in electronics and has worked in key engineering and marketing roles at Teledyne LeCroy, Summation, Wavetek, and Nicolet Scientific. He has interests in measurement technology and extensive experience with oscilloscopes, spectrum analyzers, arbitrary waveform generators, digitizers, and power meters.

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