0.1 Arbejdsblad

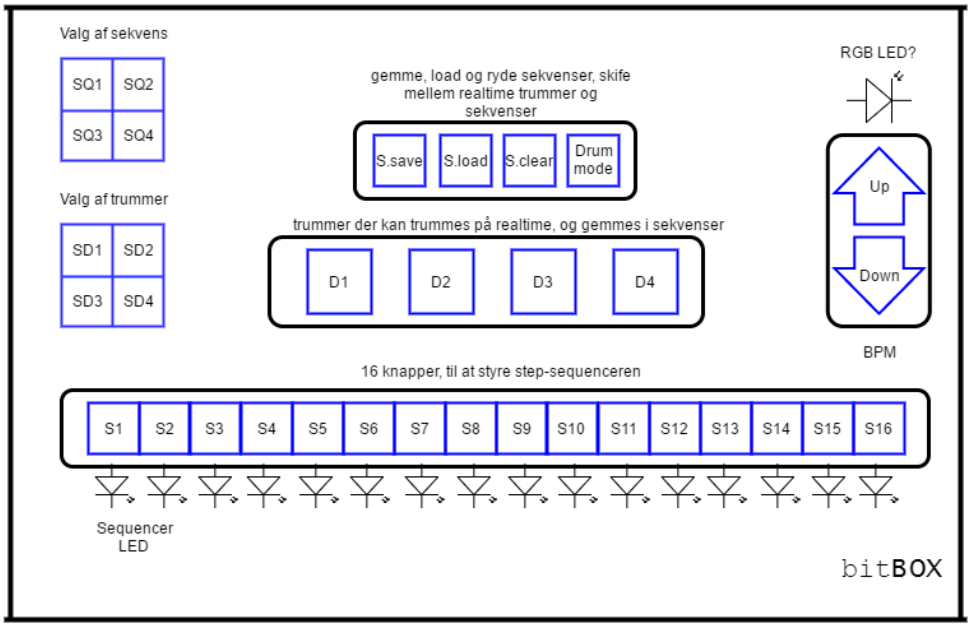
Hej Søren

Vi er så småt gået let og elegant over problemformulering/kravspec og vi vil gerne have respons på det.

Vi har fundet en DAC i skuffen kaldet TDA1541A, som vi prøver at finde hoved og hale på. Det kunne vi godt tænke os at høre lidt om. (databladet er vedlagt nederst i arbejdsbladet.

Derudover kunne vi også tænke os hjælp til implementering af .wav-filer i VHDL, og hvordan de afspilles.

Overvejelse vi skal gøre os når vi skal kommunikerer mellem ARV og FPGA. Samt hvordan information skal struktureres. I forhold til hvordan AVR og FPGA spiller sammen, se det umiddelbart ud til, at de dele pins. Kan man "blot"sætte AVR'en til at skrive information til en pin, som FPGA'en læser/reagerer"på.



Figur 0.1: umiddelbar ide til hvilke knapper der skal bruges til trumme maskinen

Indholdsfortegnelse

0.1 Arbejdsblad 1

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Problemformulering 1

1.1 Projektafgrænsning

En trommemaskine er et redskab der kan se ud på mange måder og der kan derfor tilføjes mange elementer, og endnu flere fordybelsesområder. Der foretages derfor en projektafgrænsning for at mindske projektet omfang, således at et realistisk mål for projektet kan opnåes.

På grund af projektets omfang og emne vil der ikke lægges stort fokus på at lave det hele "fra bunden". For at kunne fremstille en "spillende"demo samt at gøre det nemmere at fejlfinde og viderebygge projektet, vælges det at implementere projektet på konfigurerbar hardware, navnligt en FPGA som beskrevet i **??**.

I en trommemaskine vil det være nødtvendigt at omdanne digitale signaler til analoge hvilket kræver en D/A-konverter, men da projektets fokus ligger på groove og lækre rytmer vælges der at benytte en allerede eksisterende D/A-konverter.

Da der ikke opnås stor teoretisk indsigt i emnet ved at gøre det samme flere gange, vil projektet også begrænses i forhold til antallet af lydsamples og gembare sekvenser, i betragtning af hvad en reel gangbar trommemaskine bør have.

Istedet vil fokuset i første omgang? ligge på at fremstille de essentielle dele i en trommemaskine, såsom at gøre det muligt at programmere rytmer i en sequencer, lagre disse og afspille disse rytmer med trommesamples.

Programmeringen af sequenceren vælges at implementeres både som sampler og en step-sequencer. Der vælges at arbejde med en sampler da denne anses som en udfordrende opgave, da dette er et forholdsvist tidsfølsomt system.

Dertil vil der laves en stepsequencer da denne vil gøre det nemt at programmere en sekvens i sequenceren, og derved gøre det lettere at arbejde med trommemaskines resterende moduler.

Derudover vælges der at bruge allerede eksisterende lydsamples frem for at fremstille dem selv, grundet at de anvendte lyde ikke har stor indflydelse på resten af projektet. Der kunne i princippet benyttes lyde af hunde der gør, uden at noget betydelig effekt på resten af trommemaskinens funktioner.

flere ting følger efterhånden som vi finder på flere ting at lave

1.2 Problemformulering

På baggrund af analysen i kapitel **??** er det nu mulige at opstille en problemformulering til dette projekt.

I accidentely the whole drum machine. what do now??

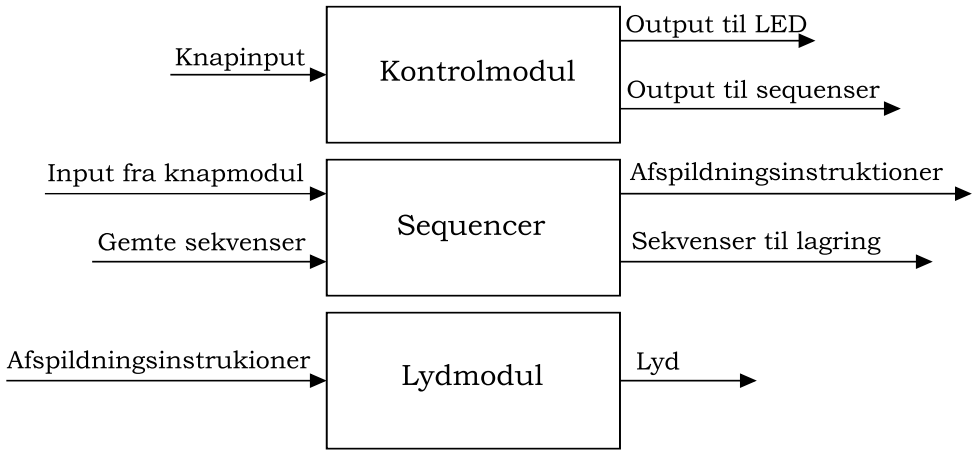
Kravspecifikation 2

2.1 Funktionelle krav

1. Skal gemme en rytme i en sequncer, med inputs fra en sampler og en step-sequencer
2. Skal have TBD forskellige kanaler at indspille til svarende til forskellige trommesamples.
3. Skal kunne afspille TBD samples på samme tid.
4. Indstille tempo mellem 50 BPM og 200 BPM.
5. Skal kunne gemme og genfinde sekvenser i hukommelse
6. skal kunne afspille sequencerens rytme som et audio-output

2.2 Krav til delmoduler

Ud fra de funktionelle krav, er funktionalliketerne blevet inddelt i tre overmoduler med hver deres inputs og outputs.



Figur 2.1: Flot modulting

2.2.1 Krav til Kontrolmodul

1. Skal tage imod brugerinput til:
   a) Indstilling af BPM
   b) Valg af trommesample
   c) Valg af, saving, loading og sletning af sekvenser
   d) Valg af samplingsmetode (step-sequencer eller fri sampling)
   e) Programmering af stepsequencer
   f) Tromning via sampler
2. Skal vise trommemaskinens status med en antal LED'er (hvordan step-sequenceren er programmeret, valg af trommesample, BPM og hvilket saveslot der benyttes)
3. Skal sende instrukser til hvad sequenceren skal gøre.

2.2.2 Krav til sequencer

1. Skal kunne blive programmet ved input fra kontrolmodulet
2. Indspillede trommeslag via sampler, skal ligge inden for 1 ms fra brugerens reelle taktslag.
3. Skal sende instrukser om hvilke lyde der skal afspilles og hvornår.
4. Skal kunne gemme og hente en sekvens fra et stykke hukommelse.
5. Skal kunne ændre den tid det tager at køre gennem en sekvens i henhold til indtastede BPM.

2.2.3 Krav til lydmodul

1. Skal kunne afspille trommesamples med en samplingfrekvens på 44,1 kHz i 16 bits opløsning.
2. Skal afspille op til 4 forskellige lydsamples samtidig.
3. Skal konvertere lyden fra et digitalt signal til et analogt outputsignal.

2.3 Beskrivelse af accepttest

if(spiller){return "fed... fyraften"} else {rubberDuckDebug(tålmodighed);}

Design 3

Der vil i dette kapitel blive beskrev hvordan trommemaskinen designes.

Philips Components

Data sheet	
status	Product specification
date of issue	February 1991

TDA1541A

Stereo high performance 16-bit DAC

FEATURES

- High sound quality
- High performance: low noise and distortion, wide dynamic range
- 4 x or 8 x oversampling possible
- Selectable two-channel input format
- TTL compatible inputs

GENERAL DESCRIPTION

The TDA1541A is a stereo 16-bit digital-to-analog converter (DAC). The ingenious design of the electronic circuit guarantees a high performance and superior sound quality. The TDA1541A is therefore extremely suitable for use in top-end high-fi digital audio equipment such as high quality Compact Disc players or digital amplifiers.

ORDERING INFORMATION

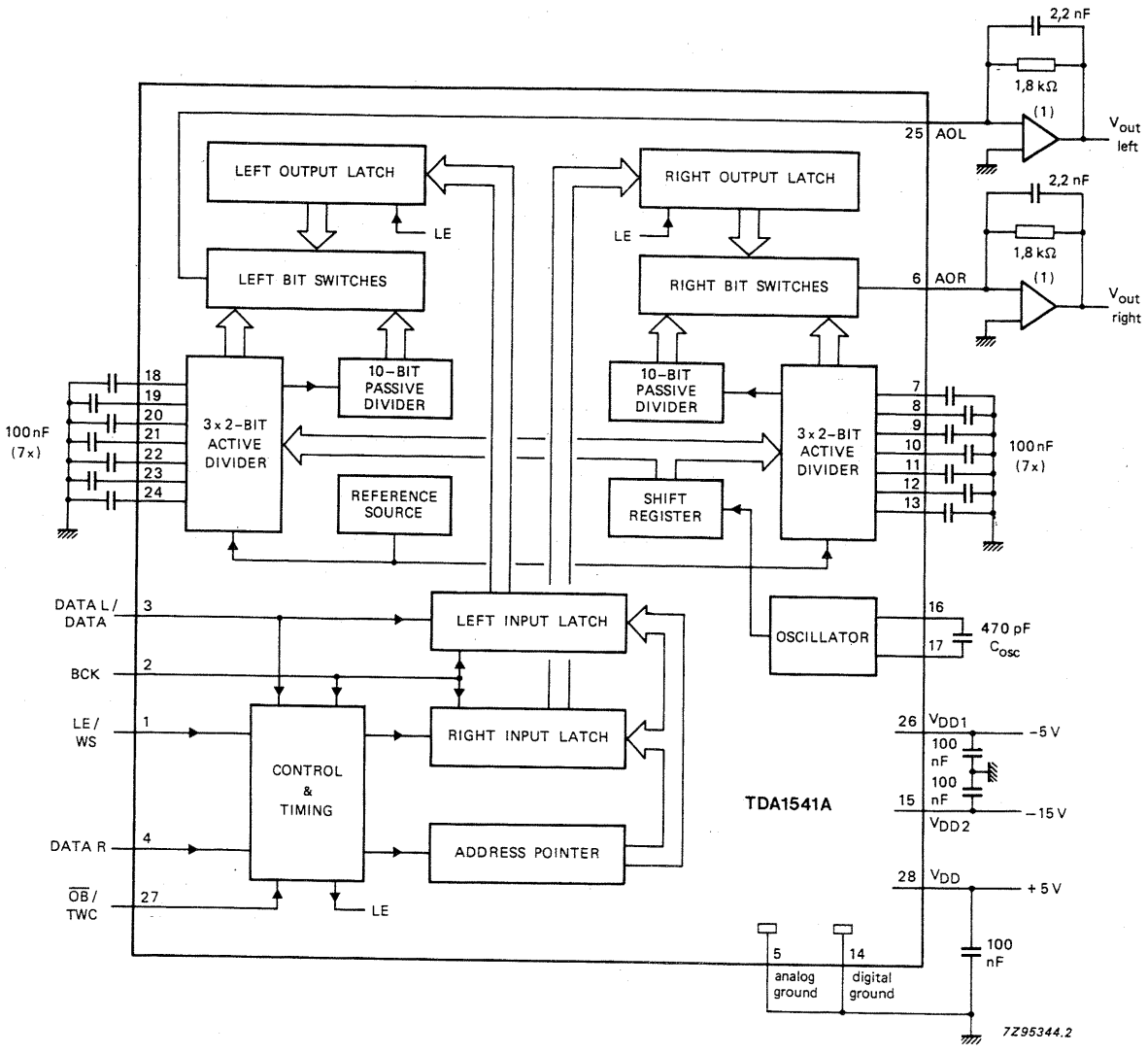
EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1541A	28	DIL	plastic	SOT117

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage; pin 28		4.5	5.0	5.5	V
$-V_{DD1}$	supply voltage; pin 26		4.5	5.0	5.5	V
$-V_{DD2}$	supply voltage; pin 15		14.0	15.0	16.0	V
I_{DD}	supply current; pin 28		-	27	40	mA
$-I_{DD1}$	supply current; pin 26		-	37	50	mA
$-I_{DD2}$	supply current; pin 15		-	25	35	mA
THD	total harmonic distortion	including noise at 0 dB	-	–95	–90	dB
			-	0.0018	0.0032	%
THD	total harmonic distortion	including noise at –60 dB	-	–42	-	dB
			-	0.79	-	%
NL	non-linearity	at T_{amb} = –20 to +85 °C	-	0.5	1.0	LSB
t_{cs}	current settling time to ±1 LSB		-	0.5	-	µs
BR	input bit rate at data input; (pin 3 and 4)		-	-	6.4	Mbits/s
f_{BCK}	clock frequency at clock input		-	-	6.4	MHz
TC_{FS}	full scale temperature coefficient	at analog outputs (AOL; AOR)	-	$\pm 200 \times 10^{-6}$	-	K^{-1}
T_{amb}	operating ambient temperature range		–40	-	+85	°C
P_{tot}	total power dissipation		-	700	-	mW

Stereo high performance 16-bit DAC

TDA1541A



(1) TDA1542
(2) 2 x NE5534 or equivalent

Fig.1 Block diagram.

Stereo high performance 16-bit DAC

TDA1541A

PINNING

SYMBOL	PIN	DESCRIPTION
LE/WS*	1	latch enable input / word select input
BCK*	2	bit clock input
DATA L /DATA*	3	data left channel input / data input (selected format)
DATA R*	4	data right channel input
GND(A)	5	analog ground
AOR	6	right channel output
DECOU	7 to 13	decoupling
GND (D)	14	digital ground
V_{DD2}	15	–15 V supply voltage
COSC	16,17	oscillator
DECOU	18 to 24	decoupling
AOL	25	left channel output
V_{DD1}	26	–5 V supply voltage
$\overline{OB}$/TWC*	27	mode select input
V_{DD}	28	+5 V supply voltage

* See Table 1 data selection input.

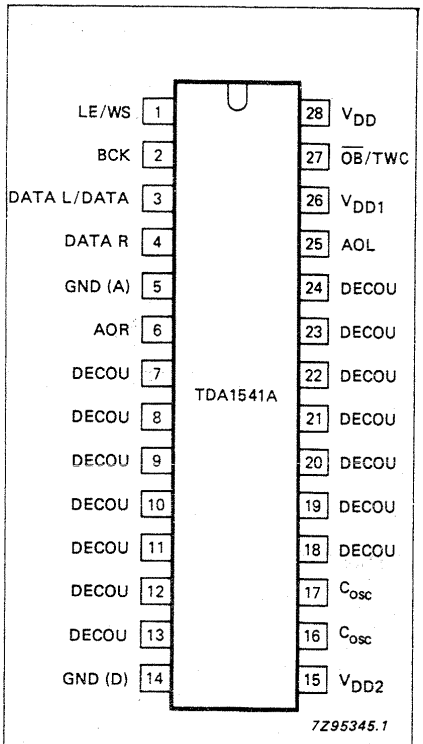


Fig.2 Pin configuration

FUNCTIONAL DESCRIPTION

The TDA1541A accepts input sample formats in time multiplexed mode or simultaneous mode up to 16-bit word length. The most significant bit (MSB) must always be first. This flexible input data format allows easy interfacing with signal processing chips such as interpolation filters, error correction circuits, pulse code modulation adaptors and audio signal processors (ASP).

The high maximum input bit-rate and fast settling facilitates application in 8 x oversampling systems (44.1 kHz to 352.8 kHz or 48 kHz to 384 kHz) with the associated simple analog filtering function (low order, linear phase filter).

Input data selection (see also Table 1)

With the input $\overline{OB}$/TWC connected to ground, data input (offset binary format) must be in time multiplexed mode. It is accompanied with a word select (WS) and a bit clock input (BCK) signal. The converted samples appear at the output, at the first positive going transition of the bit clock signal after a negative going transition of the word select signal.

With $\overline{OB}$/TWC connected to V_{DD} the mode is the same but the data format must be in the two's complement.

When input $\overline{OB}$/TWC input is connected to V_{DD1} the two channels of data (L/R) are input simultaneously via DATA L and DATA R, accompanied with BCK and a latch-enable input (LE). With this mode selected the data must be in offset binary. The converted samples appear at the output at the positive going transition of the latch enable signal.

The format of the data input signals is shown in fig.4 and 5.

True 16-bit performance is achieved by each channel using three 2-bit active dividers, operating on the dynamic element matching principle, in combination with a 10-bit passive current divider, based on emitter scaling. All digital inputs are TTL compatible.

Table 1 Input data selection

$\overline{OB}$/TWC	mode	pin 1	pin 2	pin 3	pin 4
−5 V	simultaneous	LE	BCK	DATA L	DATA R
0 V	time MUX OB	WS	BCK	DATA OB	not used
+5 V	time MUX TWC	WS	BCK	DATA TWC	not used

Where:

LE = latch enable
WS = word select, LOW = left channel; HIGH = right channel
BCK = bit clock
DATA L = data left
DATA R = data right
DATA OB = data offset binary
DATA TWC = data two's complement
MUX OB = mulitplexed offset binary
MUX TWC = multiplexed two's complement = I²S-format

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage; pin 28		0	7	V
$-V_{DD1}$	supply voltage; pin 26		0	7	V
$-V_{DD2}$	supply voltage; pin 15		0	17	V
T_{stg}	storage temperature range		−55	+150	°C
T_{amb}	operating ambient temperature range		−40	+85	°C
V_{es}	electrostatic handling*		−1000	+1000	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	30	K/W

Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

CHARACTERISTICS

V_{DD} = 5 V; $-V_{DD1}$ = 5 V; $-V_{DD2}$ = 15 V; T_{amb} = +25 °C; measured in the circuit of Fig.1; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage; pin 28		4.5	5.0	5.5	V
$-V_{DD1}$	supply voltage; pin 26		4.5	5.0	5.5	V
$-V_{DD2}$	supply voltage; pin 15		14.0	15.0	16.0	V
$V_{GND(A)}$ $-V_{GND(D)}$	voltage difference between analog and digital ground		−0.3	0	+0.3	V
I_{DD}	supply current; pin 28		-	27	40	mA
$-I_{DD1}$	supply current; pin 26		-	37	50	mA
$-I_{DD2}$	supply current; pin 15		-	25	35	mA
Inputs						
$-I_{IL}$	input current pins (1, 2, 3 and 4) digital inputs LOW	V_I = 0.8 V	-	-	0.4	mA
I_{IH}	digital inputs HIGH	V_I = 2.0 V	-	-	20	µA
$\lvert I_{\overline{OB}/TWC}\rvert$	Digital input currents (pin 27) +5 V		-	-	1	µA
$\lvert I_{\overline{OB}/TWC}\rvert$	0 V		-	-	20	µA
$\lvert I_{\overline{OB}/TWC}\rvert$	−5 V		-	-	40	µA
f_{BCK}	input frequency/bit rate clock input pin 2		-	-	6.4	MHz
BR	bit rate data input pin 3 and 4		-	-	6.4	Mbits/s
f_{WS}	word select input pin 2		-	-	200	kHz
f_{LE}	latch enable input 1		-	-	200	kHz
C_I	input capacitance of digital inputs		-	12	-	pF
Analog outputs (AOL; AOR; see note 1)						
Res	resolution		-	16	-	bits
I_{FS}	full scale current		3.4	4.0	4.6	mA
$\lvert I_{ZS}\rvert$	zero scale current		-	25	50	nA
T_{CFS}	full scale temperature coefficient	T_{amb} = −20 to +85 °C	-	±200 x 10^{-6}	-	K^{-1}
Analog outputs (V_{ref})						
E_L	integral linearity error	T_{amb} = 25 °C	-	0.5	1.0	LSB
E_L	integral linearity error	T_{amb} = −20 to +85°C	-	-	1.0	LSB
E_{dL}	differential linearity error	T_{amb} = 20°C, note 2	-	0.5	1.0	LSB
E_{dL}	differential linearity error	T_{amb} = −20 to +85°C	-	-	1.0	LSB
THD	total harmonic distortion	at 0 dB; note 3	−100	-	dB	
			-	0.0010	-	%
THD	total harmonic distortion	including noise at 0 dB;	-	−95	−90	dB
		note 3, Fig.3	-	0.0018	0.0032	%
THD	total harmonic distortion	including noise at −60 dB;	-	−42	-	dB
		note 3, Fig.3	-	0.79	-	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{cs}	settling time ±1 LSB		-	0.5	-	µs
α	channel separation		90	98	-	dB
$\lvert d_{IO} \rvert$	unbalance between outputs	note 4	-	< 0.1	0.3	dB
$\lvert t_d \rvert$	time delay between outputs		-	-	0.2	µs
SSVR	supply voltage ripple rejection	V_{DD} = +5 V; note 4	-	−76	-	dB
SSVR	supply voltage ripple rejection	V_{DD1} = −5 V; note 4	-	−84	-	dB
SSVR	supply voltage ripple rejection	V_{DD2} = −15 V; note 4	-	−58	-	dB
S/N	signal-to-noise ratio	at bipolar zero	-	110	-	dB
S/N	signal-to-noise ratio	at full scale	98	104	-	dB
Timing (Fig.4 and 5)						
t_r	rise time		-	-	32	ns
t_f	fall time		-	-	32	ns
t_{CY}	bit clock cycle time		156	-	-	ns
t_{HB}	bit clock HIGH time		46	-	-	ns
t_{LB}	bit clock LOW time		46	-	-	ns
t_{FBRL}	bit clock fall time to latch enable rise time		0	-	-	ns
t_{RBFL}	bit clock rise time to latch enable fall time		0	-	-	ns
$t_{SU;DAT}$	data set-up time		32	-	-	ns
$t_{HD;DAT}$	data hold time to bit clock		0	-	-	ns
$t_{HD;WS}$	word select hold time		0	-	-	ns
$t_{SU;WS}$	word select set-up time		32	-	-	ns

Notes to the characteristics

1. To ensure no performance losses, permitted output voltage compliance is ±25 mV maximum.

2. Selections have been made with respect to the maximum differential linearity error (E_{dL}):

   TDA1541A/N2 bit 1-16 $E_{dL} < 1$ LSB

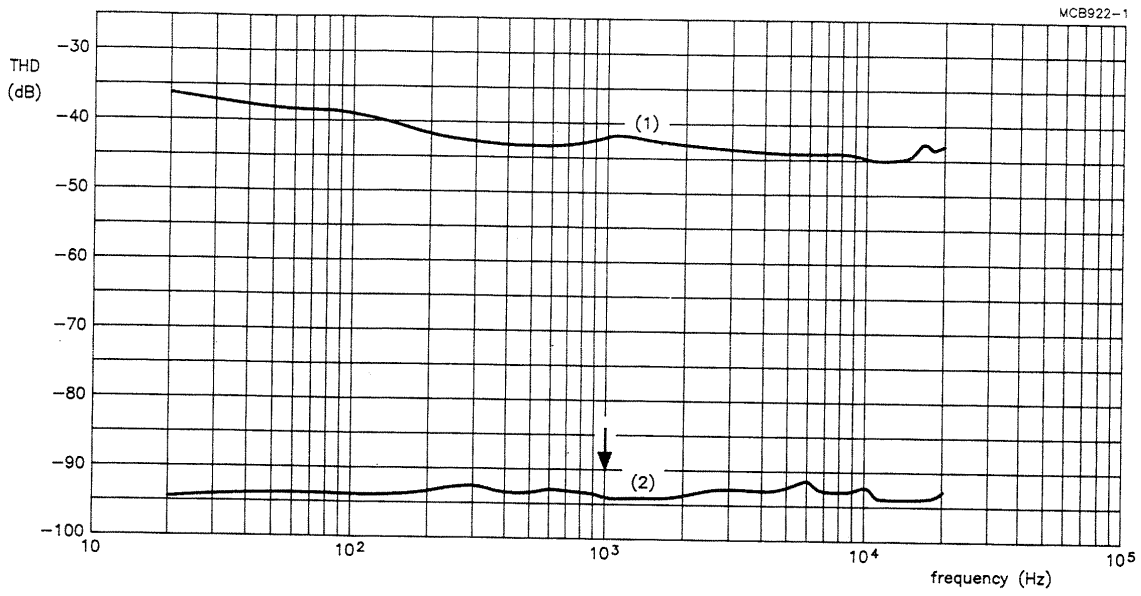
   TDA1541A/N2/R1 bit 1-16 $E_{dL} < 2$ LSB

   TDA1541A/N2/S1 bit 1-7 $E_{dL} < 0.5$ LSB
   bit 8-15 $E_{dL} < 1$ LSB
   bit 16 $E_{dL} < 0.75$ LSB

   The S1 version has been specially selected to achieve extremely good performance even for small signals.

3. Measured using a 1 kHz sinewave generated at a sampling rate of 176.4 kHz.

4. V_{ripple} = 100 mV and f_{ripple} = 100 Hz.

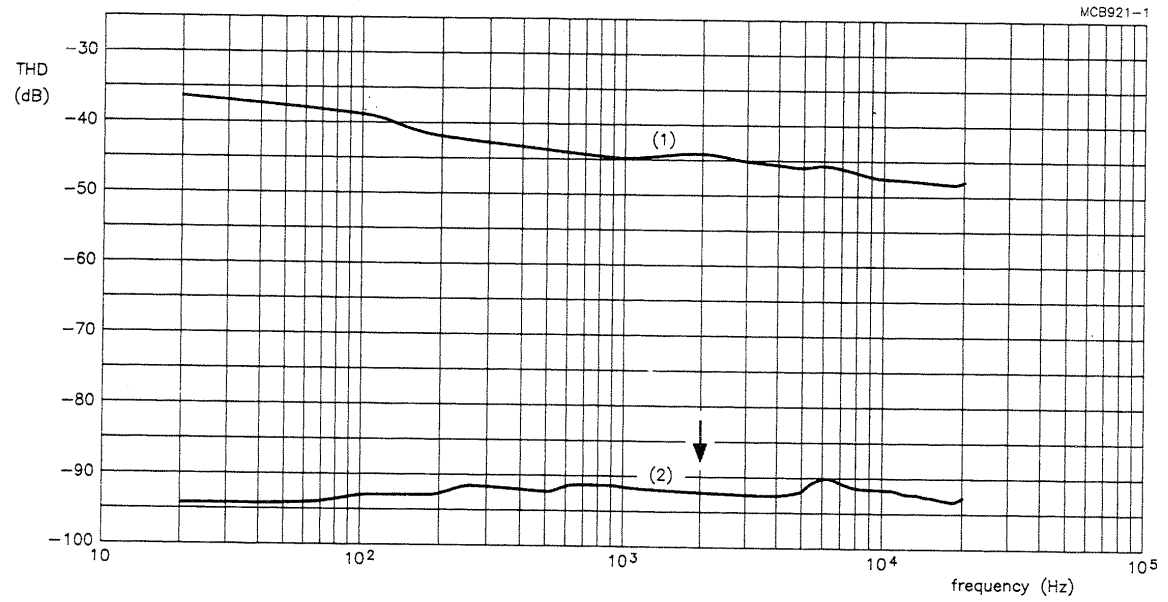


(1) Measured including all distortion plus noise at a signal level of −60 dB
(2) Measured including all distortion plus noise at a signal level of −0 dB

Fig.3a Distortion as a function of frequency (4FS)

Notes to Fig.3a

- The sample frequency 4FS: 176.4 kHz.
- Ref: 0 dB is the output level of a full scale digital sine wave stimulus.



(1) Measured including all distortion plus noise at a signal level of −60 dB
(2) Measured including all distortion plus noise at a signal level of −0 dB

Fig.3b Distortion as a function of frequency (8FS)

Notes to Fig.3b

- The sample frequency 8FS: 352.8 kHz.
- Ref: 0 dB is the output level of a full scale digital sine wave stimulus.

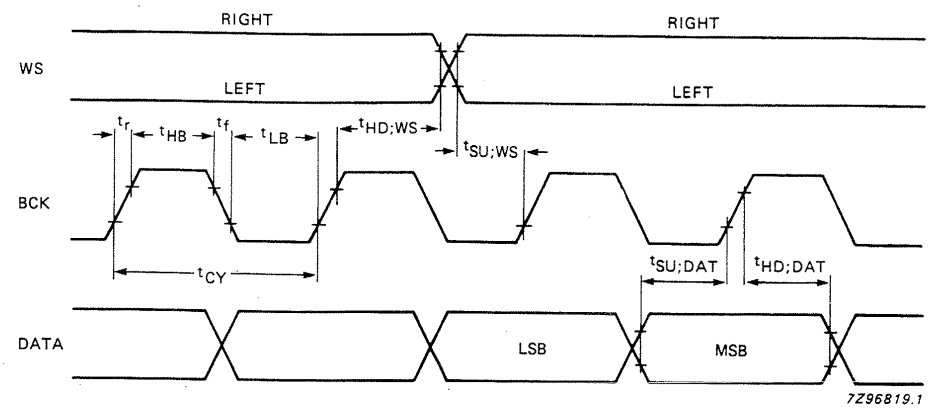


Fig.4 Format of input signals; time multiplexed (I^2S format).

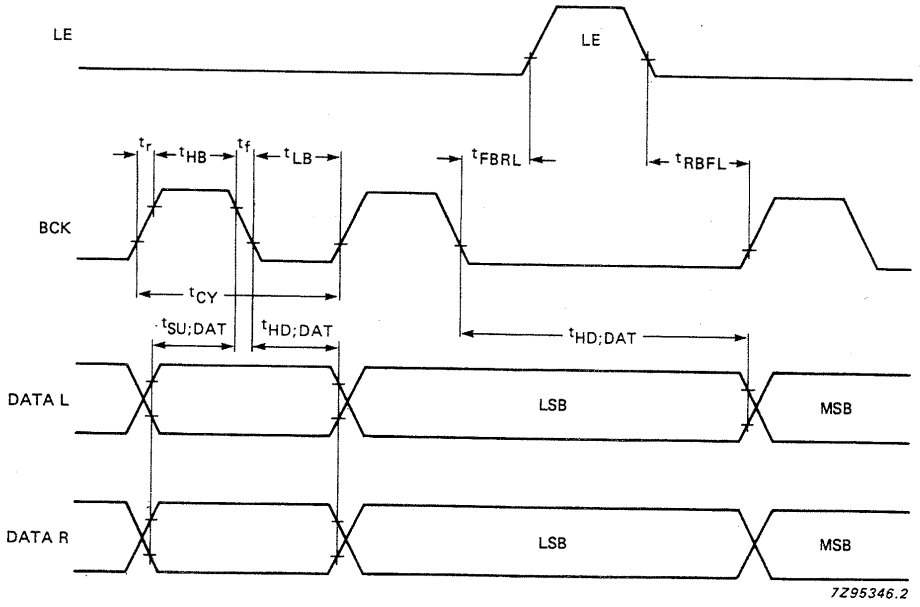


Fig.5 Format of input signals; simultaneous data.