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# This file is a general .ucf for Basys2 rev C board
# To use it in a project:
# - remove or comment the lines corresponding to unused pins
# - rename the used signals according to the project

# clock specs
NET "CLK1K" TNM_NET = CLK1K;
TIMESPEC TS_CLK1K   = PERIOD "CLK1K" TIG;

# clock pin for Basys2 Board
NET "mclk" LOC = "B8"; # Bank = 0, Signal name = MCLK
#NET "uclk" LOC = "M6"; # Bank = 2, Signal name = UCLK
NET "mclk" CLOCK_DEDICATED_ROUTE = FALSE;
#NET "uclk" CLOCK_DEDICATED_ROUTE = FALSE;

### Pin assignment for EppCtl
### Connected to Basys2 onBoard USB controller
##NET "EppAstb" LOC = "F2"; # Bank = 3
##NET "EppDstb" LOC = "F1"; # Bank = 3
##NET "EppWR"   LOC = "C2"; # Bank = 3
##NET "EppWait" LOC = "D2"; # Bank = 3
##NET "EppDB<0>" LOC = "N2"; # Bank = 2
##NET "EppDB<1>" LOC = "M2"; # Bank = 2
##NET "EppDB<2>" LOC = "M1"; # Bank = 3
##NET "EppDB<3>" LOC = "L1"; # Bank = 3
##NET "EppDB<4>" LOC = "L2"; # Bank = 3
##NET "EppDB<5>" LOC = "H2"; # Bank = 3
##NET "EppDB<6>" LOC = "H1"; # Bank = 3
##NET "EppDB<7>" LOC = "H3"; # Bank = 3


# Pin assignment for DispCtl
# Connected to Basys2 onBoard 7seg display
NET "seg<0>" LOC = "L14"; # Bank = 1, Signal name = CA
NET "seg<1>" LOC = "H12"; # Bank = 1, Signal name = CB
NET "seg<2>" LOC = "N14"; # Bank = 1, Signal name = CC
NET "seg<3>" LOC = "N11"; # Bank = 2, Signal name = CD
NET "seg<4>" LOC = "P12"; # Bank = 2, Signal name = CE
NET "seg<5>" LOC = "L13"; # Bank = 1, Signal name = CF
NET "seg<6>" LOC = "M12"; # Bank = 1, Signal name = CG
NET "seg<7>" LOC = "N13"; # Bank = 1, Signal name = DP

NET "an<3>" LOC = "K14"; # Bank = 1, Signal name = AN3
NET "an<2>" LOC = "M13"; # Bank = 1, Signal name = AN2
NET "an<1>" LOC = "J12"; # Bank = 1, Signal name = AN1
NET "an<0>" LOC = "F12"; # Bank = 1, Signal name = AN0

# Pin assignment for LEDs
NET "led<7>" LOC = "G1" ; # Bank = 3, Signal name = LD7
NET "led<6>" LOC = "P4" ; # Bank = 2, Signal name = LD6
NET "led<5>" LOC = "N4" ;  # Bank = 2, Signal name = LD5
NET "led<4>" LOC = "N5" ;  # Bank = 2, Signal name = LD4
NET "led<3>" LOC = "P6" ; # Bank = 2, Signal name = LD3
NET "led<2>" LOC = "P7" ; # Bank = 3, Signal name = LD2
NET "led<1>" LOC = "M11" ; # Bank = 2, Signal name = LD1
NET "led<0>" LOC = "M5" ;  # Bank = 2, Signal name = LD0

# Pin assignment for SWs
NET "sw<7>" LOC = "N3";  # Bank = 2, Signal name = SW7
NET "sw<6>" LOC = "E2";  # Bank = 3, Signal name = SW6
NET "sw<5>" LOC = "F3";  # Bank = 3, Signal name = SW5
NET "sw<4>" LOC = "G3";  # Bank = 3, Signal name = SW4
NET "sw<3>" LOC = "B4";  # Bank = 3, Signal name = SW3
NET "sw<2>" LOC = "K3";  # Bank = 3, Signal name = SW2
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NET "sw<1>" LOC = "L3";  # Bank = 3, Signal name = SW1
NET "sw<0>" LOC = "P11";  # Bank = 2, Signal name = SW0

NET "btn<3>" LOC = "A7";  # Bank = 1, Signal name = BTN3
NET "btn<2>" LOC = "M4";  # Bank = 0, Signal name = BTN2
NET "btn<1>" LOC = "C11"; # Bank = 2, Signal name = BTN1
NET "btn<0>" LOC = "G12"; # Bank = 0, Signal name = BTN0

### Loop back/demo signals
### Pin assignment for PS2
##NET "PS2C"    LOC = "B1"   | DRIVE = 2  | PULLUP ; # Bank = 3, Signal name = PS2C
##NET "PS2D"    LOC = "C3"   | DRIVE = 2  | PULLUP ; # Bank = 3, Signal name = PS2D

### Pin assignment for VGA
##NET "HSYNC"   LOC = "J14"  | DRIVE = 2  | PULLUP ; # Bank = 1, Signal name = HSYNC
##NET "VSYNC"   LOC = "K13"  | DRIVE = 2  | PULLUP ; # Bank = 1, Signal name = VSYNC

#NET "OutRed<2>"   LOC = "F13"  | DRIVE = 2  | PULLUP ; # Bank = 1, Signal name = RED2
#NET "OutRed<1>"   LOC = "D13"  | DRIVE = 2  | PULLUP ; # Bank = 1, Signal name = RED1
#NET "OutRed<0>"   LOC = "C14"  | DRIVE = 2  | PULLUP ; # Bank = 1, Signal name = RED0
#NET "OutGreen<2>" LOC = "G14"  | DRIVE = 2  | PULLUP ; # Bank = 1, Signal name = GRN2
#NET "OutGreen<1>" LOC = "G13"  | DRIVE = 2  | PULLUP ; # Bank = 1, Signal name = GRN1
#NET "OutGreen<0>" LOC = "F14"  | DRIVE = 2  | PULLUP ; # Bank = 1, Signal name = GRN0
#NET "OutBlue<2>"  LOC = "J13"  | DRIVE = 2  | PULLUP ; # Bank = 1, Signal name = BLU2
#NET "OutBlue<1>"  LOC = "H13"  | DRIVE = 2  | PULLUP ; # Bank = 1, Signal name = BLU1

# Loop Back only tested signals
NET "JA<0>" LOC = "B2"  | DRIVE = 2 ; # Bank = 1, Signal name = JA1
NET "JA<1>" LOC = "A3"  | DRIVE = 2 ; # Bank = 1, Signal name = JA2
NET "JA<2>" LOC = "J3"  | DRIVE = 2 ; # Bank = 1, Signal name = JA3
NET "JA<3>" LOC = "B5"  | DRIVE = 2 ; # Bank = 1, Signal name = JA4
NET "JA<1>" CLOCK_DEDICATED_ROUTE = FALSE;

#NET "JB<0>" LOC = "C6"  | DRIVE = 2 ; # Bank = 1, Signal name = JB1
#NET "JB<1>" LOC = "B6"  | DRIVE = 2 ; # Bank = 1, Signal name = JB2
#NET "JB<2>" LOC = "C5"  | DRIVE = 2 ; # Bank = 1, Signal name = JB3
#NET "JB<3>" LOC = "B7"  | DRIVE = 2 ; # Bank = 1, Signal name = JB4

#NET "JC<0>" LOC = "A9"  | DRIVE = 2 ; # Bank = 1, Signal name = JC1
#NET "JC<1>" LOC = "B9"  | DRIVE = 2 ; # Bank = 1, Signal name = JC2
#NET "JC<2>" LOC = "A10" | DRIVE = 2 ; # Bank = 1, Signal name = JC3
#NET "JC<3>" LOC = "C9"  | DRIVE = 2 ; # Bank = 1, Signal name = JC4

NET "JD<0>" LOC = "C12"  | DRIVE = 2 ; # Bank = 1, Signal name = JD1
NET "JD<1>" LOC = "A13"  | DRIVE = 2 ; # Bank = 2, Signal name = JD2
NET "JD<2>" LOC = "C13"  | DRIVE = 2 ; # Bank = 1, Signal name = JD3
NET "JD<3>" LOC = "D12"  | DRIVE = 2 ; # Bank = 2, Signal name = JD4
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