Client/Company/Organization: Signal and Systems Undergraduate Faculty/ ECpE/ ETG

Submitter Name: Matthew Post   **Email:** mpost7@iastate.edu

Project Contact: **Email:**

Project Title:

CyDAQ 2.0

Project Abstract:

Did you take EE 224 at ISU? Can you name every lab experiment? Can you name any of the lab experiments? I bet if you can, the ones you remembered involved a real world situation or hardware, not pure Matlab and fake signals. Well now is your chance to impact the future of 224!

This project will deliver a data acquisition device capable of capturing, filtering, and recreating signals for EE 224/324 lab experiments. It will also need to interface with the lab computers and an on board microcontroller.

In addition to delivering a market-ready device, the group will be expected to work with the Teaching Faculty on integrating it into existing lab experiments and developing brand new ones that bring the real world into ECpE labs. We will also increase the visibility of Iowa State Engineering by making our lab exercises available as Open Educational Resources (OER) through ISU Digital Press. This will include design documents for the CyDAQ boards. Imagine if engineering students all over the country, or even the world, were using equipment designed by you for their EE labs. This is the perfect design project for EE's and CPRE's that want to work with hardware, enjoy UI programming, and want to leave a lasting impact in our curriculum. The best part of this project is most of the work is already done – you get the fun part of putting everything together!

This project is a continuation of group sdmay18-31 and work done by ETG. The previous group created a working user interface in Python that allowed users to select their signal path (filtering), sampling rate, and desired output. This is fully functional but could use some TLC by a great UI programmer.

Over the course of last year ETG worked on redesigning the hardware aspect of this project and successfully created a filter board using multiplexers and digital potentiometers. However, to achieve the proper filter responses, a different potentiometer was chosen so the entire firmware portion of this project needs to be re-worked. Calling I2C programmers!

We would like to also expand functionality beyond EE 224, so we need EE's to help close the feedback loop. This will require finding, testing, and implementing an analog-to-digital converter that can handle the increased sampling rates and a digital-to-analog converter that can re-create the captured/filtered signal. Both will require an on-board clock generator to sync the system up and a revision of the PCB which was originally done in EAGLE.

Most of the project will be spent testing and integrating all these pieces into a final, fully working device. Have you been asked about your system level design experience in an interview? Well you won't need to worry about that again after this project.

Finally the group will work with faculty to create some real-world lab experiments that will bring various devices and sensors into students' hands and utilize the power of our new hardware platform.

Expected Deliverables:

- Front_end GUI. Minimum - Capable of allowing user to select signal path, sampling rate, and desired output (Matlab/Excel). Should be simple and intuitive to use. Must work on ECpE lab computers as a standard user.
- Firmware C – Code. Currently uses RTOS and written in C. Minimum – Takes in commands from the GUI and routes the signal as desired by the user. Also needs to control the clock generator that will allow for adjusting the sampling rates. Needs to handle all foreseen error cases and avoid any collisions.

- Hardware PCB. Currently has 7 on-board filters designed and simulated in PSPICE. Confirmed to meet design specifications by manually changing resistor values. Has not been tested using the programmable potentiometers. Minimum – Filters meet current design specifications with the potentiometers. PCB will be revised to add an A/D and D/A with clock generator. Possible filter improvements or functionality (adjusting resonance, overshoot, etc…) time permitting.

- Labs. Currently the Tuning Fork lab has been redesigned to use the CyDAQ but no other labs have been implemented. Minimum – design two additional lab assignments making use of the CyDAQ, including identification of any necessary (and affordable) sensors.

- Documentation. Currently there is a GIT repo for the previous design project. Minimum – A similar repo is to be used for this project. Code is expected to be commented to DOXYGEN standards. A user manual for each portion of the project is to be created for future work. All required SR Design documentation too.

Specialized Resources Provided by Client:

You'll be advised Dr. Julie Dickerson and Dr. Andrew Bolstad. Also ETG will be providing Engineering and Design support throughout the course of this project. You'll also be granted access to all the previous group's work.

Anticipated Cost: _____   **Financial Resources Provided by Client:** _____

Preferred Students for the Project:

- ☑ Electrical Engineering
- ☑ Computer Engineering
- ☐ Software Engineering
- ☐ Cyber Security Engineering
- ☐ Other:

Other Special Skills: Passionate about making Signals and Systems labs fun, informative, and meaningful for future students.

Anticipated Client Interaction (estimate):

- ☑ 1 meeting per week
  - ☑ In person, ☐ Over the phone, ☐ Web / video conferencing
- ☐ 1 meeting per month
  - ☐ In person, ☐ Over the phone, ☐ Web / video conferencing
- ☐ 2 or more meetings per month
  - ☐ In person, ☐ Over the phone, ☐ Web / video conferencing
- ☐ 1 meeting per semester
  - ☐ In person, ☐ Over the phone, ☐ Web / video conferencing

Meeting ABET Criteria

Please rate the following statements as they relate to your proposed project:

0 – Not at all	1 – A Little	2 – Somewhat	3 – A Lot	4 – Completely

	0	1	2	3	4
On this project, students will need to apply knowledge of mathematics, science, and engineering	☐	☐	☐	☐	☑
This project gives students an opportunity to design a system,	☐	☐	☐	☐	☑

component, or process to meet desired needs within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability

This project involves students from a variety of programs, i.e., CprE, EE, and SE	☐ 0	☐ 1	☐ 2	☐ 3	☑ 4
This project requires students to identify, formulate, and solve engineering problems	☐ 0	☐ 1	☐ 2	☐ 3	☑ 4
This project gives students an opportunity to use the techniques, skills, and modern engineering tools necessary for engineering practice	☐ 0	☐ 1	☐ 2	☐ 3	☑ 4

Project Approval – *for use by ECpE Senior Design Committee*

☐ Approved: _____

☐ Project Assigned: _____

☐ Advisor(s) Assigned: _____

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