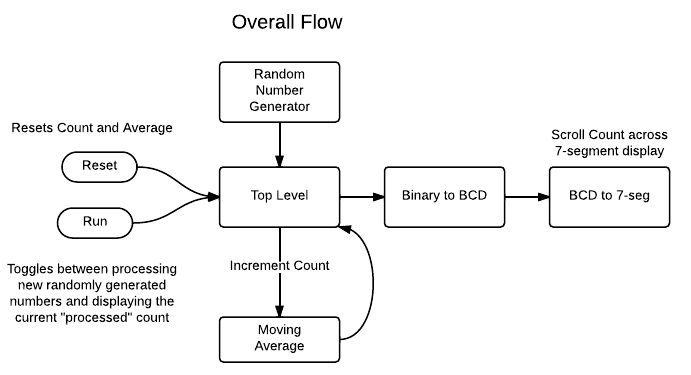
**Embedded Systems Project 4:**

**Traffic Light Controller**

We chose to do behavior model due to the fact that space was not a concern but time to complete each task is an issue. The general description of the system is a Finite Impulse Response Filter which calculates the average of the previous three inputs. Inputs are in the form of 8 bit 2’s compliment binary numbers, and are internally generated by a random number generator. The numbers are generated using a Linear Feedback Shift Register (LFSR). A large set of polynomials are used to act as feedback tap locations and are XOR’ed with the output of the original LFSR. The average is output on the LEDS, but will cycle faster than the user can actually view the result. The output will be meaningless for the first two cycles, until the “pipeline” is full. The pipeline is a simple technique for only doing one multiplication each cycle. Each time a new value comes in, it is multiplied by a binary approximation of 1/3 (000.10101). Then this result is stored in an internal register in the top level. Each time a new number is brought in and multiplied, it can then simply be added to the previous 2 multiplication results. In this way each cycle can produce output with only one multiplication.



**Testing Strategy**

The testing strategy was largely “design for test” as the tests were written independent of the designer prior to design. Each module was tested with smaller test benches. Moving average was tested with a known set of inputs to ensure functionality. The random number generator was tested for randomness. The top level module was tested to ensure state changes occur correctly.

**Interesting Design Choices**

We chose to implement a “run” key to toggle state of the device between the “processing state” and the “displaying results” state. Then with the addition of a “reset” key to set the count and average back to ‘0’, we can successfully momentarily pause the system to see the output without losing the count or the average.

The LFSR with polynomial taps was chosen because it represents a somewhat lightweight module, compared to some other more random methods.

The choice was made to scroll the inputs across the four 7-segment displays in slices of four bits each. This was chosen to make reading the output more logical, but perhaps could have benefited from a more sophisticated technique.

**Team Member Contributions**

|  |  |  |
| --- | --- | --- |
| **Name** | **Contributions** | **Modules** |
| Tom Dickman | Moving Average,  Debugging | Moving\_average.v |
| Joe Lovelace | Test benches, Final Report,  Debugging | Top\_level\_tb.v, moving\_average\_tb.v, |
| Andrew Steller | Output to 7 Segment,  Debugging | BCD\_2\_7Seg.v,  BCDconverter.v, |
| Ben Zerhusen | Random Number Generator, Debugging | Lfsr.v |

**PowerPlay Power Analysis:**

PowerPlay Power Analyzer Status            Successful - Fri Oct 12 15:01:19 2012

Quartus II 32-bit Version               12.0 Build 178 05/31/2012 SJ Web Edition

Revision Name  Project2

Top-level Entity Name   top\_level

Family   Cyclone II

Device  EP2C20F484C7

Power Models  Final

Total Thermal Power Dissipation               71.08 mW

Core Dynamic Thermal Power Dissipation             0.00 mW

Core Static Thermal Power Dissipation   47.36 mW

I/O Thermal Power Dissipation  23.72 mW

**Fitter Resource Usage Summary:**

 Total logic elements            984 / 18,752 ( 5 % )

-- Combinational with no register        809

-- Register only     19

-- Combinational with a register          156

Logic element usage by number of LUT inputs

-- 4 input functions                810

-- 3 input functions                52

-- <=2 input functions            103

-- Register only     19

Logic elements by mode

-- normal mode      858

-- arithmetic mode 107

Total registers\*      175 / 19,649 ( < 1 % )

-- Dedicated logic registers 175 / 18,752 ( < 1 % )

-- I/O registers       0 / 897 ( 0 % )

Total LABs:  partially or completely used           70 / 1,172 ( 6 % )

User inserted logic elements               0

Virtual pins             0

I/O pins  39 / 315 ( 12 % )

-- Clock pins          1 / 8 ( 13 % )

Global signals       3

M4Ks       0 / 52 ( 0 % )

Total block memory bits       0 / 239,616 ( 0 % )

Total block memory implementation bits            0 / 239,616 ( 0 % )

Embedded Multiplier 9-bit elements    0 / 52 ( 0 % )

PLLs        0 / 4 ( 0 % )

Global clocks        3 / 16 ( 19 % )

JTAGs    0 / 1 ( 0 % )

ASMI blocks           0 / 1 ( 0 % )

CRC blocks            0 / 1 ( 0 % )

Average interconnect usage (total/H/V)              1% / 1% / 1%

Peak interconnect usage (total/H/V)    6% / 6% / 6%

Maximum fan-out node         CLOCK\_50~clkctrl

Maximum fan-out   107

Highest non-global fan-out signal      enable

Highest non-global fan-out  97

Total fan-out          4156

Average fan-out     3.47