| Cycle | Instruction Retired (WB) | Reason to stall              |
|-------|--------------------------|------------------------------|
| 1     | empty                    | n/a                          |
| 2     | empty                    | n/a                          |
| 3     | empty                    | n/a                          |
| 4     | empty                    | n/a                          |
| 5     | lbi r0, 0                | n/a                          |
| 6     | lbi r5, 0                | n/a                          |
| 7     | lbi r6, 43               | n/a                          |
| 8     | lbi r7, 43               | n/a                          |
| 9     | ld r1, r0, 0             | n/a                          |
| 10    | NOP                      | RAW in r1 between I5 and I6  |
| 11    | NOP                      | RAW in r1 between I5 and I6  |
| 12    | NOP                      | RAW in r1 between I5 and I6  |
| 13    | st r5, r1, 0             | n/a                          |
| 14    | ld r1, r0, 2             | n/a                          |
| 15    | NOP                      | RAW in r1 between I7 and I8  |
| 16    | NOP                      | RAW in r1 between I7 and I8  |
| 17    | NOP                      | RAW in r1 between I7 and I8  |
| 18    | st r6, r1, 1             | n/a                          |
| 19    | ld r1, r0, 4             | n/a                          |
| 20    | NOP                      | RAW in r1 between I9 and I10 |
| 21    | NOP                      | RAW in r1 between I9 and I10 |
| 22    | NOP                      | RAW in r1 between I9 and I10 |
| 23    | st r7, r1, 1             | n/a                          |
| 24    | halt                     | n/a                          |