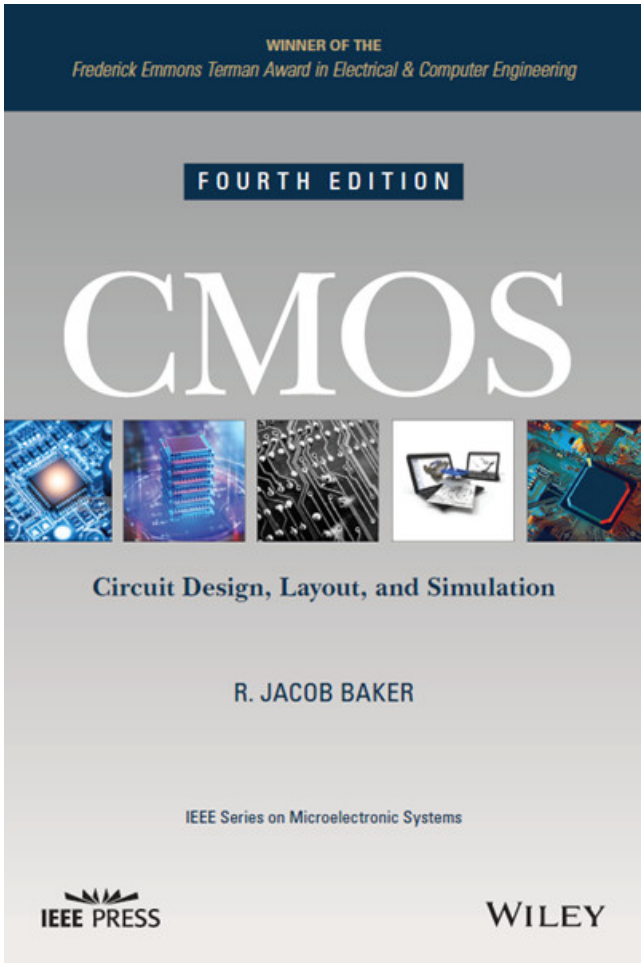
VLSI Design
Homework 2 (Midterm Practice Part 2)

Description: This assignment will survey what you have learned thus far using problems from R. Baker's "CMOS Circuit Design, Layout, and Simulation", custom problems designed by the instructor, and layout examples provided by the ARM educational kit in collaboration with the Sky130 open source PDK.

Associated Reading Material:
Chapter 2. The Well.
Chapter 3. Metal Layers.
Chapter 4. Active and Poly Layers.
Chapter 5. Resistors, Capacitors, MOSFETS.
Chapter 6. MOSFET Operation.
Chapter 7. CMOS Fabrication.
Chapter 11. The Inverter.
Chapter 12. Static Logic Gates.
Chapter 15. CMOS Layout Examples.



Problem 7. Multiple Choice Concepts.
Choose the best answer for each question:

1. Which of the following is true for an NMOS transistor operating in its *linear* or *triode* mode? (Vgs = gate to source voltage, Vds = drain to source voltage, Vt = threshold voltage)
   (a) Vds < (Vgs - Vt)
   (b) Vds > (Vgs - Vt)
   (c) Vgs < Vt
   (d) Vgs = 0v

2. Which of the following would result in the largest β?
   (a) NMOS w=3μ l=0.6μ
   (b) NMOS w=0.6μ l=3μ
   (c) PMOS w=3μ l=0.6μ
   (d) PMOS w=0.6μ l=3μ

3. The capacitance of a transistor gate is proportional to what?
   (a) The width of the gate
   (b) The length of the gate
   (c) The area of the gate
   (d) The depth of the channel

4. Which of the following processing techniques would be used to create a transistor's source and drain regions?
   (a) Oxidation
   (b) Ion implantation
   (c) Sputtering
   (d) Polysilicon deposition

Solution:
1 – a: An NMOS is in triode when Vgs > Vt and Vds < Vgs - Vt

2 – a: $\beta = \mu * Cox * W/L$. The largest W/L ratio is 3μ/0.6μ, *and μN is typically 2x to 3x larger than μP, therefore the largest β would be the NMOS transistor with W/L =* 3μ/0.6μ.

3 – c: Transistor gates act like a parallel plate capacitor, which is directly proportional to the surface area of the plates. In this case, the top plate is the area of the gate or W*L.

4 – b: Ion implantation is used to create transistor diffusion areas.

Problem 8. Short Answer Concepts.

1. How would you use Logical Effort to design a circuit that starts with a unit-sized inverter (W=1.5 μm for the NMOS and W=3 μm PMOS) that eventually has to drive a load 100 times as large as the unit inverter's input load?

2. Describe five sources of power dissipation in static CMOS circuits. Which is the most dominant source of power dissipation in today's circuits? What about future circuits in processes with deep sub-micron gate lengths?

Solution:

1 (From lecture 6, slides 20 and 22):

Since we are scaling inverters to drive a load, the Logical Effort, G, will be 1.

The Electrical Effort, H, is defined as Cload/Cin = 100/Cin. If we assume Cin = 1 for the device provided, the Electrical Effort is 100, but this can be scaled to be relative to a minimum-sized device if provided.

Then, the Path Effort, F, will be F = G*H = 100.

The delay can then be derived in terms of the number of stages, best stage delay, and the overall required drive-strength scaling of 100x.

$D = N*F^{1/N} + P \cong N*F^{1/N} + N$

Then, N should be determined to minimize this function.

2 (From lecture 7, slide 10):

Power dissipation consists of dynamic and static power. Dynamic power occurs due to the supplying of current to/from load capacitances and the short circuit current occurring when transistors in the pull-up and pull-down networks are on simultaneously during switching. Static power consists of gate leakage, sub-threshold drain-to-source leakage, junction leakage, and contention current. Dynamic power and sub-threshold leakage tend to dominate in modern devices.

Problem 9. CMOS Transistor Theory.
Consider a CMOS inverter which has ideal transistors with the following characteristics:
PMOS transistor: W/L = 2; μ_P= 72 $cm^2/V*s$; V_T= -0.4V
NMOS transistor: W/L = 1; μ_N = 180 $cm^2/V*s$; V_T = 0.4V
180 nm process; C_{ox}/unit area= 8.6E-7 F/cm^2; V_{DD} = 1.8V

a. Calculate β for each transistor, including the units.
b. What modes of operation is each transistor in when V_{in} = 0 V, 0.9 V, and 1.8 V?
c. Estimate the current through the inverter if V_{in} = 0.9 V. List any assumptions you make.
d. Would you expect the current to be higher or lower if the inverter were implemented in a 130 nm process?

Solution:

(a)
$\beta_P = \mu_P * C_{ox} * W/L$ = 72 $cm^2/V*s$ x 8.6E-7 F/cm^2 x 2 = 120 $\mu A/V^2$
$\beta_N = \mu_N * C_{ox} * W/L$ = 180 $cm^2/V*s$ x 8.6E-7 F/cm^2 x 1 = 150 $\mu A/V^2$

(b)

	Vin = 0 V	Vin = 0.9 V	Vin = 1.8 V
NMOS	Cutoff	Saturation	Linear
PMOS	Linear	Saturation	Cutoff

(c)
Since both transistors will be in Saturation when Vin = 0.9 V,

$I_{SD,P} = \frac{1}{2}\beta(V_{sg}-|V_T|)^2$ = 120/2 * (0.9-0.4)^2 = 15 μA (note that $V_{sg} = V_{DD}$-Vin)
$I_{DS,N} = \frac{1}{2}\beta(V_{gs}-V_T)^2$ = 150/2 * (0.9-0.4)^2 = 19 μA (note that V_{gs} = Vin)

Since the transistors are in series, the current must be equal. The PMOS device will limit the current and the total current can be approximated as 15 µA.

(d)
Due to velocity saturation, thus reducing mobility, the current will likely be lower in the 130 nm process.