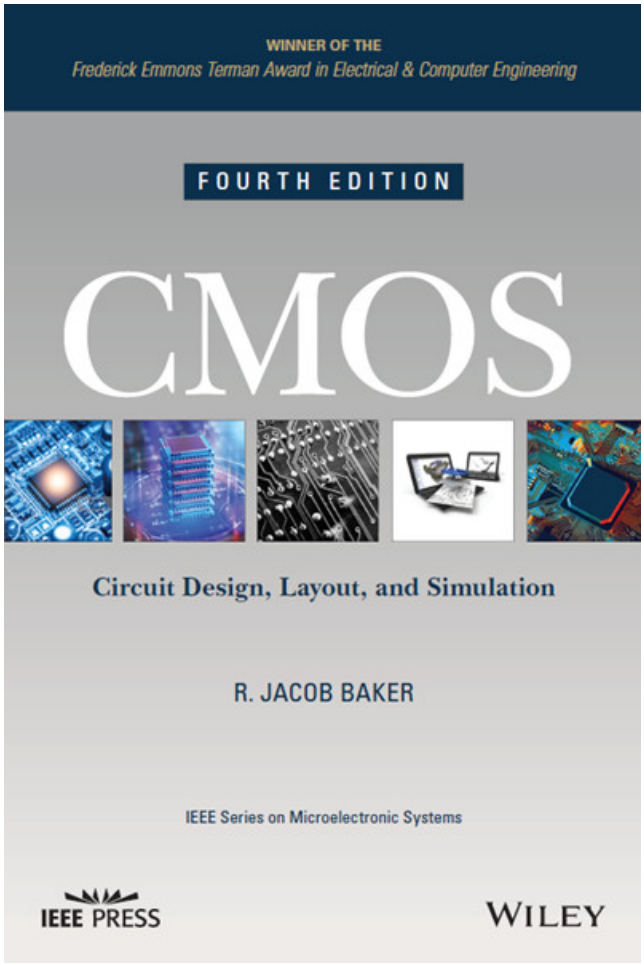
VLSI Design
Homework 2 (Midterm Practice)
Due Date: Mar. 7, 2024 @ 1:15pm (Not Graded)

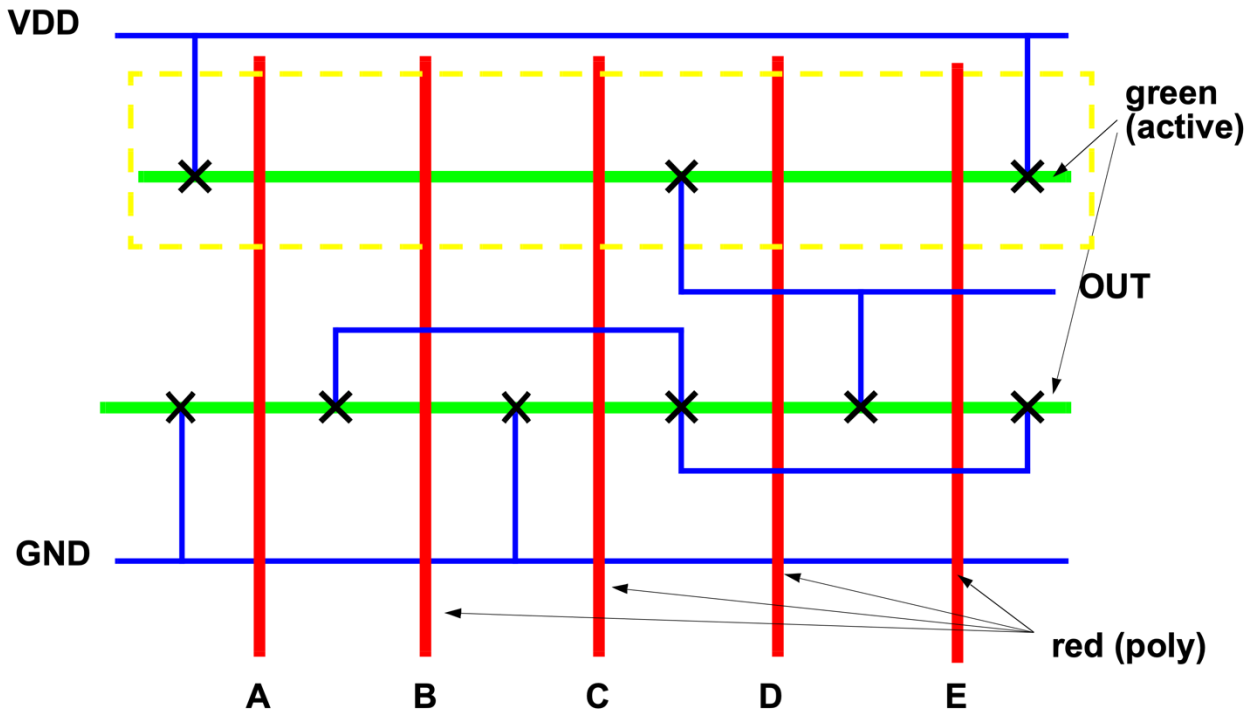
Description: This assignment will survey what you have learned thus far using problems from R. Baker's "CMOS Circuit Design, Layout, and Simulation", custom problems designed by the instructor, and layout examples provided by the ARM educational kit in collaboration with the Sky130 open source PDK.

Associated Reading Material:
Chapter 2. The Well.
Chapter 3. Metal Layers.
Chapter 4. Active and Poly Layers.
Chapter 5. Resistors, Capacitors, MOSFETS.
Chapter 6. MOSFET Operation.
Chapter 7. CMOS Fabrication.
Chapter 11. The Inverter.
Chapter 12. Static Logic Gates.
Chapter 15. CMOS Layout Examples.

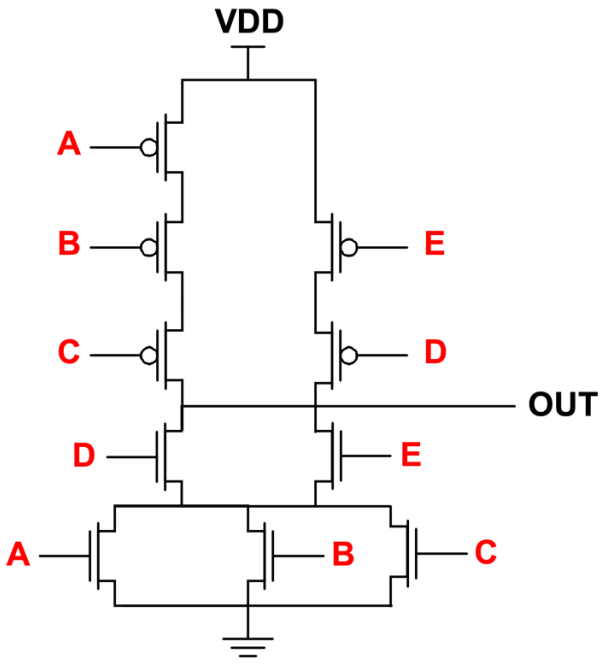


Problem 1. Layout/Stick Analysis 1.

Consider the following stick diagram. Draw the transistor-level schematic. What logic equation does this circuit implement? Assume the dashed yellow layer is the n-well and all other regions are within the p-substrate.



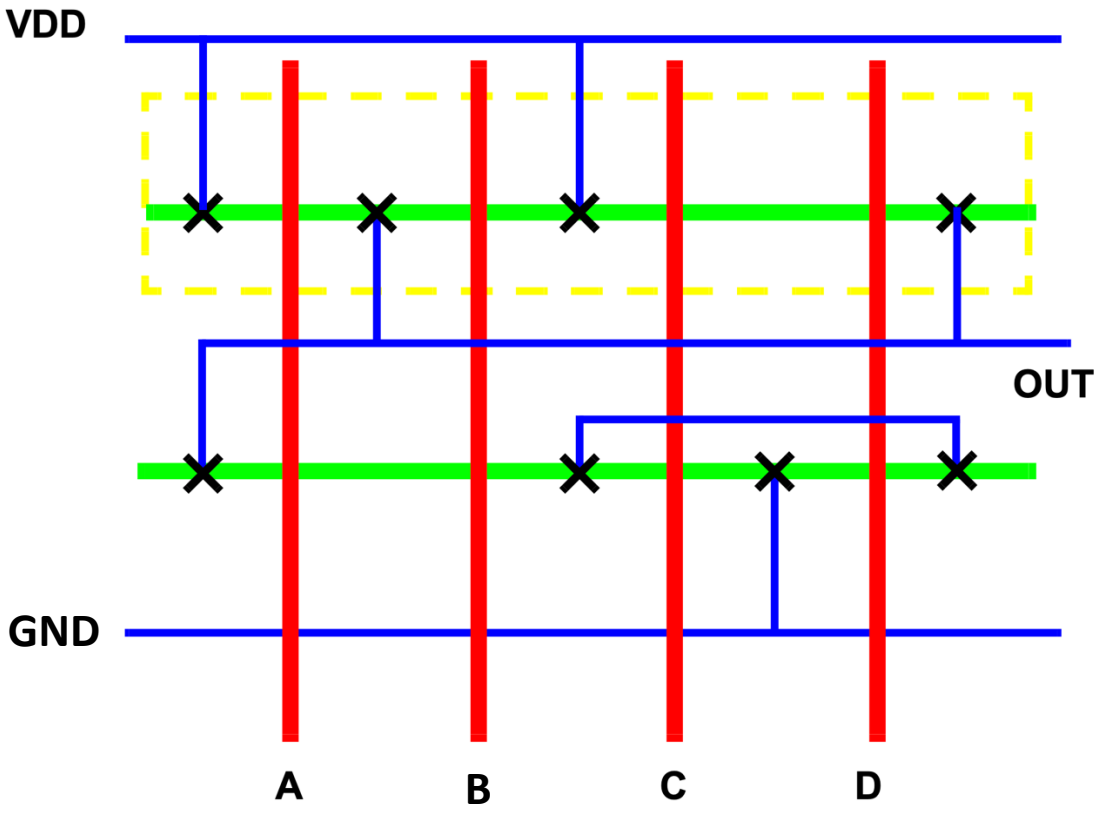
Solution:



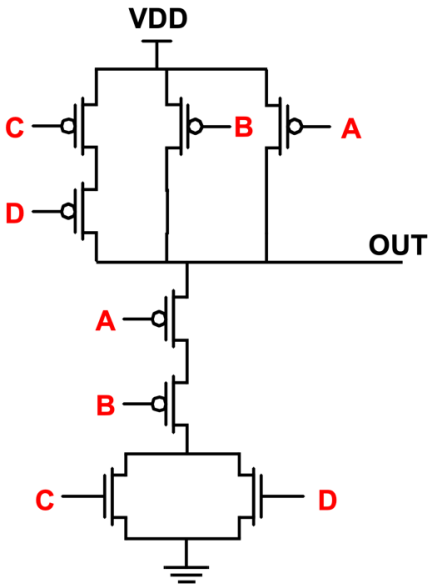
$$out = \sim((A+B+C)(D + E))$$

Problem 2. Layout/Stick Analysis 2.

Consider the following stick diagram. Draw the transistor-level schematic. What logic equation does this circuit implement? Assume the dashed yellow layer is the n-well and all other regions are within the p-substrate.

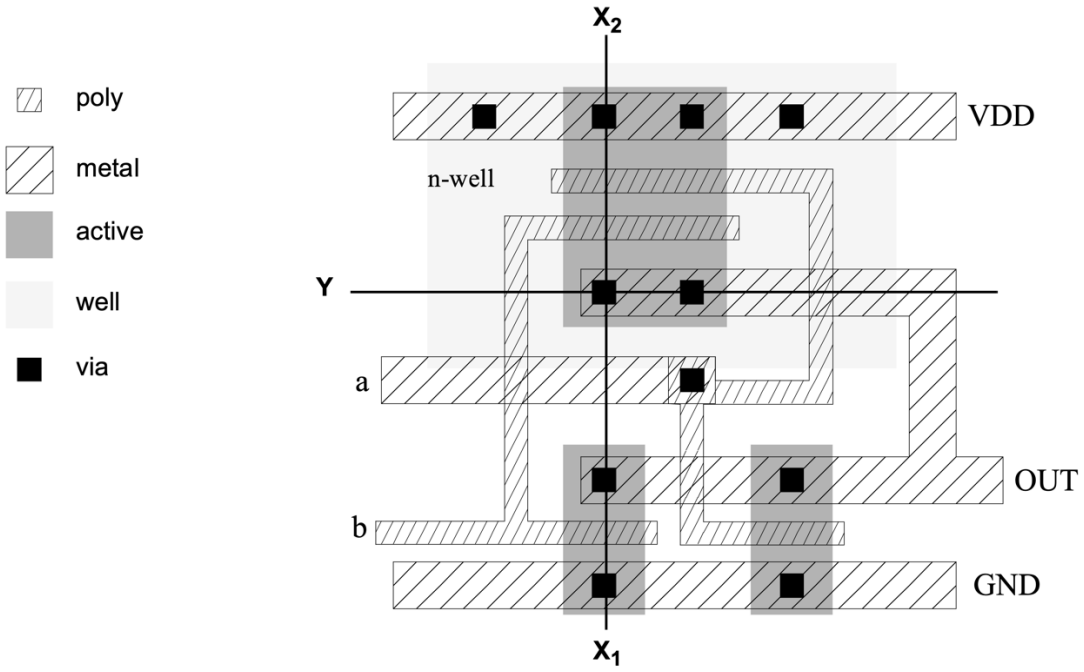


Solution:

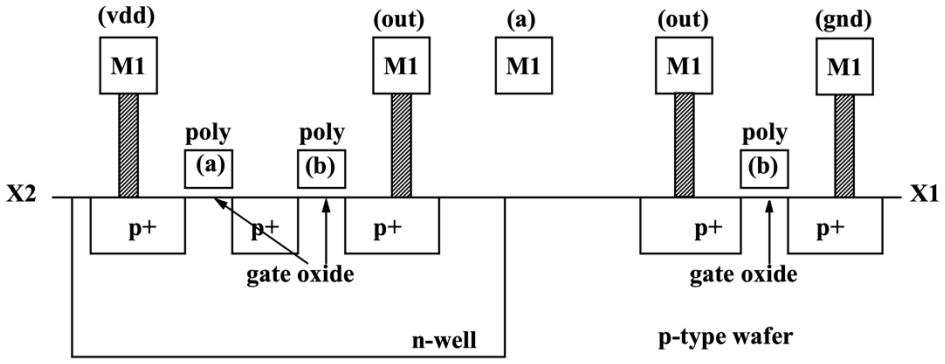


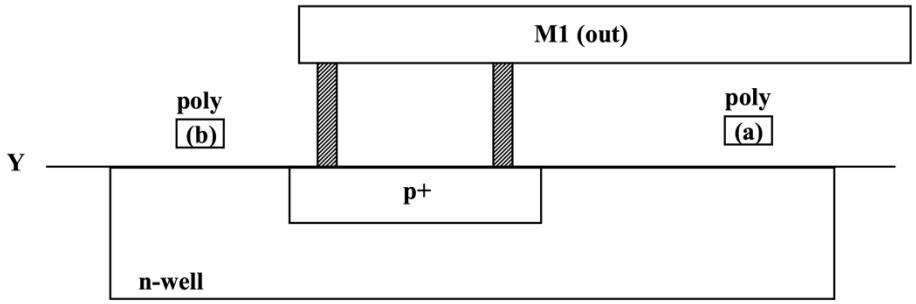
out = ~(AB(C + D))

Problem 3. Layout cross-section.
Provide a side-view diagram (vertical cross section) for each of the cut lines X and Y through the below layout. Be sure to label each of the strata and the endpoints X1 and X2.



Solution:



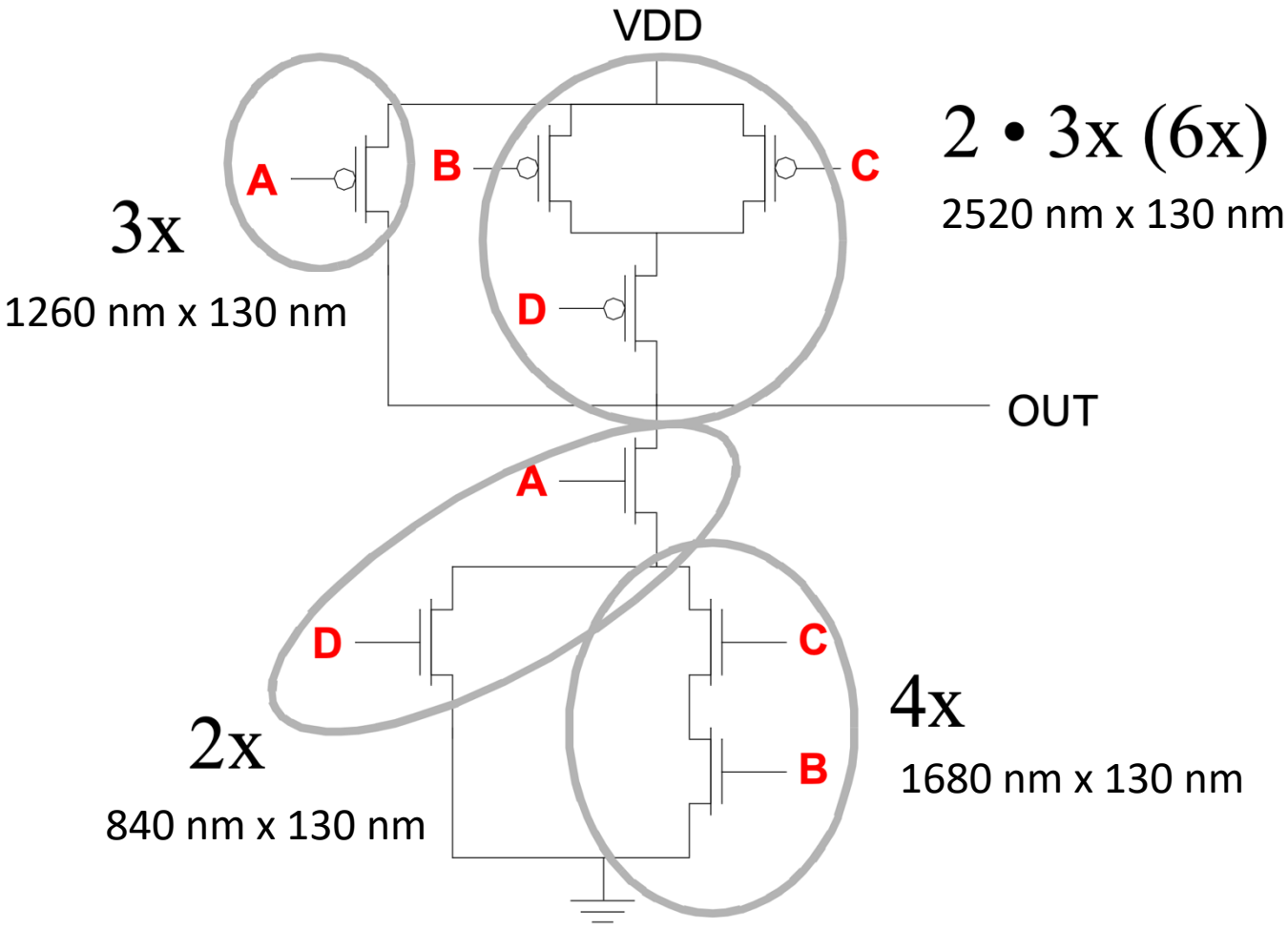


Problem 4. CMOS Logic DC Switch-Point.
Consider the Boolean logic function, out = ~(A(BC + D)). Draw the circuit and indicate the width and lengths of each transistor. Size all NMOS and PMOS transistors such that the pull-up network and pull-network have equivalent resistance to a minimum-sized MOSFET.

*Assume that the mobility of the NMOS transistors is 3x the mobility of the PMOS transistors.

*Assume that the circuit is implemented in a 130 nm technology and that the dimensions of a minimum-sized MOSFET are W_{min} = 420 nm & L_{min} = 130 nm.

Solution :



Problem 5. Example 3.3 in textbook.
Table 3.1 in the textbook shows the estimated parasitic capacitances and resistances associated with various layers within a CMOS technology.

Table 3.1 Typical parasitic capacitances in a CMOS process. Note that while the physical distance between the layers decreases, as process technology scales downwards, the dielectric constant used in between the layers can be decreased to keep the parasitic capacitances from becoming too significant. The values are representative of the parasitics in both long- and short-channel CMOS processes.

	Plate min	Cap. typ	aF/μm² max	Fringe min	Cap. typ	aF/μm max
Poly1 to subs. (FOX)	53	58	63	85	88	92
Metal1 to poly1	35	38	43	84	88	93
Metal1 to substrate	21	23	26	75	79	82
Metal1 to diffusion	35	38	43	84	88	93
Metal2 to poly1	16	18	20	83	87	91
Metal2 to substrate	13	14	15	78	81	85
Metal2 to diffusion	16	18	20	83	87	91
Metal2 to metal1	31	35	38	95	100	104

Estimate the resistance of a 1 mm long and 200 nm wide piece of metal1. What is the drawn size of this metal line if the scale factor is 50 nm? Also estimate the delay through this piece of metal, treating the metal line as an RC transmission line. Verify your answer with a SPICE simulation.

Solution:
Note that the drawn size of the metal line is 1 mm/50 nm (= 20,000) by 200/50 (= 4). Figure 3.6 (below) shows the layout of the metal wire (not to scale). The line consists of 1,000/0.2 = 20,000/4 = 5,000 squares of metal1. To calculate the resistance of the metal line, we use Eq. (2.3), below.

$$R = \frac{0.1\ \Omega}{\text{square}} \cdot \frac{20,000}{4} = 0.1 \cdot 5,000 = 500\ \Omega$$

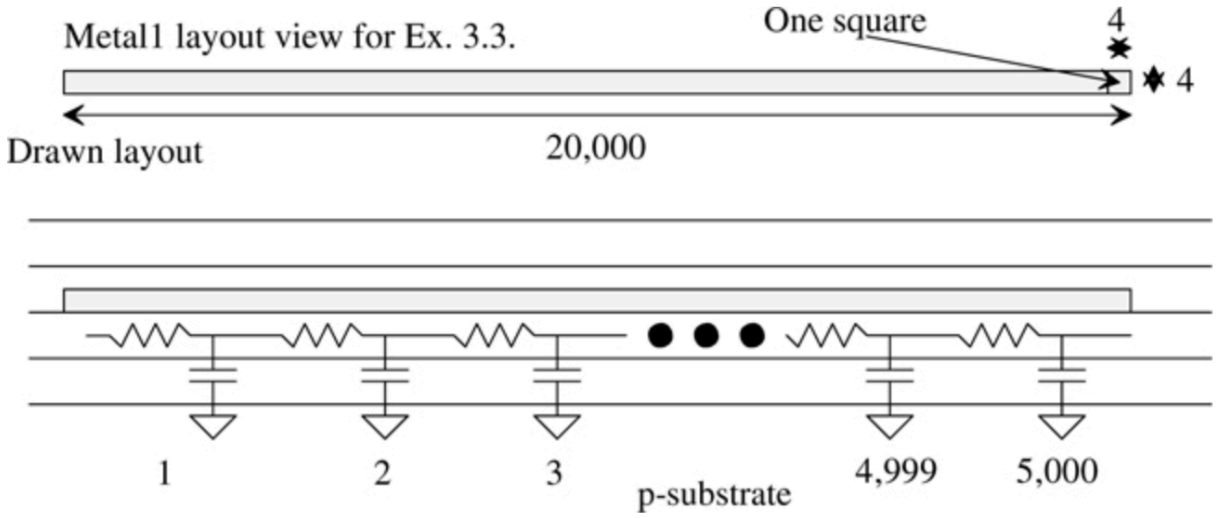


Figure 3.6 Layout and cross-sectional view with parasitics for the metal line in Ex. 3.3.

To calculate the capacitance, we use the information in Table 3.1 and either Eq. (3.1) or (3.2)

$$C = (1{,}000 \cdot 0.2) \cdot 23\ aF + (2{,}000 + 0.4) \cdot 79\ aF = 162\ fF$$

The capacitance for each 200 nm by 200 nm square (4 by 4) of metal1 is

$$C_{square} = \frac{162\ fF}{5{,}000} = 32\ aF/\text{square}$$

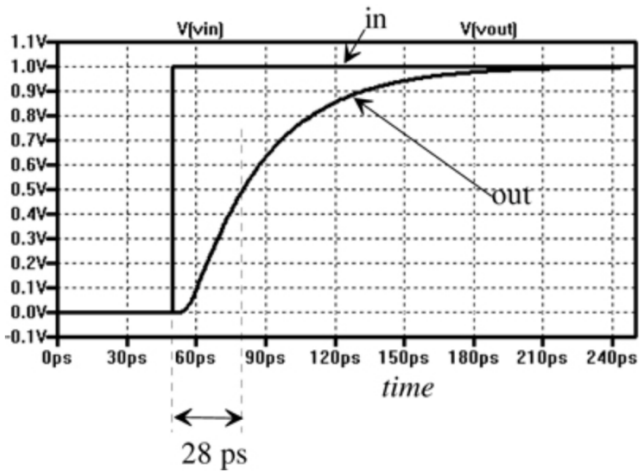
The delay through the metal line is, using Eqs. (2.32) or (2.33)

$$t_d = 0.35 \cdot R_{square} C_{square} \cdot l^2 = 0.35(0.1)(32\ aF)(5{,}000)^2 = 28\ ps$$

or

$$t_d = 0.35RC = 0.35 \cdot 500 \cdot 162\ fF = 28\ ps$$

The delay of a metal1 line (with nothing connected to it) is 28 ps/mm when the parasitic capacitance and resistance are the limiting factors. The SPICE simulation results are seen in Fig. 3.7 below.

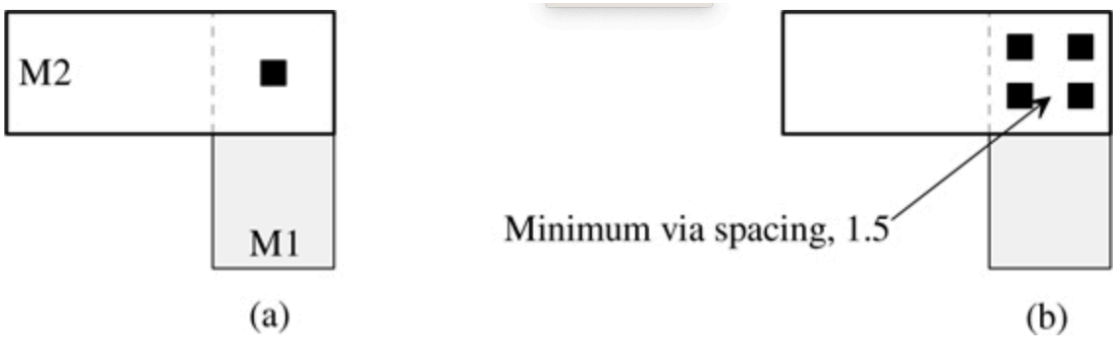


*** Figure 3.7 CMOS: Circuit Design, Layout, and Simulation ***

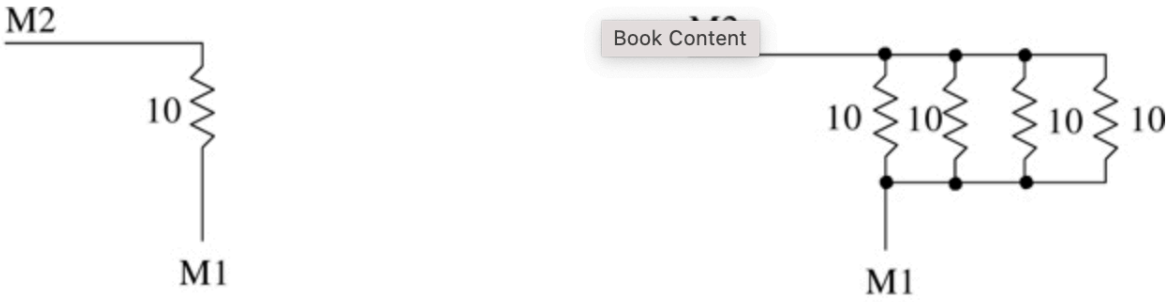
```
.control
destroy all
run
plot vin vout
.endc
.tran 1p 250p

O1 Vin 0 Vout 0 TRC
Rload Vout 0 1G
Vin vin 0 DC 0 pulse 0 1 50p 0
.model TRC ltra R=0.1 C=32e-18 len=5k
.end
```

Problem 6. Example 3.8 in textbook.
Sketch the equivalent electrical schematic for the layout depicted in Fig. 3.14a showing the via contact resistance. Estimate the voltage drop across the contact resistance of the via when 1 mA flows through the via. Repeat for the layout shown in Fig. 3.14b.

Assume one via has an equivalent of 10 ohms of resistance.



Solution:



(a) The contact resistance of the via in Fig. 3.14a.

(b) The contact resistance of the four vias in Fig. 3.14b.

The equivalent schematics are shown in Fig. 3.15a and (b) for the layouts in Figs. 3.14a and (b) respectively. If the via contact resistance is 10 Ω, and 1 mA flows through the via in (a), then a voltage drop of 10 mV results. Further, the reliability of the single via will be poor with 1 mA flowing through it due to electromigration effects. A “rule-of-thumb” is to allow no more than 100 μA of current flow per via. The four vias shown in Fig. 3.14(b) give an effective contact resistance of 10/4 or 2.5 Ω because the contact resistances of each of the vias are in parallel. The voltage drop across the vias decreases to 2.5 mV with 1 mA flowing in the wires. Increasing the metal overlap and the number of vias will further decrease the voltage drop (and electromigration effects).