Syllabus for ENGR-E 599: Topics in Intelligent Systems Engineering, VLSI Design
Section: 11764

Course Description:
VLSI Design introduces students to fabrication and layout techniques for designing large-scale integrated circuits (ICs) and systems. Students will use industry-standard tools for designing and fabricating ICs in nanometer-scale technology nodes. Specific topics include MOSFET and FinFET theory, CMOS logic, standard fabrication processes, layout design rules, and all the factors required for a practical circuit design. Analog and digital design techniques for creating static and dynamic logic structures, interconnect analysis, chip layout, simulation, and testing will be explored.

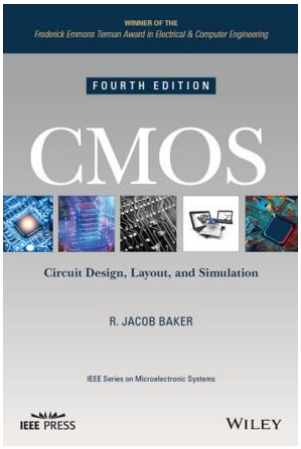
Course Pre/Co-Requisites: None

Meeting Dates: Tuesday / Thursday, 12:45 pm-2:00 pm Luddy Hall (IF) Room 4133

Course delivery method: in-person

Learning Outcomes:
- Identify, formulate, and solve engineering problems related to the use of microelectronics in space environments
- Demonstrate an ability to communicate effectively
- Recognize the need for, and an ability to engage in life-long learning
- Demonstrate the use of techniques, skills, and modern tools for analyzing microelectronics radiation effects and reliability degradation

Required Texts and Supplies:
CMOS Circuit Design, Layout, and Simulation, *John Wiley & Sons,* July 2019. ISBN 9781119481515 (Errata)
- https://www.amazon.com/CMOS-Circuit-Simulation-Microelectronic-Systems/dp/1119481511
- https://www.bkstr.com/indianastore/course-materials-results?shopBy=course&divisionDisplayName=&departmentDisplayName=ENGR-E&courseDisplayName=599&sectionDisplayName=13738&programId=5130&termId=100086336



Additional Online Resources for Textbook:
- https://cmosedu.com/

Assessment:

Lab Notebook	10%
Assignments	20%
Review Article	15%
Design project	30%
Midterm exam	15%
Final quiz	10%
Total	100%

Syllabus for ENGR-E 599: Topics in Intelligent Systems Engineering, VLSI Design
Section: 11764

Major due dates:
Note to students: these dates are subject to change with adequate notification via Canvas.

- Homework assignments: due most Thursdays
- Midterm exam: Thursday, Mar. 12, 2026 (in lecture)
- Spring Break: Mar. 15 – Mar. 20, 2026 (no class)
- Review paper: Thursday, Apr. 16, 2026
- Final quiz: Apr. 30, 2026
- Final project and notebook deadline: Thursday, May 7, 2026 @ 12:40 pm (regular final exam time)

Required materials:

- All course reference materials are supplied in-class and on the course GitHub page.
- No software purchases are required; VLSI Design will utilize the Cadence Design electronic design automation (EDA) tool suite. The Cadence EDA is a high-quality, industry-standard tool heavily used to design and simulate integrated circuits. We will be using the Cadence Design System for circuit schematic design (Virtuoso), simulation (Spectre), circuit layout (Virtuoso), and verification (Pegasus). Information about Cadence can be found here: https://www.cadence.com/en_US/home/tools/custom-ic-analog-rf-design/layout-design/virtuoso-layout-suite.html
- Cadence is installed on the burrow-rhel server at IU. You will be given accounts on this Red Hat Linux system and can access it via the classroom (IF 4111) or remotely through IU's VPN. More information will be provided in week 1 of class.
- All course material will be published to https://github.com/tdloveless/iu-vlsi
- Note that Canvas will only be used to publish grades and links to submit assignments. Students are expected to supply a personal working laptop computer with permissions to install and use course software.

Other considerations: Not applicable.