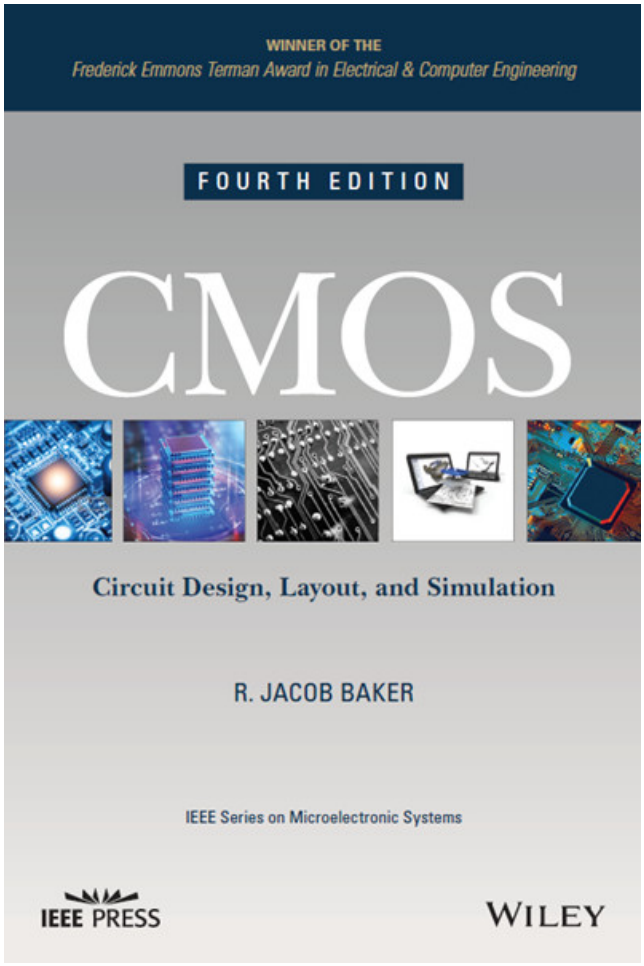
VLSI Design
Homework 1 SOLUTIONS

Description: This assignment will survey what you have learned thus far using problems from R. Baker's "CMOS Circuit Design, Layout, and Simulation"

Associated Reading Material:
Chapters 5 (Sections 5.1-5.3), 6 (Entire Chapter), 7 (Entire Chapter), 11 (Sections 11.1-11.3), and 12 (Sections 12.1-12.3)



5.7 (Layout-to-Schematic Analysis)

TBA

6.4 (MOS capacitance): If the oxide thickness of a MOSFET is 40 A°. What is C'_{ox}?

Solution:

$C'_{ox} = \varepsilon_{ox}/T_{ox} = (8.85 \times 3.97\ aF/\mu m)/(40 \times 10^{-10}\ m) =$ **$8.784\ fF/\mu m^2$**

6.12 (Channel resistance): Using Eq. (6.35) estimate the small-signal channel resistance (the change in the drain current with changes in the drain-source voltage) of a MOSFET operating in the triode region (the resistance between the drain and source.

Solution:

Eq 6.35: $I_D=\beta^*[(V_{gs}-V_{thn})V_{ds}-V_{ds}^2/2]$

$r = \Delta V_{ds} / \Delta ID$

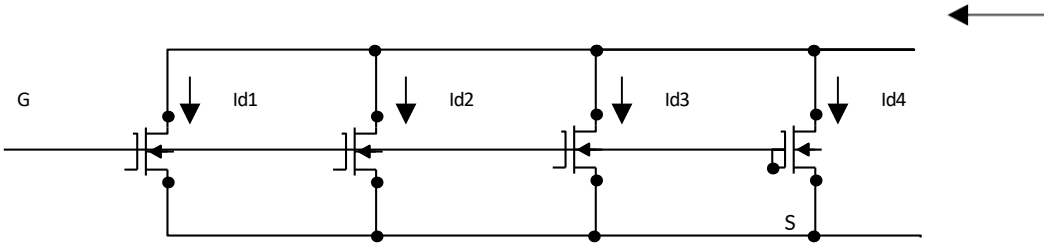
$= (V_{ds1}- V_{ds2}) / [(\beta^*[(V_{gs}-V_{thn})^*(V_{ds1})-(V_{ds1})^2/2]- \beta^*[(V_{gs}-V_{thn})^*(V_{ds2})-(V_{ds2})^2/2]]$

$= (V_{ds1}- V_{ds2}) / [(\beta^*[(V_{gs}-V_{thn})^*(V_{ds1}- V_{ds2})-(V_{ds1})^2/2+(V_{ds2})^2/2]]$

$=1 / [(\beta^*[(V_{gs}-V_{thn})-(V_{ds1}+ V_{ds2})/2]]$

$r =1 / [\beta^*(V_{gs}-V_{thn}- V_{ds})]$

6.13 (Parallel MOSFET Connections): Show, using Eqs. 6.33 and 6.37, that the parallel connection of MOSFETs shown in Fig. 5.18 behaves as a single MOSFET with a width equal to the sum of the individual MOSFET's widths.



Equivalent of Fig. 5.18

Solution: From Kirchoff's Current Law, we know that Id = Id1 + Id2 + Id3 + Id4. So if each MOSFET has the same KP, L, V_{GS}, V_{DS} and V_{THN}, equations 6.33 and 6.37 become:

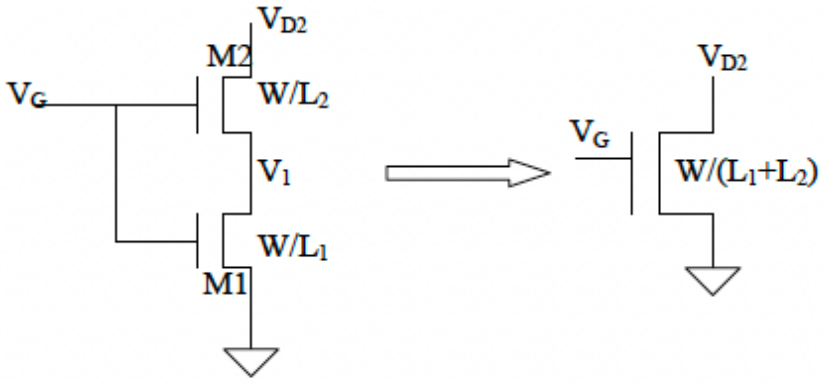
$$Id = KP_n \cdot \frac{W1+W2+W3+W4}{L} \cdot \left[(V_{GS} - V_{THN}) V_{DS} - \frac{V_{DS}^2}{2} \right] \qquad \text{for Eq. 6.33}$$

$$Id = KP_n \cdot \frac{W1+W2+W3+W4}{L} \cdot \left[(V_{GS} - V_{THN})^2 \right] \qquad \text{for Eq. 6.37}$$

This shows that the total drain current, Id, is equal to a single MOSFET with a width equal to W1 + W2 + W3 + W4.

6.15 (Series MOSFET Connections): Show that the series connection of MOSFETs shown in fig. 6.21 behaves as a single MOSFET with Twice the length of the individual MOSFETs. Again neglect the body effect.

Solution:



Assuming both MOSFETs are in triode region

For M_1 $I_{D1} = I_D$

$I_{D1} = I_D = KP_n\,(W/L_1)\,[(V_G - V_{THN})V_1 - V_1^2/2]$

$(I_D\,L_1)/\,(KP_n\,W) = [(V_G - V_{THN})V_1 - V_1^2/2]$

As Both MOSFETs are in series i.e., $I_{D1} = I_{D2} = I_D$

For M_2 $I_{D2} = I_D$

$I_{D2} = I_D = KP_n\,(W/L_2)\,[(V_G - V_1 - V_{THN})(V_{D2}-V_1) - (V_{D2}-V_1)^2/2]$

$(I_D\,L_2)/\,(KP_n\,W) = [(V_G - V_1 - V_{THN})(V_{D2}-V_1) - (V_{D2}-V_1)^2/2]$

$[(I_D\,L_1)/\,(KP_n\,W)] + [(I_D\,L_2)/\,(KP_n\,W)] = [(V_G - V_{THN})V_1 - V_1^2/2] + [(V_G - V_1 - V_{THN})(V_{D2}-V_1) - (V_{D2}-V_1)^2/2]$

$[(I_D\,(L_1+L_2)/\,(KP_n\,W)] = [(V_G - V_{THN})\,V_{D2} - (V_{D2})^2/2]$

This is the current from drain to source for a single MOSFET with length (L_1+L_2)

If $L1 = L_2 = L$

$[(2I_D\,L)/\,(KP_n\,W)] = [(V_G - V_{THN})\,V_{D2} - (V_{D2})^2/2]$

$I_D = [(KP_n\,W)/2L]\,[(V_G - V_{THN})\,V_{D2} - (V_{D2})^2/2]$

7.4 (Ion Implantation)

TBA

7.10 (Metal Deposition)

TBA

11.1 (Inverter DC Characteristics)

Solution:

From the graphs in Fig. 11.4 and the text in p11.3, we have V_{OH} =

5V
V_{OL} = 0V
V_{IL} = 1.8V
V_{IH} = 2.1V

Process — Long channel

Therefore, noise margins,
$NM_H = V_{OH} - V_{IH} = 5 - 2.1 = 2.9V$
$NM_L = V_{IL} - V_{OL} = 1.8 - 0 = 1.8V$

For the short channel process, similarly from the graph and text in the book, V_{OH} =

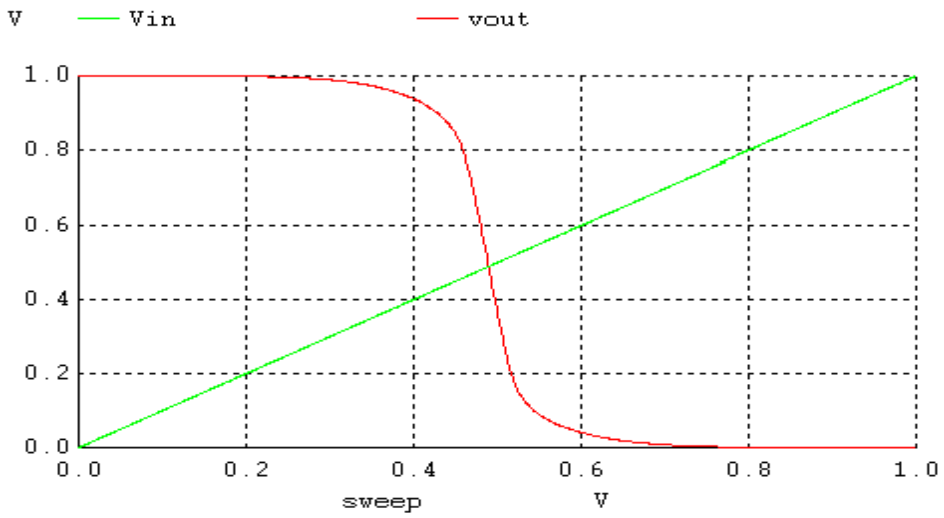
1V
V_{OL} = 0V
V_{IL}= 400mV
V_{IH}= 500mV

So, noise margins,
$NM_H = V_{OH} - V_{IH} = 1 - 0.5 = 0.5V = 500mV$
$NM_L = V_{IL} - V_{OL} = 0.4 - 0 = 0.4V = 400mV$

11.3 (Inverter Switching Point): Show that the switching point of three inverters in series is dominated by the Vsp id the first inverter.

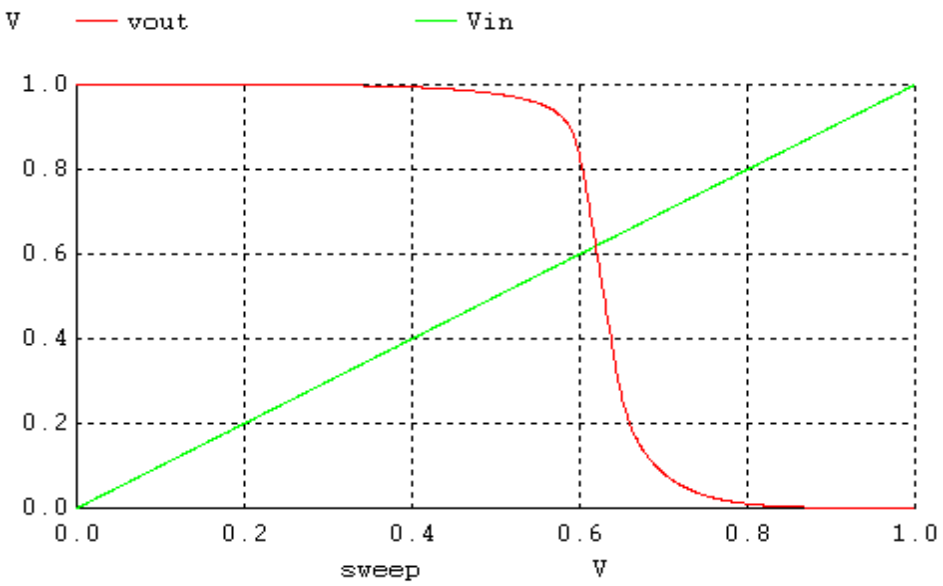
Solution: Three inverters with different switching points are simulated as below:

```
 *Stage1 Inverter
 .control
 destroy all
 run
 let Icross=-i(vdd)
 *plot Icross
 plot vout Vin
 .endc
 .option scale=50n
 .dc vin 0 1 1m
 vdd      vdd     0     DC      1
 Vin      vin     0     DC      0
 M1       vout    vin   0       0          NMOS L=1 W=10
 M2       vout    vin   vdd     vdd        PMOS L=1 W=20
* 50nm BSIM4 models
```

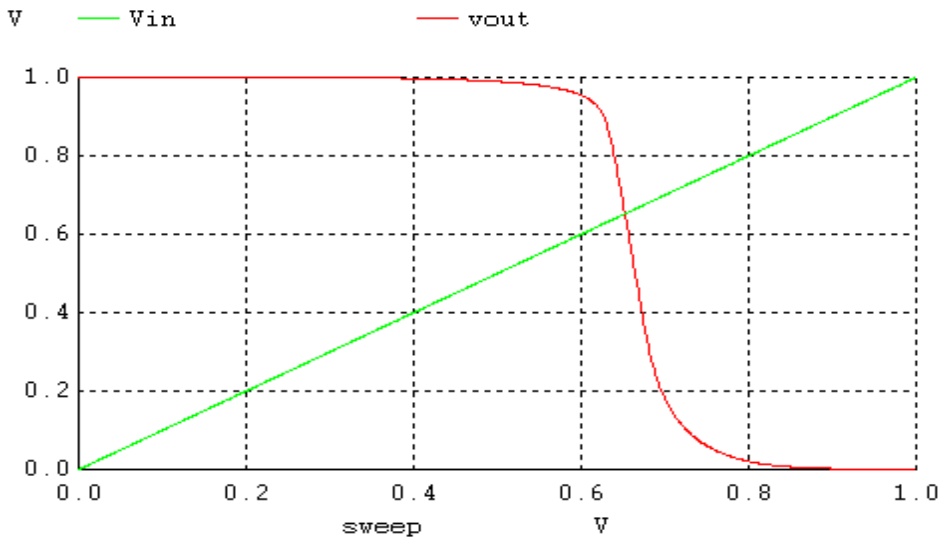


Stage2 and 3 Inverters with different Switching points:

```
*Stage2 Inverter
.control destroy all run
let Icross=-i(vdd)
*plot Icross plot vout Vin
.endc
.option scale=50n
.dc vin 0 1 1m
vdd       vdd     0       DC      1
Vin       vin     0       DC      0
M1        vout    vin     0       0       NMOS L=1 W=10 M2     vout    vin     vdd     vdd     PMOS L=1
W=200
* 50nm BSIM4 models
```



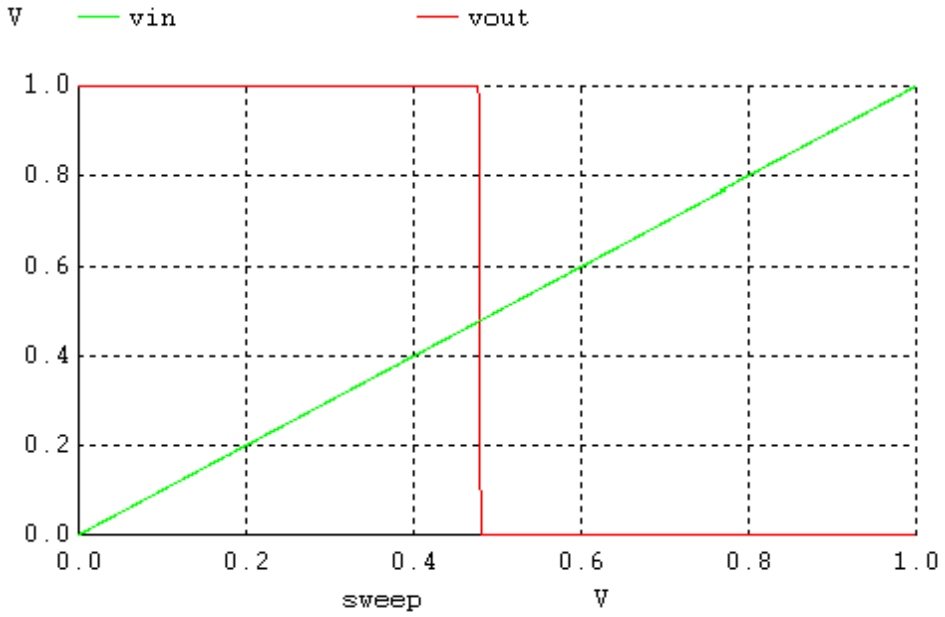

```
*Stage3 Inverter
.control destroy all run
let Icross=-i(vdd)
*plot Icross plot vout Vin
.endc
.option scale=50n
.dc vin 0 1 1m
vdd       vdd     0       DC      1
Vin       vin     0       DC      0
M1        vout    vin     0       0       NMOS L=1 W=10 M2      vout    vin     vdd     vdd     PMOS L=1
W=400
* 50nm BSIM4 models
```



```
*Three inverters in series
.control destroy all run
plot vout vin
.endc
.option scale=50n
.dc vin 0 1 1m

 vdd    vdd        0      DC     1
 Vin    vin        0      DC     0
 M1     vout1      vin    0      0       NMOS L=1 W=10
 M2     vout1      vin    vdd    vdd     PMOS L=1 W=20
 M3     vout2      vout1  0      0       NMOS L=1 W=10
 M4     vout2      vout1  vdd    vdd     PMOS L=1 W=200
 M5     vout       vout2  0      0       NMOS L=1 W=10
 M6     vout       vout2  vdd    vdd     PMOS L=1 W=400

*   50nm BSIM4 models
*   Don't forget the .options scale=50nm if using an Lmin of 1
*   1<Ldrawn<200    10<Wdrawn<10000 Vdd=1V
*   Change to level=54 when using HSPICE
```



Notice the switching point of the 3stage inverters is around 500mv though the second and third stage switching points are at 640mv.

12.2 (Logic Gate Design and Simulation)

Solution: A half adder circuit calculates a half sum (HS) and a carry out (CO). It takes two input bits, A and B. The logic equations for HS and CO are

$$HS = A \oplus B$$

$$CO = A \cdot B = \overline{(\overline{A} + \overline{B})}$$

Figure 1 shows a circuit schematic of a half adder's components. For clarity, the components are not wired together in the figure. The SPICE simulation and code appear on the next page.

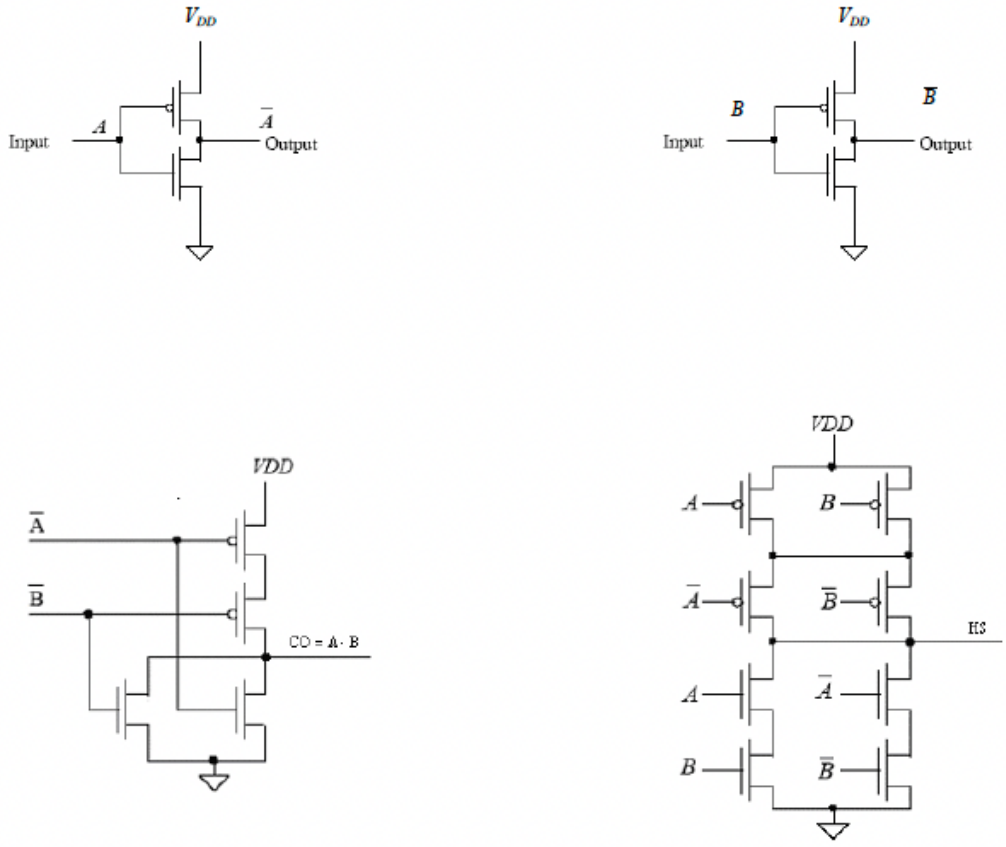
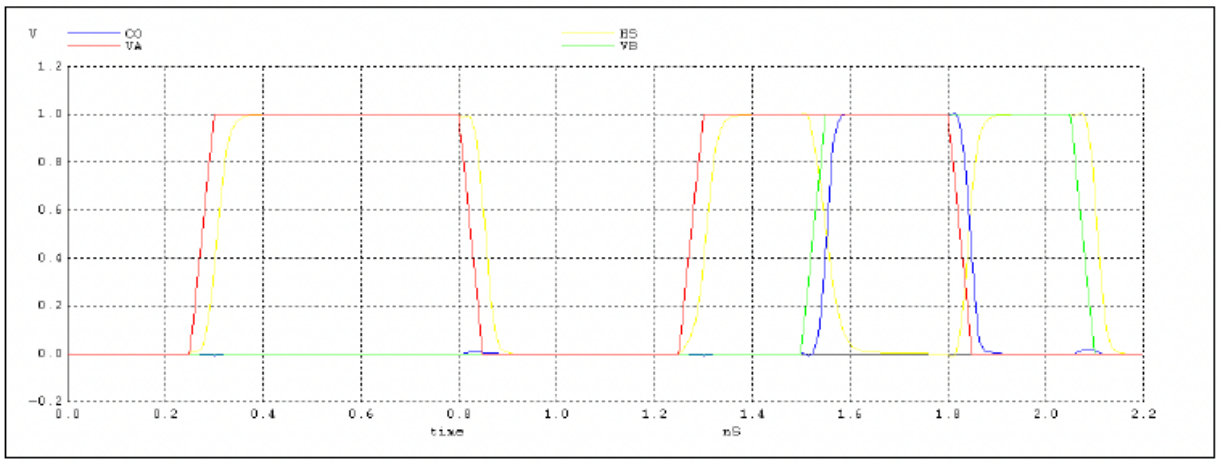


Figure 1: Half adder components



*** Problem 12.2 ***

```
.control
destroy all
run
plot VA VB CO HS
.endc

.option scale=50n
.tran 10p 2.2n

Vdd     Vdd     0       DC      1
VA      VA      0       DC      0       pulse 0 1 250p 50p 50p 0.5n 1n
VB      VB      0       DC      0       pulse 0 1 1.5n 50p 50p 0.5n 1n

*XOR gate -- A XOR B = HS
M12     N3      VB      Vdd     Vdd     PMOS L=1 W=20
M11     HS      B_      N3      Vdd     PMOS L=1 W=20

M10     N3      VA      Vdd     Vdd     PMOS L=1 W=20
M9      HS      A_      N3      Vdd     PMOS L=1 W=20

M8      HS      A_      N2      0       NMOS L=1 W=10
M7      N2      B_      0       0       NMOS L=1 W=10

M6      HS      VA      N1      0       NMOS L=1 W=10
M5      N1      VB      0       0       NMOS L=1 W=10

*A inverter
M2      A_      VA      Vdd     Vdd     PMOS L=1 W=20
M1      A_      VA      0       0       NMOS L=1 W=10

*B inverter
M4      B_      VB      Vdd     Vdd     PMOS L=1 W=20
M3      B_      VB      0       0       NMOS L=1 W=10

*NOR gate -- A_ NOR B_ = AB = CO
M16     N4      A_      Vdd     Vdd     PMOS L=1 W=20
M15     CO      B_      N4      Vdd     PMOS L=1 W=20
M14     CO      B_      0       0       NMOS L=1 W=10
M13     CO      A_      0       0       NMOS L=1 W=10

.MODEL NMOS NMOS LEVEL  = 14
.MODEL PMOS PMOS LEVEL  = 14

.end
```