ENGR-E 399/599 VLSI Design
Spring 2024
Midterm Exam

Due Date: Mar. 7, 2024 @ 11:59pm

Description: The Midterm Exam for ENGR-E 399/599 VLSI Design Covers Material from Lecture Modules 1-8, Chapters 2, 3, 4, 5, 6, 7, 11, 12, and 15 from R. Baker's CMOS Circuit Design, Layout, and Simulation, 4th Ed., as well as HW 1, Lab 0, and Lab 1.

Open Book, Open Notes. You must work INDEPENDENTLY.

Deliverables: Create a single PDF document with your solutions.

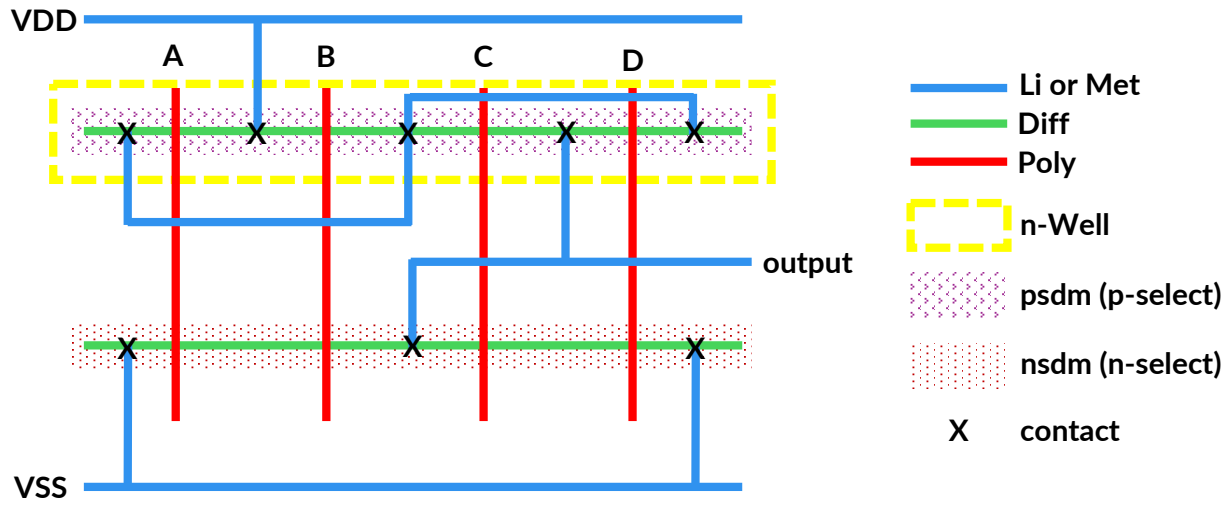
Name: SOLUTIONS

Honor Code Pledge:
I certify that I abide by the academic code of honor, according to https://studentcode.iu.edu

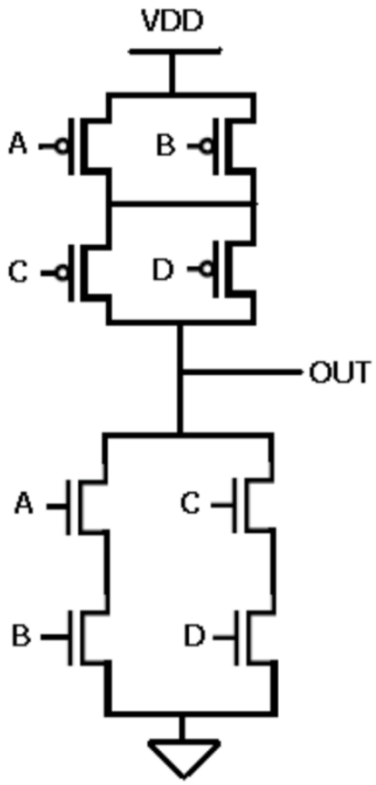
Signature: _____

Problem 1	**_____ /20**
Problem 2	**_____ /20 (+2 EC)**
Problem 3	**_____ /20 (+5 EC)**
Problem 4	**_____ /20**
Problem 5	**_____ /20**
Total	**_____ /100**

Problem 1 (+20 points)
Consider the following stick diagram. Draw the transistor-level schematic.



Solution:



Problem 2 (+20 points + 2 E.C.)
For the circuit in problem 1, fill in the below truth table with the correct outputs. Using your favorite method, write the simplified Boolean expression for the output in terms of the inputs A, B, C, and D (you may also use their complements).

For +2 points extra credit, what is a common name of this standard logic cell?

Solution:

A	B	C	D	output
0	0	0	0	**1**
0	0	0	1	**1**
0	0	1	0	**1**
0	0	1	1	**0**
0	1	0	0	**1**
0	1	0	1	**1**
0	1	1	0	**1**
0	1	1	1	**0**
1	0	0	0	**1**
1	0	0	1	**1**
1	0	1	0	**1**
1	0	1	1	**0**
1	1	0	0	**0**
1	1	0	1	**0**
1	1	1	0	**0**
1	1	1	1	**0**

The K-Map:

AB \ CD	00	01	11	10
00	1	1	0	1
01	1	1	0	1
11	0	0	0	0
10	1	1	0	1

From the K-Map,

Output $= A'C' + B'C' + A'D' + B'D'$

Combining terms and reducing
$= C'(A' + B') + D'(A' + B')$
$= (A' + B')(C' + D')$

Applying De-Morgan's Theorem
Output $= (\boldsymbol{AB} + \boldsymbol{CD})'$

E.C.: This expression represents an And-Or-Invert-22 cell (i.e. AOI22)

Problem 3 (20 points + 5 E.C.)
Consider the following Boolean expression.

Output = $(A + BC')D$

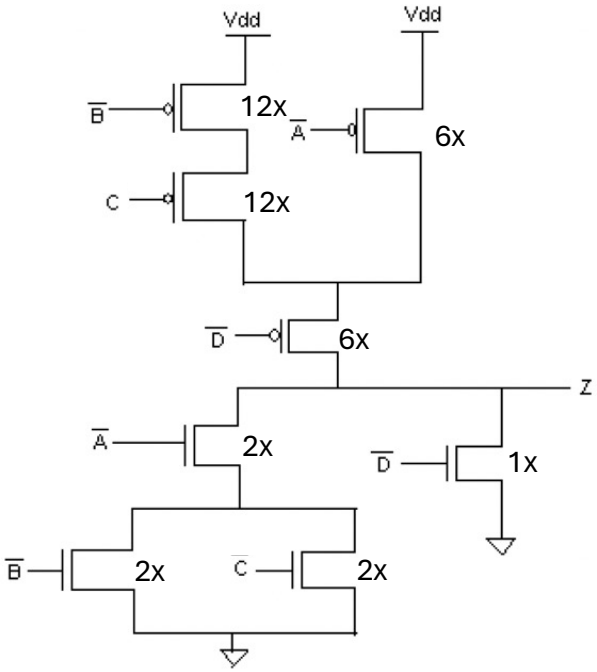
Draw the circuit and indicate the width and lengths of each transistor. Size all NMOS and PMOS transistors such that the pull-up network and pull-network have equivalent resistance to a minimum-sized MOSFET when a single pull-up or pull-down path is active.

For 5 points of extra credit, if the resistance of a minimum-sized PMOS, RP = 60kohm, and the resistance of a minimum-sized NMOS, RP = 20kohm, what the worst-case propagation delay be when driving a 50 fF capacitive load?

*Assume that the mobility of the NMOS transistors is 3x that of the PMOS transistors.

*Assume that the circuit is implemented in a 130 nm technology and that the dimensions of a minimum sized MOSFET are W_{min} = 420 nm & L_{min} = 130 nm.

Solution:



Worst-case occurs when B', C, and D' are on and 3 PMOS devices are in series. The equivalent resistance would be Req = RP/12+RP/12+RP/6 = RP/3 = 6.67 kohm

tPLM = 0.7*Req*Cload = 0.7*(6.67e3)*(50e-12) = 0.23 µsec.

Problem 4 (20 points)

Choose the best answer for each question:

1. Which of the following is true for an NMOS transistor operating in its *saturation* mode? (Vgs = gate to source voltage, Vds = drain to source voltage, Vt = threshold voltage)
   (a) Vds < (Vgs - Vt)
   (b) Vds > (Vgs - Vt)
   (c) Vgs < Vt
   (d) Vgs = 0v

2. Which of the following would result in the smallest β?
   (a) NMOS w=3μ l=0.6μ
   (b) NMOS w=0.6μ l=3μ
   (c) PMOS w=3μ l=0.6μ
   (d) PMOS w=0.6μ l=3μ

3. The resistance of a transistor channel is proportional to what?
   (a) The width of the gate
   (b) The length of the gate
   (c) The doping in the substrate
   (d) None of the above

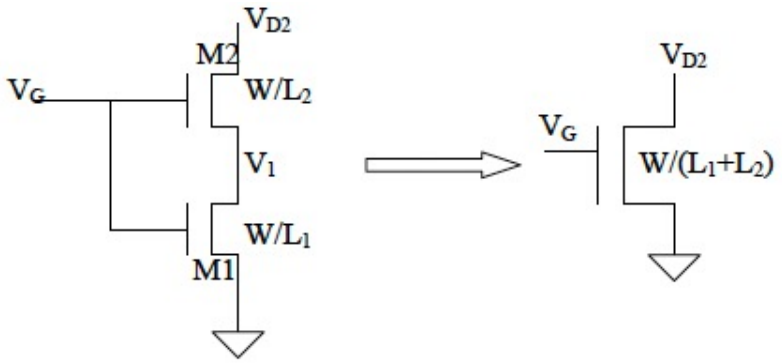
4. Which of the following processing techniques would be used to create metal interconnect?
   (a) Oxidation
   (b) Ion implantation
   (c) Sputtering
   (d) Polysilicon deposition

Solution:

1-b, 2-d, 3-b, 4-c

Problem 5 (20 points)
Show that the series connection of MOSFETs below behaves as a single MOSFET with twice the length of the individual MOSFETs. Neglect the body effect.

Consider the potential tradeoffs if you were to construct layouts for the circuits below. Which design would have the shortest propagation delay, and why?



Solution:

Assuming both MOSFETs are in triode region
For M_1 $I_{D1} = I_D$
$I_{D1} = I_D = KP_n (W/L_1) [(V_G - V_{THN})V_1 - V_1^2/2]$

$(I_D L_1)/ (KP_n W) = [(V_G - V_{THN})V_1 - V_1^2/2]$

As Both MOSFETs are in series i.e., $I_{D1} = I_{D2} = I_D$

For M_2 $I_{D2} = I_D$
$I_{D2} = I_D = KP_n (W/L_2) [(V_G - V_1 - V_{THN})(V_{D2}-V_1) - (V_{D2}-V_1)^2/2]$

$(I_D L_2)/ (KP_n W) = [(V_G - V_1 - V_{THN})(V_{D2}-V_1) - (V_{D2}-V_1)^2/2]$

$[(I_D L_1)/ (KP_n W)] + [(I_D L_2)/ (KP_n W)] = [(V_G - V_{THN})V_1 - V_1^2/2] + [(V_G - V_1 - V_{THN})(V_{D2}-V_1) - (V_{D2}-V_1)^2/2]$

$[(I_D (L_1+L_2)/ (KP_n W)] = [(V_G - V_{THN}) V_{D2} - (V_{D2})^2/2]$

This is the current from drain to source for a single MOSFET with length (L_1+L_2)

If $L1 = L_2 = L$

$[(2I_D L)/ (KP_n W)] = [(V_G - V_{THN}) V_{D2} - (V_{D2})^2/2]$

$I_D = [(KP_n W)/2L] [(V_G - V_{THN}) V_{D2} - (V_{D2})^2/2]$

While the DC behavior of the two circuits is identical, the design on the left would have a larger parasitic capacitance due to the internal node connecting the two transistors in series. This would result in a larger parasitic-induced delay. Therefore, the design on the right will have the better AC performance.