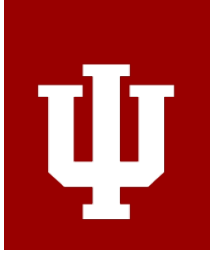


VLSI Design Course

LAB 1
Layout Design

Issue 1.1
portions of this lab from Mincey, 2009 (Texas A&M University)

1. Introduction

In this lab you will learn how to generate a simple transistor layout. Next, techniques will be developed for generating optimal layouts of wide transistors and matched transistors. Layout techniques for resistors and capacitors will also be introduced.

Reading Material: Chapters 11 and 22

2. Learning Objectives

At the end of this lab, you should be able to:

- Draw wide transistor-level cell layouts with multiple gate fingers using Cadence Virtuoso
- Draw matched transistor-level cell layouts with multiple instances using Cadence Virtuoso

2.1. Layout Techniques

2.1.1. Transistors

In Lab 0 you learned how to layout small size transistors and CMOS logic gates. Most analog designs, CMOS input/output (I/O) cells, and large buffers will not be limited to these small width transistors, thus special layout techniques need to be learned to layout large width MOSFETS. Luckily, wide transistors can be broken into parallel combinations of small width transistors as seen in Figure 2-1. By doing this horizontal expansion technique for the wide transistor, the drain and source area can be reduced which decreases parasitic capacitance and resistance.

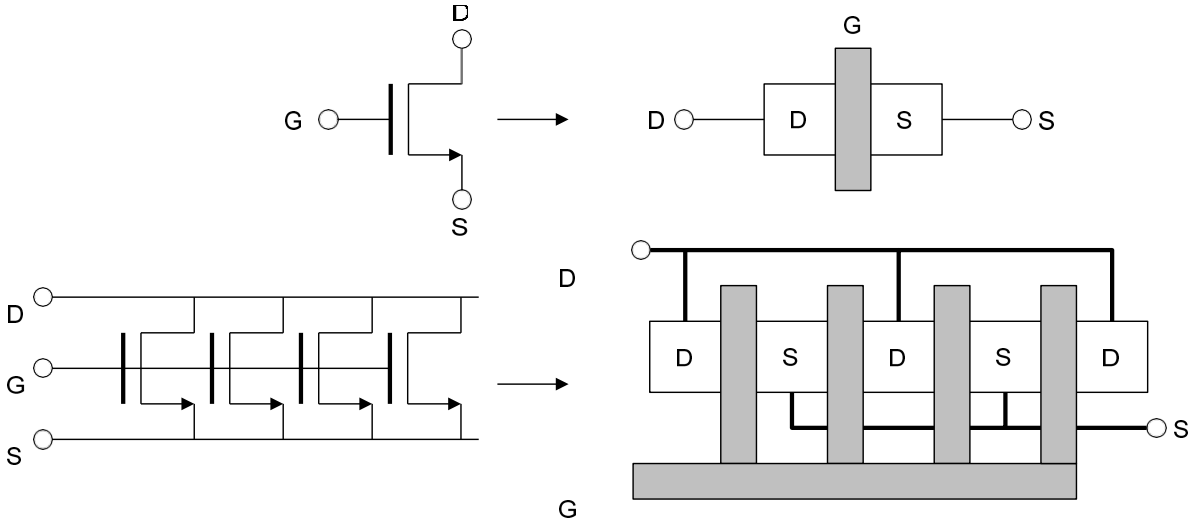


Figure 2-1: Wide MOS transistor layout

Another good layout technique is to use "dummy" transistors on both ends of a transistor layout, as in Figure 2-2. These dummy transistors ensure that the etching and diffusion. processes occur equally over all segments of the transistor layout.

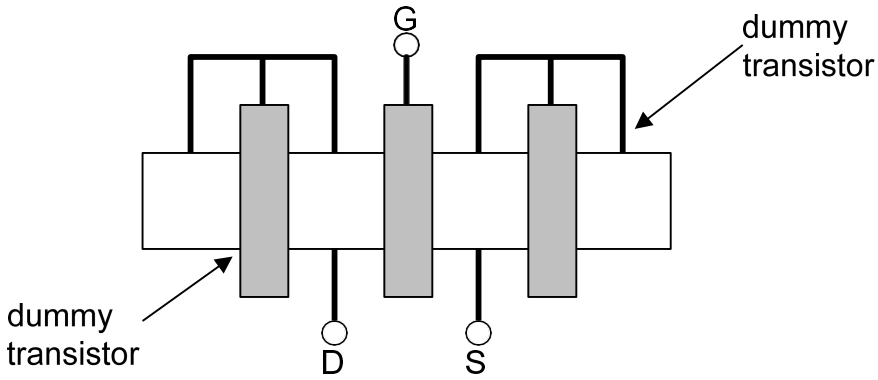


Figure 2-2: Dummy transistor layout

Notice the gate, drain, and source are connected which keeps the transistor from conducting. These shorted transistors are connected to the drain or source of the functional transistor. Another alternative for dummy transistors is to have the gate and source tied together.

When laying out any device the key is symmetry, especially when laying out fully differential components. For matched devices, use interdigitized or common-centroid layout techniques. A matched device is one where two transistors need to have exactly the same geometries. Examples include current mirrors and differential pairs.

An interdigitized layout is shown in Figure 2-3. Notice that the two transistors have been split into smaller size devices and interleaved. This layout minimizes the effects of process variations on the parameters of the transistors.

The idea behind splitting a transistor up is to average the process parameter gradient over the area of the matched devices. For example, the process variation of KP and of the transconductance parameter on the wafer is characterized by a global variation and a local variation. Global variations appear as gradients on the wafer as in Figure 2-4. However, local variations describe the random change in the parameter from one point on the chip to another nearby point. By using layout techniques such as interdigitized and common-centroid, the process variation can hopefully be averaged out among the matched devices.

When laying out wider matched transistors the common-centroid layout may be a better choice. This layout technique is illustrated in Figure 2-5 for the case of 8 matched M1 and M2 transistors of a differential pair.

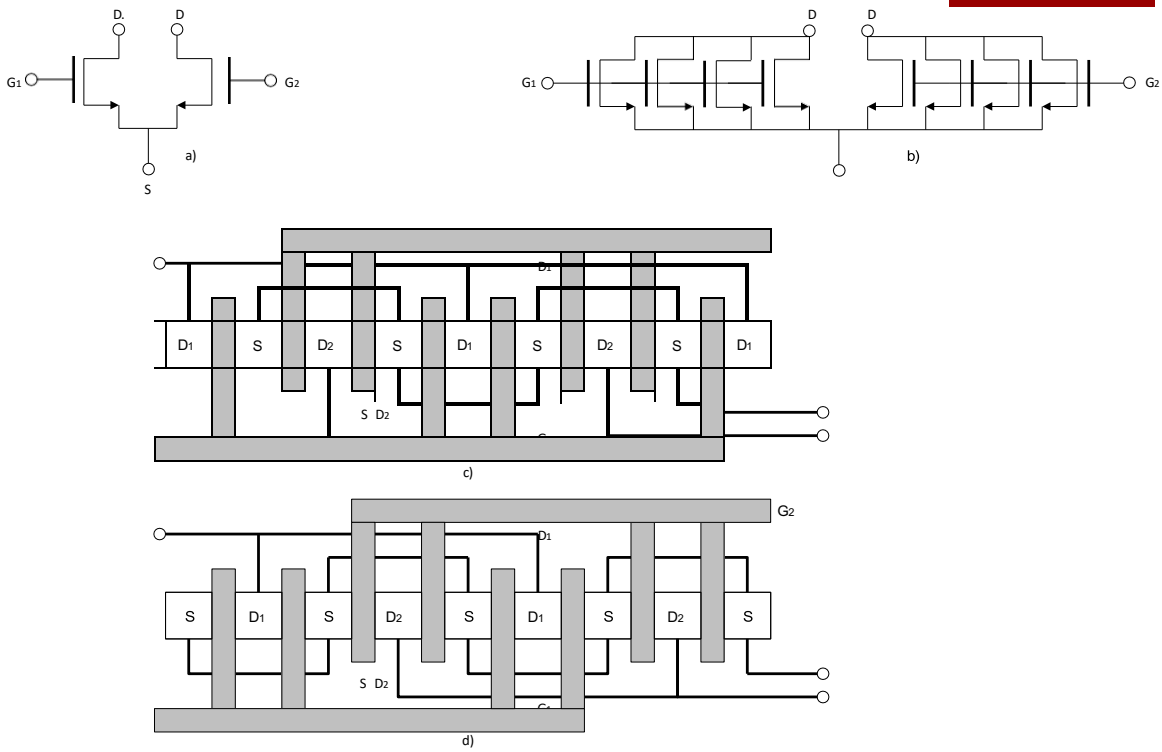


Figure 2-3: Interdigitized layout of a differential pair: (a) schematic; (b) horizontal expansion of device multiples; (c) interdigitized layout (common centroid) with differing drain areas; (d) interdigitized layout (not common centroid) with equal drain areas;

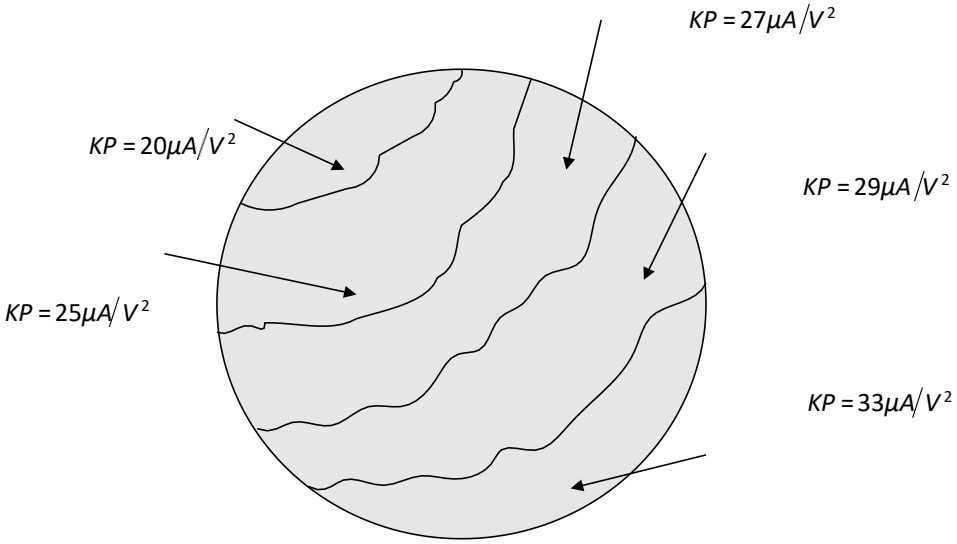


Figure 2-4: Gradient of KP on a wafer

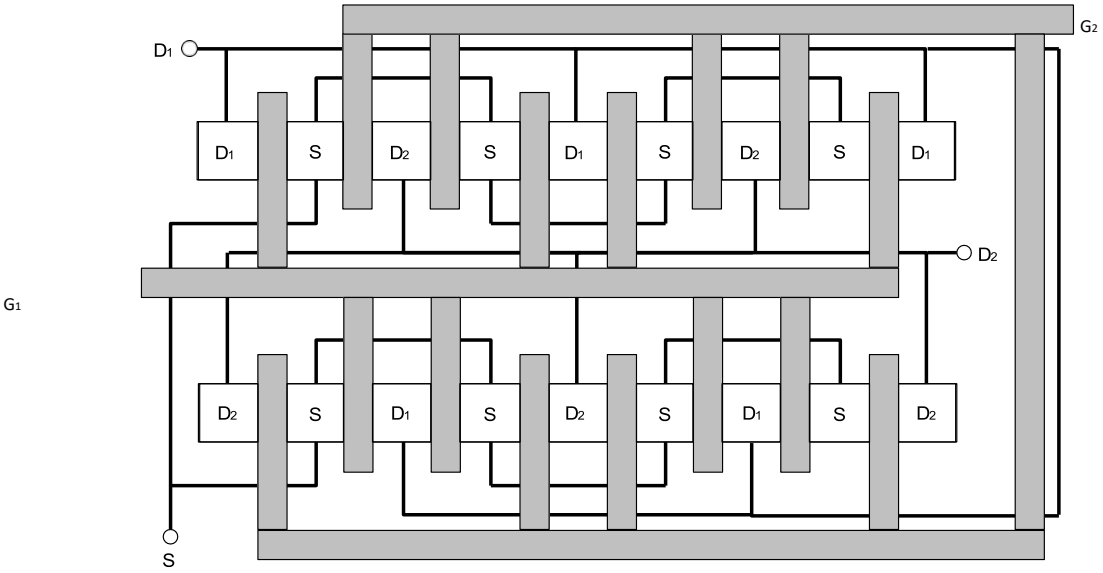


Figure 2-5: Common-centroid layout of a differential pair

The idea behind the common-centroid layout is to average linear processing gradients that affect the transistors' electrical properties. Common-centroid layouts should have the centroid (center of mass) of each transistor positioned at the same location. The following examples illustrate what is common-centroid and what is not common-centroid.

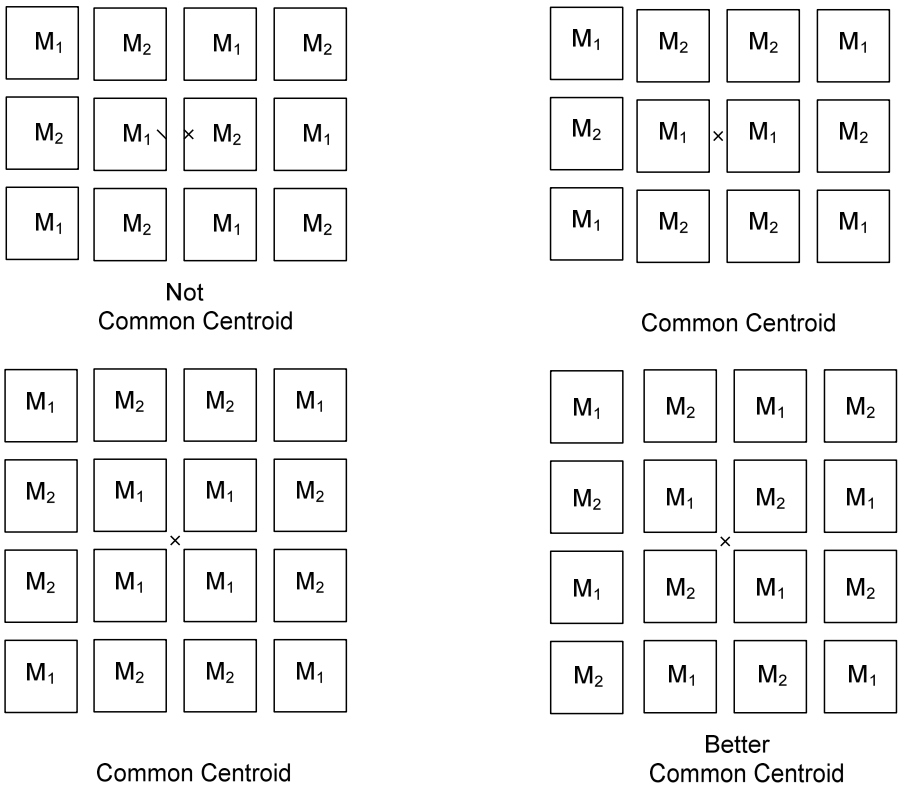


Figure 2-6: Common-centroid examples

2.1.2. Capacitors

Capacitors of various types can be fabricated on integrated circuits. A capacitor is formed when an insulator separates two conducting sheets. This conducing sheet can be formed laterally (using a fingering technique) or vertically, as shown in Figure 2-7.

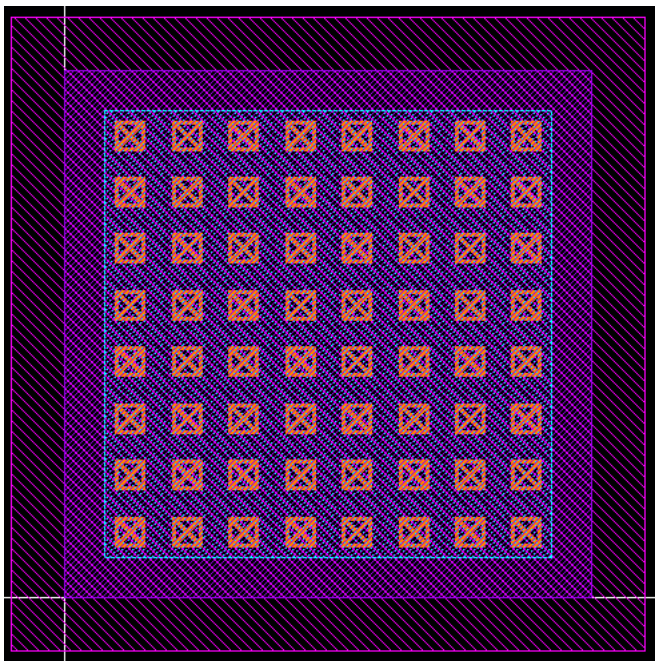


Figure 2-7: met2-met3 mim (metal-insulator-metal) capacitor layout

Figure 2-7 illustrates the layout of the met2-met3 mim capacitor. The capacitor is formed by laying a second (smaller rectangle) layer of metal (met3, in this case) over the base metal layer (met2, in this case). A third rectangle using the capm layer in sky130 is used to identify this cell as a capacitor. The area of the top plate (met3) and the perimeter determine the capacitance by the following equation:

$$C = C_A \cdot A + C_F \cdot P$$

where:

C_A is the capacitance per unit area for the chosen capacitor type

A is the area of the top capacitor plate

C_F is the fringe capacitance per unit length for the chosen capacitor type for diffusion based capacitors

P is the perimeter of the top capacitor plate

For mim capacitors, a parasitic capacitance between the substrate and bottom layer can inject unwanted signals and noise into the circuit at the bottom plate of the capacitor. To reduce this problem, put the capacitor in an N-well (for an N-well process) and connect the well to a “clean” ground. A ground plane (metal sheet connected to ground) can be used as

a shield by covering all capacitors where possible.

For poly-diffusion capacitors, the bottom plate is placed in a special capacitor well to reduce noise injection and to prevent voltage signals from altering the capacitance. This produces a high-quality linear capacitance.

To prevent the injection of noise from the substrate into the bottom plate of the capacitor, always be sure to connect it to a low impedance node such as ground or the output of an op-amp. Do not connect the bottom plate of a capacitor to an op-amp input. The substrate noise is due partly to power supply noise and connecting the bottom plate to the op-amp input allows direct injection of power supply noise into the op-amp input. The power supply is used to bias the substrate, so they are usually directly connected.

When designing circuits, sometimes desired circuit performance depends on the ratio of two capacitors. In such cases, it is important that two are more capacitors are properly matched. Divide each capacitor into many smaller "unit" capacitors. For matched devices this keeps the ratio of the areas and the ratios of the perimeters the same.

Like matched MOSFETS, the common-centroid layout technique can be employed for matched capacitors. Figure 2-8 gives a simplified layout floor plan for two equally sized, well-matched capacitors.

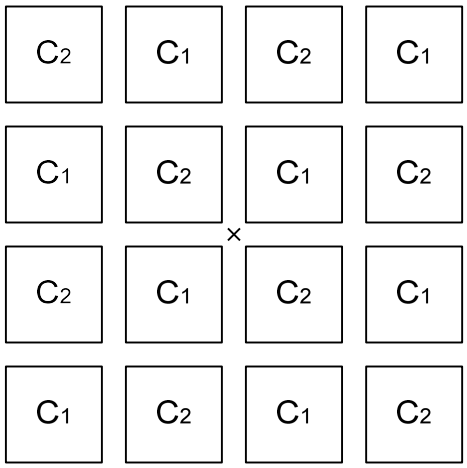
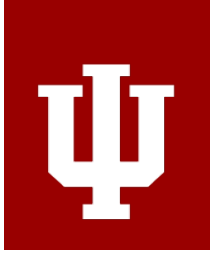


Figure 2-8: Common-centroid capacitor layout

The absolute and matching accuracy for various types of capacitors is given in the following table:

Capacitor	Absolute Accuracy	Matching Accuracy
mim	±20%	±0.06%
Poly-Diffusion	±10%	±0.06%

Remember, the purpose of using the unit capacitor is to keep the ratio of the areas and perimeters the same. This prevents (delta) variations in capacitor dimensions from changing the capacitor ratio. If a non-integral number of unit capacitors are required, then the perimeters and areas can still be kept the same.



Keep the unit capacitor side length L_0 in the range from 10µm-25µm. Also, within the capacitor array, use a consistent method of routing lines between the capacitor segments. Each unit capacitor should be surrounded by similar routing lines. For capacitors near the edge of the array, use "dummy" routing lines. Also, be sure that parasitic capacitance formed by overlapping conductors is the same for the matched capacitors.

Large unmatched capacitors can be divided into smaller unit capacitors to reduce distributed effects caused by the relatively high resistivity polysilicon. This prevents a large capacitor which possesses considerable resistivity as well as capacitance from acting as a lossy transmission line.

2.1.3. Resistors

As for capacitors, many different types of resistors are available in integrated circuits. Other than active devices biased to act as resistors, we can use the inherent resistivity of the polysilicon or diffusions to create resistors. The following table shows the typical values of resistance for the AMI 0.5µm process.

PROCESS PARAMETERS	**N+**	**P+**	**POLY**	**M1**	**M2**	**UNITS**
Sheet Resistance	83.9	109.5	22.3	**0.09**	**0.09**	**ohms/sq**
Contact Resistance	64.7	169.6	15.6	**0.90**		**ohms**

The total resistance of a monolithic resistor is the sum of the contact resistance and the ohmic resistance of the diffusion material. The following formula can be used to estimate resistance for polysilicon and diffusion resistors:

$$R = R_S \cdot \frac{L}{W} + 2 \cdot R$$

where:

R_S is the resistance per square for the chosen resistor type L is the length of the resistor W is the width of the transistor R_C is the contact resistance

Figure 2-9 shows a polysilicon resistor layout. The resistor is constructing by adding a strip of poly and then by adding poly contacts. Next the "res_id" layer is added which tells the extraction program that this is a resistor that needs to be included in the extracted netlist.

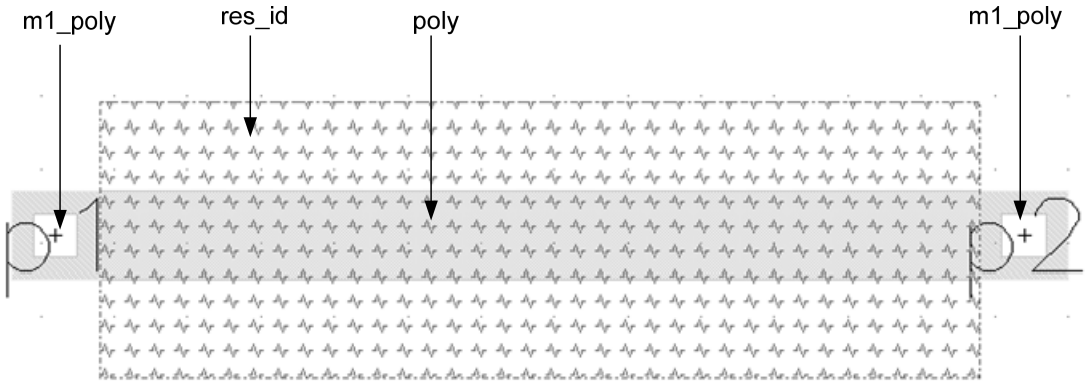


Figure 2-9: Poly resistor layout

If the circuit operation depends on the ratio of resistance, then good matching can be obtained by using interdigitized or common-centroid techniques. When matching resistors, be sure to keep device orientation and sizes the same. Also, since contacts contribute resistance, keep the contacts in the same ratio. An interdigitized layout of resistors is illustrated in Figure 2-10. Notice that the interconnecting metal is overlapping the resistor array and non-overlapping the resistor array in equal lengths for the two resistors.

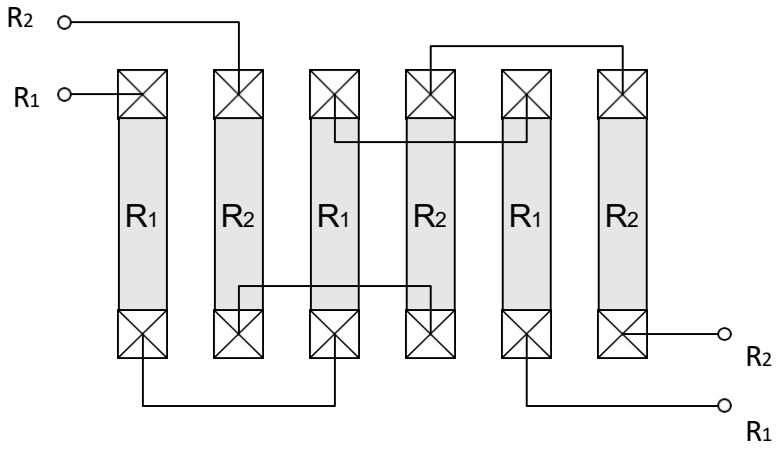


Figure 2-10: Interdigitized resistor layout

3. Lab

- Design and simulate the operation of a 5-stage buffer designed to drive a 5 pF load, starting with the inv1 cell. Plot the propagation delay, using hand calculations, of the buffer, vs load capacitance (up to 5 pF). Compare your hand calculations, on the same plot, against simulation results.
- Lay out the 5-stage buffer. Use a strategy for laying out wide transistors discussed in this lab. Verify that the layout satisfies all DRC and LVS rules.
- Suppose an inverter is driving a 5 pF capacitive load at 100 MHz. Neglecting the power dissipated by the inverter because of cross-over (contention) current (the current that flows from VDD directly to ground when both MOSFETs are on) estimate the power dissipated by the circuit. How much power is dissipated by the NMOS? By the PMOS? Show your work.
- Lay out a differential pair where each transistor has W/L = 10/2. Use a common-centroid strategy of your choice.

4. What to Turn In

A single document containing the following:

- Please indicate how many hours you spent on this lab. This will not affect your grade but will be helpful for calibrating the workload for the future.
- Copy of your hand calculations
- Plot of propagation delay vs. load capacitance (theory and simulation)
- A printout of your inverter layouts and the entire 5-stage buffer.
- A printout of your differential pair layout.