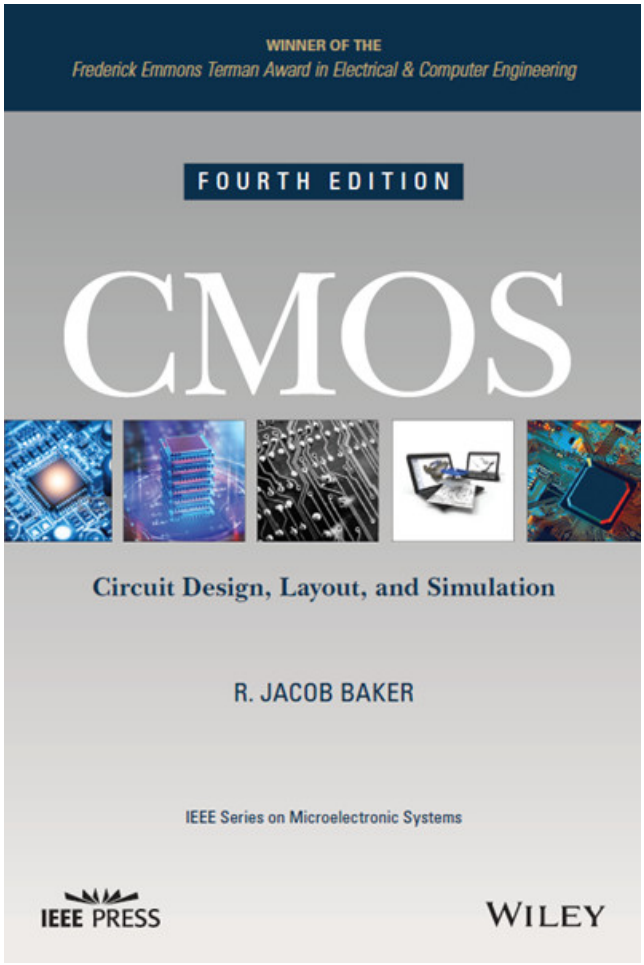
VLSI Design
Homework 2 (Midterm Practice Part 2)
Due Date: Mar. 7, 2024 @ 1:15pm (Not Graded)

Description: This assignment will survey what you have learned thus far using problems from R. Baker's "CMOS Circuit Design, Layout, and Simulation", custom problems designed by the instructor, and layout examples provided by the ARM educational kit in collaboration with the Sky130 open source PDK.

Associated Reading Material:
Chapter 2. The Well.
Chapter 3. Metal Layers.
Chapter 4. Active and Poly Layers.
Chapter 5. Resistors, Capacitors, MOSFETS.
Chapter 6. MOSFET Operation.
Chapter 7. CMOS Fabrication.
Chapter 11. The Inverter.
Chapter 12. Static Logic Gates.
Chapter 15. CMOS Layout Examples.



Problem 7. Multiple Choice Concepts.

Choose the best answer for each question:

1. Which of the following is true for an NMOS transistor operating in its *linear* or *triode* mode? (Vgs = gate to source voltage, Vds = drain to source voltage, Vt = threshold voltage)
   (a) Vds < (Vgs - Vt)
   (b) Vds > (Vgs - Vt)
   (c) Vgs < Vt
   (d) Vgs = 0v

2. Which of the following would result in the largest β?
   (a) NMOS w=3μ l=0.6μ
   (b) NMOS w=0.6μ l=3μ
   (c) PMOS w=3μ l=0.6μ
   (d) PMOS w=0.6μ l=3μ

3. The capacitance of a transistor gate is proportional to what?
   (a) The width of the gate
   (b) The length of the gate
   (c) The area of the gate
   (d) The depth of the channel

4. Which of the following processing techniques would be used to create a transistor's source and drain regions?
   (a) Oxidation
   (b) Ion implantation
   (c) Sputtering
   (d) Polysilicon deposition

Solution:

Problem 8. Short Answer Concepts.

1. How would you use Logical Effort to design a circuit that starts with a unit-sized inverter (W=1.5 μm for the NMOS and W=3 μm PMOS) that eventually has to drive a load 100 times as large as the unit inverter's input load?

2. Describe five sources of power dissipation in static CMOS circuits. Which is the most dominant source of power dissipation in today's circuits? What about future circuits in processes with deep sub-micron gate lengths?

Solution:

Problem 9. CMOS Transistor Theory.
Consider a CMOS inverter which has ideal transistors with the following characteristics:
PMOS transistor: W/L = 2; μ_P= 72 $cm^2/V*s$; V_T= -0.4V
NMOS transistor: W/L = 1; μ_N = 180 $cm^2/V*s$; V_T = 0.4V
180 nm process; C_{ox}/unit area= 8.6E-7 F/cm^2; V_{DD} = 1.8V

a. Calculate β for each transistor, including the units.
b. What modes of operation is each transistor in when V_{in} = 0 V, 0.9 V, and 1.8 V?
c. Estimate the current through the inverter if V_{in} = 0.9 V. List any assumptions you make.
d. Would you expect the current to be higher or lower if the inverter were implemented in a 130 nm process?

Solution: