E399/599: VLSI Design

Lab 1 – Introduction to Digital Cell Design, Simulation, and Verification

SOLUTIONS

Assumptions used in this lab:
SkyWater S130 V0.01
$\lambda = 0.065\mu m$

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nor2: 2-input NOR gate: nor2
W_N=8 λ=520nm
W_P=16 λ=1.04µm

Schematic

The nor2 diagram is shown in Figure 1. The gate uses pfet_01v8 (W=1.04 µm, L=150 nm) and nfet_01v8 (W=520 nm, L=150 nm) cells. The inputs are 'a' and 'b' and the output is 'y'. V_{DD} is provided via a global VDD symbol and V_{SS} is provided via a global GND symbol.

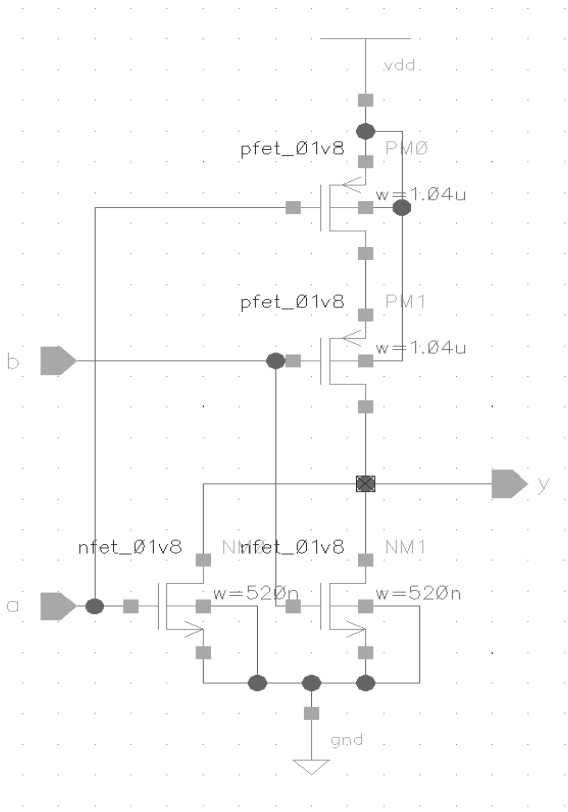

Figure 1. nor2 schematic.

DC Simulation

The switching characteristics of the nor2 cell were simulated by using the DC simulation tool and the Spectre simulation software. Figure 2 shows the output ‘y’ (shown in pink) versus the input ‘a’ (shown in green) for two cases: (1) input ‘b’ was held fixed to 0 V and (2) input ‘b’ was equal to ‘a’ as the input was swept from 0 V to VDD in 0.05 V increments. In both cases, the output switches from VDD to 0V as expected and prior to ‘a’ reaching the midpoint (0.9 V). This “early switching” indicates that the strength of the pull-down network is greater than the pull-up network, which is accentuated in the case where ‘b’=’a’.

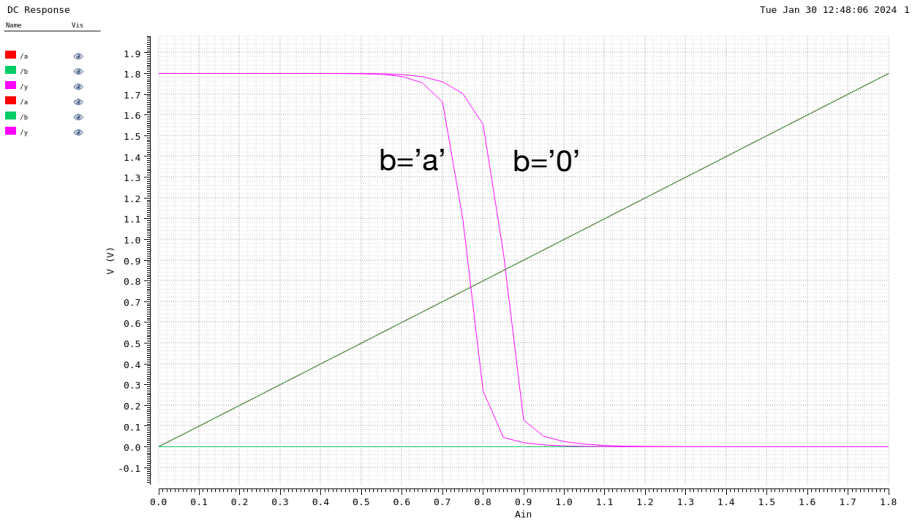

Figure 2. DC simulation results of nor2.

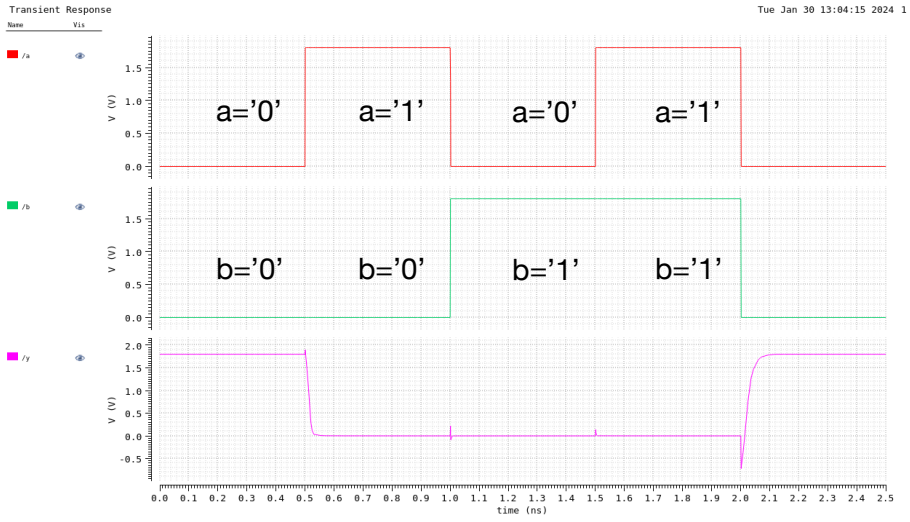

Figure 3. Transient simulation results of nor2.

Transient Simulations

Transient simulations were conducted using the TRAN simulation tool and the Spectre simulation software. Figure 3 shows the output ‘y’ (shown in pink), along with the input ‘a’ (shown in red) and input ‘b’ (shown in green) for a 2.5 ns period. Pulse source functions were applied to inputs ‘a’ and ‘b’ so that all input combinations of ‘b-a’ were applied in a sequence (0-0, 0-1, 1-0, 1-1, and 0-0). The results indicate a functioning gate with clear transitions at the output.

Layout

Figure 4 shows the layout of the nor2 cell. The cell is 6.5 μm tall by 1.57 μm wide. The pmos and nmos transistors share common diffusions, allowing for the cell to be compressed horizontally. Vertically, the cell is designed to be 12-track, with inputs ‘a’ and ‘b’ separated by 1 metal track spacing, where the output ‘y’ is located. The power rails are designed to be 520 nm wide. Figures 5 and 6 show the DRC and LVS results. One DRC flag is noted (licon.12), indicating that there is a diffusion region without a contact (i.e., net1 between the 2 pmos transistors), though there is no violation.

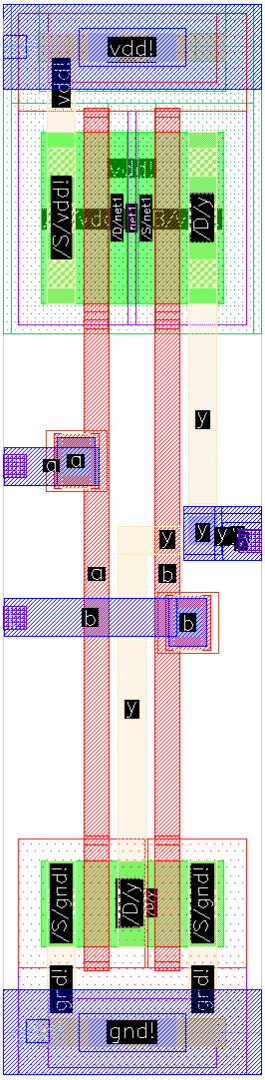

Figure 4. Layout of nor2 gate.

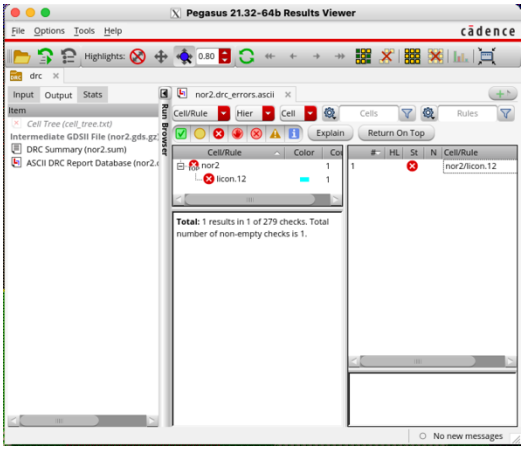

Figure 5. DRC Results for nor2 cell, indicating a single licon.12 warning.

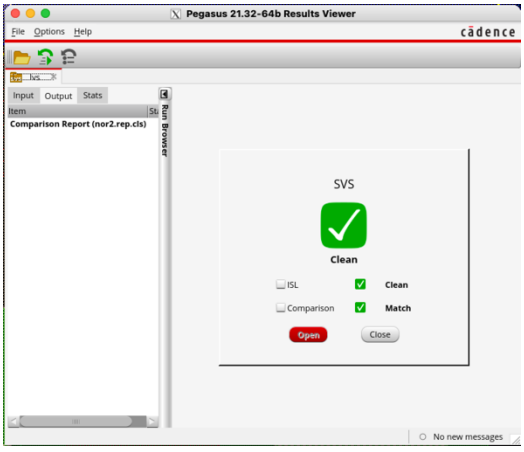

Figure 6. LVS results for nor2 cell.

Or2

or2: 2-input OR gate: or2

The or2 gate is designed with the nor2 from the previous section, and an inv1 cell. All nmos and pmos transistors use:

W_N=8 λ=520nm

W_P=16 λ=1.04µm

Schematic

The or2 diagram is shown in Figure 7. The gate uses the nor2 with pfet_01v8 (W=1.04 µm, L=150 nm) and nfet_01v8 (W=520 nm, L=150 nm) cells as well as a custom inv1 cell using the same parameters. The inputs are ‘a’ and ‘b’ and the output is ‘y’. V_{DD} is provided via a global VDD symbol and V_{SS} is provided via a global GND symbol.

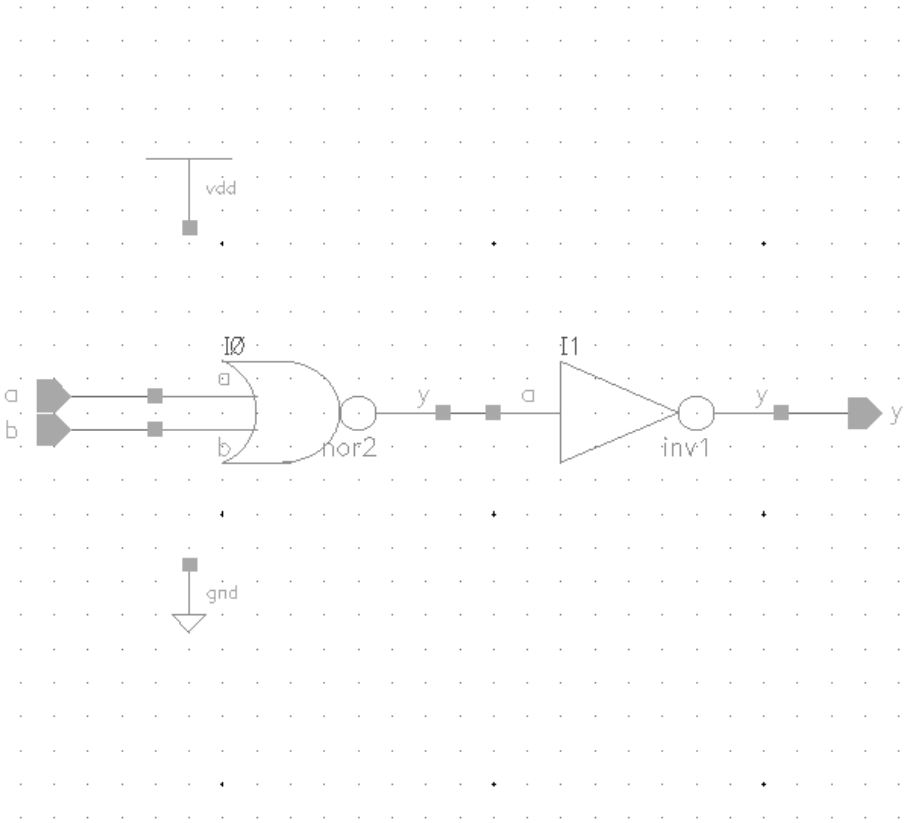

Figure 7. or2 schematic.

DC Simulation

The switching characteristics of the or2 cell were simulated by using the DC simulation tool and the Spectre simulation software. Figure 8 shows the output ‘y’ (shown in pink) versus the input ‘a’ (shown in green) for two cases: (1) input ‘b’ was held fixed to 0 V and (2) input ‘b’ was equal to ‘a’ as the input was swept from 0 V to VDD in 0.05 V increments. In both cases, the output switches from 0V to VDD as expected and prior to ‘a’ reaching the midpoint (0.9 V). This “early switching” is a result of the mismatch in the nor2 as previously discussed. Note that since the nor2 cell is followed by the inv1 cell, the switching characteristics are sharper – this is due to the two gates in series both having to reach their switching points before passing the logic state.

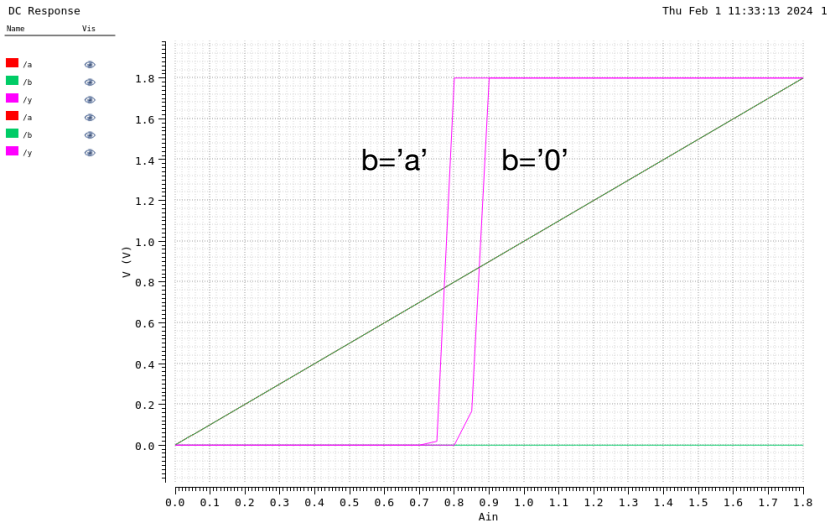

Figure 8. DC simulation results of nor2.

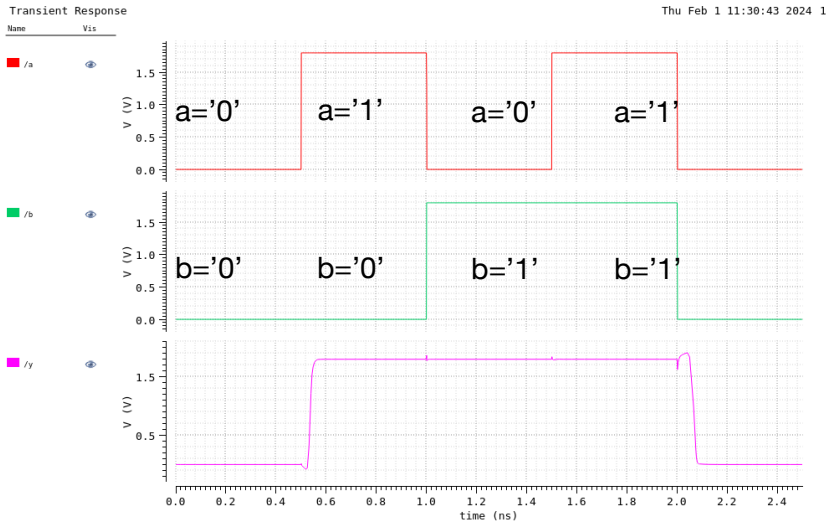

Figure 9. Transient simulation results of or2.

Transient Simulations

Transient simulations were conducted using the TRAN simulation tool and the Spectre simulation software. Figure 9 shows the output ‘y’ (shown in pink), along with the input ‘a’ (shown in red) and input ‘b’ (shown in green) for a 2.5 ns period. Pulse source functions were applied to inputs ‘a’ and ‘b’ so that all input combinations of ‘b-a’ were applied in a sequence (0-0, 0-1, 1-0, 1-1, and 0-0). The results indicate a functioning gate with clear transitions at the output.

Layout

Figure 10 shows the layout of the or2 cell. The cell is 6.5 μm and consists of the nor2 and inv1 cells adjacent to each other. The cell was designed such that the output of the nor2 lines up with the input on the inv1 cell without the need for additional metal routing in the top level. Figures 11 and 12 show the DRC and LVS results. One DRC flag is noted (licon.12), indicating that there is a diffusion region without a contact (i.e., net1 between the 2 pmos transistors within the nor2), though there is no violation.

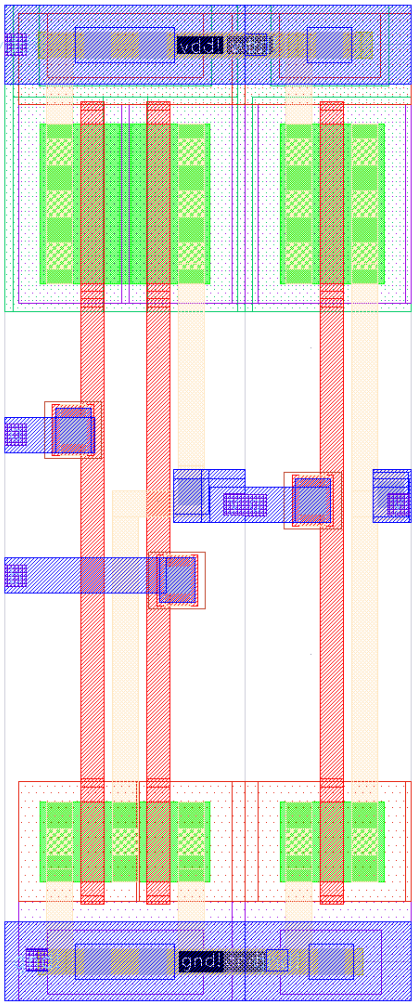

Figure 10. Layout of or2 gate.

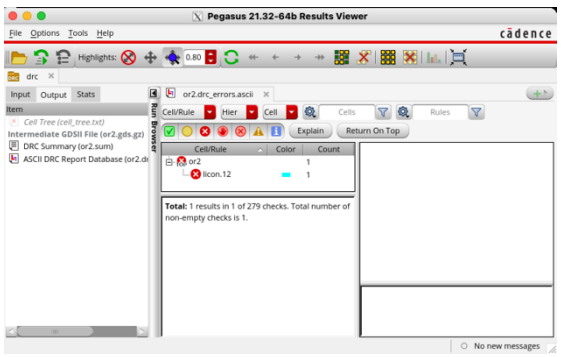

Figure 11. DRC Results for nor2 cell, indicating a single licon.12 warning.

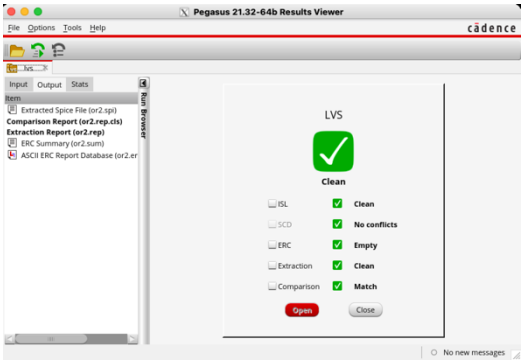

Figure 12. LVS results for nor2 cell.