Microelectronics Radiation Effects and Reliability

HW 5

Mitigation of Single-Event Effects

Issue 1.0

1 Introduction

This HW explores strategies for mitigating single-event effects (SEE) through simulation using the LTSpice IV software. Single-event transients (SET) and single-event upsets (SEU) will be analyzed in sequential logic cells, and various strategies for increasing the critical charge to upset will be evaluated.

LTSpice IV can be downloaded here: https://www.analog.com/en/resources/design-tools-and-calculators/ltspice-simulator.html. Before beginning the assignment, it is recommended that you complete the Getting Started Tutorial, review the LTSpice IV tutorials from class, and complete HW 3.

In the first part of this HW assignment, you will download a D Flip-Flop cell and simulate the various SEU responses, resulting in an estimate of the critical charge. In the second part of the assignment, you will employ capacitive, resistive, and current compensation strategies for mitigation.

2 Learning Objectives

At the end of this lab, you should be able to:

- Design and demonstrate SEE mitigation solutions

3 SPICE Models

This assignment uses the following custom LEVEL 3 SPICE models:

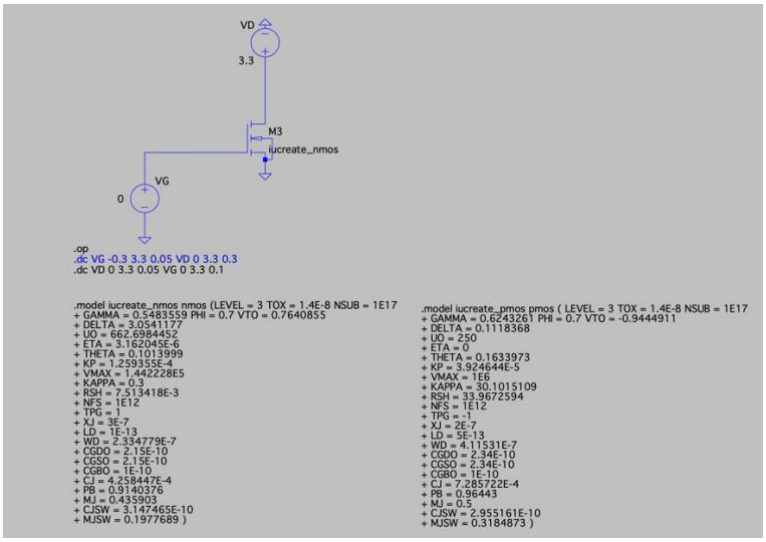
```
.model iucreate_nmos nmos (LEVEL = 3
+ TOX = 1.4E-8
+ NSUB = 1E17
+ GAMMA = 0.5483559
+ PHI = 0.7
+ VTO = 0.7640855
+ DELTA = 3.0541177
+ UO = 662.6984452
+ ETA = 3.162045E-6
+ THETA = 0.1013999
+ KP = 1.259355E-4
+ VMAX = 1.442228E5
+ KAPPA = 0.3
+ RSH = 7.513418E-3
+ NFS = 1E12
+ TPG = 1
+ XJ = 3E-7
+ LD = 1E-13
+ WD = 2.334779E-7
+ CGDO = 2.15E-10
+ CGSO = 2.15E-10
+ CGBO = 1E-10
+ CJ = 4.258447E-4
+ PB = 0.9140376
+ MJ = 0.435903
+ CJSW = 3.147465E-10
+ MJSW = 0.1977689 )
.model iucreate_pmos pmos (LEVEL = 3
+ TOX = 1.4E-8
+ NSUB = 1E17
+ GAMMA = 0.6243261
+ PHI = 0.7
+ VTO = -0.9444911
+ DELTA = 0.1118368
+ UO = 250
+ ETA = 0
```

+ THETA = 0.1633973
+ KP = 3.924644E-5
+ VMAX = 1E6
+ KAPPA = 30.1015109
+ RSH = 33.9672594
+ NFS = 1E12
+ TPG = -1
+ XJ = 2E-7
+ LD = 5E-13
+ WD = 4.11531E-7
+ CGDO = 2.34E-10
+ CGSO = 2.34E-10
+ CGBO = 1E-10
+ CJ = 7.285722E-4
+ PB = 0.96443
+ MJ = 0.5
+ CJSW = 2.955161E-10
+ MJSW = 0.3184873)

The custom technology can be assumed to be generally reflective of a 0.5 µm CMOS technology node with the following specifications:

Parameter	Value
Gate Length (minimum), Lmin	0.5 µm
Gate Width (minimum), Wmin	1.5 µm
NMOS Threshold Voltage (VTN)	0.9 V
PMOS Threshold Voltage (VTP)	-1 V

In LTSPICE IV, the models can be copied and pasted into a SPICE directive in a schematic as shown below, or saved as a .model file and referenced in a .include SPICE directive statement. Be sure to use the **nmos4** and **pmos4** symbols in LTSpice IV when creating your schematic. Once a device is placed, right-click the device and change the **Model:** field to point to the appropriate model (iucreate_nmos or iucreate_pmos). You may adjust the Length and Width parameters of each instance as well.



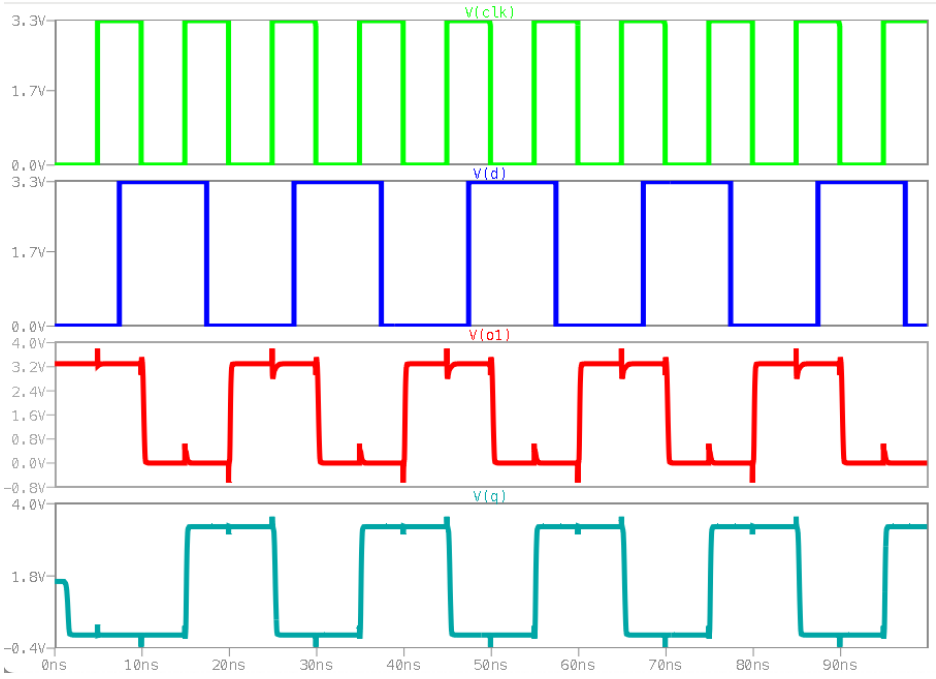
The following SPICE files are required for this HW:

- dff_rh_ex

4 Baseline Performance of a DFF

Before proceeding, download the LTSPICE IV examples and ensure that you are comfortable with .OP, .DC, and .TRAN simulations.

- dff_rh_ex: In this simulation deck, connect source D2 to the input of the DFF (node D) and remove the connection to source D1. Plot the CLK signal, data input D, and nodes o1 and to reproduce the DFF transient charts below. Save the file as “dff_rh_hw5”.



CLK (top), D (upper middle), o1 (lower middle), and output O (bottom) signals for provided DFF simulation deck. The simulation shows a 100 MHz signal clocking in a data pattern of alternating 1s and 0s (i.e., 0101010101). The output O is aligned with the rising edge of the clock signal.

QUESTION 1: Adjust the clock frequency to 200 MHz but leave the data input unchanged. What is the resulting data pattern?

QUESTION 2: Continue to double the clock frequency. What is your best estimate of the maximum clock frequency before the DFF is unable to capture the data?

- dff_rh_hw5: When the clock signal is 100 MHz, modify the provided SET current source model, attaching it to node *o1* as a strike to transistor *M1*. Take care to ensure the correct directionality. Adjust the paramter IPEAK to be 1 mA and ensure the TS parameter is 25 ns (note that this is the start time of the ion strike).

QUESTION 3: Provide a chart showing the *CLK (top), D (upper middle), o1 (lower middle), and output O (bottom) signals.* Explain the observed response; what is the output data pattern? Is there an SEU? What was the collected charge?

- Uncomment the line starting with ".step param IPEAK".

QUESTION 4: Vary the value of IPEAK to determine the critical charge (a 0.1 mA accuracy of IPEAK is fine) when M1 is struck at 25 ns. Provide a chart showing the responses of nodes *o1* and *O* when the collected charge is just below and just above the critical charge.

- Comment the line starting with ".step param IPEAK" and adjust the value of parameter IPEAK so that you are simulating the SEU at the determined critical charge. Uncomment the line starting with ".step param TS" and adjust the sweep of the TS parameter to be between 25 ns and 35 ns.

QUESTION 5: What is the most sensitive time during the clock cycle for strikes on M1?

QUESTION 6: Choose a time of strike, TS, of 32 ns. Determine the critical charge to upset.

QUESTIONS 7-10: Repeat Q3-6 for a clock frequency of 200 MHz. Are there any differences? Why?

QUESTIONS 11-14: Repeat Q3-6 for a PMOS strike on transistor M2. What is the critical charge and the most sensitive time during the clock cycle to the SEU?

- Compare the NMOS and PMOS sensitivity. Choose the most vulnerable state: NMOS vs. PMOS strike, time of strike, and critical charge. Uncomment the line starting with ".step param CL" and adjust the sweep

QUESTIONS 15: How much capacitance, CL, is required to increase the critical charge by 100 fC?

QUESTIONS 16: What the applied hardening capacitors, what is the new maximum frequency of operation?

5 What to Turn In

A single document uploaded to Canvas containing the following:

1. Please indicate how many hours you spent on this HW. This will not affect your grade but will be helpful for calibrating the workload for the future.
2. Answers to the 16 questions, along with supporting work. Results in the form of simulation printouts are encouraged – with supporting statements.