Journal Club: Minimum Size and Maximum Packing Density of Nonredundant Semiconductor Devices

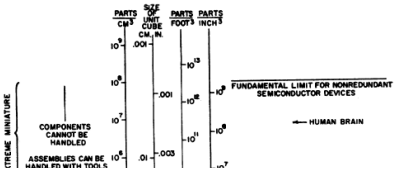
Daniel Loveless
Director, IU Center for Reliable and Trusted Electronics (IU CREATE)
Associate Professor of Intelligent Systems Engineering
Luddy School of Informatics, Computing, and Engineering
Indiana University Bloomington

Article Information

Minimum Size and Maximum Packing Density of Nonredundant Semiconductor Devices*

J. T. WALLMARK†, SENIOR MEMBER, IRE, AND S. M. MARCUS‡, MEMBER, IRE

Summary—It is shown that there exists an absolute lower limit to device size and an absolute upper limit to packing density of nonredundant semiconductor devices, whether integrated or non-integrated, based on fundamental physical phenomena such as statistical variations in impurity distribution, maximum resolution of semiconductor fabrication methods, power density and influence of cosmic rays. The influence of these phenomena falls in two categories, namely failures that appear during the fabrication of the devices (impurity distribution, dividing operation) and failures that appear during use. The latter may be temporary failures (cosmic



J. T. Wallmark and S. M. Marcus, "Minimum Size and Maximum Packing Density of Nonredundant Semiconductor Devices," *Proc. of the IRE*, vol. 50, no. 3, pp. 286-298, March 1962.

Overview of Wallmark and Marcus, 1962

- Wallmark and Marcus claim a lower limit to semiconductor device size and upper limit to semiconductor packing density based on:
  - Statistical variations
  - Fabrication resolution
  - Power density
  - Cosmic rays!
- The lower limit to device size (active dimension) is claimed to be about 2 μm (in 1962, the minimum semiconductor dimension (feature size) was ~ 10 μm)

The Proceedings of the IRE

- Journal was stablished in 1913 as a flagship publication of the Institute of Radio Engineers (IRE), ceasing production in 1962.
- IEEE was formed in 1963 (1 year after the topic paper) following a merger of IRE with the American Institute of Electrical Engineers. Now, the *Proceedings of the IEEE* is ranked 5th by the *Journal of Citation Reports* – based on impact factor.
- Current impact factor of *Proceedings of the IEEE* is 10.961 (measure of the frequency with which the average article in a journal has been cited in a particular year
- Single-blind peer review

Wallmark and Marcus, 1962

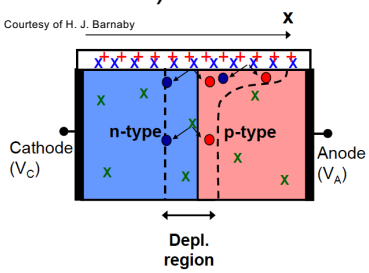
- J. T. Wallmark and S. M. Marcus, "Minimum Size and Maximum Packing Density of Nonredundant Semiconductor Devices," in *Proceedings of the IRE*, vol. 50, no. 3, pp. 286-298, March 1962, doi: 10.1109/JRPROC.1962.288321.
- Most cited paper (93) in vol. 50, no. 3
- J. T. Wallmark was a Swedish scholar (Chalmers University moved to U.S. RCA Labs in Princeton) with 20 listed publications in IEEE (471 total citations between 1952-1988)
- S. M. Marcus (Defense Electronics Products, RCA and Univ. PA) only published 4 papers between 1959-1962 (with 106 citations)
- Paper was funded by AF Cambridge Research Labs, Office of Aerospace Research (1945-2011) – founded as a Cold War systems development organization. Consolidated under Air Force Research Labs (AFRL).

The Context

- The author's published this paper only 15 years after the first transistor was invented!
- Two major claims are stated:
  - lower limit to semiconductor device size
  - upper limit to semiconductor packing density based
- A number of insightful analyses in regard to the limitations of semiconductors:
  - Statistical variations
  - Fabrication resolution
  - Power density
  - Cosmic rays!

The Context

- During the 60s, and up through the 80s, cosmic rays were really only thought to result in cumulative damage (total dose)



Total-Ionizing Dose (TID) in Microelectronics

Semiconductor device dielectrics:

- **Interface traps** (N_{it}) increase the recombination rate in the depletion region
- **Fixed oxide traps** (N_{ot}) increase the depletion region, thus enhancing recombination
- **Trap defects** increase the generation in RB junctions

The Context

- The prediction that cosmic rays would be a technology limitation because of “single event effects” (authors discuss this as an increase in the probability of failures) is remarkable
- The first anomalies (single event upsets) in satellites were first reported 13 years later (Binder *et al.,* 1975, and Pickel *et al.,* 1978)
- Earliest paper on single event transients in 1984 (Diehl *et al.*)– not an observation, but a simulation study predicting dominate error type!
- The latest major incident was the loss of the Russian Phobos-Grunt mission (2012)

Technology Scaling

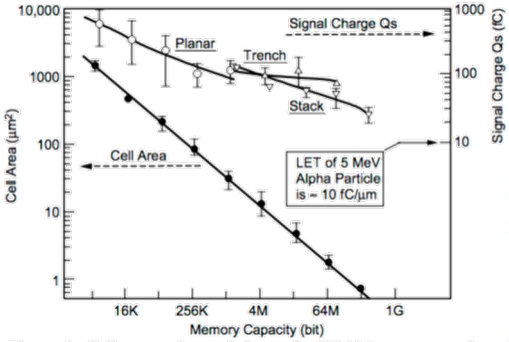
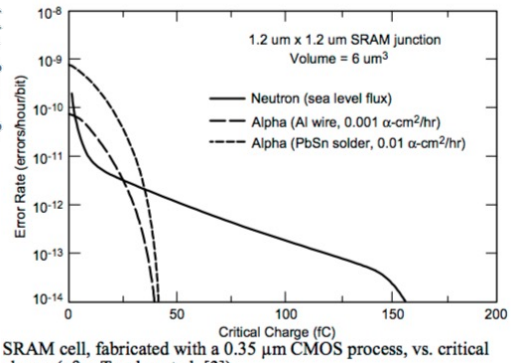


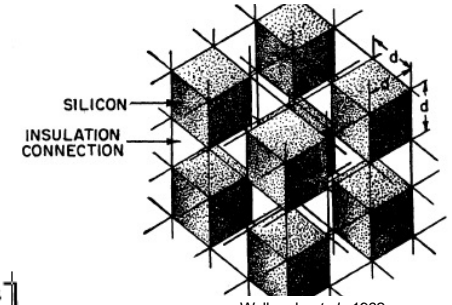
Figure 6. Cell area and stored charge for DRAMs over several generations (after Itoh, et al. [23]).



SRAM cell, fabricated with a 0.35 μm CMOS process, vs. critical charge (after Tosaka, et al. [3]).

Methods

- Assume a basic computing system (10^5) components segmented into cubes
- Resistance is derived and used to examine sensitivity to variability (basic sensitivity analysis by examining parameters that determine resistance)

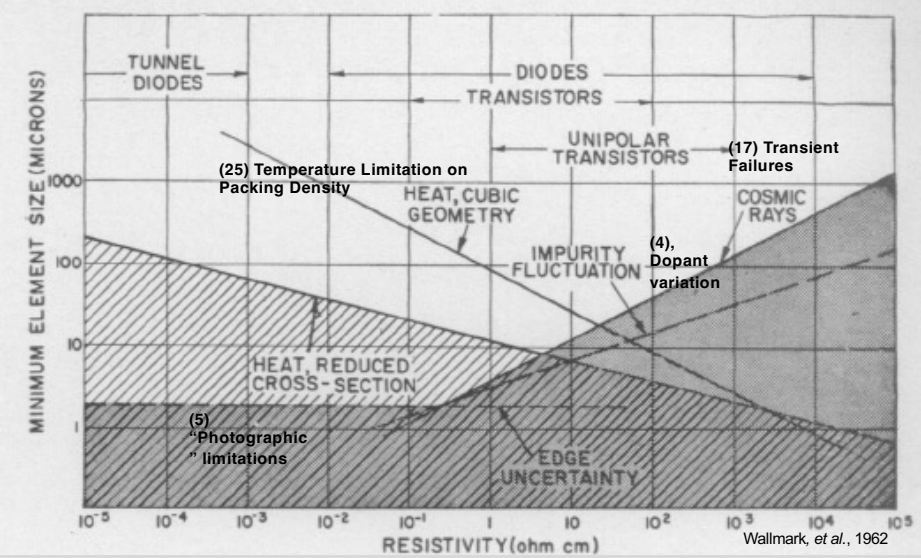


Wallmark, *et al.*, 1962

$$\frac{dR}{R} = -\frac{1}{q}\left[\frac{d(n_1+n)}{n_1+n} + \frac{3dd}{d} + \frac{d\mu}{\mu}\right].$$

Authors use this equation as basis for conjectures that variation in doping and cosmic rays (term 1), mechanical limitations in fabrication (term 2), an power density constrained by temperature (term 3) are the primary concerns for semiconductor advancement

Results



Wallmark, *et al.*, 1962

Conclusions

- Device scaling limited due to variability in doping (impurities), fabrication methods, heat generation, and cosmic rays
- Cosmic rays are the limiting factor for high resistivity (> 5 ohm cm) devices whereas power density limits low resistivity devices
- Methods for circumventing the limitations suggested such as:
  - Redundancy
  - Negative feedback

Discussion Questions

- Do you think that enough justification for this study was presented? Do you think the findings contribute in a meaningful/novel way to the scientific community?
- Authors state that in 1962 the active region of a semiconductor is already close to the minimum possible, yet in 2016 we are 3 orders of magnitude smaller. How? Is this paper still meaningful?
- What were some (technical) aspects of the paper they did well?
- What were some (technical) aspects of the paper they could have done better?
- Did they communicate their method and findings well?
- Would you stash or trash this article?