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Mitigation of Radiation Effects

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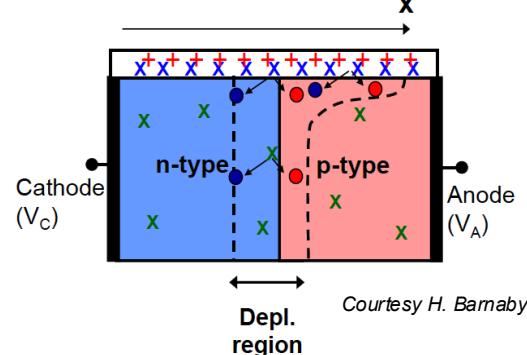
Indiana University Bloomington

Module 6: Objective and Outcomes

- This module will
 - Review TID and SEE
 - Describe the basic strategies for mitigating TID and SEE
 - Show example hardening strategies for devices, circuits, and systems
- Student Outcomes
 1. Students will demonstrate an understanding of TID and SEE at the transistor, schematic, and layout levels.
 2. Students will demonstrate an understanding of the core principles for mitigation of SEE and TID.
 3. Students will show an ability to apply mitigation strategies to design radiation hardened circuits.

Total Ionizing Dose and Basic Mitigation Strategies

Total-Ionizing Dose Effects



Total-Ionizing Dose (TID) in Microelectronics

Semiconductor device dielectrics:

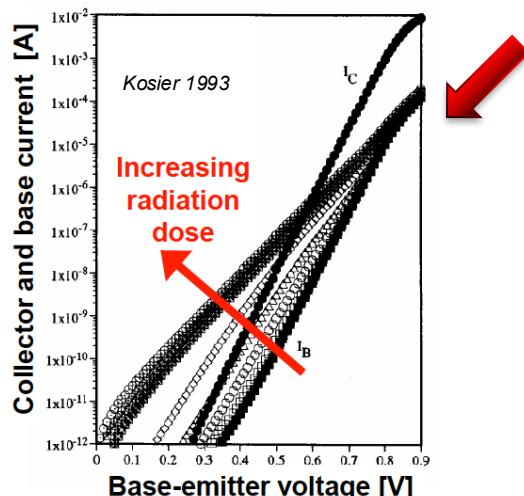
- **Interface traps (N_{it})** increase the recombination rate in the depletion region
- **Fixed oxide traps (N_{ot})** increase the depletion region, thus enhancing recombination
- **Trap defects** increase the generation in RB junctions

In BJTs, TID damage to oxide dielectrics leads to:

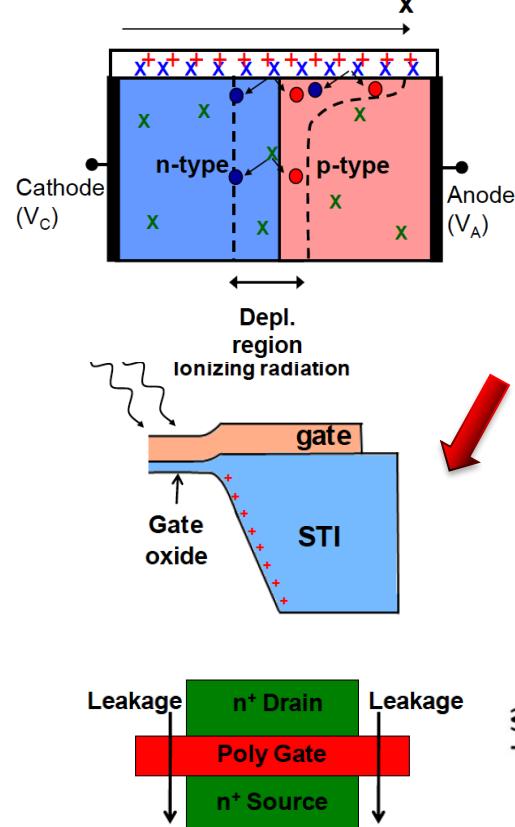
- Excess base current (via enhanced recombination with traps and beta degradation)
- Increased collector current in *npn* devices due to increased emitter area (via surface inversion from N_{ot})
- Increased reversed leakage current from collector to base (CB) due to increased carrier generation (via traps) in CB junction

Enhanced Low-Dose-Rate Sensitivity (ELDRS)

- Larger TID effects observed at low dose-rates (impacts testing methodologies)
- Primarily affects lateral bipolar devices



Total-Ionizing Dose Effects



Total-Ionizing Dose (TID) in Microelectronics

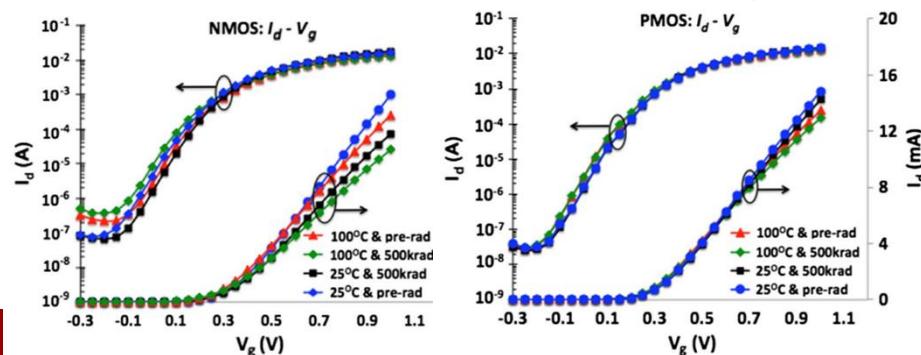
Semiconductor device dielectrics:

- **Interface traps (N_{it})** increase the recombination rate in the depletion region
- **Fixed oxide traps (N_{ot})** increase the depletion region, thus enhancing recombination
- **Trap defects** increase the generation in RB junctions

In CMOS, TID leads to:

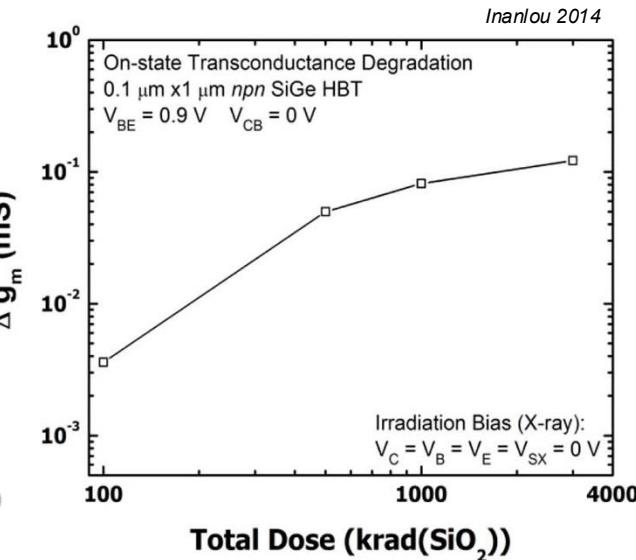
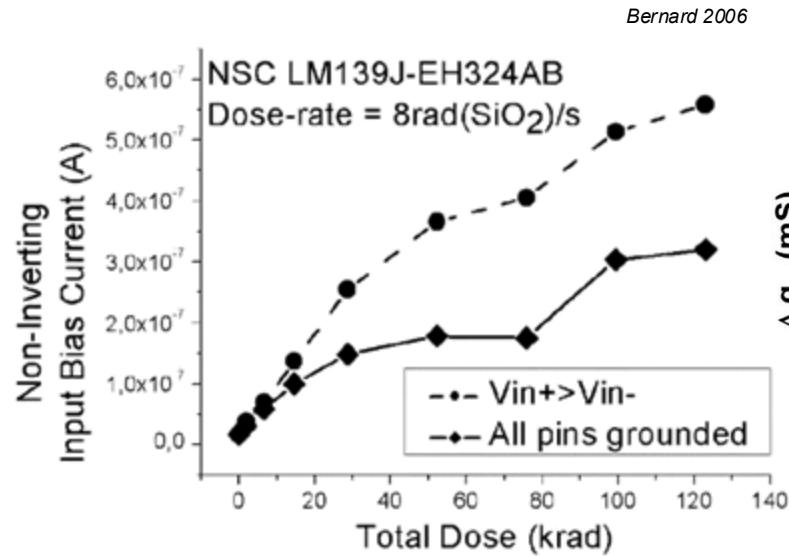
- Threshold voltage (V_t) shifts, sub-threshold slope reduction, and mobility degradation in older CMOS technologies
- Increase intra-device (edge) leakage in nMOS transistors (both old and advanced SOI technologies)
- Increased inter-device leakage in parasitic n-channel devices
- Increased static supply current

Jagannathan 2013



TID in Analog Circuits

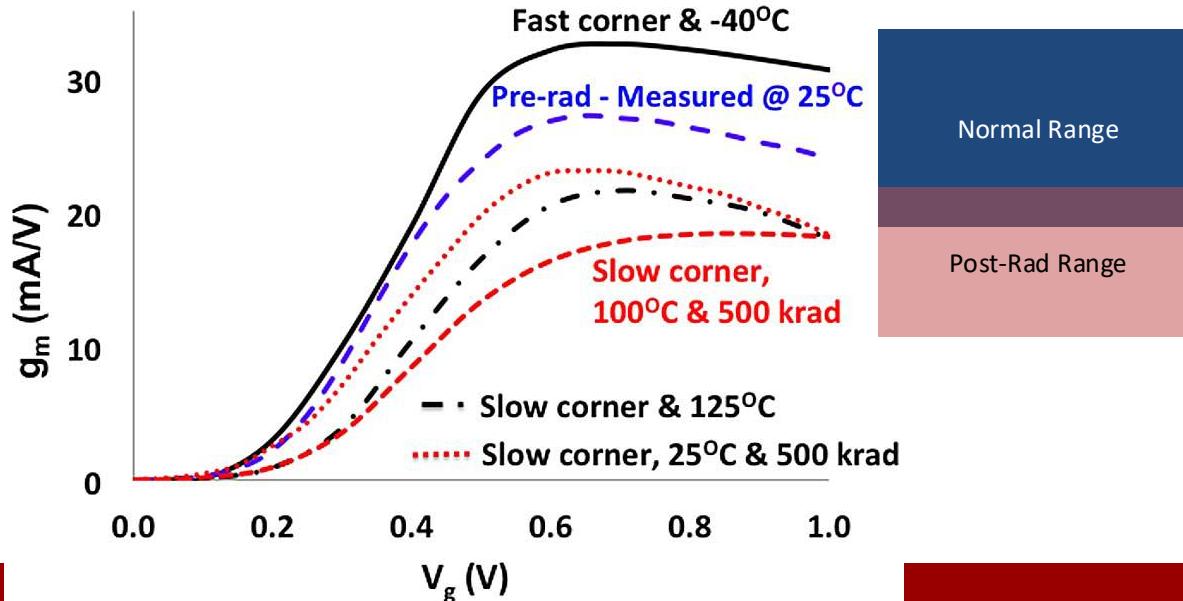
- Mismatch and degradation in AC parameters due to TID tend to be problematic for analog and RF circuits



Importance of Temperature

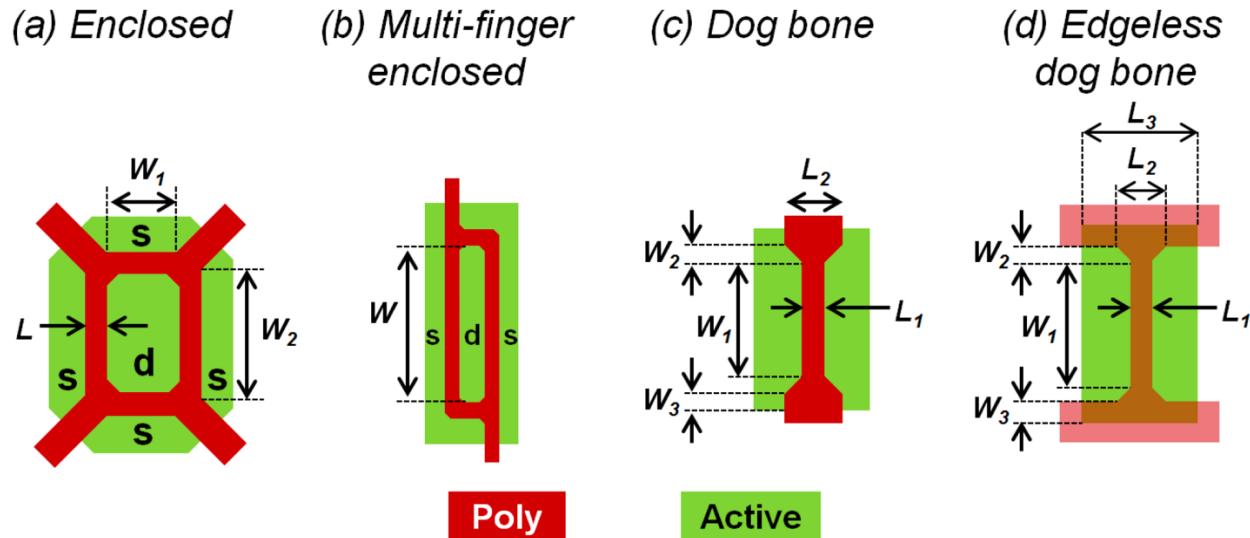
- High Performance RF circuits tend to be ultra-sensitive to TID due to the tight design margins (process, voltage, temperature, radiation)

Process-Voltage-Temperature (PVT) and TID Analysis
of a Commercial RF 45 nm Process Jagannathan 2013



TID Mitigation Through Transistor Layout

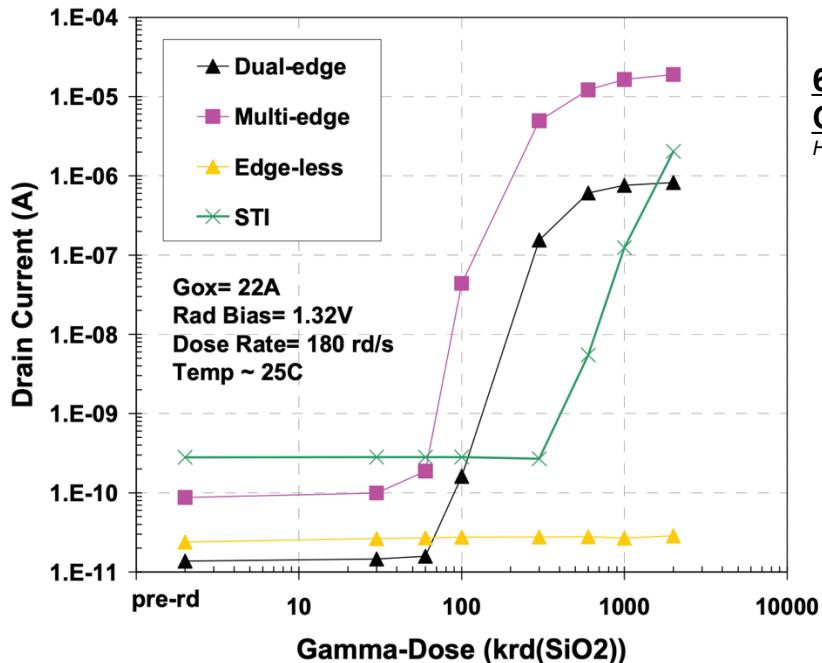
- The most common TID mitigation approach is through individual transistor layout
- Edgeless transistor layout** eliminates the radiation-induced sidewall channel leakage in nFETs and reduces trapped charge in the field oxide bordering the channel that can contribute slightly to threshold voltage shifts



Atkinson 2013

Concentric Edgeless Layout

- Concentric edgeless layout eliminates STI trapped-charge responsible for leakage



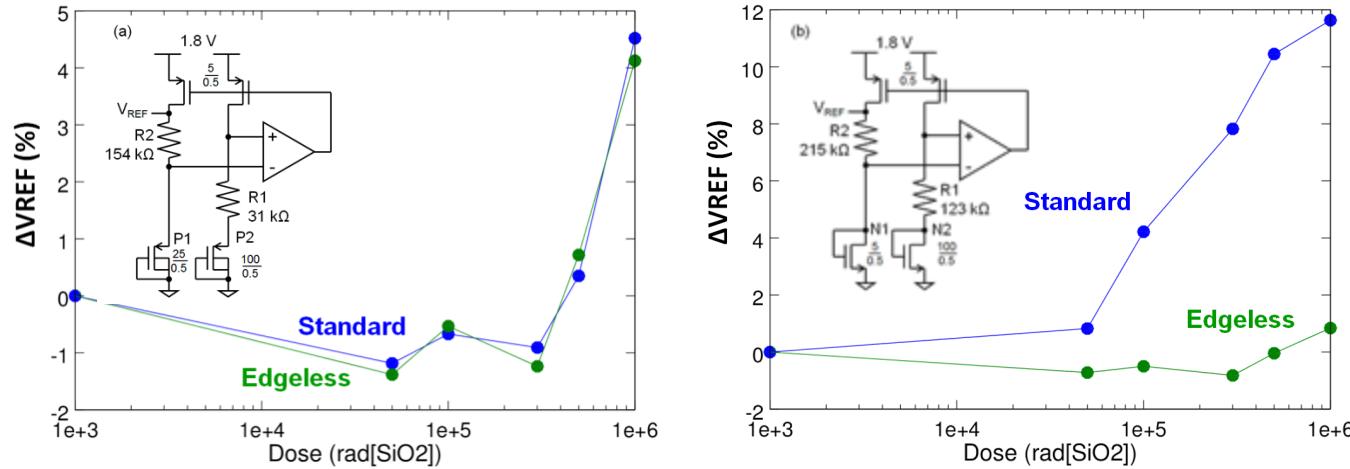
60Co TID Evaluation of a Commercial 90 nm Process
Haddad 2008

Any cell that has not been designed for “critical node isolation” must be investigated for TID-induced failure

Edgeless Layout May Not Help

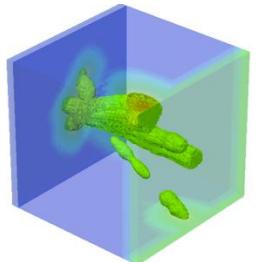
- Dynamic threshold voltage MOSFETs (DTMOS) have appeared as an option for very-low-voltage design – however, TID may not be mitigated through standard layout approaches

Shift in Reference Voltage vs. Dose for DTMOS-Based (Left) and NMOS-Based (Right) Voltage Reference Circuits Atkinson 2013



Single Event Effects and Basic Mitigation Strategies

Single-Event Effects



Courtesy Vanderbilt



Single-Event Effects in Microelectronics

Single-Event Effects (SEE):

- Caused by the interaction of a single energetic particle

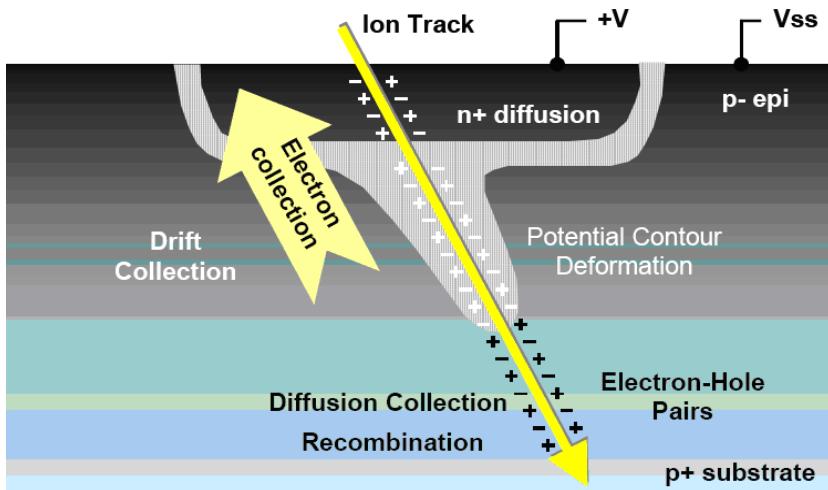
Ionizing Particles:

Heavy ions from deep space
(galactic cosmic rays)

Energetic protons
(trapped in the Van Allen belts)

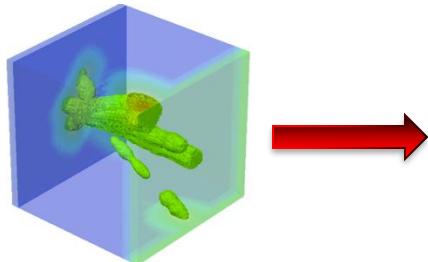
Neutron products
(terrestrial)

Alpha particles
(from contaminants)



Example of Ion Penetrating Reverse-Biased p-n Junction

Single-Event Effects

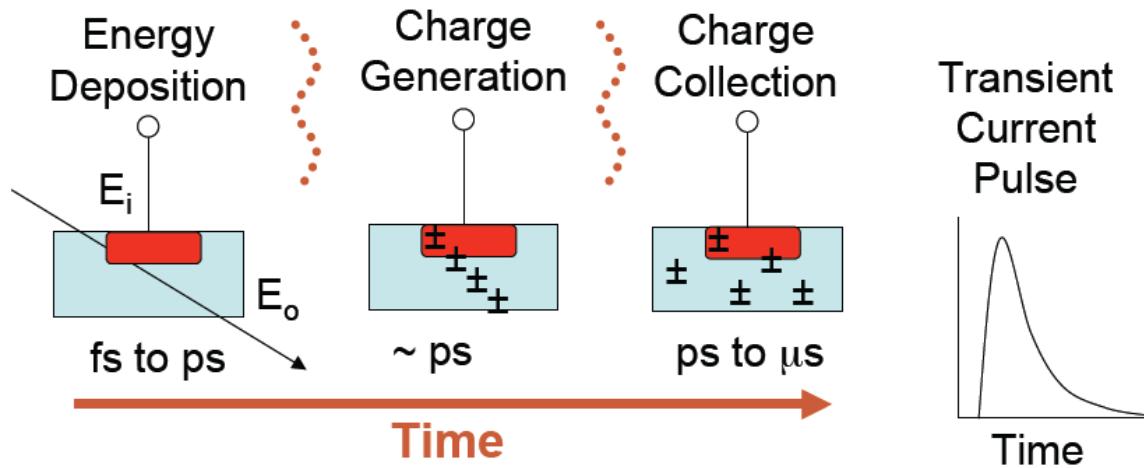


Courtesy Vanderbilt

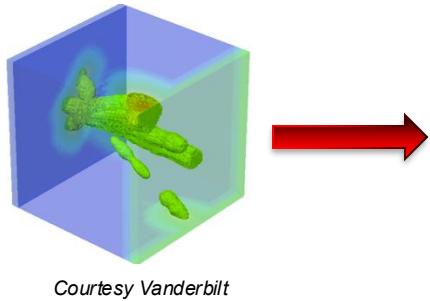
Single-Event Effects in Microelectronics

Single-Event Effects (SEE):

- Caused by the interaction of a single energetic particle
- SEE are determined by:
 - Charge generation
 - Charge collection
 - Circuit response



Single-Event Effects

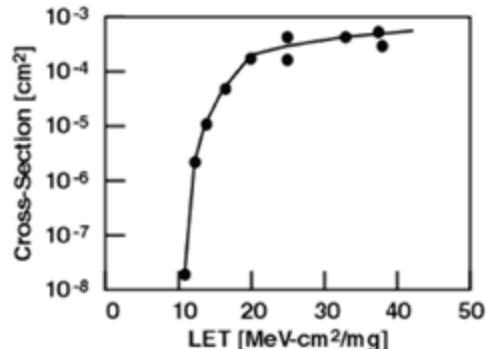


Courtesy Vanderbilt

Important Concepts:

Linear Energy Transfer (LET) & Cross-Section

Sensitive Area vs. LET



Single-Event Effects in Microelectronics

Single-Event Effects (SEE):

- Caused by the interaction of a single energetic particle

- SEE are determined by:

- Charge generation
 - Charge collection
 - Circuit response

- Types:

Non-destructive:

- Single-event upsets (soft errors)
 - Single-event transients
 - Single-event functional interrupt
 - Multiple-bit upsets

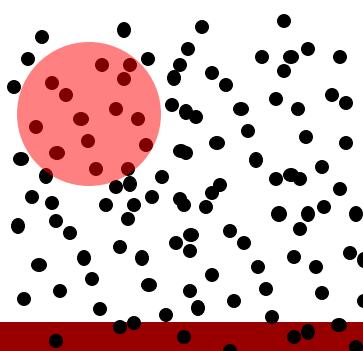
Destructive:

- Single-event latchup
 - Single-event burnout
 - Single-event gate rupture
 - Single-event snap-back

Calculation of Cross-Section

Known Areal Density of Shots (Ions)
Ex. 10 shots/cm²

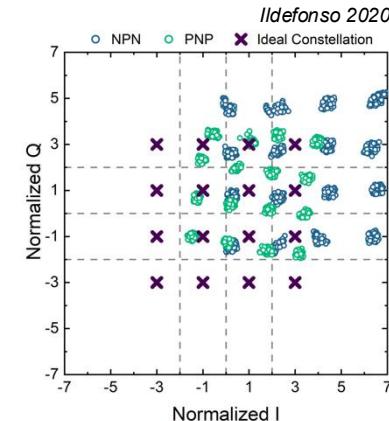
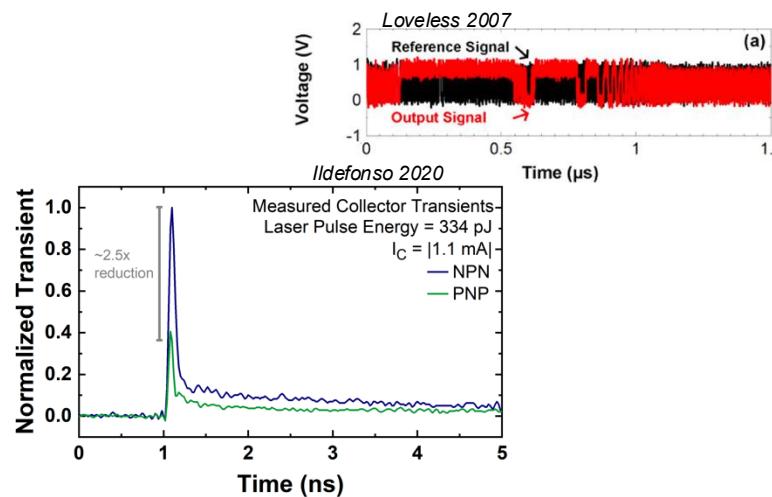
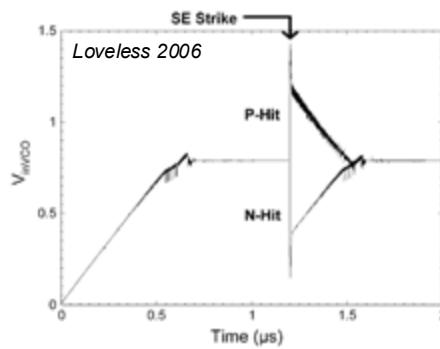
Number of shots that hit an **unknown** target



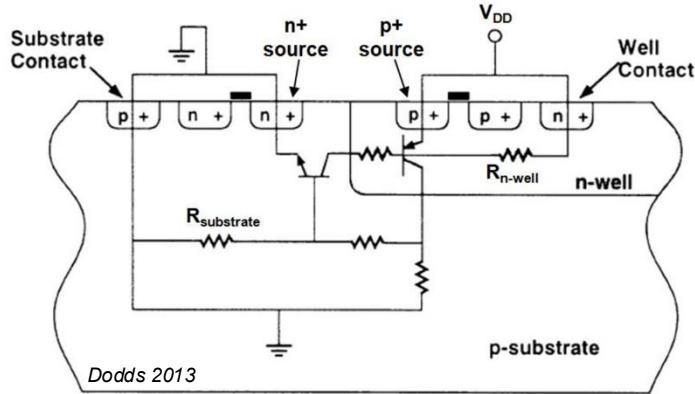
$$\text{Cross-section} = \frac{14 \text{ shots/target}}{10 \text{ shots/cm}^2} = 1.4 \text{ cm}^2/\text{target}$$

Single-Event Transients

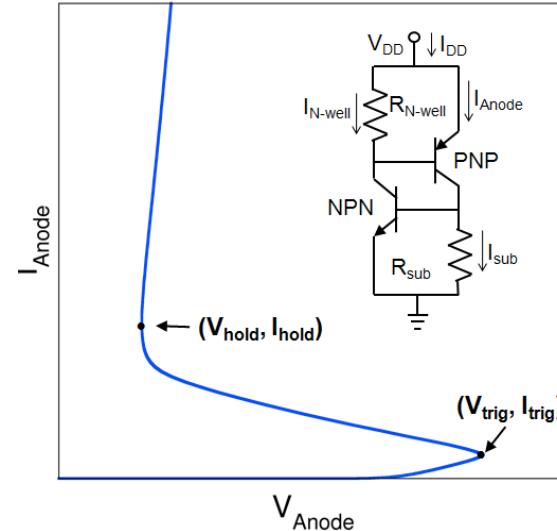
- In digital electronics, an SET may lead to a single-event upset (SEU) – *alteration of memory cell state* – that can propagate through circuit
- In analog electronics, a single-event (SE) particle strike results in a single-event transient (SET)
 - Competes with legitimate signals or perturbs functionality
 - Can result in a wide range of circuit responses



Single-Event Latchup

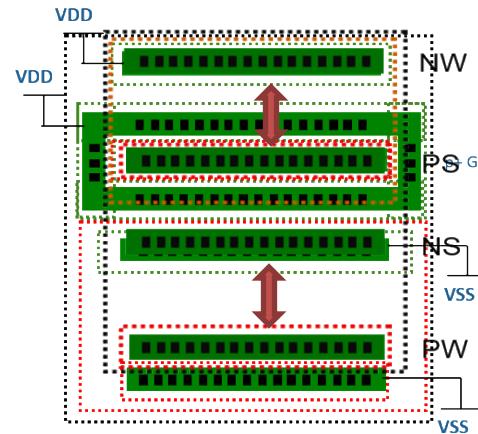
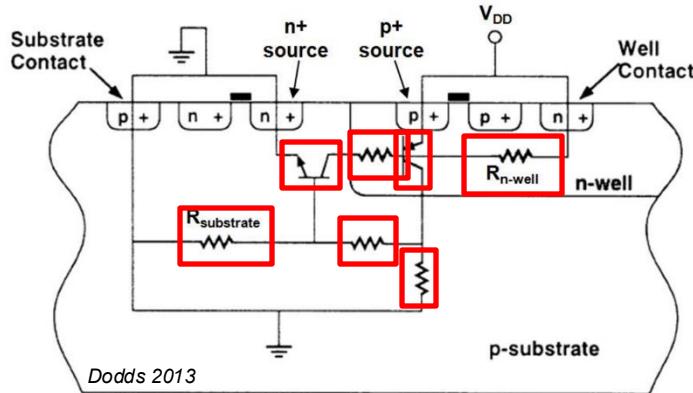


Cross-section of typical CMOS technology showing **parasitic thyristor** that can be triggered into low impedance state



- Latchup occurs when parasitic $p-n-p-n$ regions (*composed of cross-coupled $p-n-p$ and $n-p-n$ BJTs*) are activated by an energetic ionizing particle
- The collector of each BJT is connected to the base of the other, creating a positive feedback loop
- Latchup can occur when:
 - both BJTs conduct, creating a low-resistance path between V_{DD} and V_{SS}
 - the product of the gains in the BJTs in the feedback loop is greater than 1

Single-Event Latchup Mitigation



- Sensitivity depends on parasitic bipolar gains and well/substrate resistances
- Mitigation of SEL involves

- 1) reduction of BJT gain
- 2) decoupling BJTs or increasing the coupling resistance
- 3) decreasing resistances from the BJTs to well and substrate contacts

Process engineering:
channel doping,
decrease source-to-well spacing
Decrease proximity
Increase contact density
strain

Geometry, density, and spacing of wells, sources, source-to-well contacts, and source-to-source contacts have large impact on overall vulnerability

Summary of SEE Mitigation Techniques

- SEE mitigation involves one or both of the following, irrespective of the technology:
 - *reducing the amount of collected charge (Q_{col}) at a metallurgical junction:*
 - layout alternatives such as guard rings, drains, or diodes (MOS)
 - n-rings, substrate-tap rings, and nested minority-carrier guard rings (BJT)
 - substrate engineering: charge blocking layers in the substrate, use of very thin epitaxial silicon layer, silicon-on-insulator (SOI)
 - addition of dummy collector for charge collection in HBT devices
 - increased substrate and well contacts (reduced substrate and well impedances)

Hardening-by-process
(technology modifications)

Hardening-by-design (layout
modifications)

Summary of SEE Mitigation Techniques

- SEE mitigation involves one or both of the following, irrespective of the technology:
 - *reducing the amount of collected charge (Q_{col}) at a metallurgical junction:*
 - *increasing the critical charge (Q_{crit}) required to generate an SET*
conventional, perhaps “brute force” methodology include:
 - increasing the transistor sizes (buffering)
 - increasing the drive currents
 - increasing the supply voltage
 - increasing capacitor sizes

Hardening-by-design
(layout, circuit, and/or system
modifications)

Hardening by Design

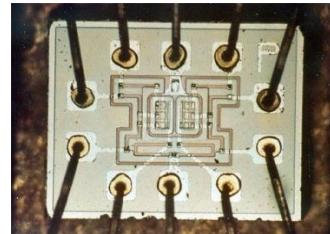
Radiation Hardening by Design

The Big Picture

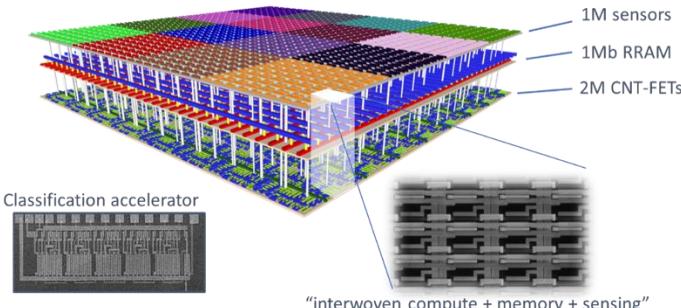
- State-of-the-art chip systems contain billions of transistors, integrated analog and digital, 3D IC stacks, and multiple voltage domains
- Critical charge can be just a few fC

Challenges for RHBD

- Integration of process, layout, topology, and system-level approaches
- Architecture-level SE simulation and high-level RHBD approaches
- SEE for low-power circuits
- Development and analysis of RHBD libraries
- Effects of **charge-sharing**
- Integrated modeling, simulation and experimental analysis methodologies for advanced technology ICs

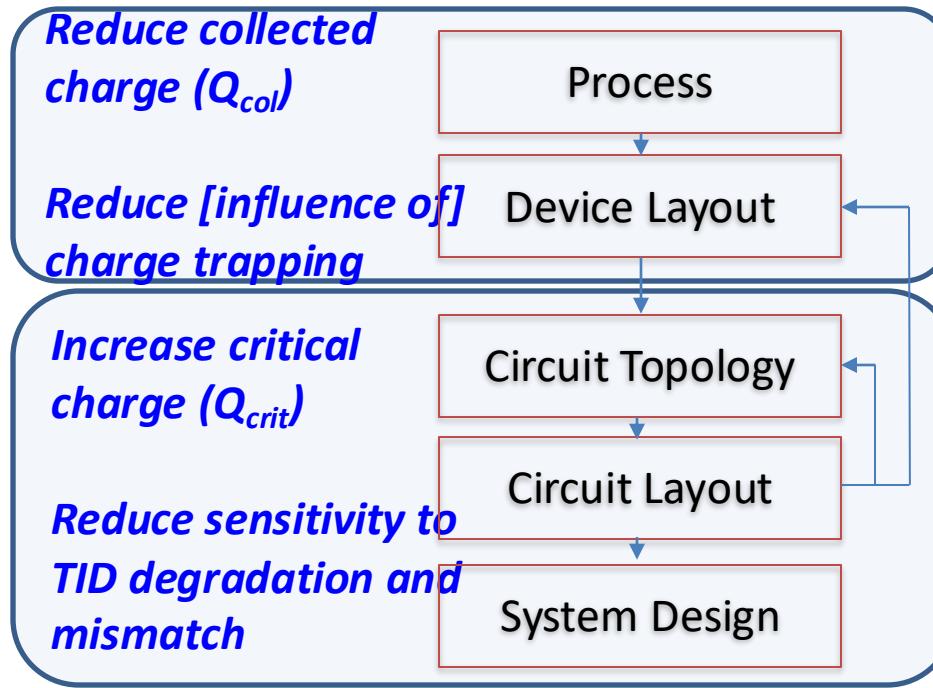


Logical NOR IC from Apollo
(~1961)

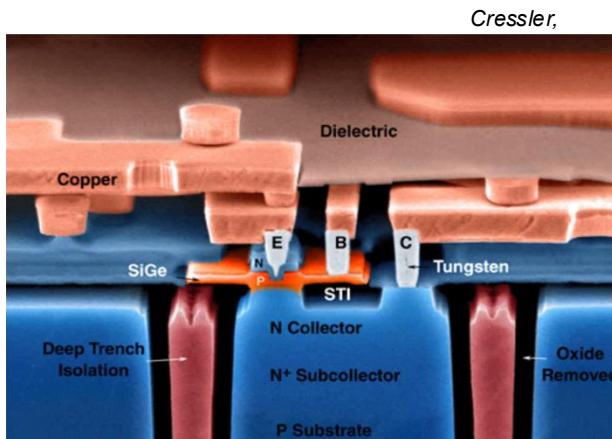
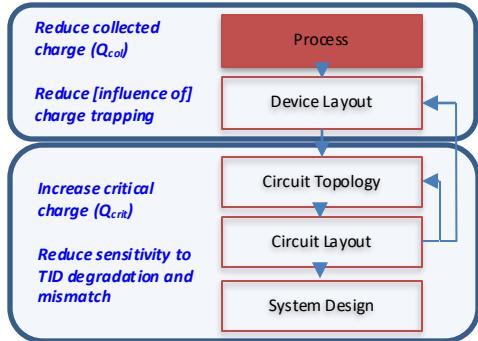


3D-SoC sensor/machine learning
IC from Stanford (2017)

Basic RHBD for AMS

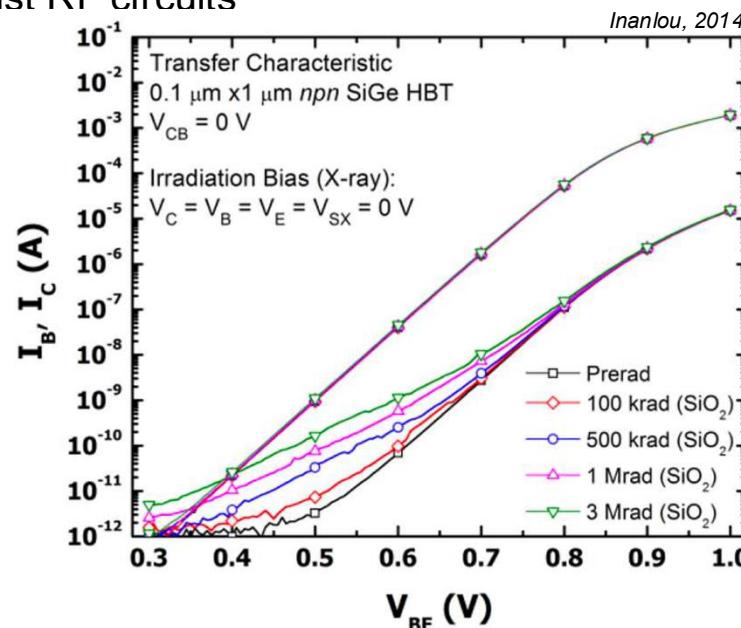


Basic RHBD: By Process

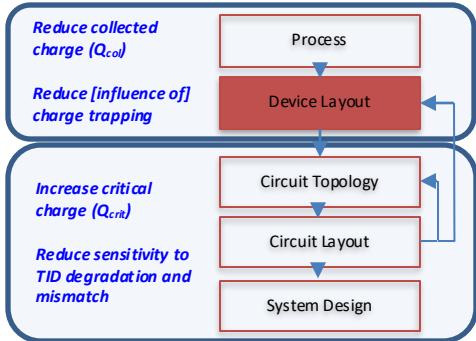


By-Process example:

Strained-enhanced SiGe HBTs (graded Ge layer in the base of a Si transistor) have emerged as an excellent alternative for TID-robust RF circuits

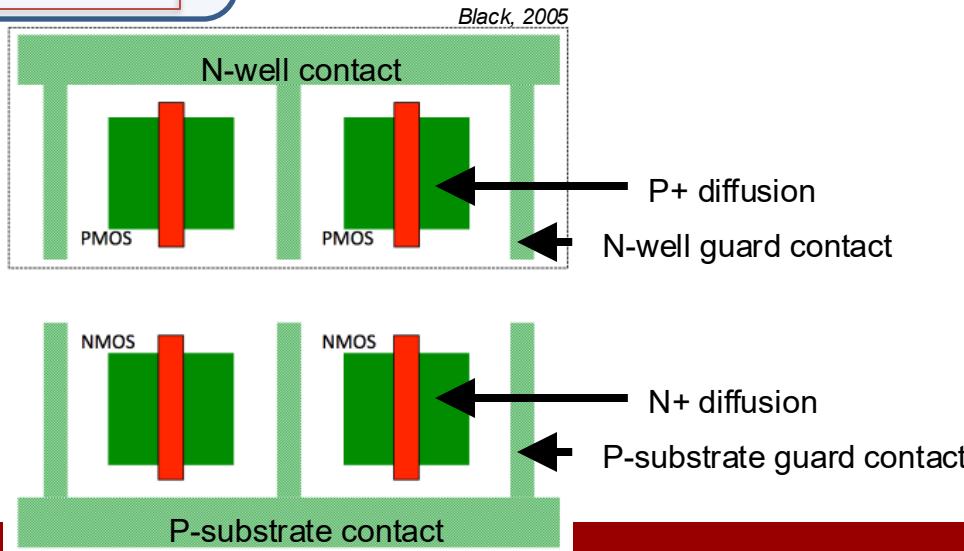


Basic RHBD: By [Layout] Design

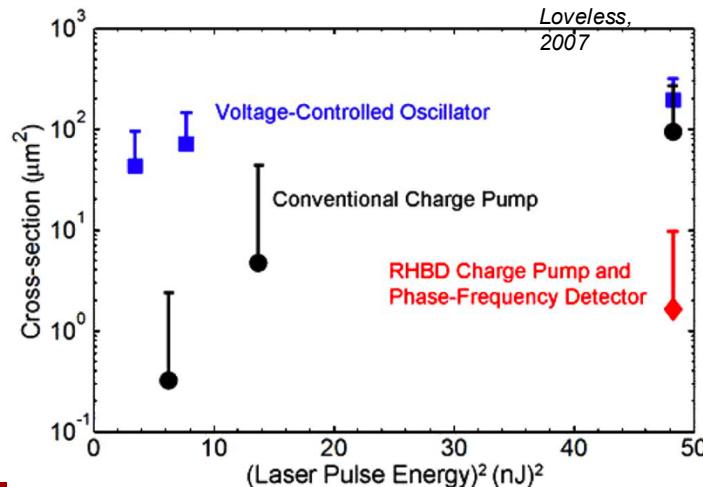
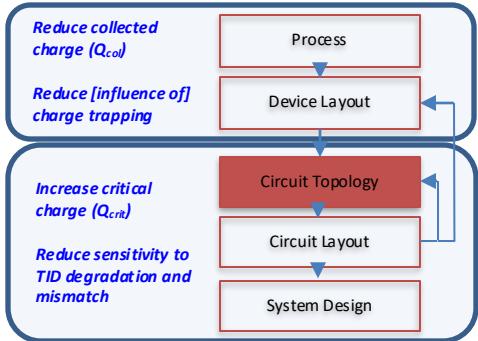


By-Design (Device Layout) example:

Guard contacts, formed from N-well and P-substrate diffusion contacts limit the charge collection at the circuit diffusions

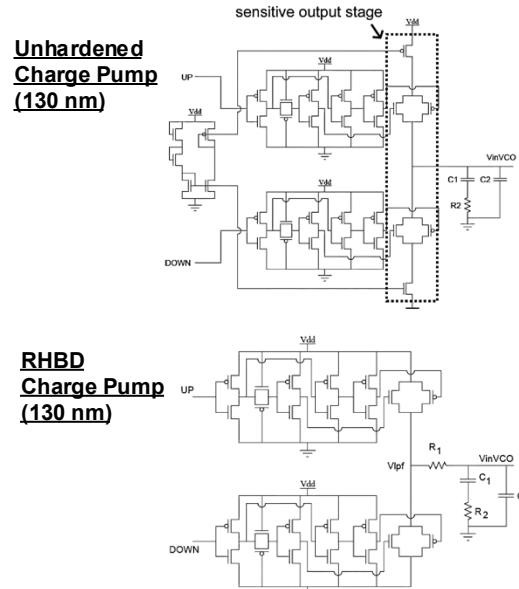


Basic RHBD: By [Circuit] Design

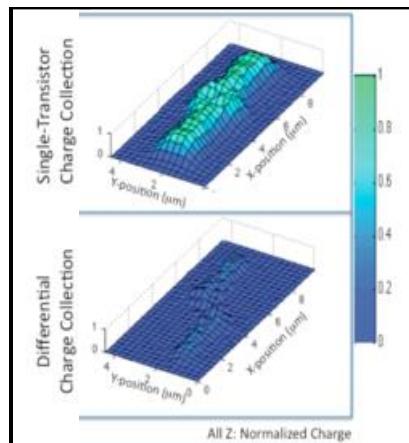
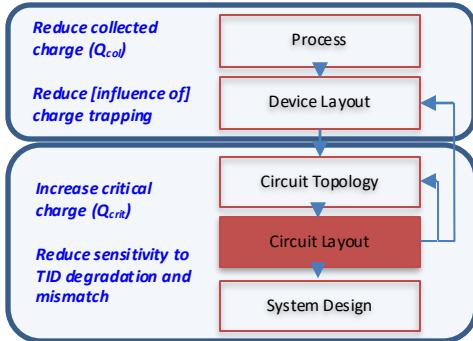


By-Design (Circuit) example:

Small changes to the circuit topology can lead to large gains in SEE performance

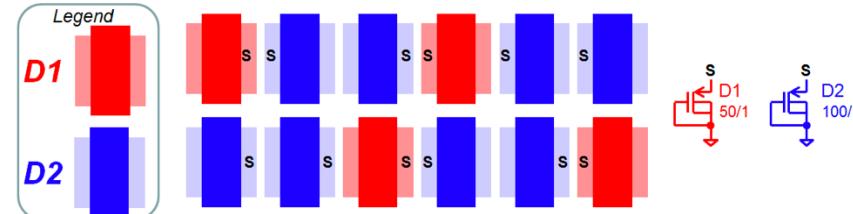


Basic RHBD: By [Layout] Design

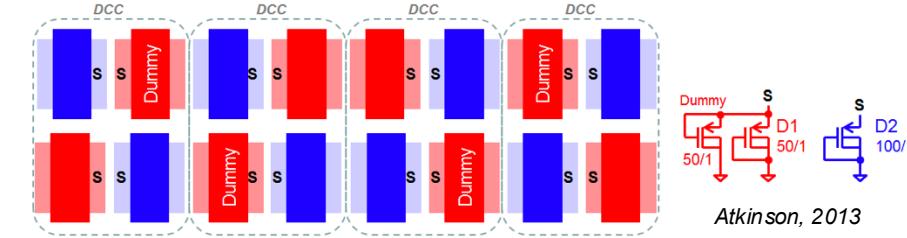


By-Design (Circuit Layout) example:

(a) Baseline quadrant layout of D1 and D2



(b) DCC quadrant layout of D1 and D2



(c) Common-centroid layout of quadrants

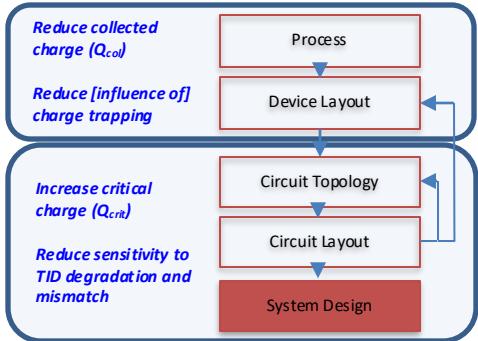
| | |
|----------|----------|
| Quadrant | Quadrant |
| Quadrant | Quadrant |

Atkinson, 2013

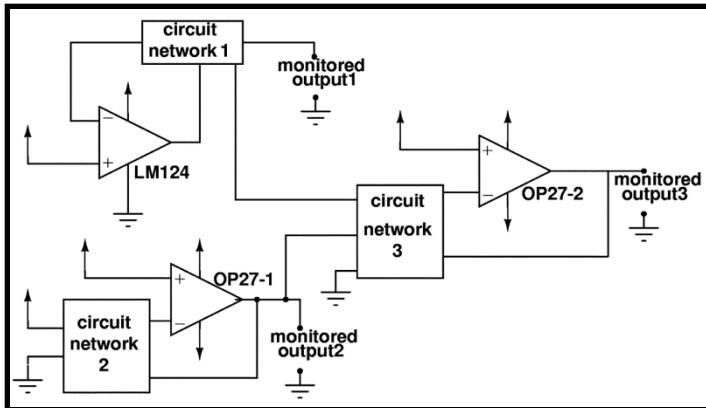
Armstrong,
2010

Module 6: Radiation Mitigation

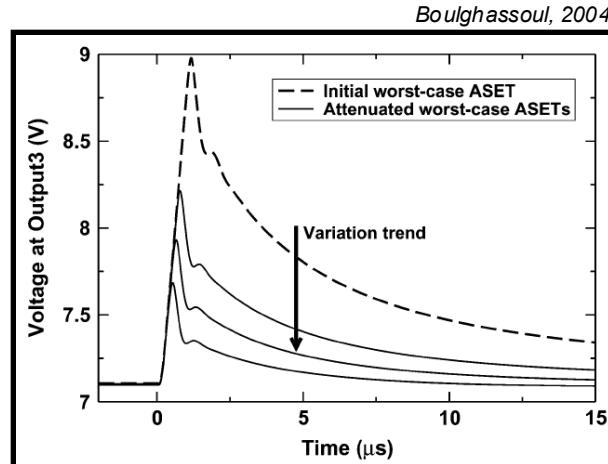
Basic RHBD: By [System] Design



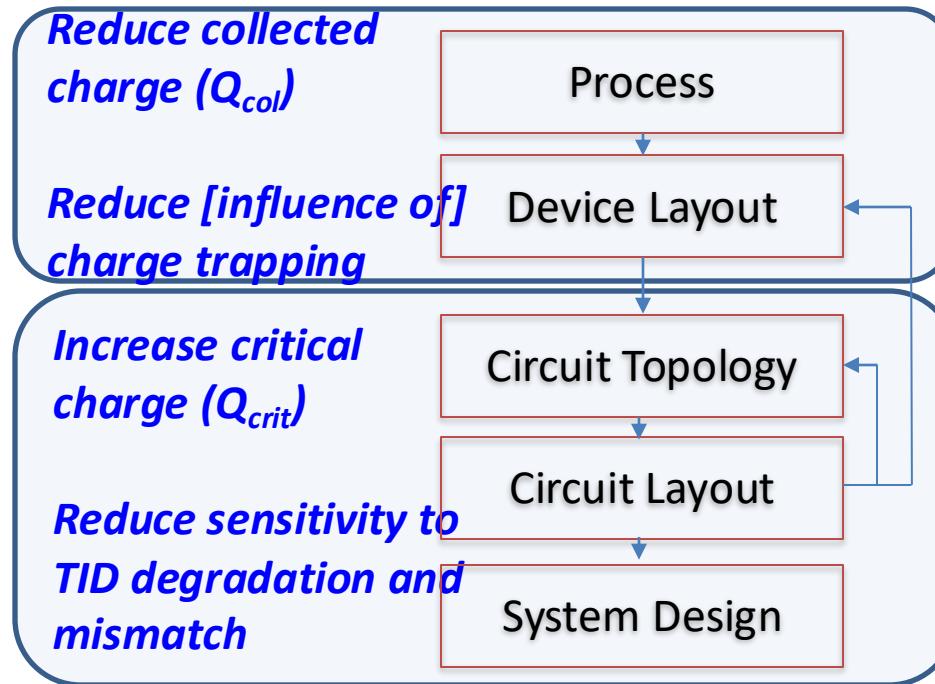
By-Design (System) example:
Low-pass filtering at system-level can effectively reduce SETs



Block Diagram of Satellite Power Distribution
Controller/Monitor



Ok, Lets Start To Pull It All Together



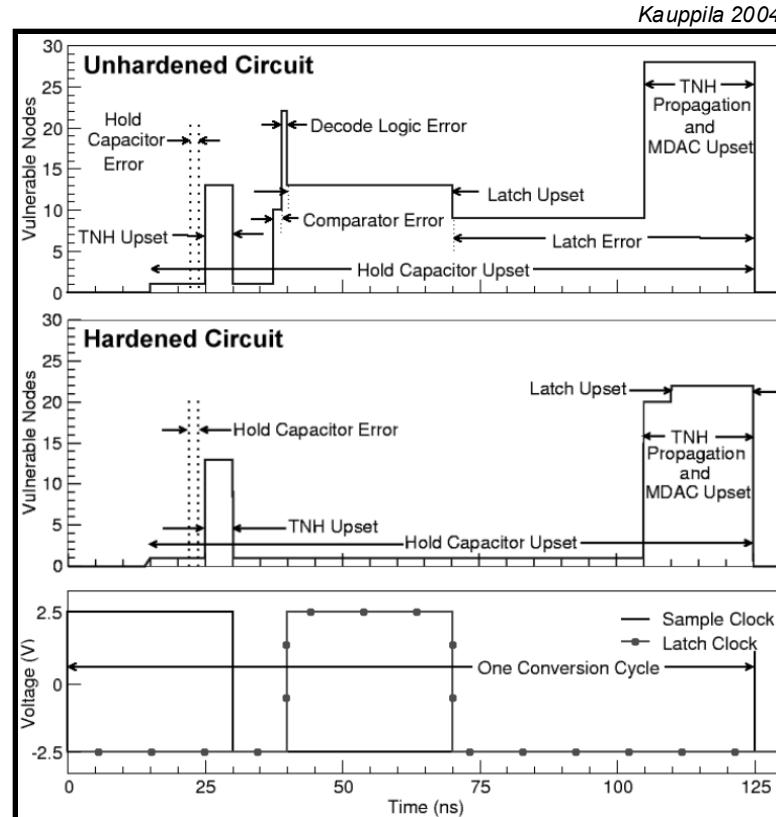
Where Do We Begin?

Reduction of Window of Vulnerability (WOV)

more common for digital systems - shows system dependence on clock

WOV analysis may indicate vulnerable regions within circuit and help predict upset probabilities

Simulated WOV of a Pipelined Analog-to-Digital Converter



Targeted Laser Excitation

- Laser single-photon (SPA) or two-photon absorption (TPA) is a powerful tool for RHBD
- PLL used as an example: laser SET mapping performed on sensitive block

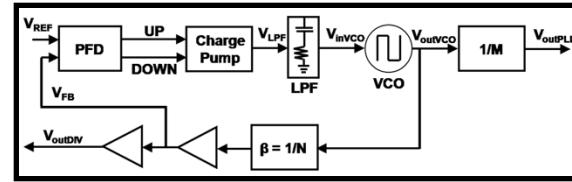
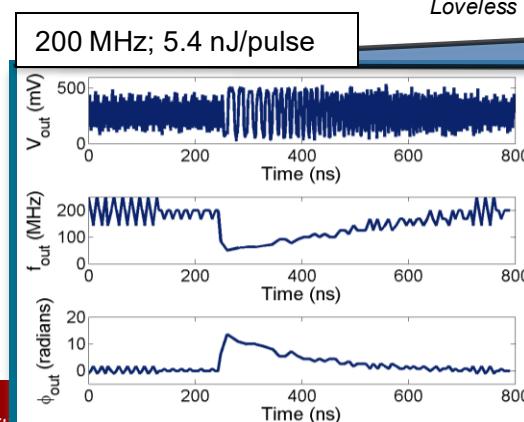
output signals following 10 strikes per

x-y location were recorded

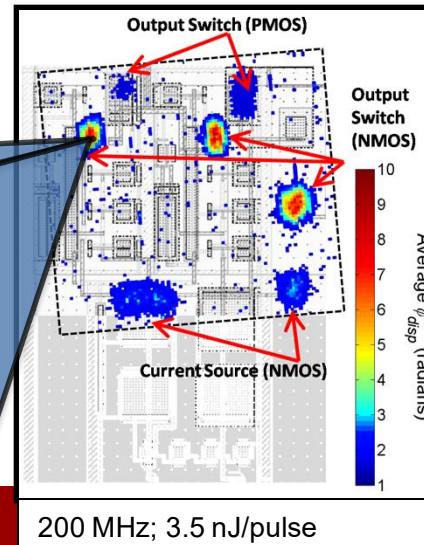
frequency/phase transients

extracted from

transient output



Two-Photon Absorption Laser-Induced SET Map of PLL Sub-Circuit (Charge Pump)



Now We Know the Issues, Start With ... ?

- **Resistive Decoupling**

effectively increases the time constant seen by the two storage nodes and limit the maximum change in voltage during a single-event, thus increasing Q_{crit}

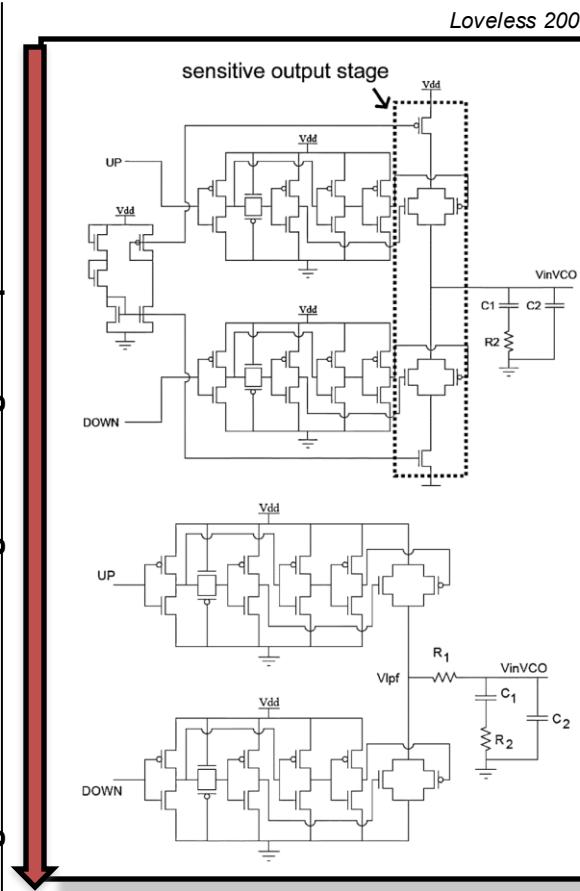
- **Filtering**

high-frequency transients may be filtered by decoupling nodes sensitive to ASETs and introducing a time constant through a series resistor or low-pass filter

- **Increased Capacitance**

increases the amount of charge, Q_{crit} , required to generate an ASET

Single-Event Hardening of Charge Pump Sub-Block of PLL



Loveless 2006

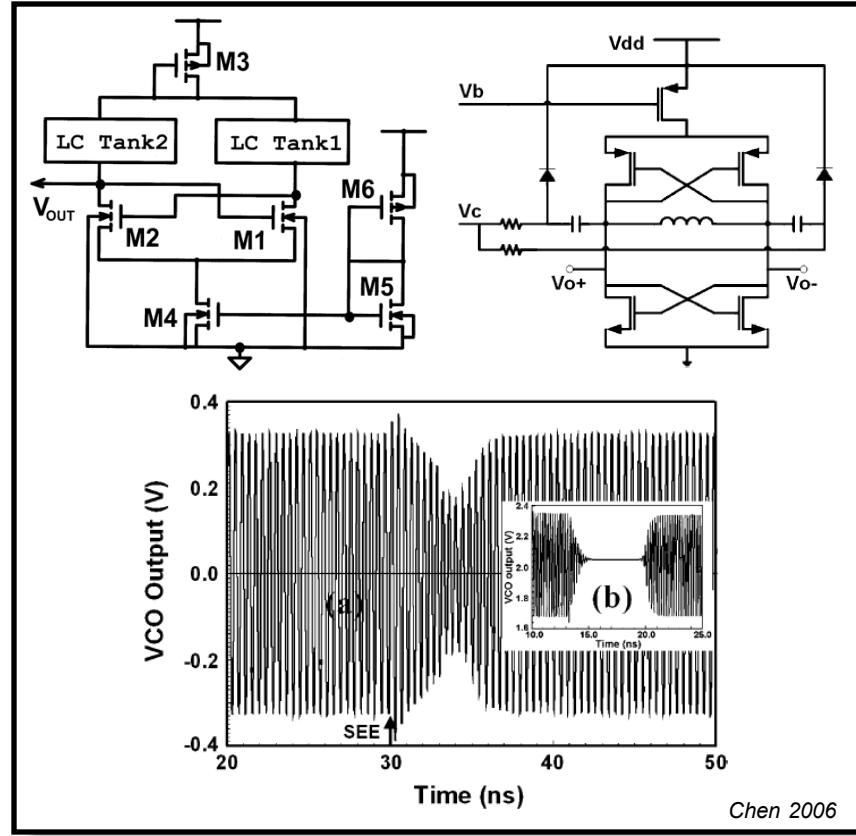
High Impedance Nodes

- Reduction of High Impedance Nodes**

high impedance nodes have consistently been identified as the culprits!

can be reduced or eliminated at the circuit- or transistor-levels

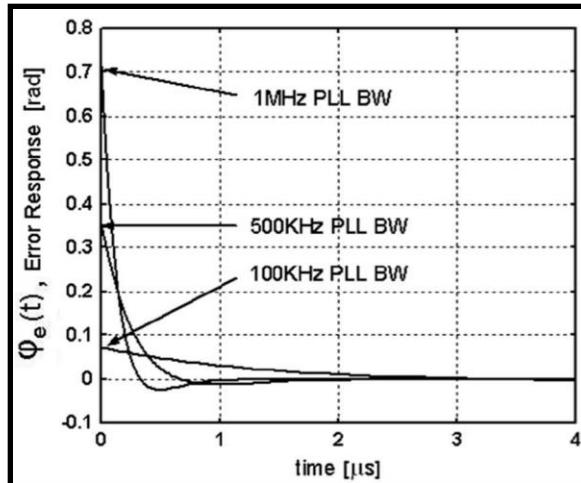
Single Event Mitigation By Elimination of High-Impedance Nodes in an LC Tank Oscillator



Gain-Bandwidth Tradeoffs

- **Modifications in Bandwidth and Gain**

in general, many works on amplifiers, phase-locked loops, voltage-controlled oscillators, ... have shown that **reduction in bandwidth** results in **reduction in SE vulnerability**



Chung 2006

Error Response versus Time During a Single Event in the PLL at Various Bandwidths

Gain-Bandwidth Tradeoffs

- **Modifications in Bandwidth and Gain**

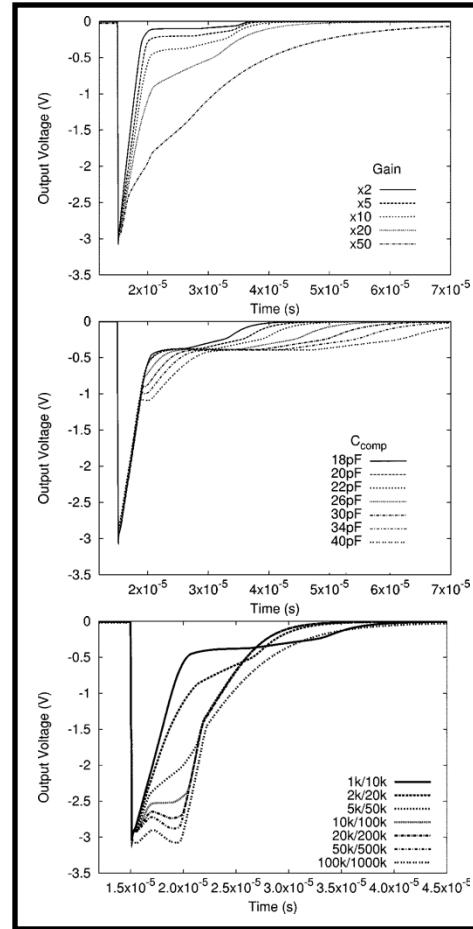
in general, many works on amplifiers, phase-locked loops, voltage-controlled oscillators, ... have shown that **reduction in bandwidth** results in **reduction in SE vulnerability**

gain and operating speed also play a particular role in determining the SET response

Ex. “Faster operational amplifier with a smaller gain will have a better SET response than a slower operational amplifier run at a high gain. It also seems to be best to use the smallest practical values to set the closed-loop gain of the amplifier”, Sternberg

Boulghassoul 2004

SET Dependence on Gain, Capacitance, and Resistance Values in Various Stages in an LM124 Op-Amp



Gain-Bandwidth Tradeoffs

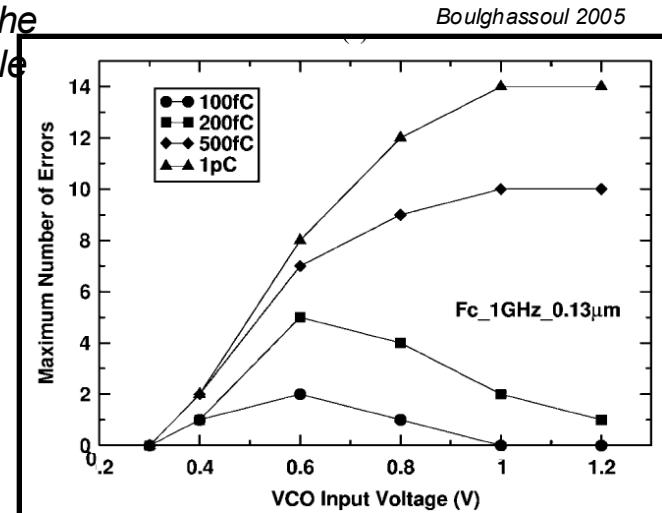
- Modifications in Operating Speed and Current Drive

analog circuits have been shown to exhibit reduced ASET vulnerability for increased operating frequency

- *increased speed is often accompanied by increased drive current and an improved ability to dissipate the deposited energy, making the circuit less vulnerable*
- **important to attribute the improvement to either speed or drive strength** (increased bias current is a well-known technique and is often used in AMS circuits for improved SET performance)

Number of Errors in VCO Output Bits Versus Input Voltage (Proportional to Drive Strength and Frequency)

Contrary to that seen in digital circuits



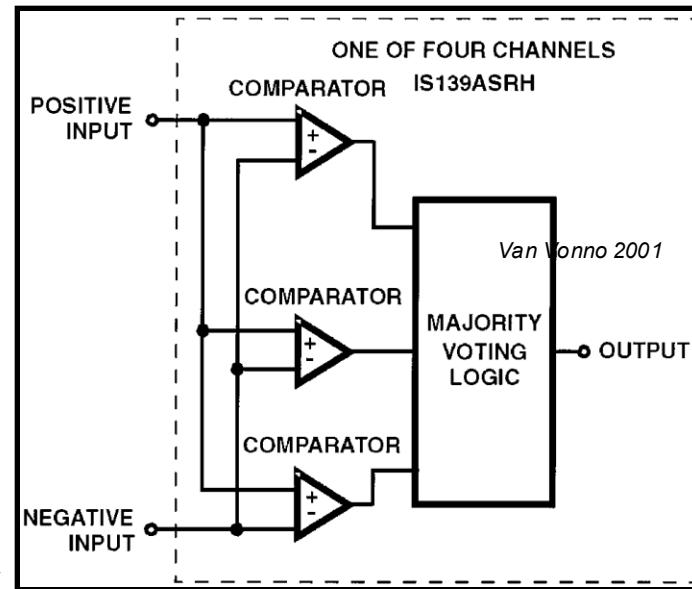
What About Triple Modular Redundancy?

Triple Modular Redundancy (TMR):

three identical copies of a circuit; majority voting at the output

while more common in digital electronics,
TMR has been successfully implemented
in **mixed-signal circuits** with digital
output signatures, such as the voltage
comparator

not straight forward for analog
circuits

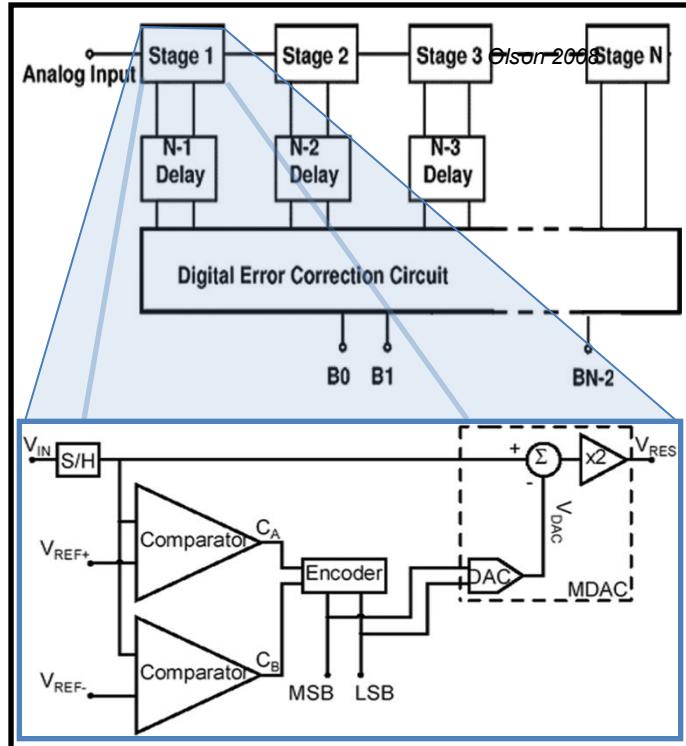
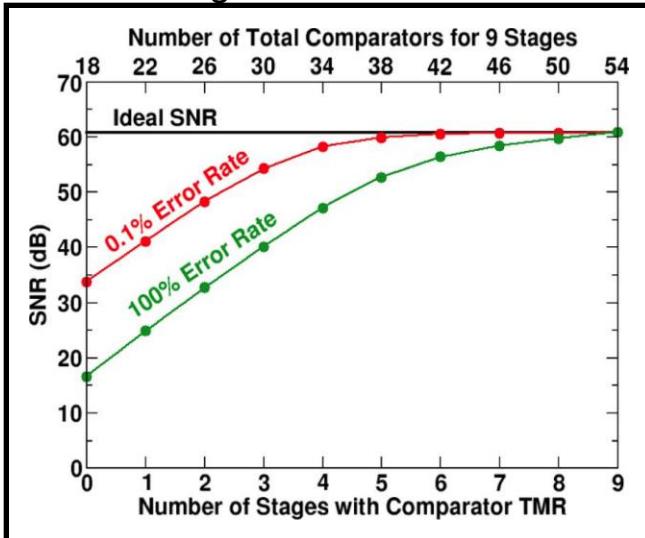


3x Power and Area Penalty

Strategic TMR

Triple Modular Redundancy (TMR):

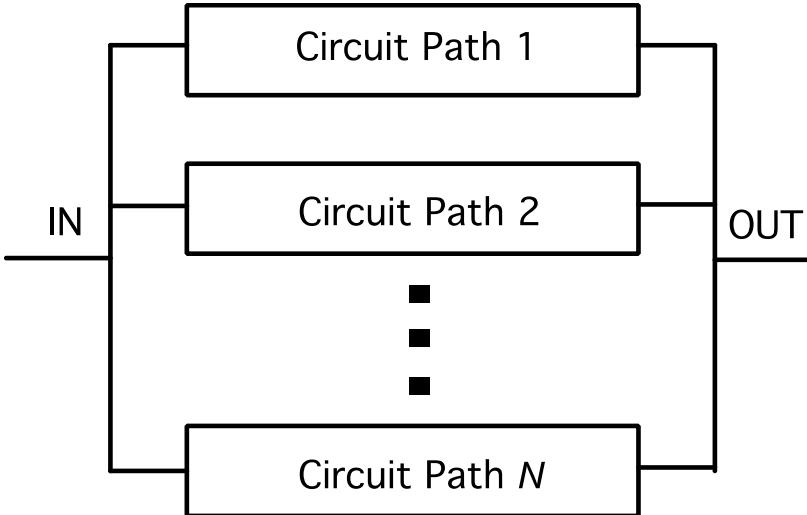
when used in a pipelined analog-to-digital converter (ADC)
TMR need only be applied to the first 50% of the stages



Signal-to-Noise Ratio at ADC Output
for Randomly Injected Errors

Hardening Via Node Splitting

- One versatile methodology for hardening AMS circuits is that of *node splitting*
- Discrete- or continuous-time
- Negligible impact on performance, area, power dissipation
- Form of redundancy – however, circuit is *divided into 2 or more paths* (ideally, struck path is disabled during ion strike)

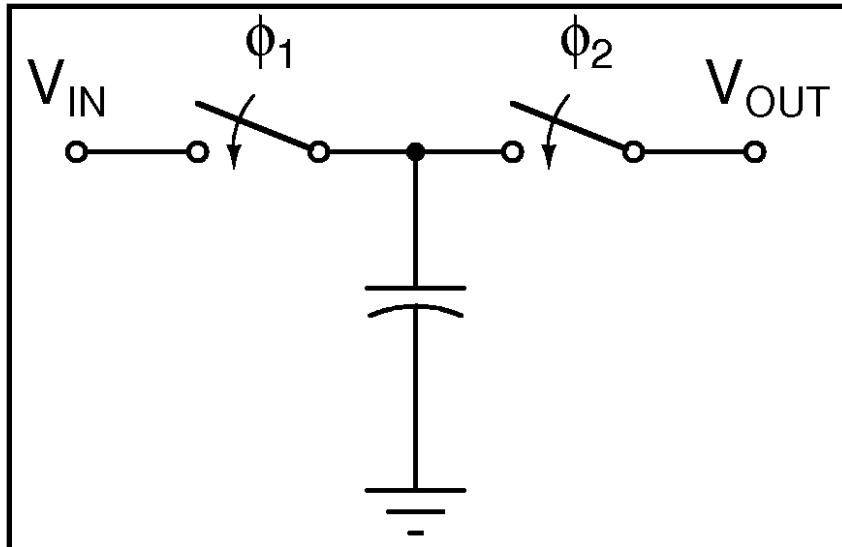


Hardening Via Node Splitting: *Dual-Path*

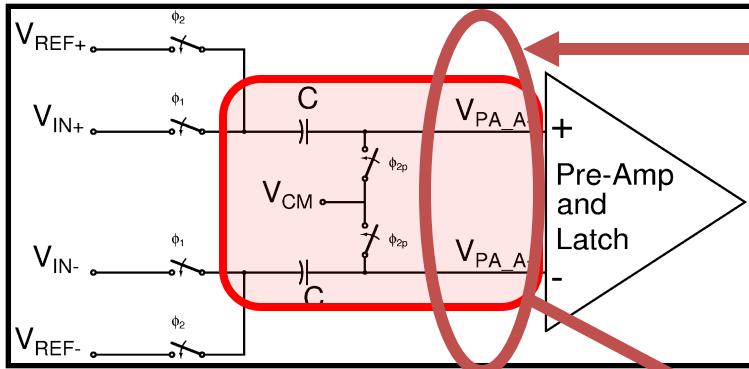
Dual-Path Hardening

conventional wisdom: avoid floating nodes in designs for radiation environments

dual-path hardening technique has been developed that dramatically decreases floating nodes vulnerability in switched-capacitor mixed-signal circuits

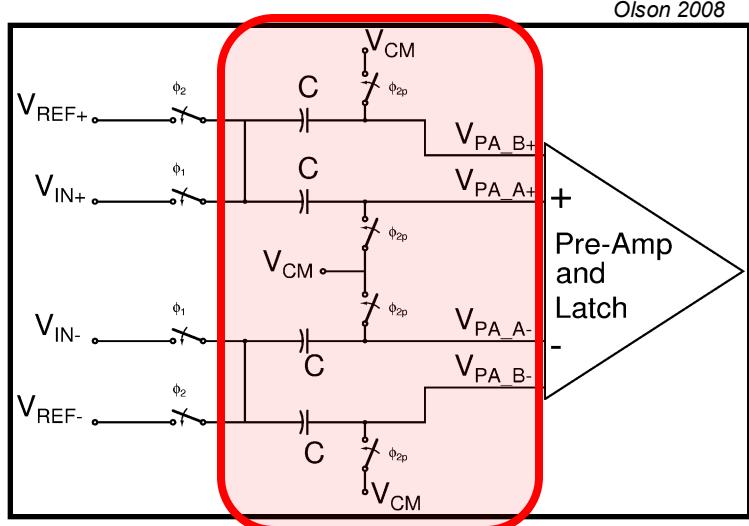


Hardening Via Node Splitting: *Capacitors*

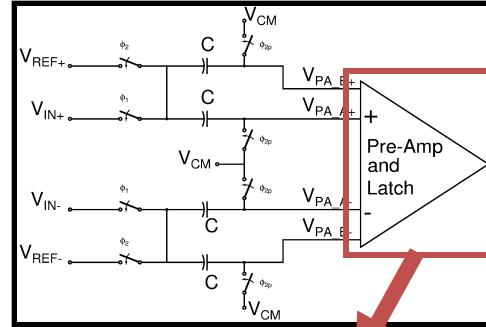
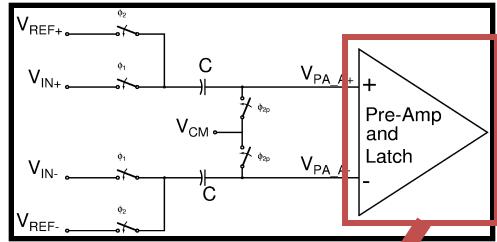


Floating nodes during evaluate phase

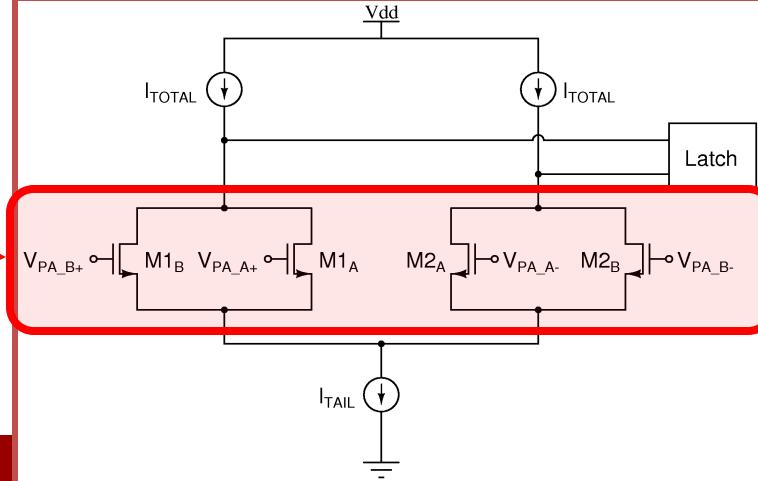
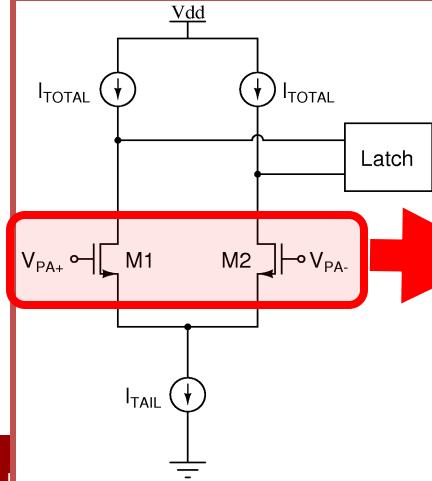
- Duplicate the floating input nodes
- An SE may disrupt one input node, but the correct response will be preserved by the additional path



Dual-Path Hardening: *Pre-Amplifier/Latch*

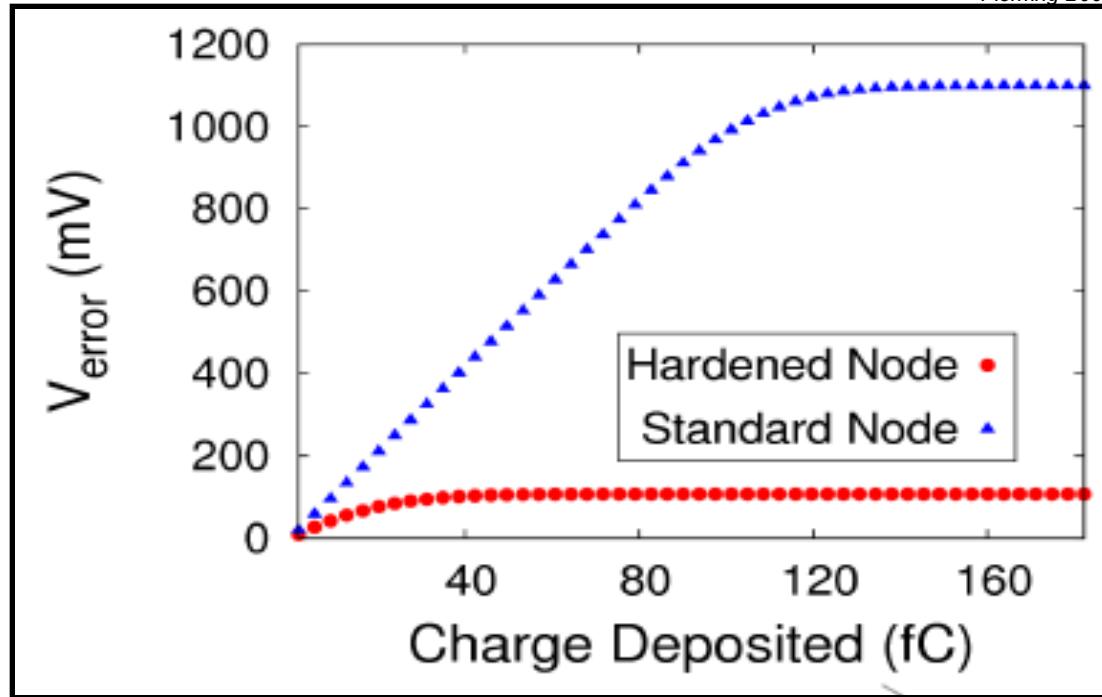


Olson 2008

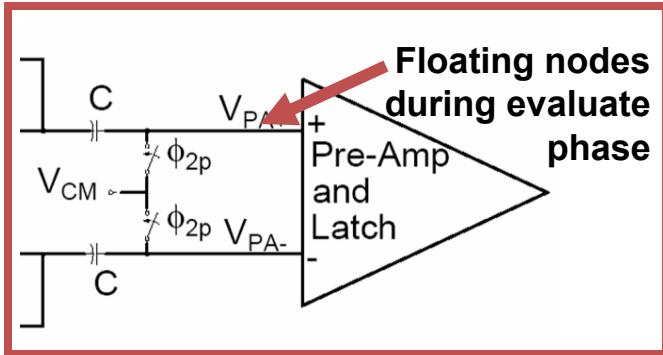


Hardening Via Node Splitting: *Dual-Path*

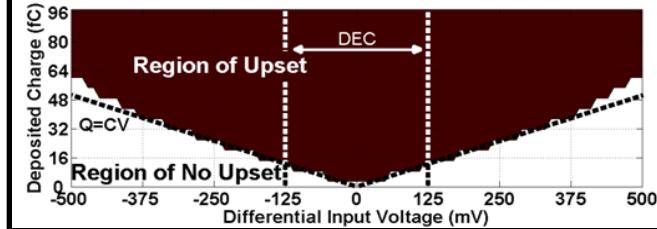
Fleming 2008



Hardening Via Node Splitting: *Dual-Path*



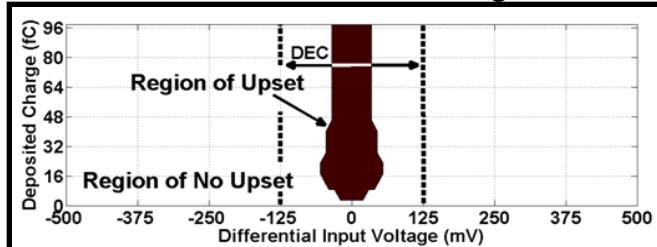
90 nm CMOS Simulations of Baseline



Olson 2008

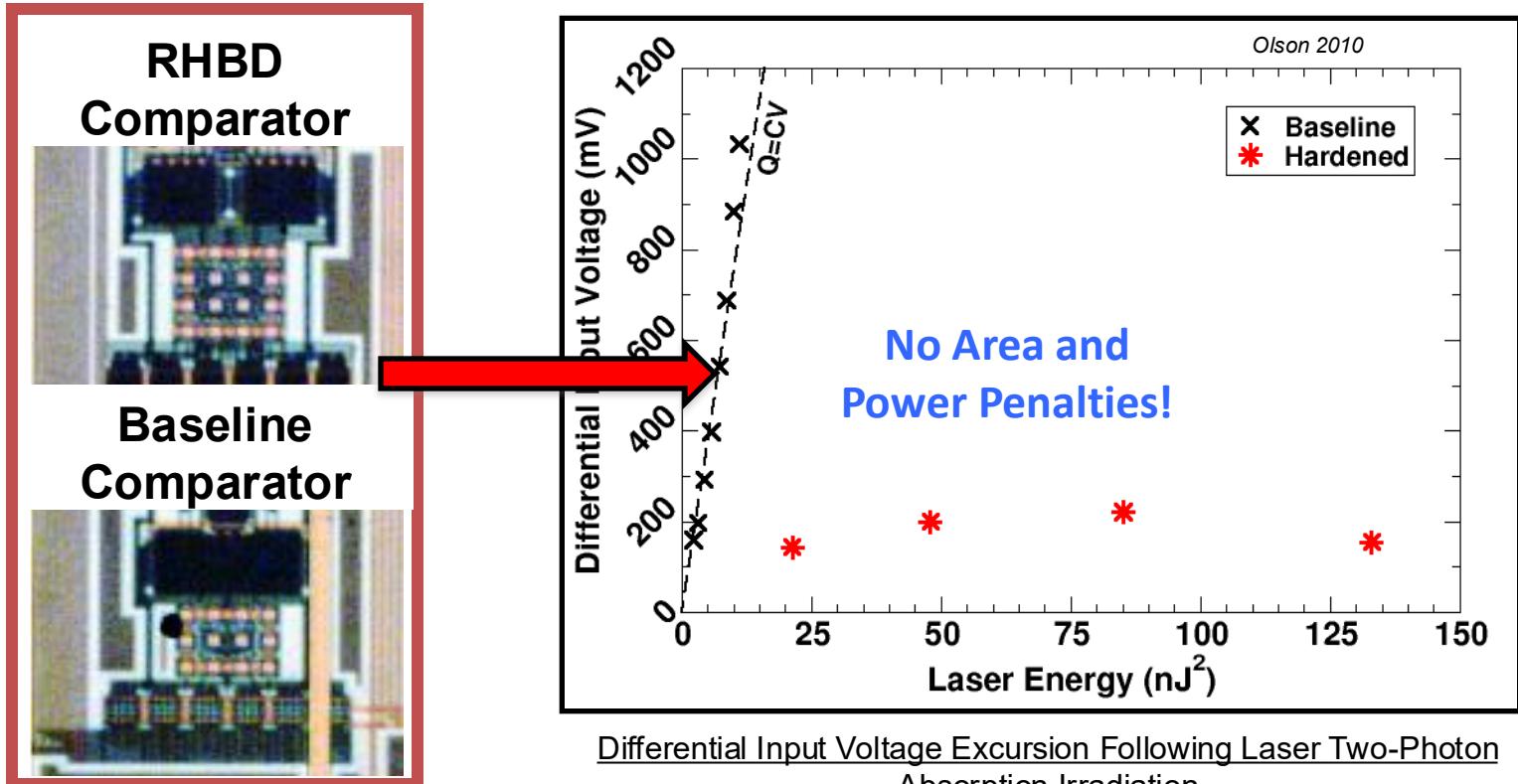


Dual-Path Hardening



- Maximum differential input voltage vulnerable to SEU increases roughly linearly with collected charge at the rate of $Q=CV$
- Dual-path hardening decouples the comparator response from increasing collected charge

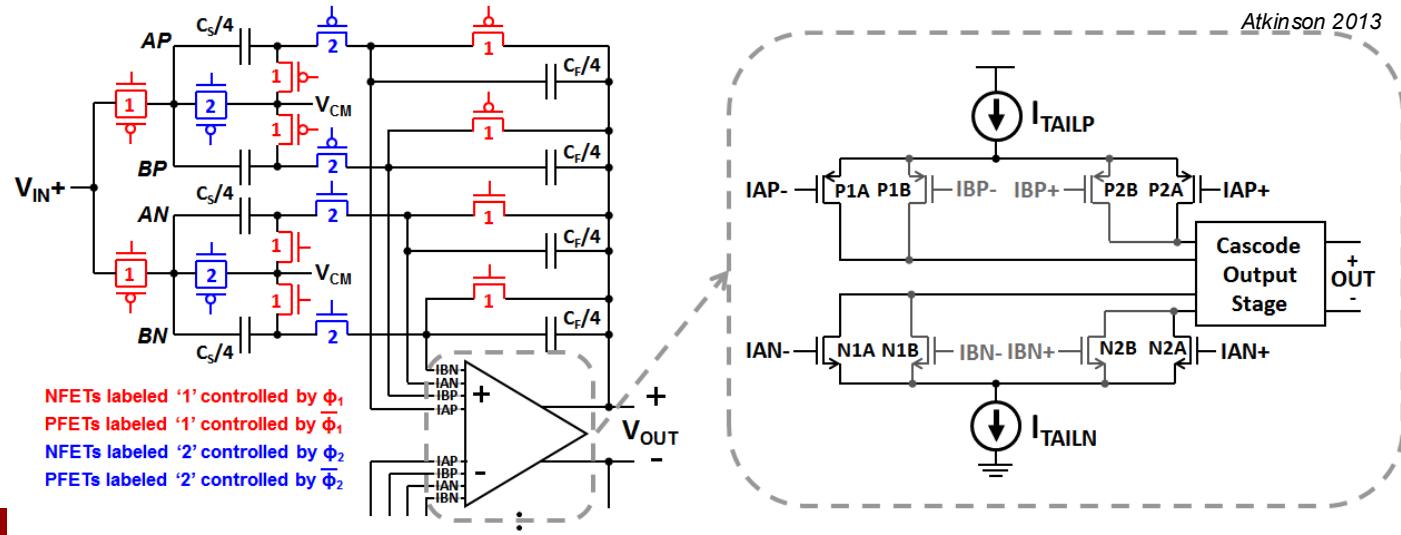
Hardening Via Node Splitting: *Dual-Path*



Differential Input Voltage Excursion Following Laser Two-Photon Absorption Irradiation

Hardening Via Node Splitting: Quad-Path

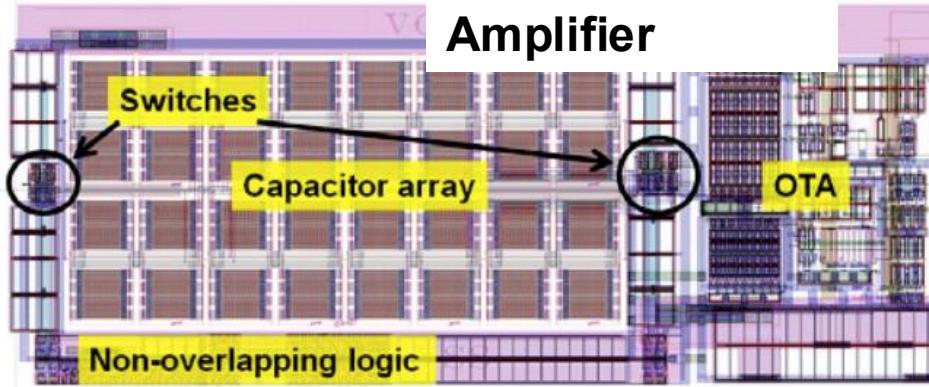
- The main drawback of dual-path hardening is that the transistor switches must be the same type as the input transistors (ensures that the struck path will be disabled, but also *limits dynamic input range*)
- Quad-path hardened designs address this limitation at the added cost of increased layout complexity (though at no area or power penalties!)



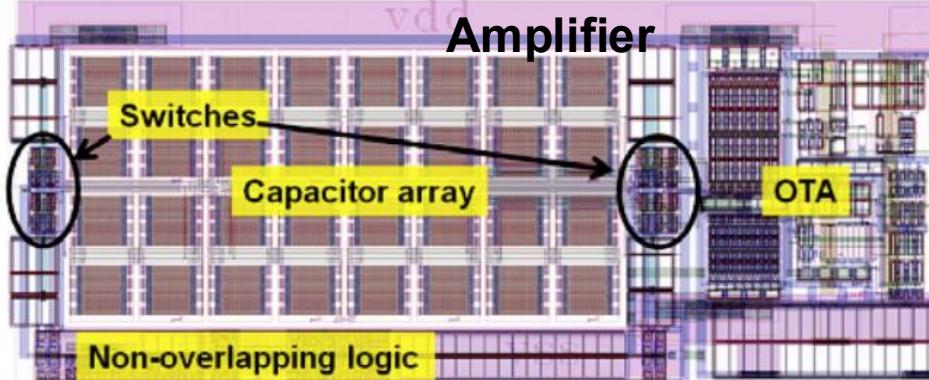
Hardening Via Node Splitting: *Quad-Path*

Atkinson 2013

(a) Baseline S/H
Amplifier

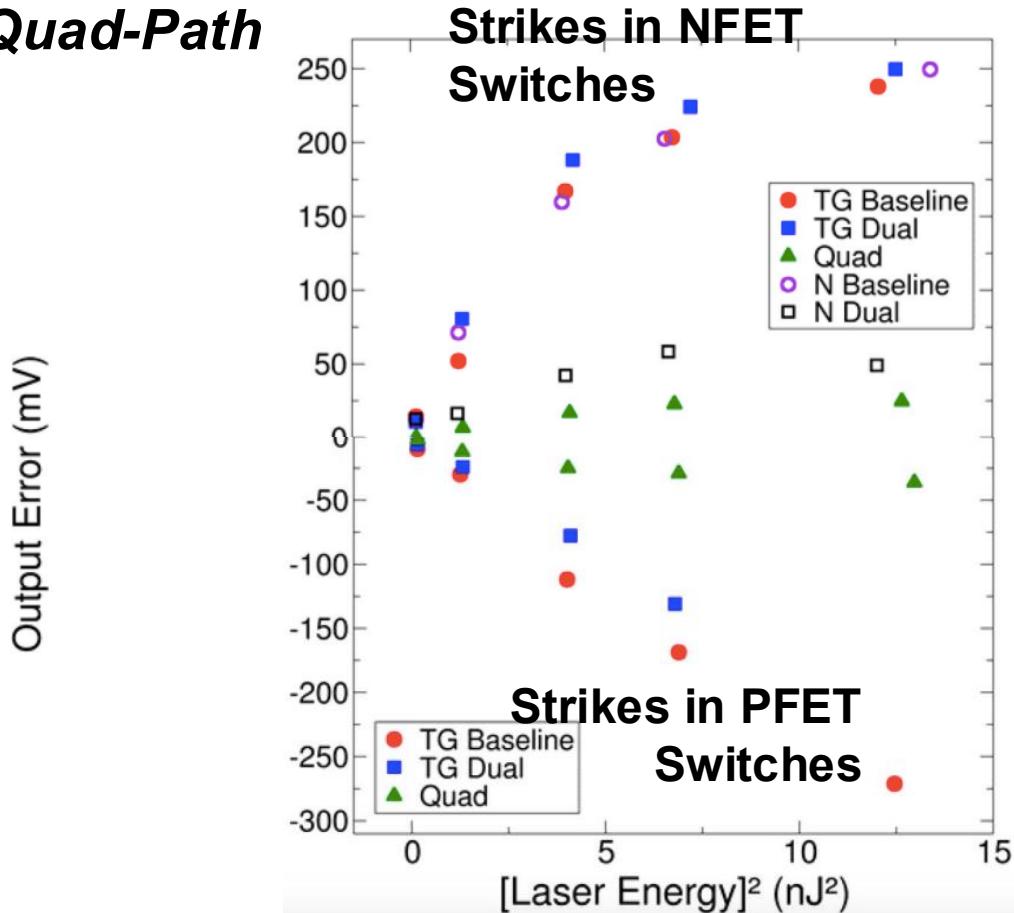


(b) RHBD S/H
Amplifier



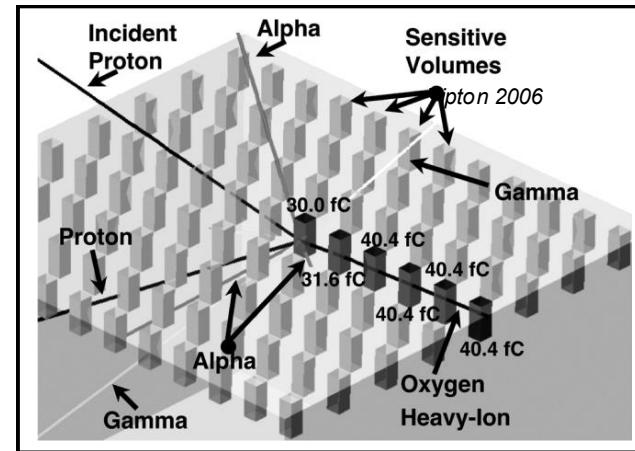
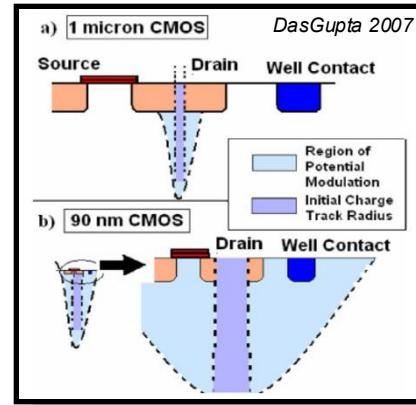
Hardening Via Node Splitting: *Quad-Path*

- Up to 90% reduction in output error observed at higher laser energy tested with less than 2% area penalty and negligible power penalty
- Equivalent levels with capacitive hardening would result in:
 - 10x capacitance
 - 7.5x total area
 - 0.1x slew rate



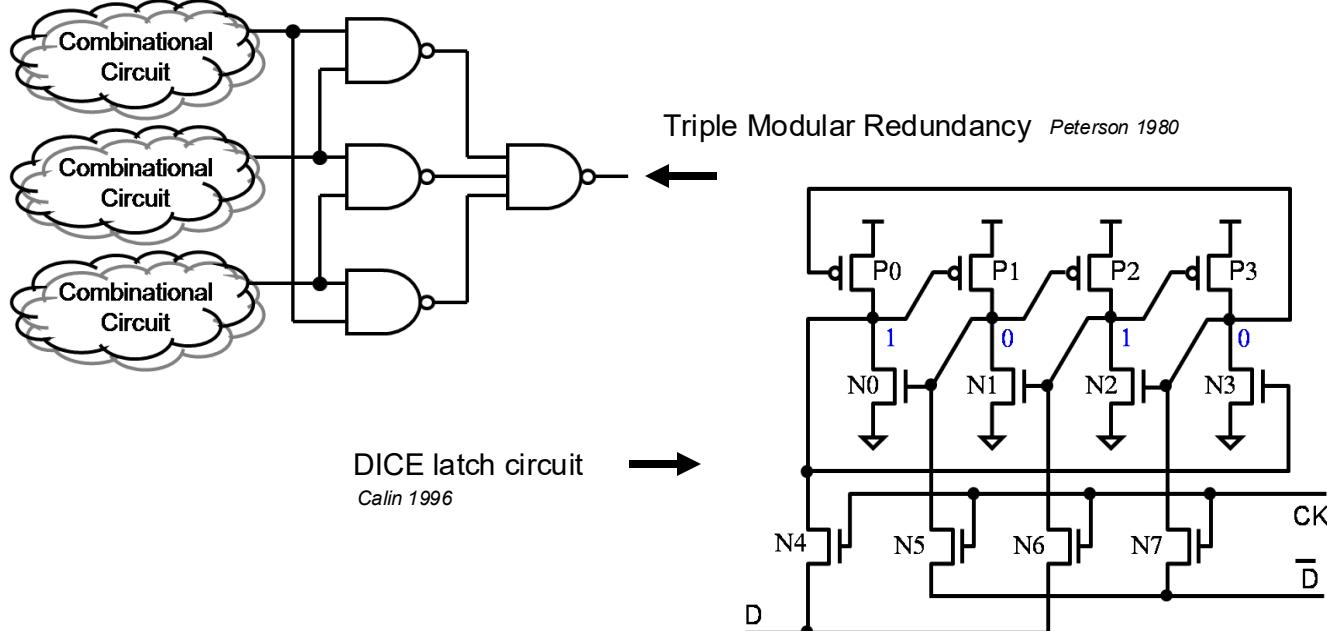
Circuit Layout-Aware Mitigation

- In recent years, “charge sharing” between transistors has become commonplace:
 - decreased spacing of devices with technology scaling can increase the charge collection at nodes other than the primary struck node
 - layout-level mitigation is becoming increasingly important for ensuring radiation hardness



Charge Sharing Reliability Issues

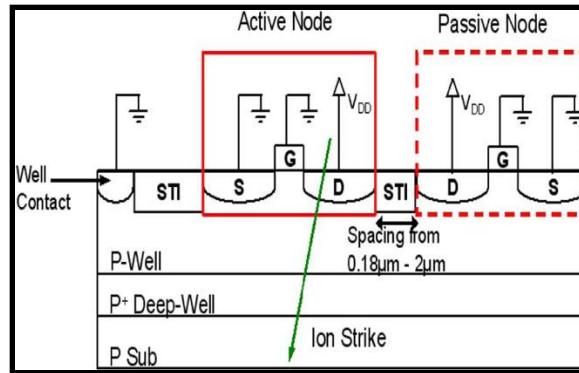
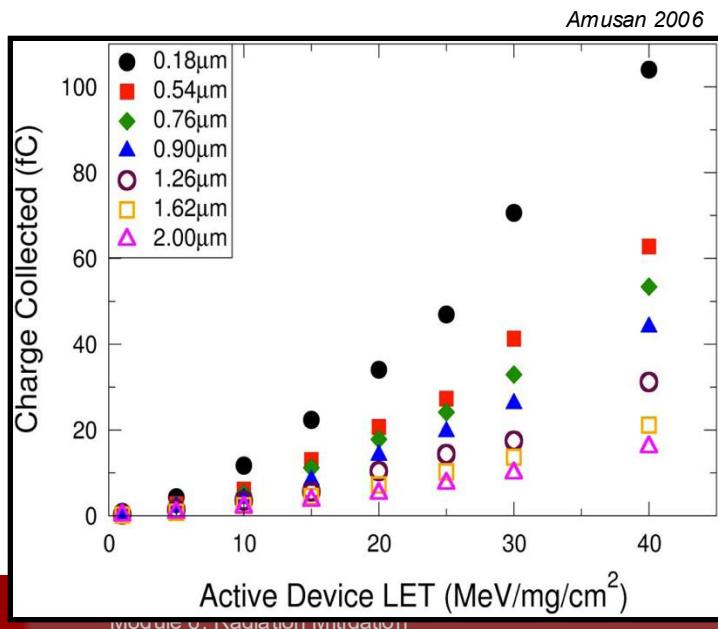
Charge sharing can render redundancy-based methods (e.g., Triple Modular Redundancy - TMR and Dual Interlocked Storage Cell - DICE latch) for SEU mitigation less effective



Layout-Level Mitigation: *Nodal Separation*

Nodal separation:

increasing the distance between devices can reduce the amount of charge collected on “passive” devices



NMOS Cross Section Showing Active (Device Struck by Ionizing Particle) and Passive (Device that Indirectly Collects Charge) Device

Large Spacing Required To Mitigate Entirely

Nodal Separation of Two PMOS Devices (130 nm CMOS): Charge Collected on Passive Device

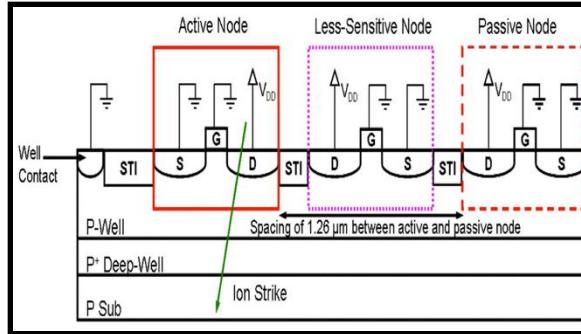
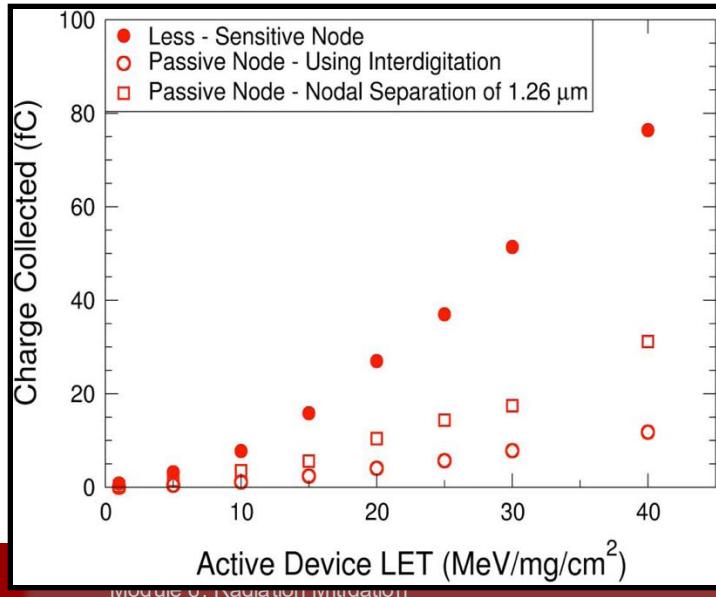
Layout-Level Mitigation: *Interleaving*

Interdigitation (Interleaving):

“less sensitive” devices placed between critical nodes

gain benefits of nodal separation without adversely affecting total area

Amusan 2006

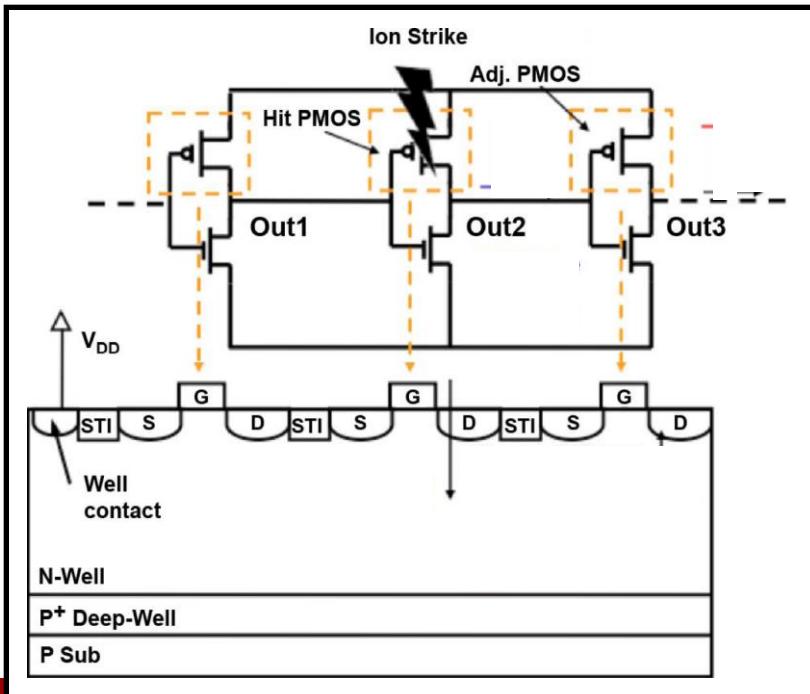


**NMOS Cross Section Showing
Active and Passive Devices: Less-
Sensitive Node is Placed Between
Active and Passive Devices**

**Nodal Separation of Two NMOS Devices (130 nm CMOS):
Charge Collected on Passive Device with and without
Interdigititation**

Instead of Mitigate - Integrate (charge sharing)

The layout orientation and device spacing may be designed so the electrical signal and charge diffusion may interact as to truncate a propagated voltage transient (pulse quenching)



A Similar
Mechanism can be
Exploited for AMS
ASICs

Illustration of Pulse Quenching