Total Ionizing Dose
Modeling Mechanisms of TID

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Module 5: Objective and Outcomes

- This module will
  - Overview the basic modeling techniques for MOS technologies
  - Details the basic principles of total ionizing dose
  - Introduce state-of-the-art techniques for modeling TID in MOS technologies

- Student Outcomes

  1. Students will demonstrate an understanding of cumulative radiation effects.

  2. Students will demonstrate an understanding of the primary compact modeling strategies in modern circuit simulation software.

  2. Students will apply modeling strategies for aiding in the understanding of total ionizing dose.

Thanks to …

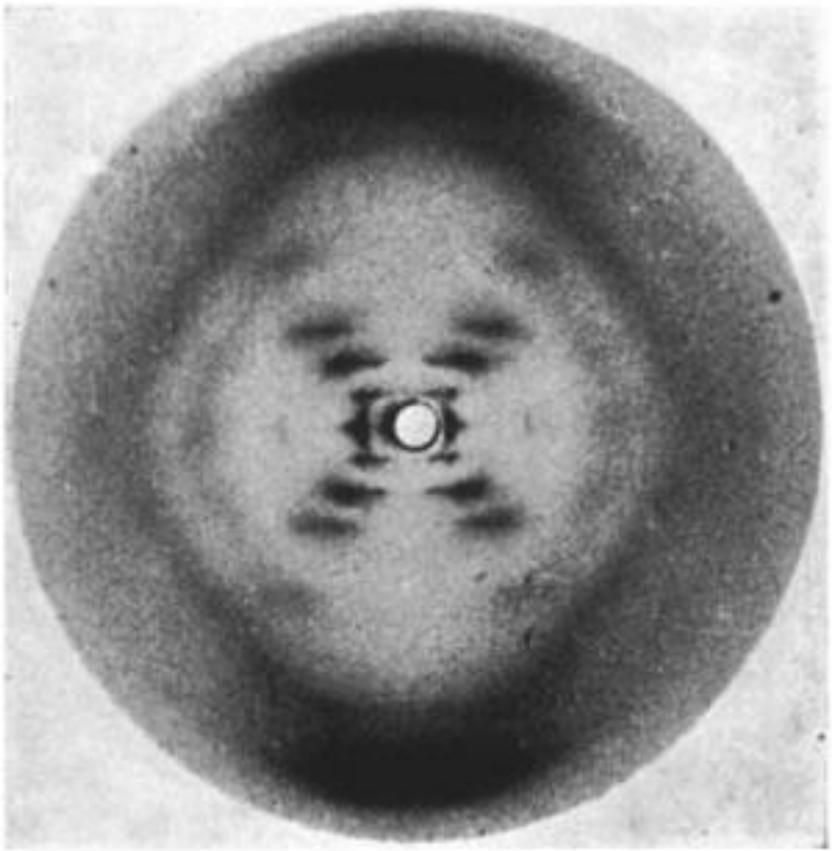
Hugh Barnaby
Professor of Electrical Engineering, Arizona State University

Ivan Sanchez Esqueda
Assistant Professor of Electrical Engineering, Arizona State University

Arizona State University

SERESSA 2022

The Need for Experimentation

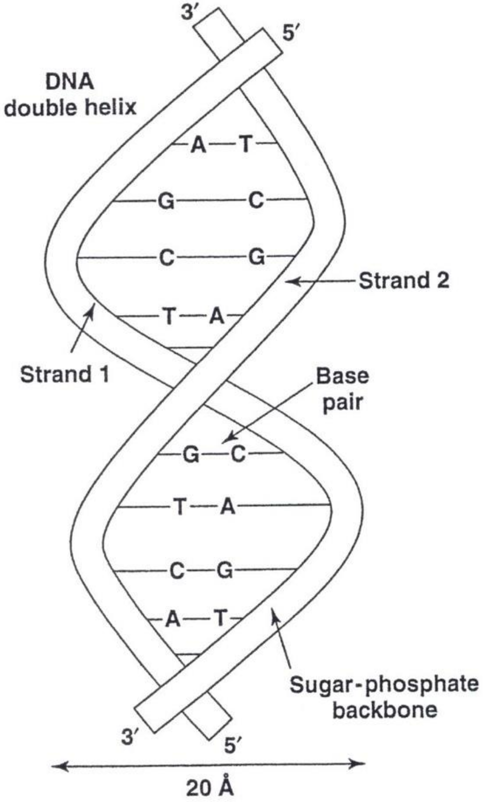


X-ray photograph of DNA in the B form taken by Rosalind Franklin in 1952.

- J. D. Watson, The Double Helix

By Raymond Gosling/King's College London - http://www-project.slac.stanford.edu/wis/images/photo_51.jpg, Fair use, https://en.wikipedia.org/w/index.php?curid=38068629

The Need for Modeling



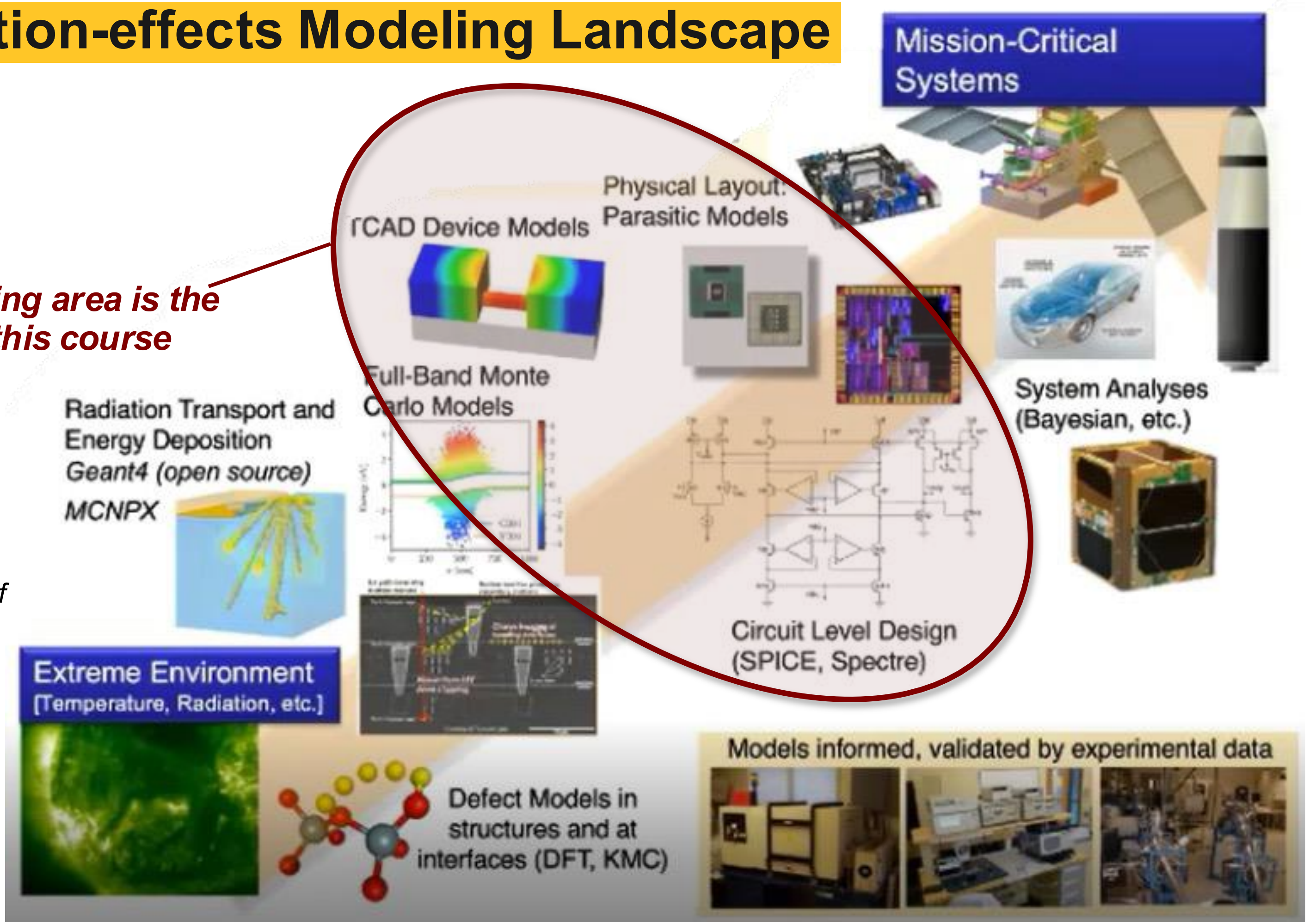
By K. K. Mardaneh, 06/28 2022

Watson and Crick with their DNA model. Photographed in the Cavendish Laboratory, University of Cambridge, UK, in May 1953.A. BARRINGTON BROWN, © GONVILLE & CAIUS COLLEGE/COLOURED BY SCIENCE PHOTO

Radiation-effects Modeling Landscape

The modeling area is the subject of this course

by R.D. Schrimpf



Module Outline

- **Introduction**
  - Compact Modeling for Circuit Simulation
- **Modeling Mechanisms of Cumulative Radiation Effects**
  - Ionizing Radiation Effects (TID)
  - Displacement Damage (DD) – *not covered in this course*
- **Modeling MOSFET Devices and Circuits**
  - MOSFET Structure and Operation
  - Compact Models for MOSFETs
  - Modeling Impact of TID on MOSFET I-V characteristics
  - Simulating TID and Aging Effects in CMOS Circuits
- **Summary**

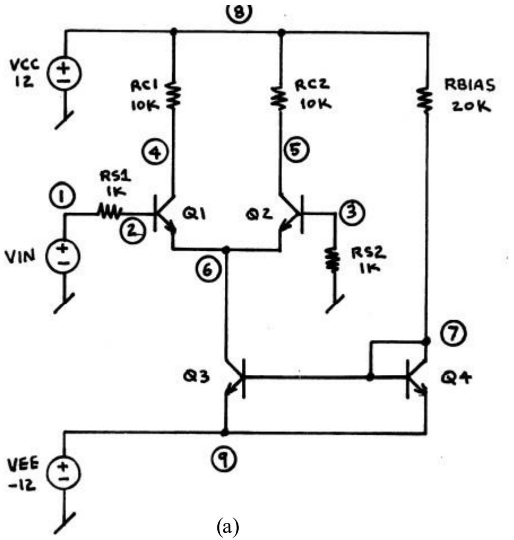
05

Compact Modeling for Circuit Simulation

Introduction

SPICE EDA for Circuit Analysis

The “Simulation Program with Integrated Circuit Emphasis,” **SPICE**, was developed in 1972 by Larry Nagel at the University of California, Berkeley.



(a)

```
DIFFPAIR CKT - SIMPLE DIFFERENTIAL PAIR
VIN 1 0 SIN(0 0.1 5MEG 5NS) AC 1
VCC 8 0 12
VEE 9 0 -12
Q1 4 2 6 QNL
Q2 5 3 6 QNL
RS1 1 2 1K
RS2 3 0 1K
RC1 4 8 10K
RC2 5 8 10K
Q3 6 7 9 QNL
Q4 7 7 9 QNL
RBIAS 7 8 20K
.MODEL QNL NPN(BF=80 RB=100 CCS=2PF TF=0.3NS TR=6NS CJE=3PF
+ CJC=2PF VA=50)
.END
```

(b)

By L. W. Nagel, no. ERL-M520, 1975

By W. R. Huber, IEEE Solid-State Circuits Magazine, 2019

Introduction

Compact Modeling for EDA

The purpose of compact modeling

to derive simple, fast and accurate analytical representations of the terminal electrical characteristics of transistors. Compact models are needed to compute numerically the transistor characteristics, rapidly enough, for use in circuit simulators to design and optimize the performance of silicon monolithic integrated circuits …

C. T. Sah

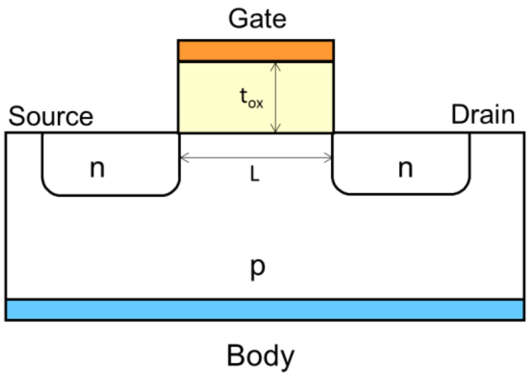
The Compact Model Coalition (CMC) selects and maintains an active list of accepted compact models, e.g.,

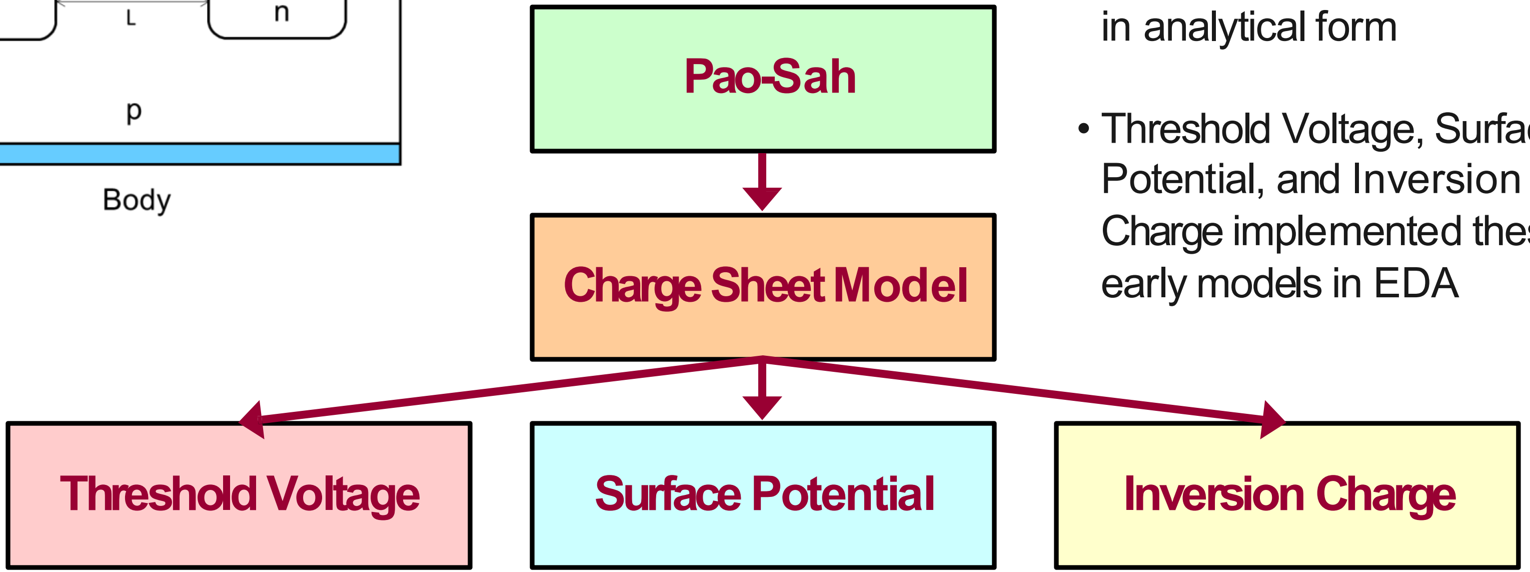
- MOSFETs: BSIM3, BSIM4, BSIMSOI, BSIM-CMG, EKV and PSP
- BJTs: Ebers-Moll and Gummel-Poon, HICUM, MEXTRAM

C. T. Sah, TechConnect Briefs, 2005

Introduction

History of Compact Modeling for MOSFET



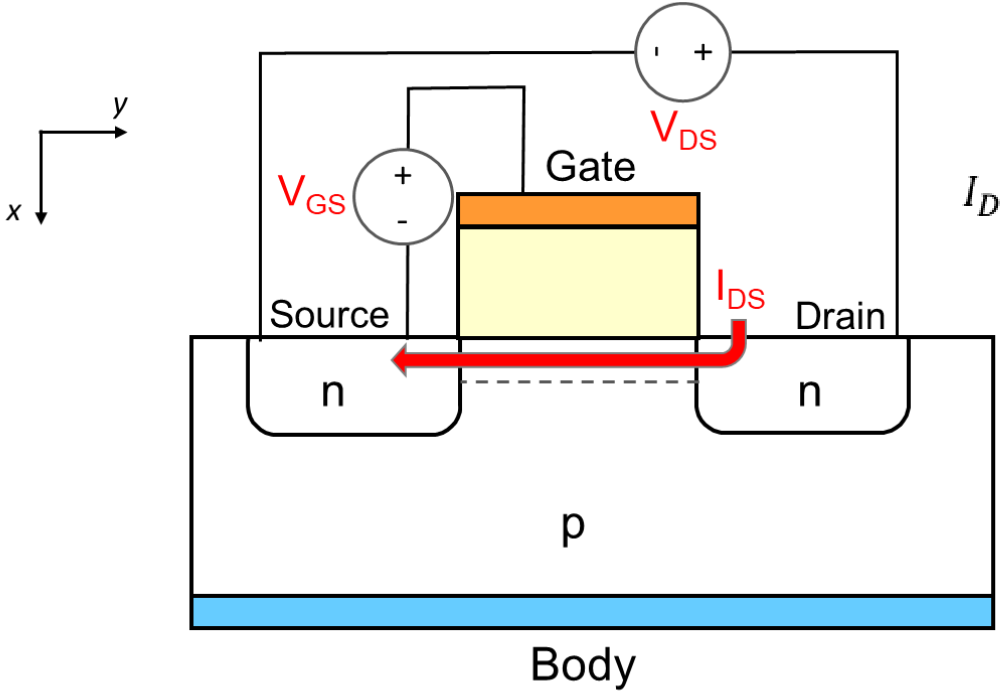


- Pao-Sah and Charge Sheet were early models that described MOSFET operation in analytical form
- Threshold Voltage, Surface Potential, and Inversion Charge implemented these early models in EDA

by Gildenblat, SRC Electronic Workshop, 2006

Introduction

The Pao-Sah Model (for n-channel MOSFET)



$$I_{DS} = \mu \frac{W}{L} \int_0^{V_{DS}} \underbrace{\left(\int_0^{\psi_s} qn(\psi, V) \frac{dx}{d\psi} d\psi \right)}_{Q_i \text{ (inversion charge)}} dV$$

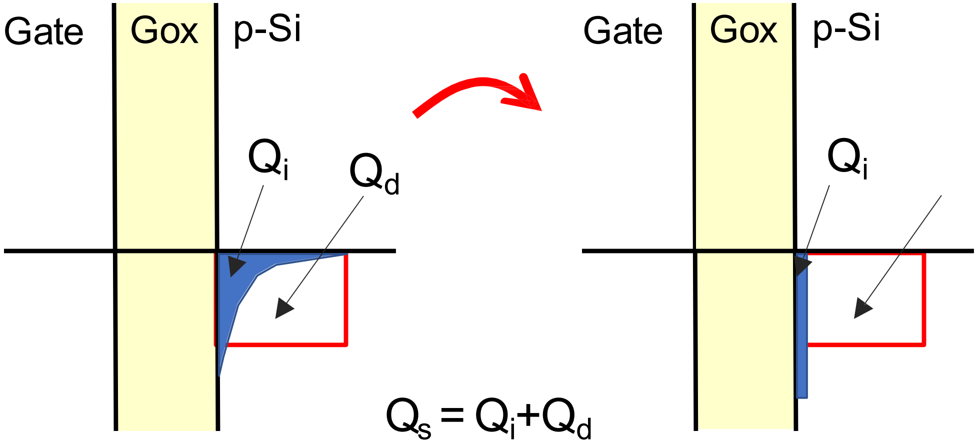
channel potential

$$\underbrace{\psi_s = V_{GS} - V_{fb} + \frac{Q_s}{C_{ox}}}_{\text{surface potential}}$$

By Pao and Sah, Solid-State Electron, 1966.
In Taur and Ning, Modern VLSI Devices, 1998

Introduction

The Charge Sheet Approximation



$Q_s = Q_i + Q_d$

$$Q_s = C_{OX}(V_{GS} - V_{fb} - \psi_s)$$

$$Q_d = \sqrt{2\epsilon_{Si} q N_A \psi_s}$$

$$Q_i = C_{OX}(V_{GS} - V_{fb} - \psi_s) - \sqrt{2\epsilon_{Si} q N_A \psi_s}$$

$$\psi_s = 2\phi_B + V$$

Channel potential

Bulk potential

$$I_{DS} = u\frac{W}{L}C_{OX}\left[\left(V_{GS} - V_{fb} - 2\phi_B - \frac{V_{DS}}{2}\right)V_{DS} - \frac{2}{3}\gamma\left[(2\phi_B - V_{DS})^{3/2} - (2\phi_B)^{3/2}\right]\right]$$

By J. R. Brews, Solid-State Electron., 1978.
In Taur and T. H. Ning, Modern VLSI Devices, 1998

Introduction

Threshold Voltage Model

Threshold Voltage

$$V_t = V_{fb} + 2\phi_B + \gamma\sqrt{2\phi_B}$$

Drain Current in Triode Mode

$$I_{DS} = u\frac{W}{L}C_{ox}\left[(V_{GS} - V_t)V_{DS} - \frac{n}{2}V_{DS}^2\right]$$

Drain Current in Saturation

$$I_{DSsat} = u\frac{W}{L}C_{ox}\frac{(V_{GS} - V_t)^2}{2n}$$

In Taur and Ning, Modern VLSI Devices, 1998

Introduction

BSIM4 Vt-based Compact Model

Strong Inversion Current

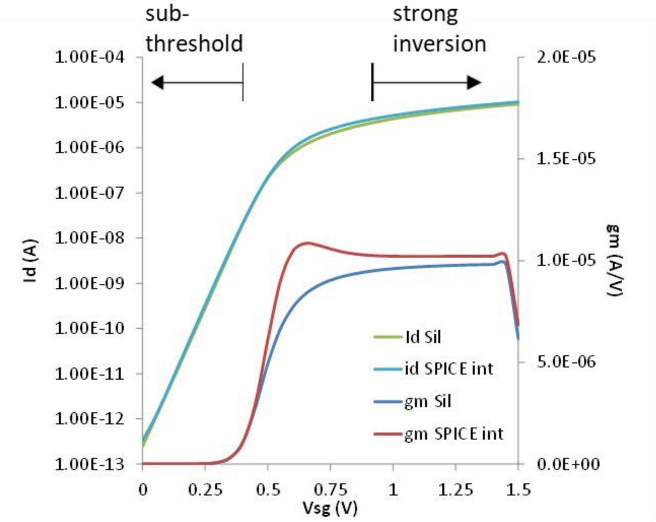
$$I_{ds} = \mu_{eff} C_{ox} \frac{W}{L} \frac{1}{1+V_{ds}/E_{sat}L}(V_{gs} - V_{th} - A_{bulk}V_{ds}/2)V_{ds}$$

Subthreshold Current

$$I_{ds} = I_{s0}(1-\exp(-\frac{V_{ds}}{v_t}))\exp(\frac{V_{gs}-V_{th}-V_{off}}{nv_t})$$

$$n = 1 + N_{factor}\frac{C_d}{C_{ox}} + \frac{(C_{dsc} + C_{dscd}V_{ds} + C_{dscb}V_{bseff})\left(\exp(-D_{VT1}\frac{L_{eff}}{2l_t}) + 2\exp(-D_{VT1}\frac{L_{eff}}{l_t})\right)}{C_{ox}} + \frac{C_{it}}{C_{ox}}$$

In BSM3 V3.2 Manual, 1998



.MODEL PMOD PMOS (LEVEL=11 TOX=5e-9 K1=0 K2=0 NCH=5E17
NSUB=5E17 VTH0=-0.4631 IS=1E-18
+VOFF=-.055 U0=300 NFACTOR=1 NLX=0 K3=0 DVT0W=0 DVT0=0
ETA0=0 ETAB=0 UA=0 UB=0 UC=0
+JSGBR=1E-8 JSDBR=1E-8 JSGSR=1E-8 JSDSR=1E-8 JSGGR=1E-8
JSDGR=1E-8 DIOMOD=0 PSCBE1=0 PSCBE2=0
+BF=.0001 CIT=0)

Introduction

Surface Potential Model

Surface Potential at Source

$$\psi_{S0} = V_{GB} - V_{fb} - \gamma\left(\psi_{S0} + \frac{kT}{q} e^{q(\psi_{S0} - 2\psi_B - V_{SB})/kT}\right)$$

Surface Potential at Source

$$\psi_{SL} = V_{GB} - V_{fb} - \gamma\left(\psi_{SL} + \frac{kT}{q} e^{q(\psi_{SL} - 2\psi_B - V_{DB})/kT}\right)$$

Channel Drift Current

$$I_{DS1} = u\frac{W}{L}C_{OX}\left[(V_{GB} - V_{fb})(\psi_{SL} - \psi_{S0}) - \frac{1}{2}(\psi_{SL}^2 - \psi_{S0}^2) - \frac{2}{3}\gamma\left(\psi_{SL}^{3/2} - \psi_{S0}^{3/2}\right)\right]$$

Channel Diffusion Current

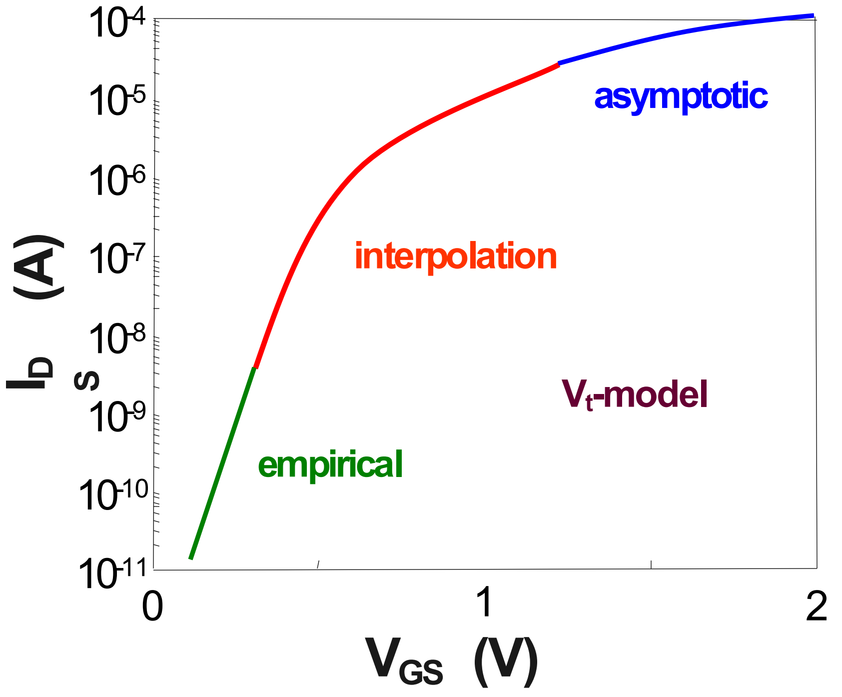
$$I_{DS2} = u\frac{W}{L}C_{OX}\left[\frac{kT}{q}(\psi_{SL} - \psi_{S0}) + \frac{kT}{q}\gamma\left(\psi_{SL}^{1/2} - \psi_{S0}^{1/2}\right)\right]$$

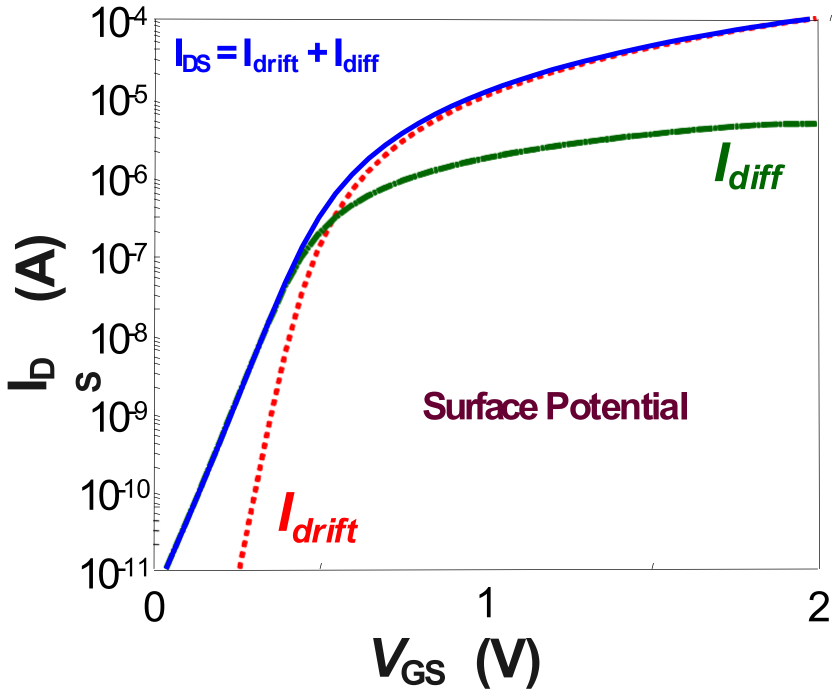
In Tsividis and McAndrew, 2011

In the surface potential model, solving for ψ_{S0} and ψ_{SL} explicitly is the tough part …

Introduction

Surface Potential vs. Vth Model





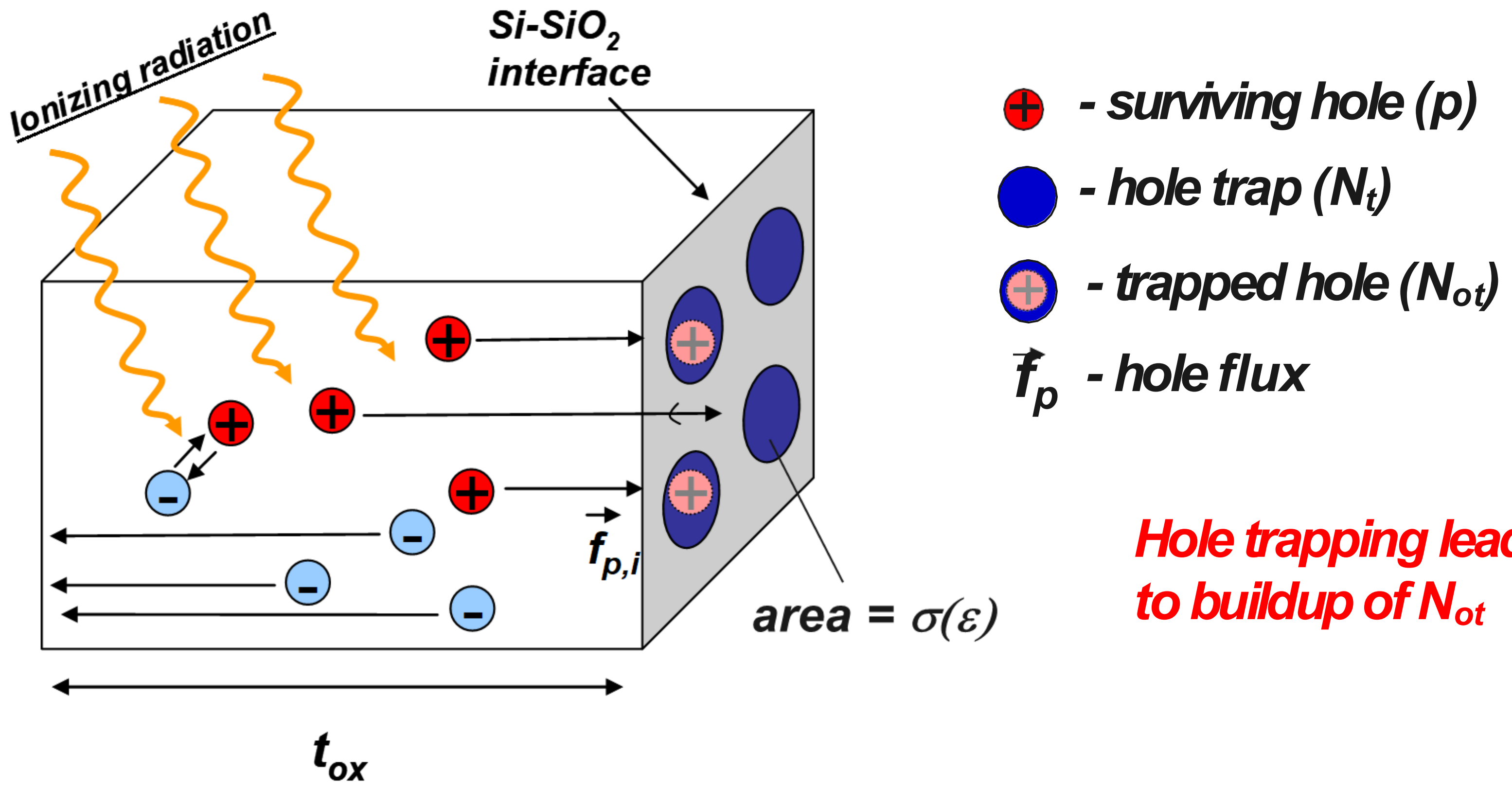
by Gildenblat, SRC Electronic Workshop, 2006

05

Modeling Mechanisms of Cumulative Radiation Effects

Modeling TID Effects

Hole Trapping Processes



Hole trapping leads to buildup of N_{ot}

Modeling TID Effects

Modeling Hole Trapping

$$\Delta N_{ot} = D g_0 f_y(\vec{\varepsilon}) N_T \sigma(\vec{\varepsilon}) t_{ox}$$

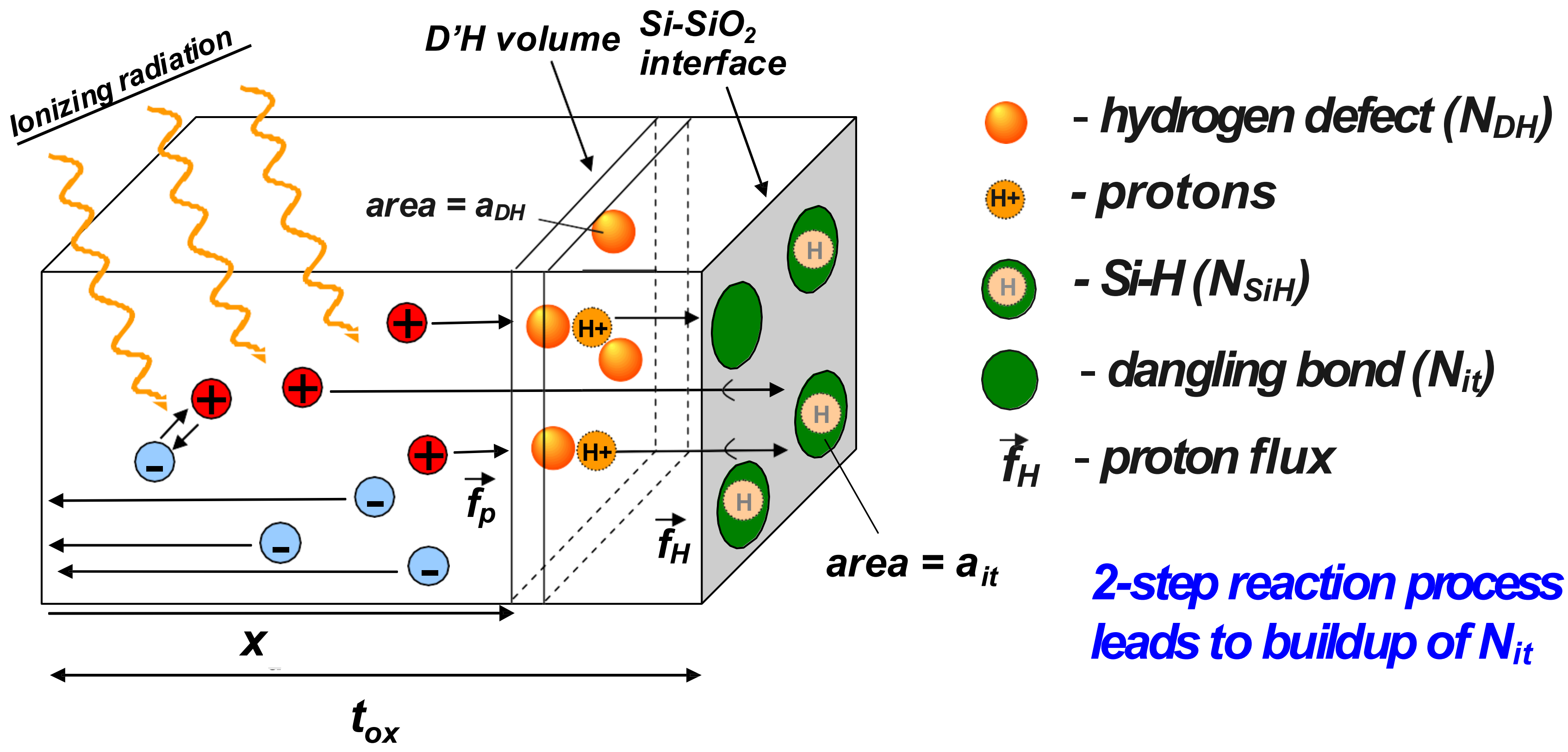
(by Fleetwood et al., TNS, 1994)

Model Parameters

- *D* - *total dose [rad]*
- g_0 - *8.1 x 10^12 [ehp/radcm^3]*
- f_y - *field dependent hole yield [hole/ehp]*
- N_T - *trapping efficiency [trapped hole/hole]*
- *a* - *field dependent cross-sectional area [cm^2]*
- t_{ox} - *oxide thickness [cm]*
- *ε* - *local electric field [V/cm]*

Modeling TID Effects

Interface Trap Formation



2-step reaction process leads to buildup of N_{it}

Modeling TID Effects

Modeling Interface Trap Formation

$$\Delta N_{it} = D g_0 f_y(\vec{\varepsilon}) N_{DH} \sigma_{DH} N_{SiH} \sigma_{it} \frac{{t_{ox}}^2}{2}$$

Model Parameters

(by Rashkeev et al. TNS, 2002)

- D - *total dose [rad]*
- g_0 - *8.1 x 10^{12} [ehp/radcm^3]*
- f_y - *field dependent hole yield [hole/ehp]*
- N_{DH} - *Hydrogen defects [cm^{-3}]*
- a_{DH} - *cross-section for hole trapping at hydrogen defects [cm^2]*
- N_{SiH} - *passivated dangling bands [cm^{-2}]*
- a_{it} - *cross-section for Hydrogen trapping [cm^2]*
- t_{ox} - *oxide thickness [cm]*

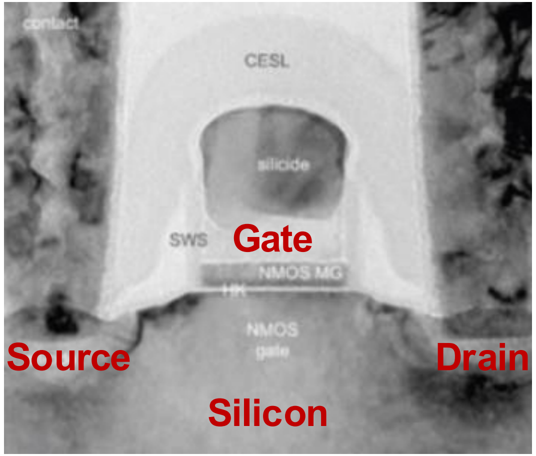
05

Modeling MOSFET Devices and Circuits

MOSFET structure

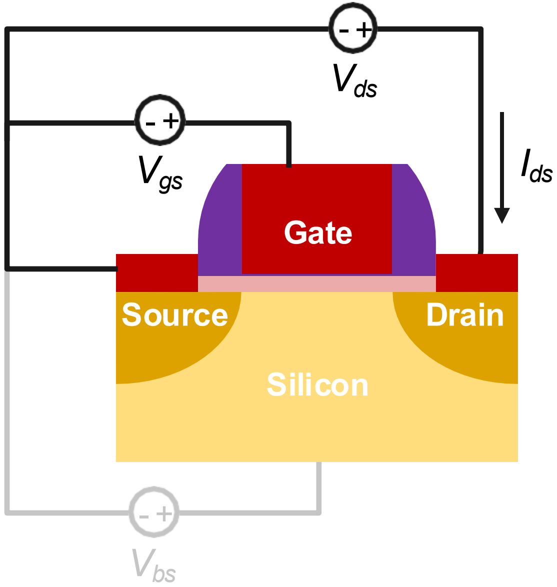
(bulk MOSFET)

28 nm bulk MOSFET



J. Yuan *et al.*, *IEEE ICSICT*, 2010.

Bulk MOSFET cross-sectional schematic



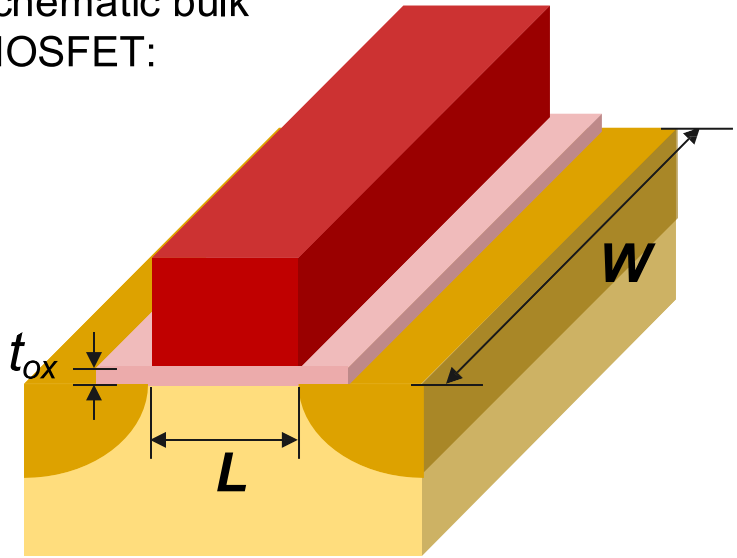
<u>In this section of the short course:</u>

- What are the (compact) modeling techniques to describe MOSFET operation?
- How are TID effects introduced into these models?
- Will focus on steady-state (DC) operation.

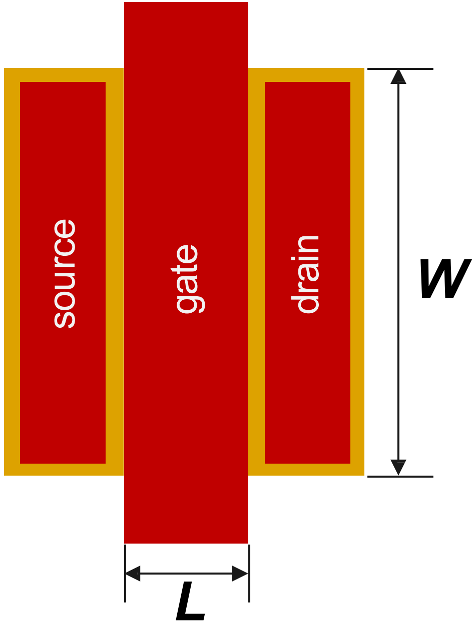
Critical Parameters

(bulk MOSFET)

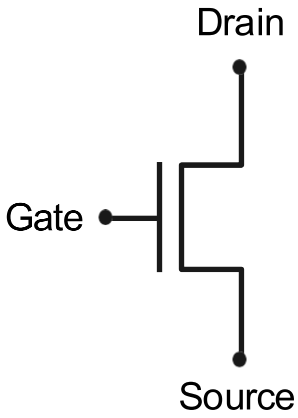
3-D cross-sectional schematic bulk MOSFET:



Top-view (layout):

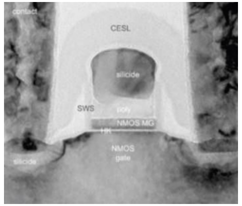


Circuit schematic symbol:

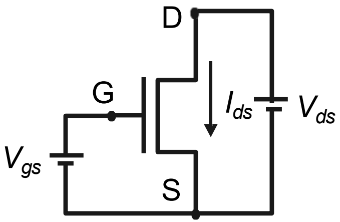


Example: 28 nm MOSFET data

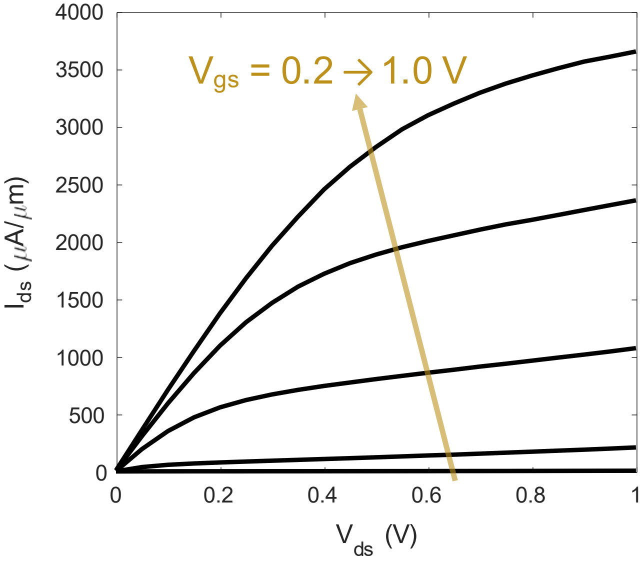
Measured at room temperature (300 K)



n-channel MOSFET
W = 200 nm
L = 30 nm

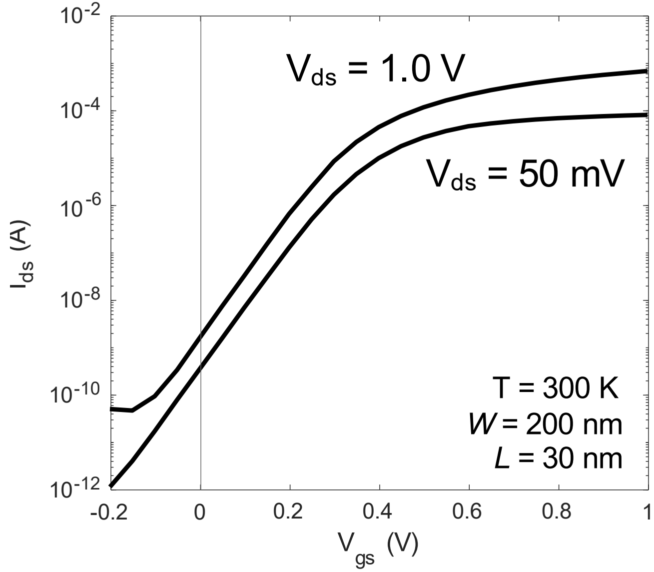


Output characteristics



- Fix V_{gs}, sweep V_{ds}
- Linear region: low V_{ds} (I ~ V)
- Saturation region: high V_{ds}
- Critical voltage V_{dsat}

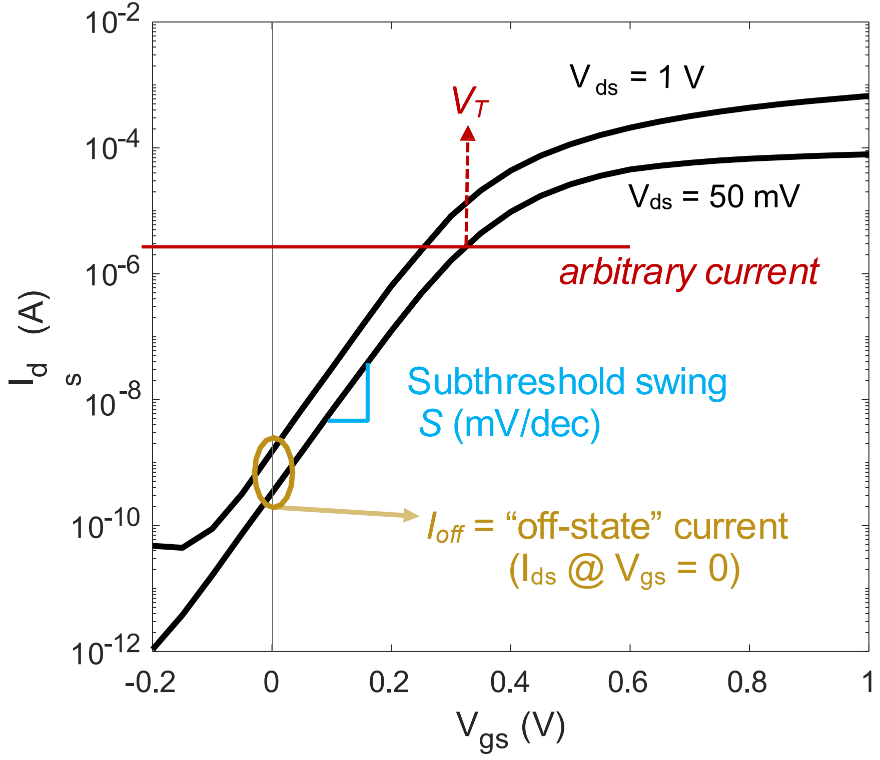
Transfer characteristics



- Fix V_{ds}, sweep V_{gs}
- Critical voltage V_T (threshold)
- Subthreshold region: $V_{gs} < V_T$
- Above V_T, device is “on”

Subthreshold current

Plot I_{ds} in log-scale!

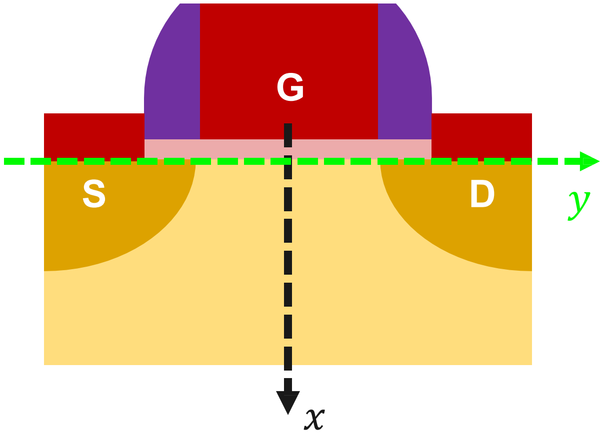


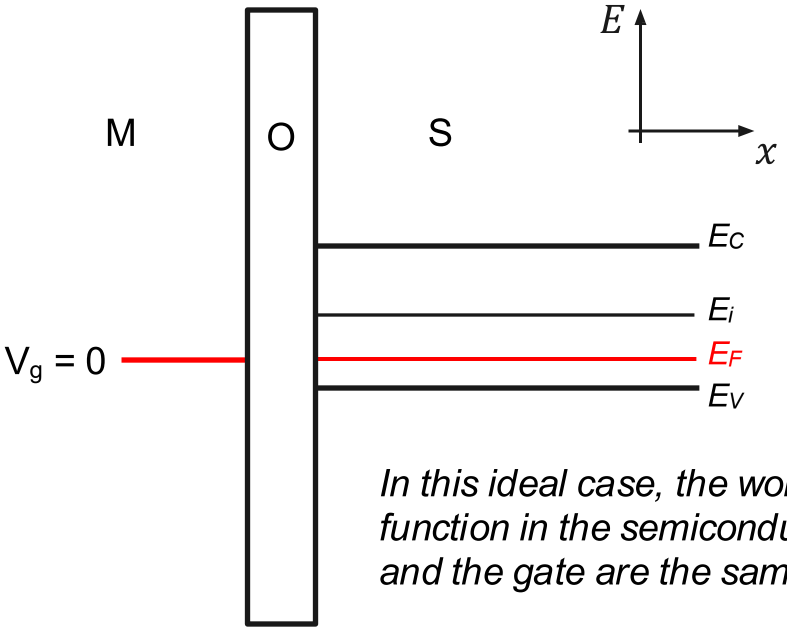
- Current not zero for V_{gs} below V_T
- We can see subthreshold current when I_{ds} plotted in log scale
- Below V_T current increases exponentially with V_{gs}
- V_T changes with V_{ds}! Drain-induced barrier lowering (DIBL)

- **What happens to these MOSFET parameters (I_{on}, I_{off}, V_T, S) with TID?**
- **How do we capture TID effects in compact models for circuit simulations?**

Energy Band Diagrams

A qualitative view of MOSFET operation

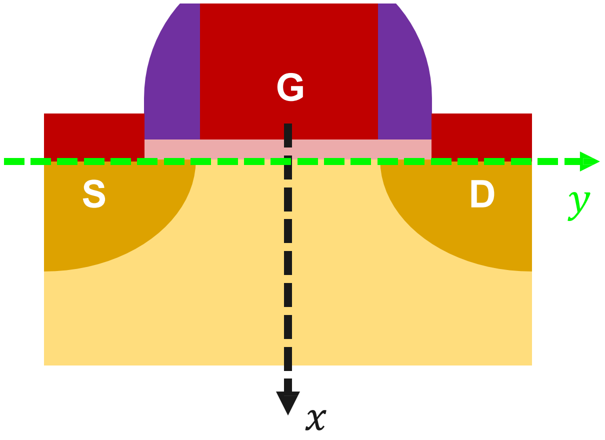




In this ideal case, the work function in the semiconductor and the gate are the same

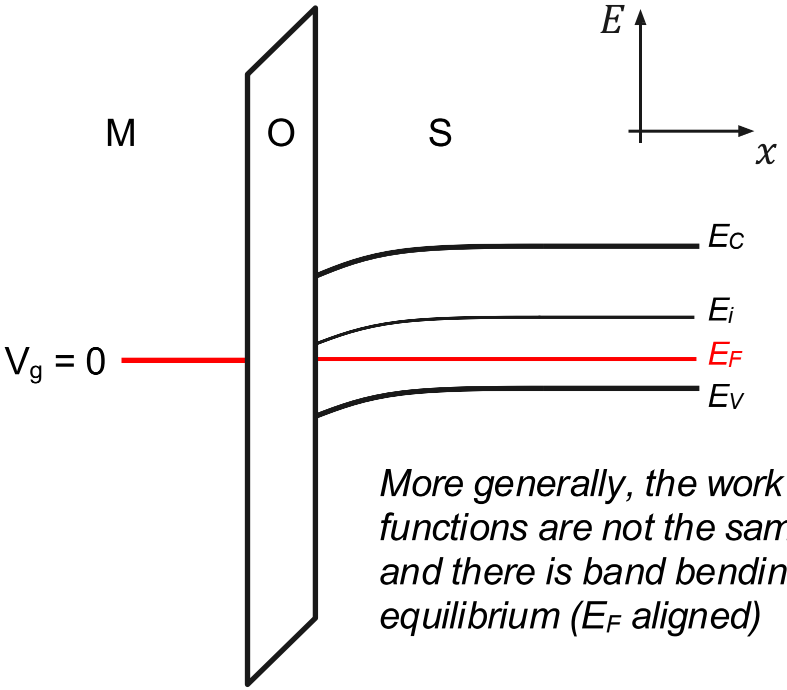
Energy Band Diagrams

A qualitative view of MOSFET operation



$$V_{FB} = q\Phi_{MS} = q\Phi_M - q\Phi_S$$

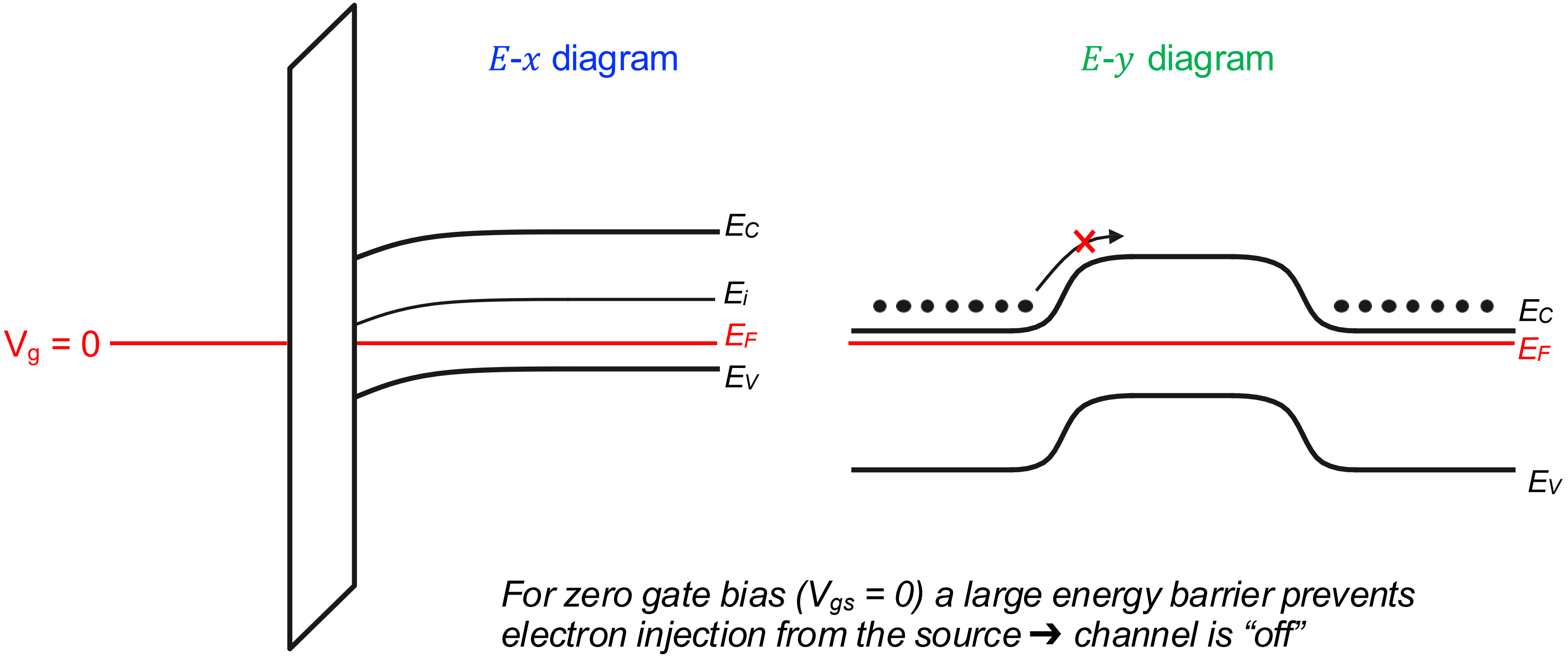
Flat-band voltage is the gate voltage needed to make the bands flat



More generally, the work functions are not the same, and there is band bending at equilibrium (E_F aligned)

Energy Band Diagrams

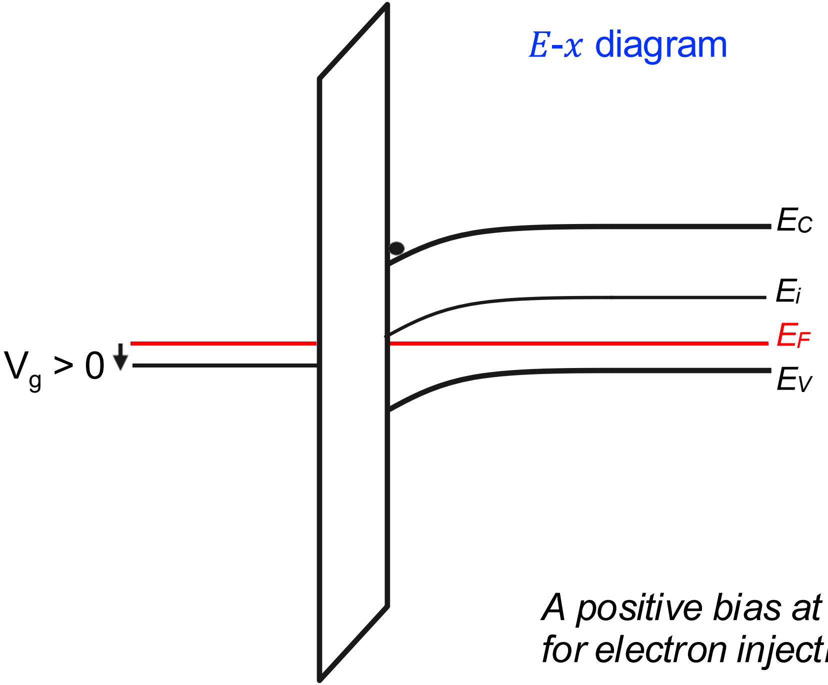
A qualitative view of MOSFET operation

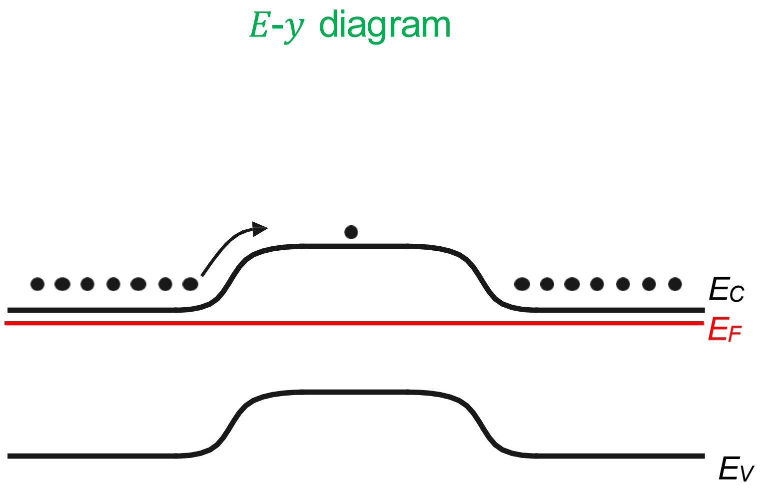


For zero gate bias ($V_{gs} = 0$) a large energy barrier prevents electron injection from the source ➔ channel is "off"

Energy Band Diagrams

A qualitative view of MOSFET operation

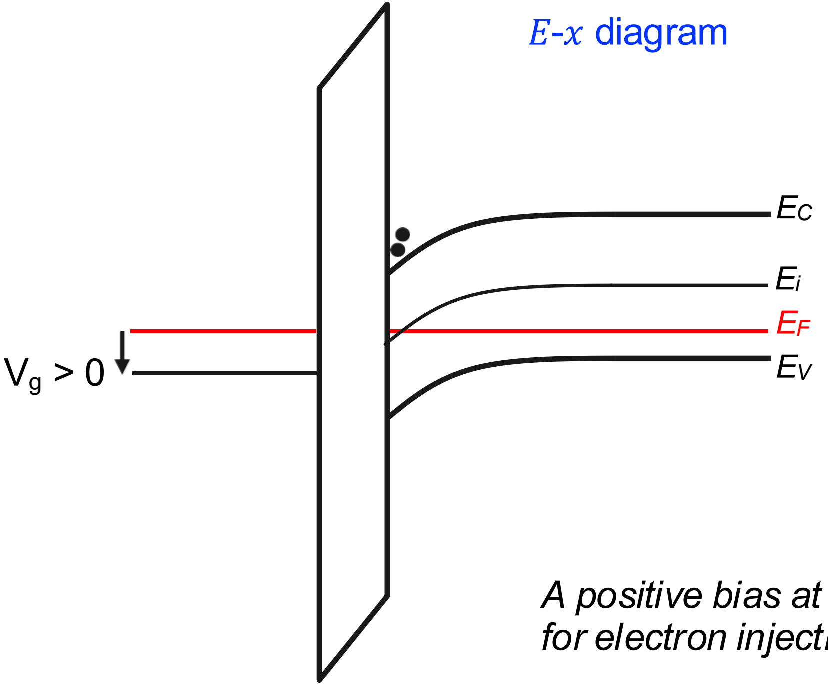


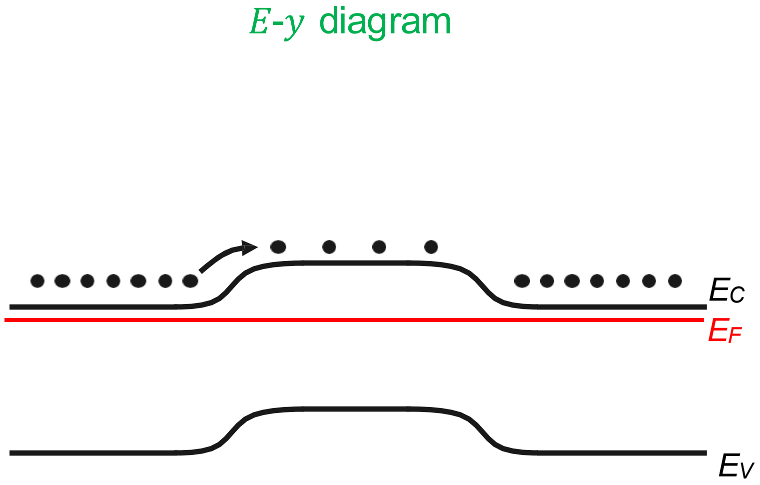


A positive bias at the gate ($V_{gs} > 0$) lowers the energy barrier for electron injection from the source ➔ channel turns "on"

Energy Band Diagrams

A qualitative view of MOSFET operation

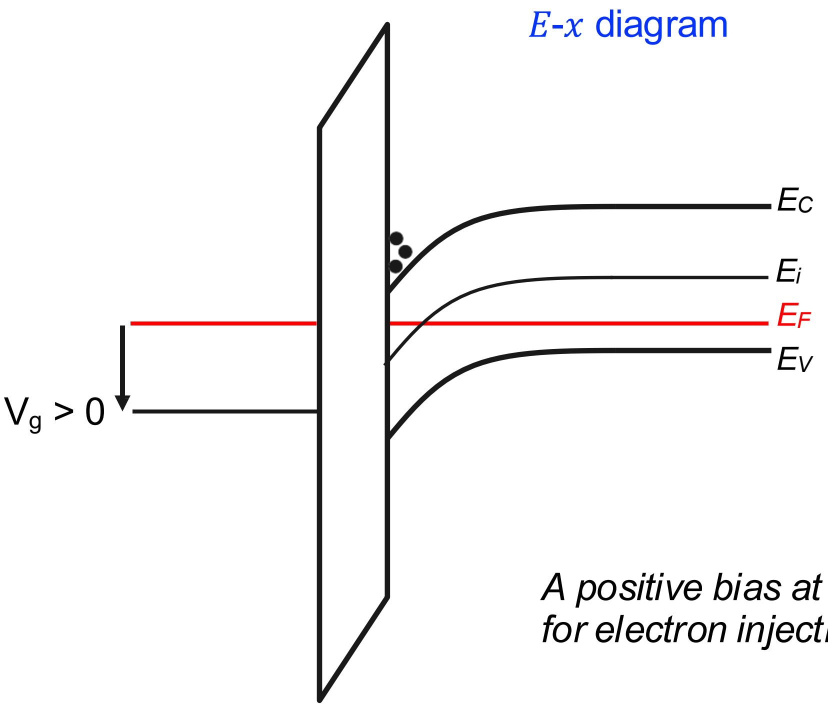


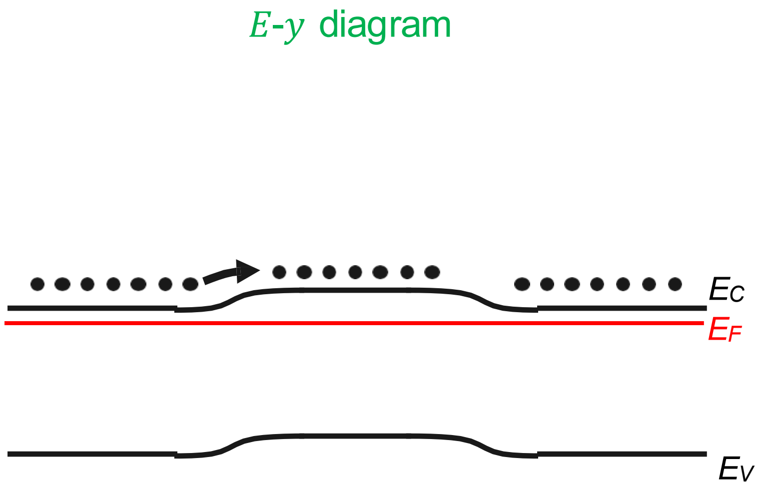


A positive bias at the gate (V_{gs} > 0) lowers the energy barrier for electron injection from the source ➔ channel turns "on"

Energy Band Diagrams

A qualitative view of MOSFET operation

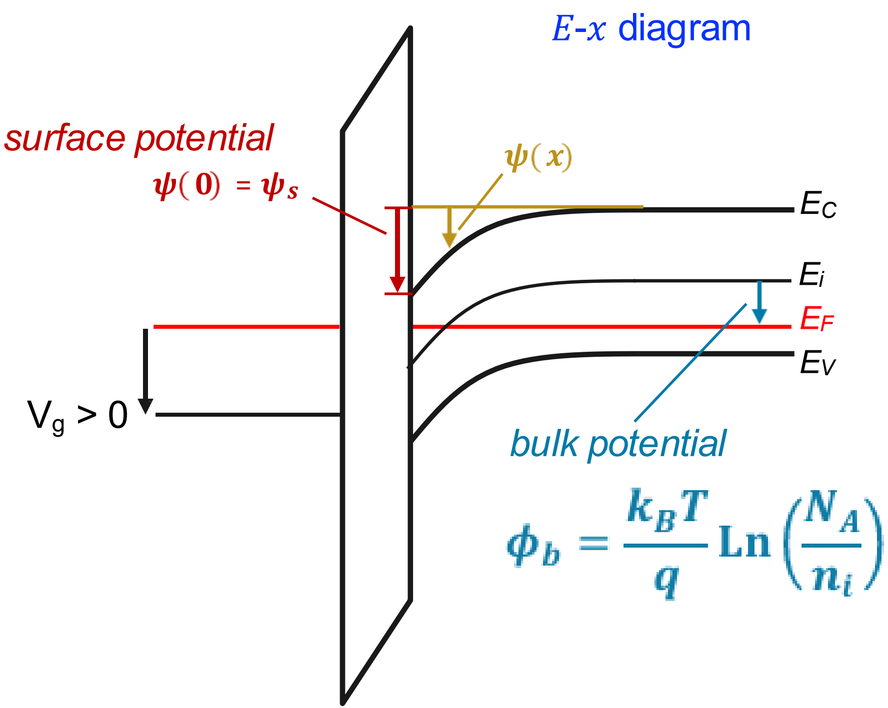




A positive bias at the gate (V_{gs} > 0) lowers the energy barrier for electron injection from the source ➔ channel turns "on"

Energy Band Diagrams

A qualitative view of MOSFET operation

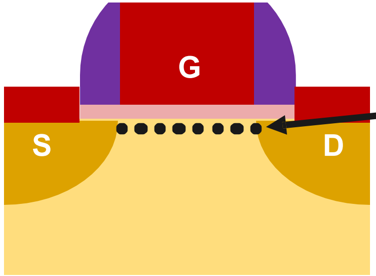


- Gate voltages above flatband result in positive surface potentials.
- Energy bands bend down, depletes surface of holes, builds up layer of electron charge (the inversion charge)
- When surface potential is twice the bulk potential, density of electrons at surface is equivalent to density of holes in bulk.
- We call this onset of strong inversion

Current-Voltage Relation

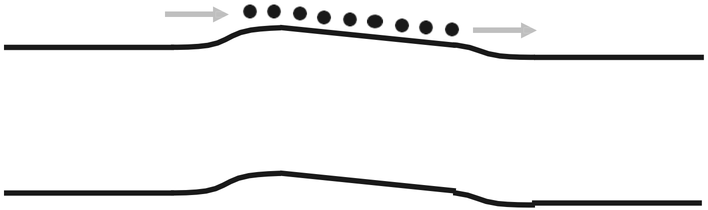
Linear (low V_{ds}) region

- With $V_{<(} > V_{=}$, the device is "on" and there is charge in the channel: $Q_{>}$



$V_{<(} > V_{=}$

Electron charge in channel (inversion layer)



- Current is given by: $I = -WQ_i v$
- $Q_i = -C_{ox}(V_{gs} - V_T)$
- $C_{ox} = \varepsilon_{ox}/t_{ox}$
- $v = \mu_n \mathcal{E}$
- $\mathcal{E} = V_{ds}/L$

$$\Rightarrow I = \frac{W}{L}\mu_n C_{ox}(V_{gs} - V_T)V_{ds}$$

Valid for small V_{ds}, $V_{gs} > V_T$

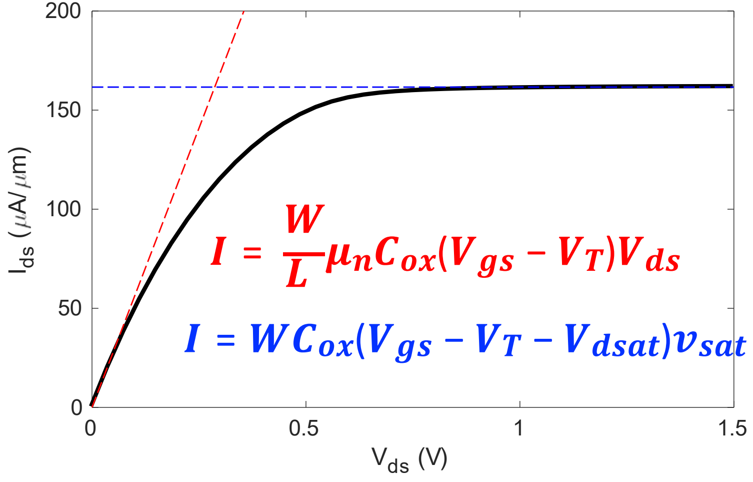
$$I_{ds} = \mu_{eff} C_{ox} \frac{W}{L} \frac{1}{1 + V_{ds}/E_{sat}L}(V_{gs} - V_{th} - A_{bulk}V_{ds}/2)V_{ds}$$ **BSIM4**

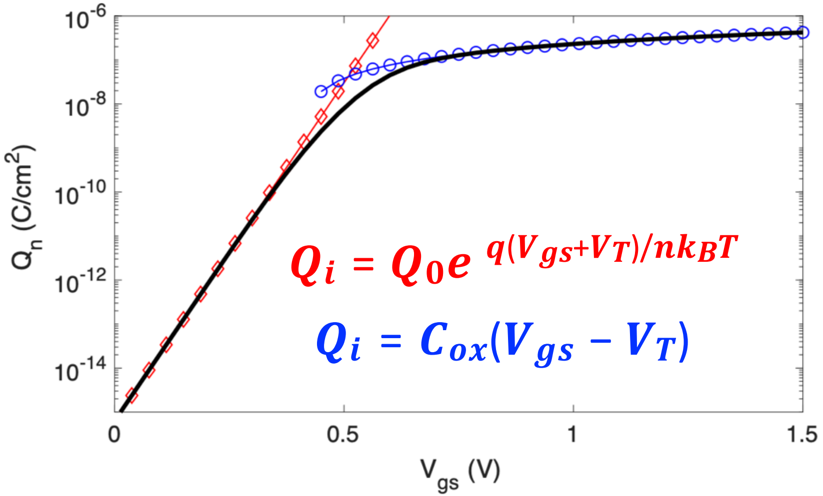
$$\mathrm{Id} = \mathrm{Q_i(x_0) \times (vxo) \times (Fsat) W}$$ ***MIT VS model***

Empirical unified models

BSIM, VS, etc.

- In BSIM (earlier V_T based versions) **smoothing functions** used to transition between:
  1. V_{ds} and V_{dsat} (linear to saturation regions)
  2. Inversion charge Q_i below and above V_T (weak to strong inversion regions)

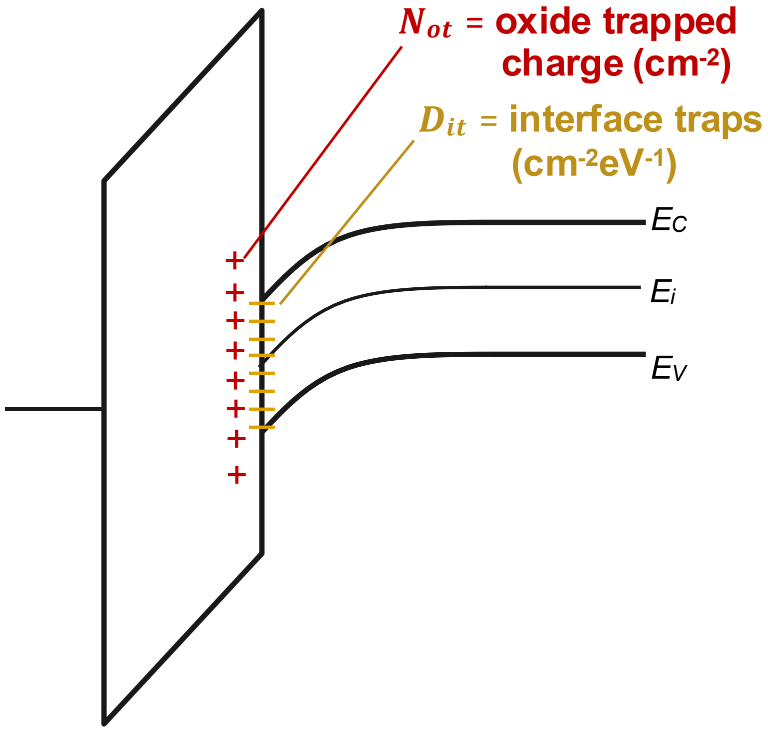




How do we define V_T and n such that we account for TID effects?

TID-induced defects

Oxide and interface traps



- The effect of N_{ot} is typically captured as a change in the flat-band voltage (ΔV_{FB})

$$\Delta V_{FB} = -\frac{qN_{ot}}{C_{ox}}$$

- Can account for this ΔV_{FB} in the threshold voltage parameter as

$$\Rightarrow V_T = V_{T0} - \frac{qN_{ot}}{C_{ox}}$$

- What about interface traps? Charge due to D_{it} depends on the type of traps (acceptor-like or donor-like) and their occupancy (trap energy level relative to E_F)

TID-induced defects

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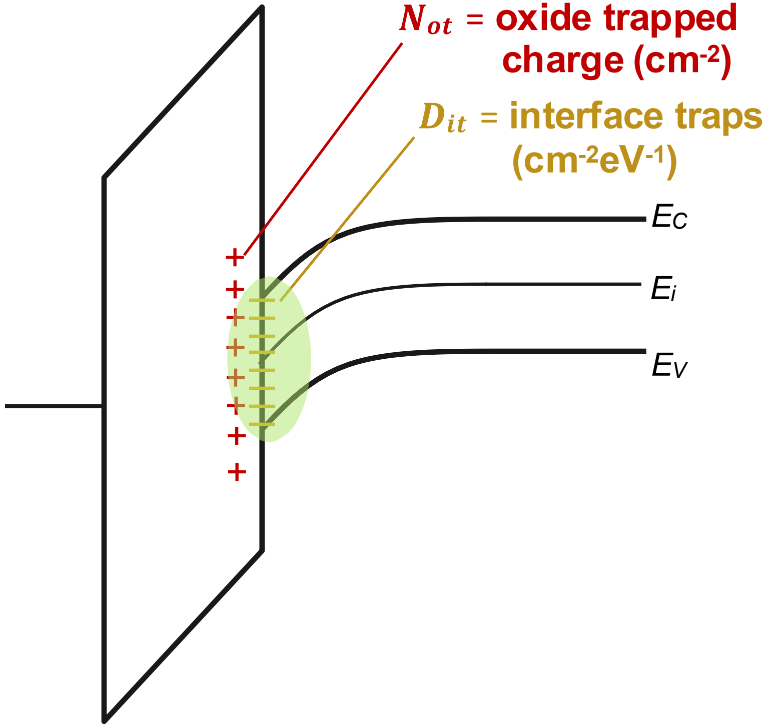

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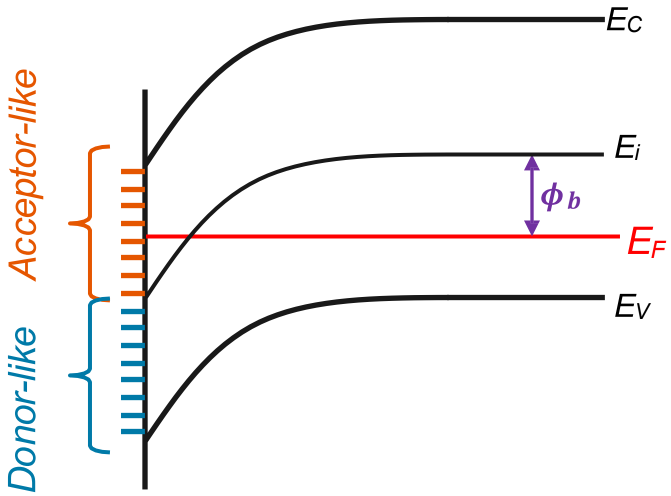

➔ Acceptor-like: Neutral when empty, negatively charged when filled

➔ Donor-like: Neutral when filled, positively charged when empty

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  In this example, the net charge contribution from interface traps is *<u>negative</u>* *(filled acceptor-like traps)*

TID-induced defects

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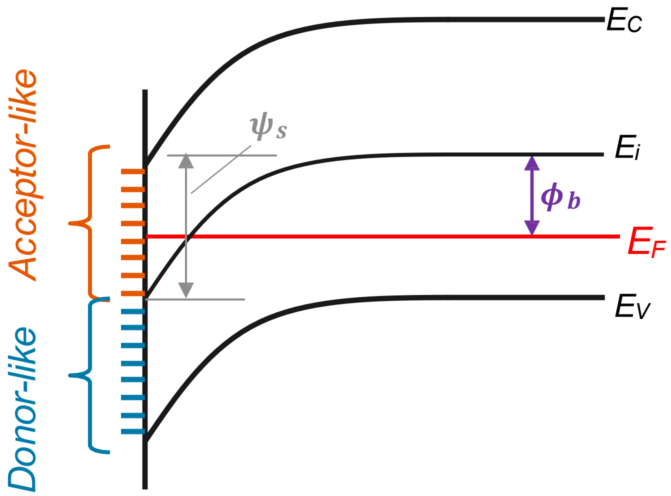

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TID-induced defects

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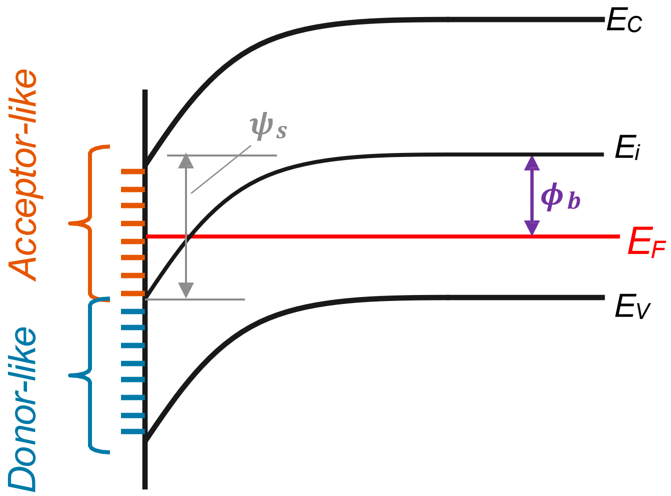

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  More generally, can be modeled as a function of the surface potential ψ_s as:

$$qN_{it} = -qD_{it}(\psi_s - \phi_b)$$

- Total TID-induced charge contribution to MOS:

$$q_{TID} = qN_{ot} - qD_{it}(\psi_s - \phi_b)$$

Subthreshold charge and current

- By solving Poisson's equation, we obtain the charge in the semiconductor:

$$-Q_S = \sqrt{2\varepsilon_s k_B T N_A}\left[\frac{q\ \ _s}{k_B T} + \frac{n_i^2}{N_A^2} e^{q\psi_s/k_B T}\right]^{1/}$$

- This contains both depletion and inversion charge, $Q_S = Q_d + Q_i$.
- For weak inversion (subthreshold) we obtain Q_i from a power series expansion:

$$-Q_i = \sqrt{\frac{\varepsilon_s q N_A}{2\psi_s}}\left(\frac{k_B T}{q}\right)\frac{n_i^2}{N_A^2} e^{q\psi_s/k_B T}$$

- **We want ψ_s in terms of V_{gs}…**

$$V_{gs} - V_{FB} = V_{ox} + \psi_s = \mathcal{E}_{ox} t_{ox} + \psi_s$$

- <u>Boundary condition at interface</u>:

$$\varepsilon_s \mathcal{E}_s - \varepsilon_{ox}\mathcal{E}_{ox} = q_{TID} = qN_{ot} - qD_{it}(\psi_s - \phi_b)$$

Normal component of the displacement field is discontinuous across an interface where a surface charge exists.

- Using $V_{gs} = V_{FB} + \mathcal{E}_{ox} t_{ox} + \psi_s$, expand at $\psi_s = 2\phi_b$:

$$V_{gs} = V_{FB} + 2\phi_b - \frac{Q_{d(2\phi_b)}}{C_{ox}} - \frac{qN_{ot}}{C_{ox}} + \frac{qD_{it}\phi_b}{C_{ox}}$$

$$+ \left[1 - \frac{dQ_d/d\psi_s}{C_{ox}} + q\frac{D_{it}}{C_{ox}}\right](\psi_s - 2\phi_b)$$

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$$+ \left[1 - \frac{dQ_d/d\psi_s}{C_{ox}} + q\frac{D_{it}}{C_{ox}}\right](\psi_s - 2\phi_b)$$

$$n = 1 + C_D/C_{ox} + C_{it}/C_{ox}$$

Subthreshold charge and current

- Now we can solve for ψ_s

$$\psi_s = (V_{gs} - V_T)/n + 2\phi_b$$

- And substitute into Q_i to obtain

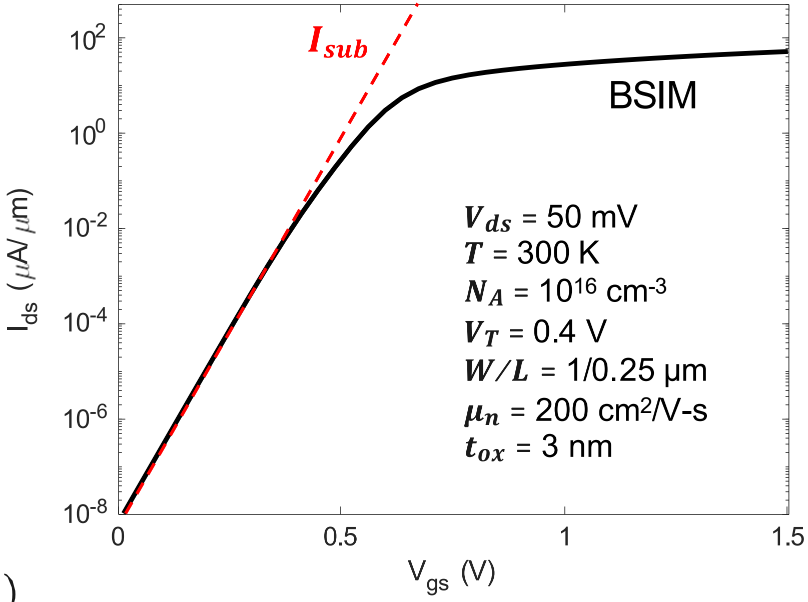
$$-Q_i = \sqrt{\frac{\varepsilon_s q N_A}{4\phi_b}}\left(\frac{k_B T}{q}\right) e^{q(V_{gs}-V_T)/nk_BT}$$

$$n = 1 + C_b/C_{ox} + C_{it}/C_{ox}$$

$$V_T = V_{T0} - q(N_{ot} - qD_{it}\phi_b)/C_{ox}$$

- From Q_i we can get the subthreshold current:

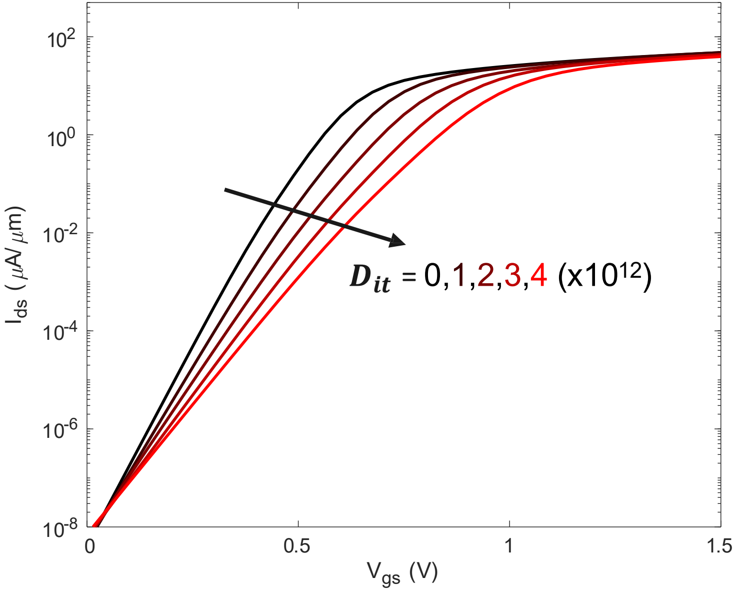
$$I_{sub} = \mu_n \frac{W}{L}\sqrt{q N_A \varepsilon_s / 4\phi_b}\left(\frac{k_B T}{q}\right)^2 e^{\frac{q(V_{gs}-V_T)}{nk_BT}}\left(1 - e^{-qV_{ds}/k_BT}\right)$$

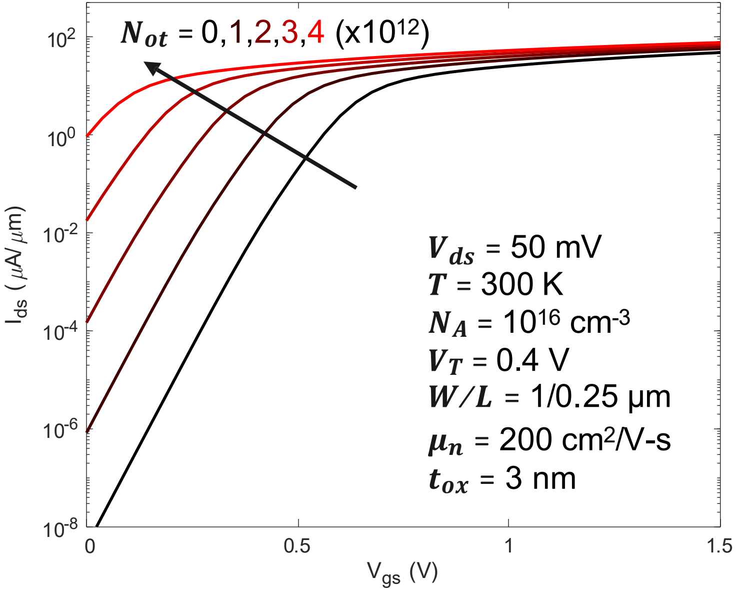


Example model calculations

Including oxide and interface traps

- The following calculations (using correct versions of V_T and n) show the individual effects of D_{it} and N_{ot} :

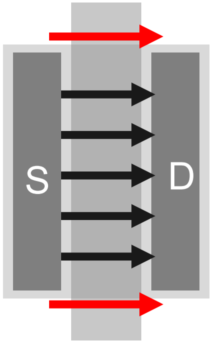




Edge leakage in bulk MOSFETs

Defect buildup in STI ➔ parasitic device

- In modern MOSFETs the gate oxide is thin (~ few nm) and less susceptible to buildup of TID-induced defects. Main concern is in the shallow trench isolation (STI) oxide ➔ parasitic edge leakage



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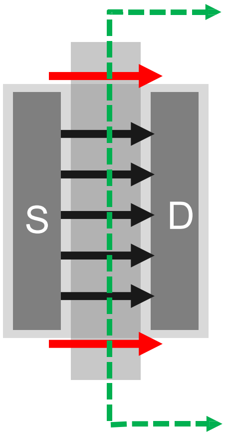

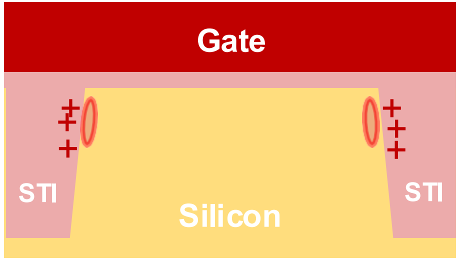

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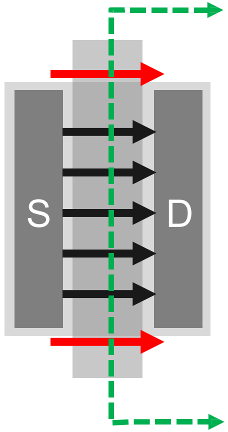
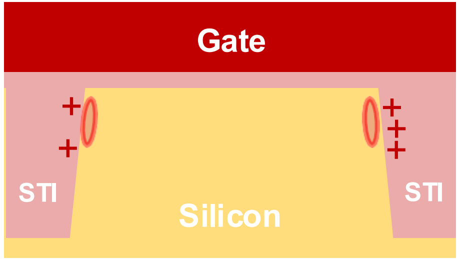
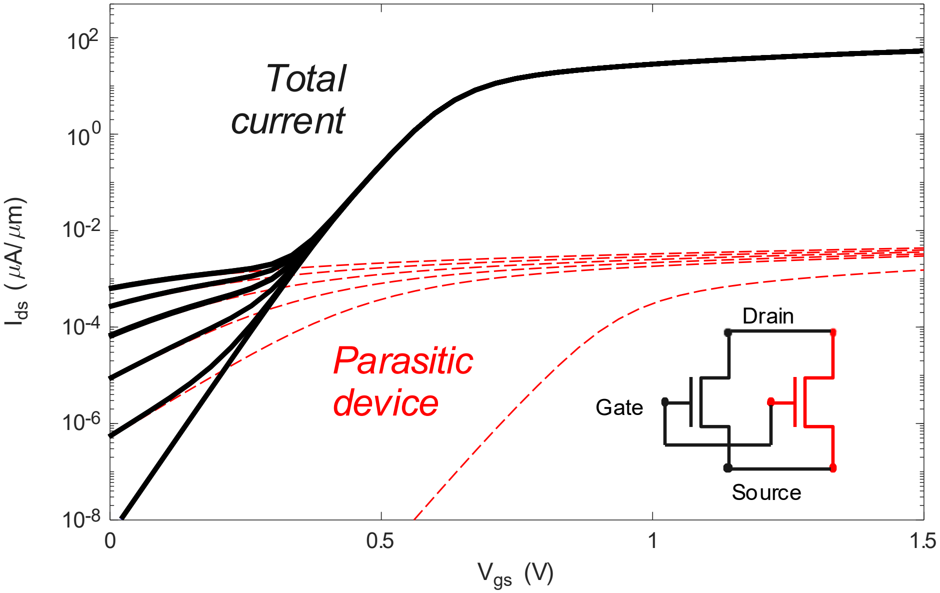






Surface-potential based models

Modified SPE

- Most recent versions of industry standard MOSFET compact models are based on surface-potential ψ_s, not V_T.
- A ψ_s approach makes sense for modeling impact of radiation and stress-induced defects (N_{ot} and D_{it}).

<u>Approach:</u>

1. Solve modified surface potential equation (mSPE): Introduces N_{ot} and D_{it} into calculations of ψ_s
2. From calculations of ψ_s can then obtain current (drift diffusion), charge, etc.

► <u>A defect potential approach</u>: Does not require to change foundry provided model parameters or equations.

- We start with Poisson's equation:

$$\frac{d^2\psi}{dx^2} = -\frac{\rho}{\varepsilon_s} = -\frac{q}{\varepsilon_s}(p - n - N_A)$$

- Using Boltzmann statistics, we integrate to obtain:

$$\mathcal{E}_s^2 = \left(\frac{2qN_a}{\beta\varepsilon_s}\right) H(\beta\psi_s)$$

$$H(\beta\psi_s) = e^{-\beta\psi_s} + \beta\psi_s - 1 + e^{-2\beta\phi_b}(e^{\beta\psi_s} - \beta\psi_s - 1)$$

- To obtain relation between gate voltage and surface potential: $V_{gs} - V_{FB} = V_{ox} + \psi_s$ and boundary condition: $\varepsilon_s\mathcal{E}_s - \varepsilon_{ox}\mathcal{E}_{ox} = q_{TID}$

$$q_{TID} = qN_{ot} - qD_{it}(\psi_s - \phi_b)$$

Surface-potential based models

Modified SPE

- Putting it all together we obtain:

$$\left(V_{gs} - V_{FB} - \psi_s\right)^2 = \gamma^2 \phi_t\, H(\beta\psi_s)$$

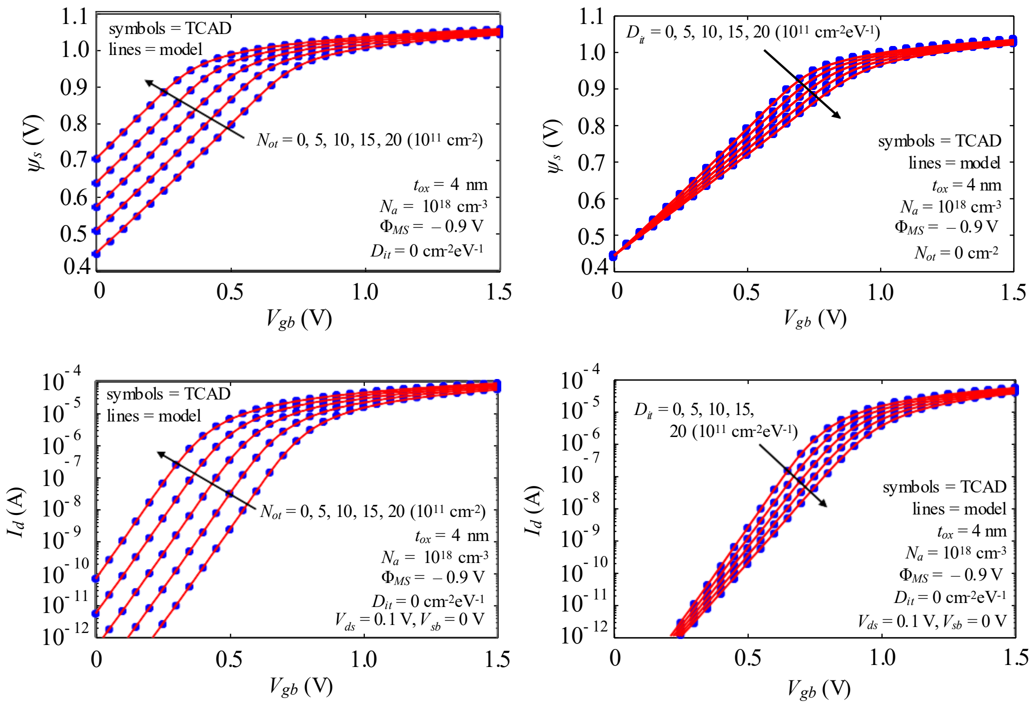
$$V_{FB} = q\Phi_{MS} - \frac{q}{C_{ox}}\left[N_{ot} - D_{it}\left(\psi_s - \phi_b\right)\right]$$

$$\gamma = \sqrt{2q\varepsilon_s N_A}\,/C_{ox}$$

***"modified* SPE"**

- mSPE incorporates the charge contribution from N_{ot} and D_{it}
- mSPE is an implicit function of ψ_s, can be solved numerically as a function of V_{gs} for a given N_{ot} and D_{it}
- Accurate analytical approximations (closed-form) are available.

See Esqueda *et al*, *JSSE,* vol. 91, pp. 81-86, 2014 for non-iterative approach.

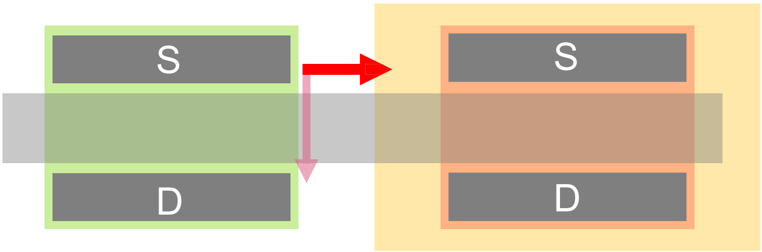


I. S. Esqueda *et al*, IEEE TNS 2015

Surface-potential based models

Inter-device leakage

- N_{ot} and D_{it} buildup in STI can also lead to inter-device leakage (leakage between two separate devices)



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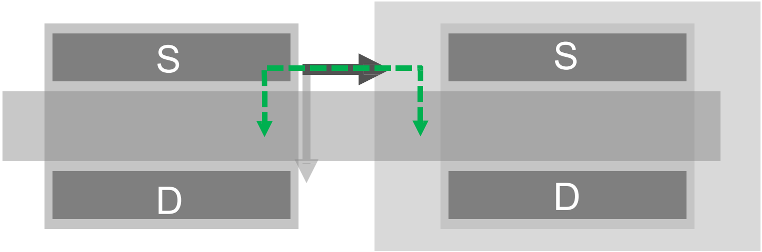

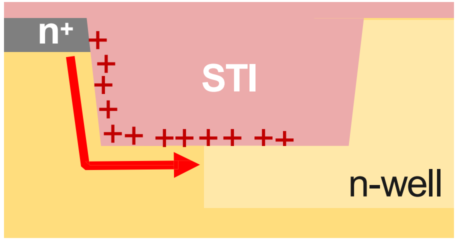

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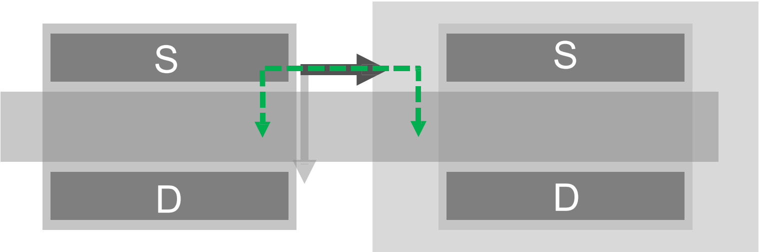
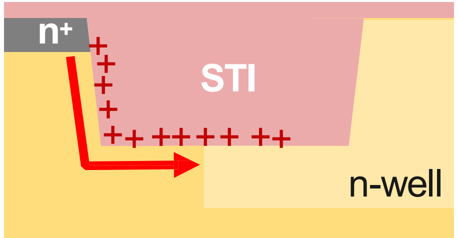
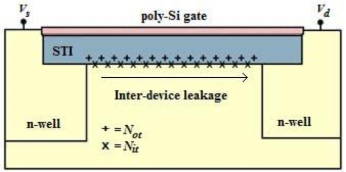
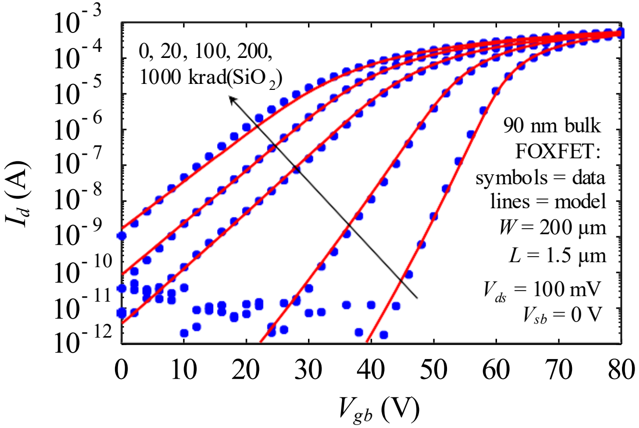


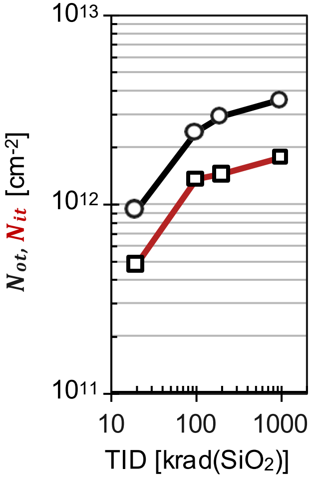


- We can extract/study the buildup of N_{ot} and D_{it} in STI using FOXFETs:



I. S. Esqueda *et al*, IEEE TNS 2011
I. S. Esqueda *et al*, IEEE TNS 2015
(model incorporated into PSP)





Defect potential *external* model

A "sub-circuit" Verilog-A approach

- In this approach, we do **not** need to change the foundry provided model parameters or equations
- An accurate non-iterative method is used to solve the mSPE (Esqueda *et al*, *JSSE*, vol. 91, pp. 81-86, 2014)

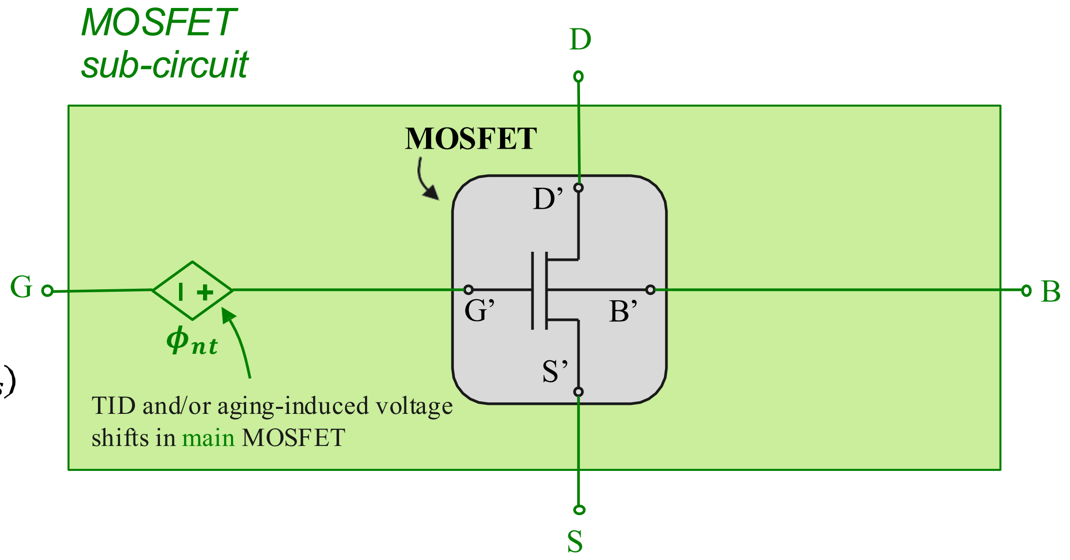
1. Solve the mSPE:

$$\left(V_{gs} - q\Phi_{MS} + \phi_{nt} - \psi_s\right)^2 = \gamma^2 \phi_t H(\beta\psi_s)$$

2. From solution (ψ_s):

$$\phi_{nt} = \frac{q}{C_{ox}}\left[N_{ot} - D_{it}(\psi_s - \phi_b)\right]$$

"defect potential"



I. S. Esqueda *et al*, *IEEE IIRW* 2013, **(Hot Carriers, Bias-Temperature Instability)**
I. S. Esqueda *et al*, *JSSE* 2014 **(Hot Carriers)**
I. S. Esqueda *et al*, *IEEE TNS* 2015 **(Total-Ionizing Dose)**
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R. Fang *et al*, *J. Appl. Phys.*, 2018 **(Hot Carriers, Bias-Temperature Instability)**

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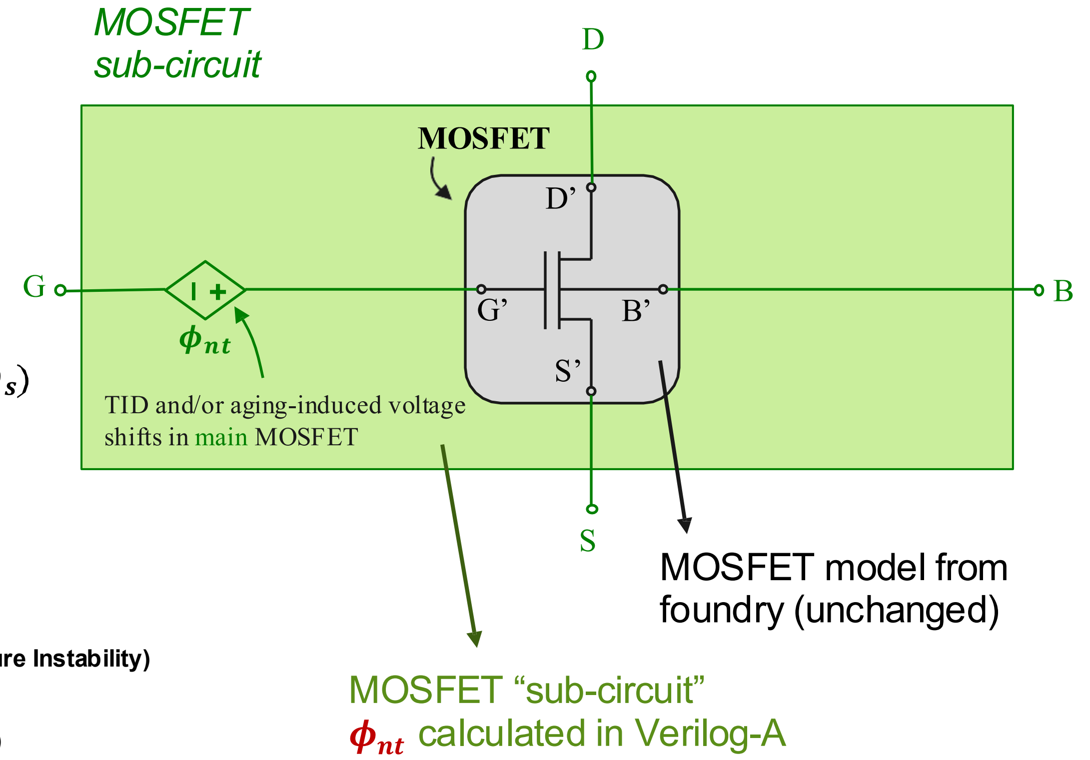

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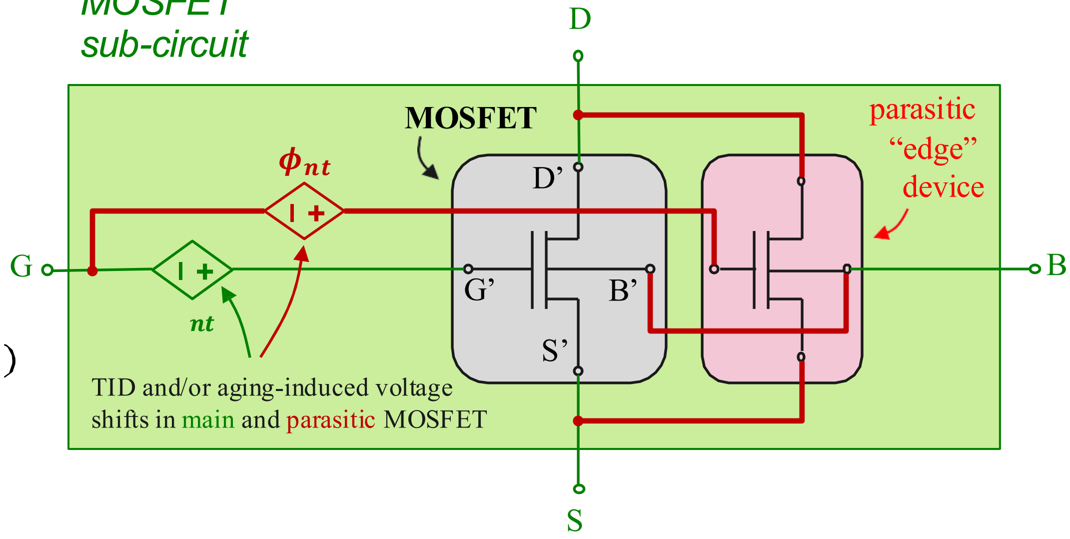
"defect potential"

MOSFET sub-circuit



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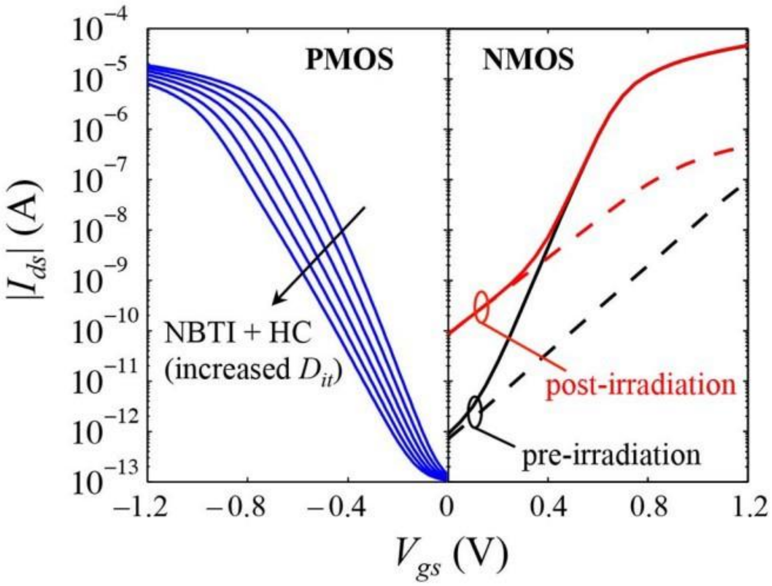
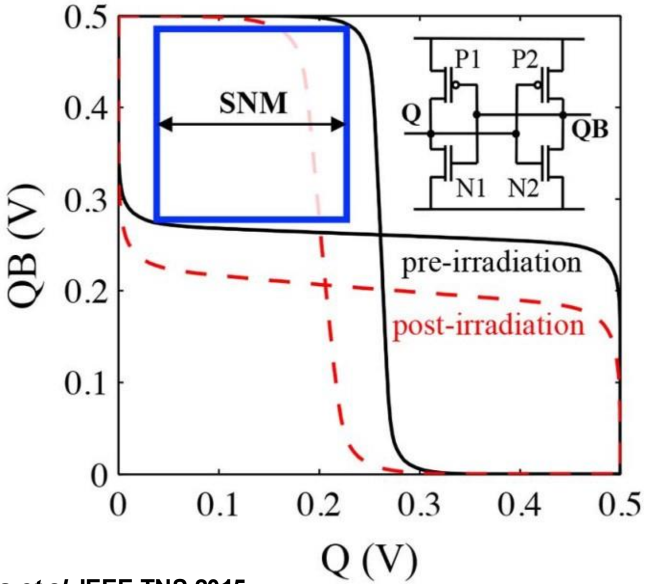
Combined effects (Aging + TID)

Example: SRAM SNM and minimum retention voltage

- In this example, pMOS devices are degraded as a result of BTI and HCD (buildup of D_{it}), nMOS devices suffer TID-induced edge leakage (modeled as parasitic device)
- The static noise margin (SNM) is extracted from the mirrored voltage transfer characteristics (VTC) of SRAM inverters.



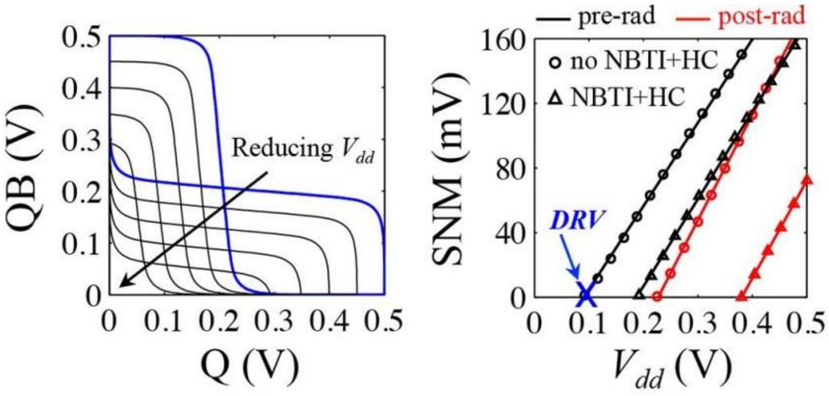


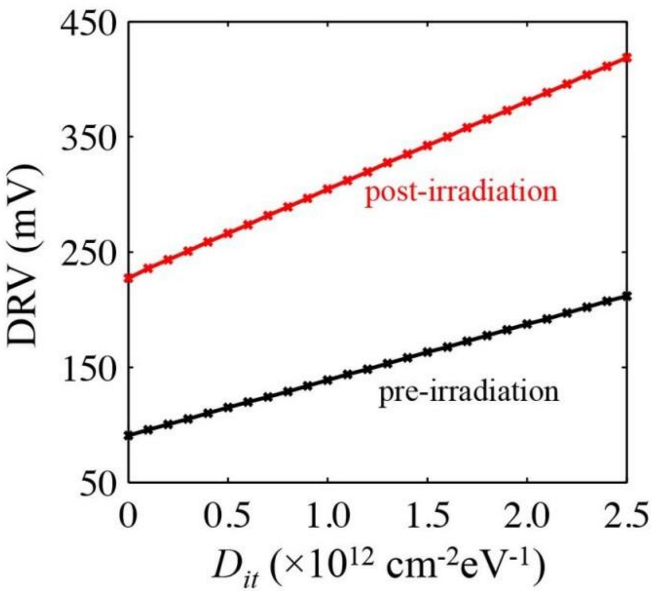
I. S. Esqueda *et al*, IEEE TNS 2015

Combined effects (Aging + TID)

Example: SRAM SNM and minimum retention voltage

- Can extract SNM as a function of the supply voltage V_{dd}, and obtain the minimum data retention voltage (DRV), i.e., the supply voltage for which SNM vanishes.
- The combined impact of TID and aging effects on SRAM cell stability can be analyzed based on this modeling approach.





I. S. Esqueda *et al*, IEEE TNS 2015

Module Summary

In this module we have described techniques and tools for modeling cumulative radiation effects in MOSFETs and CMOS circuits

- At beginning of course, we introduced many of the models, modeling approaches, and tools that make IC analysis and design possible
- Next, we presented models and tools for calculating the build-up and annealing of defects when semiconductor materials are damaged by TID
- We presented TID radiation-aware modeling techniques for MOSFETs and CMOS circuits