



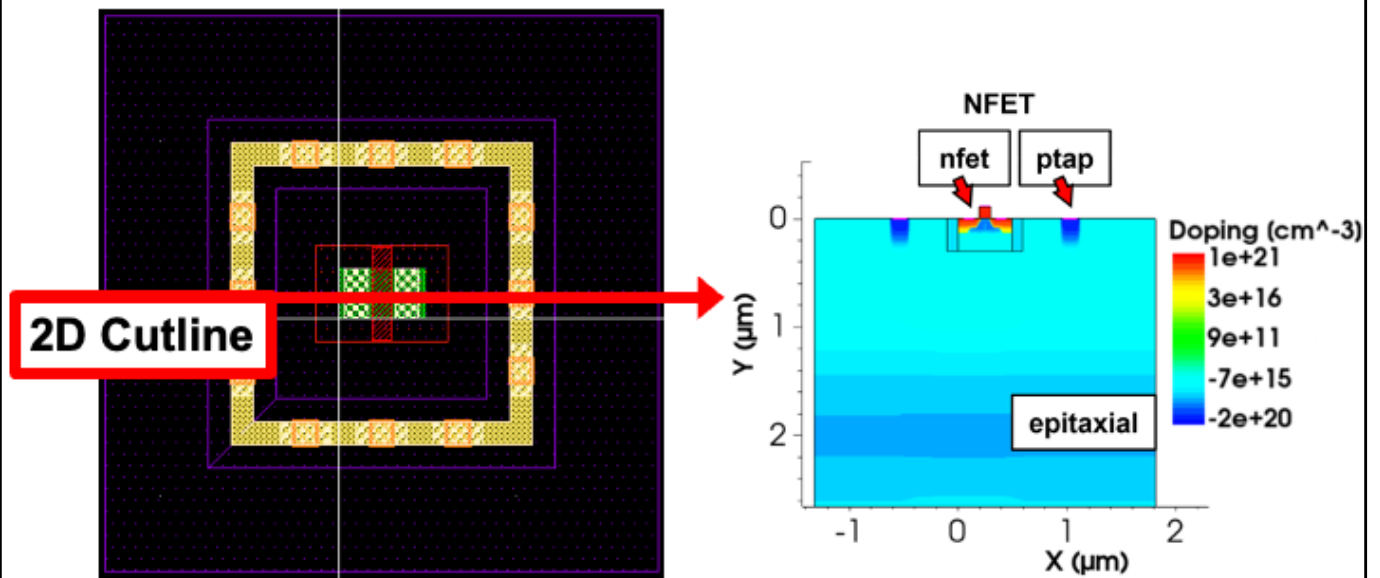
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INDIANA UNIVERSITY

# **TCAD Modeling of SEE in a 90 nm Blk CMOS Process**

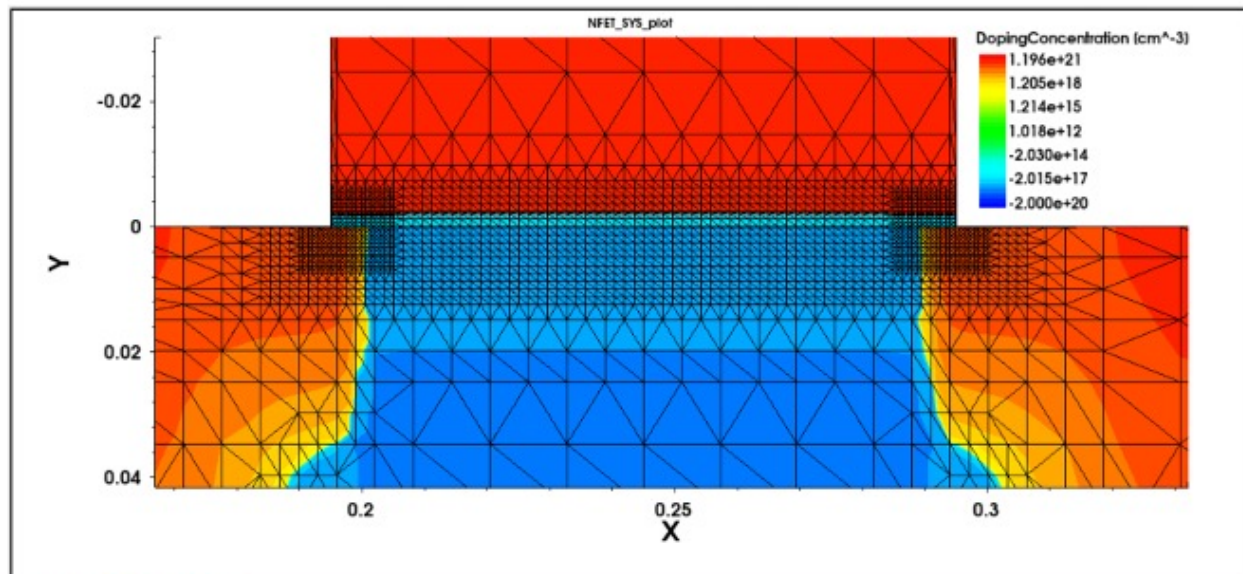
Courtesy John Barney

| [barneyjo@iu.edu](mailto:barneyjo@iu.edu)

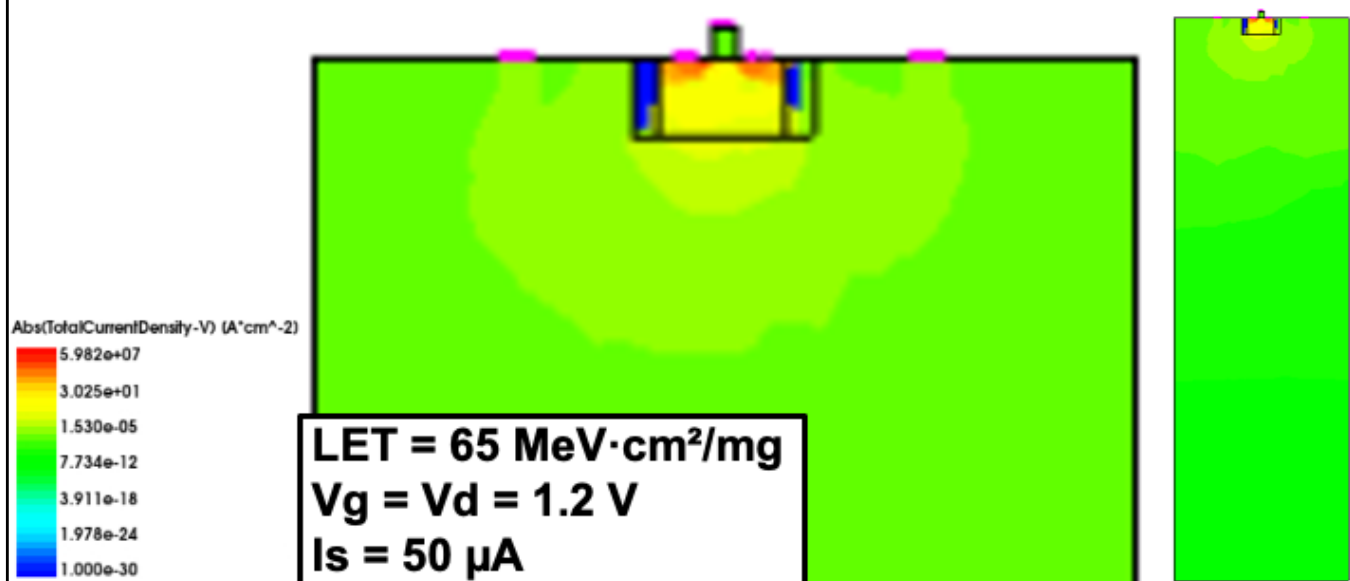
## Layout (left) & TCAD Model (right)



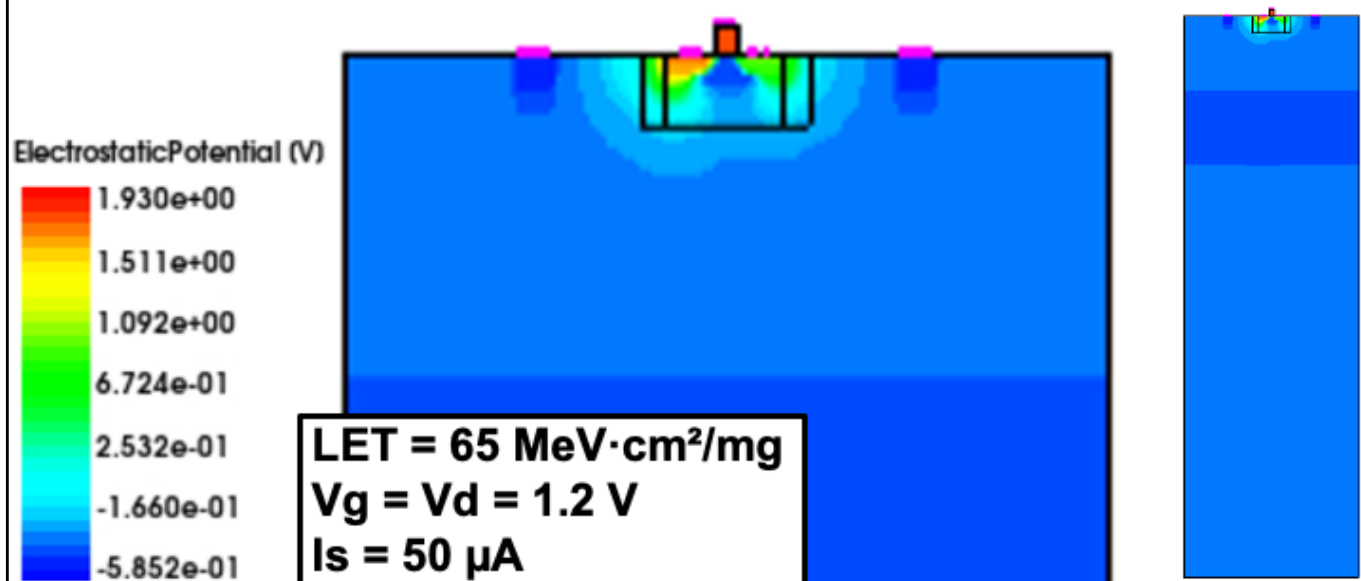
# Channel Region Meshing for Simulation



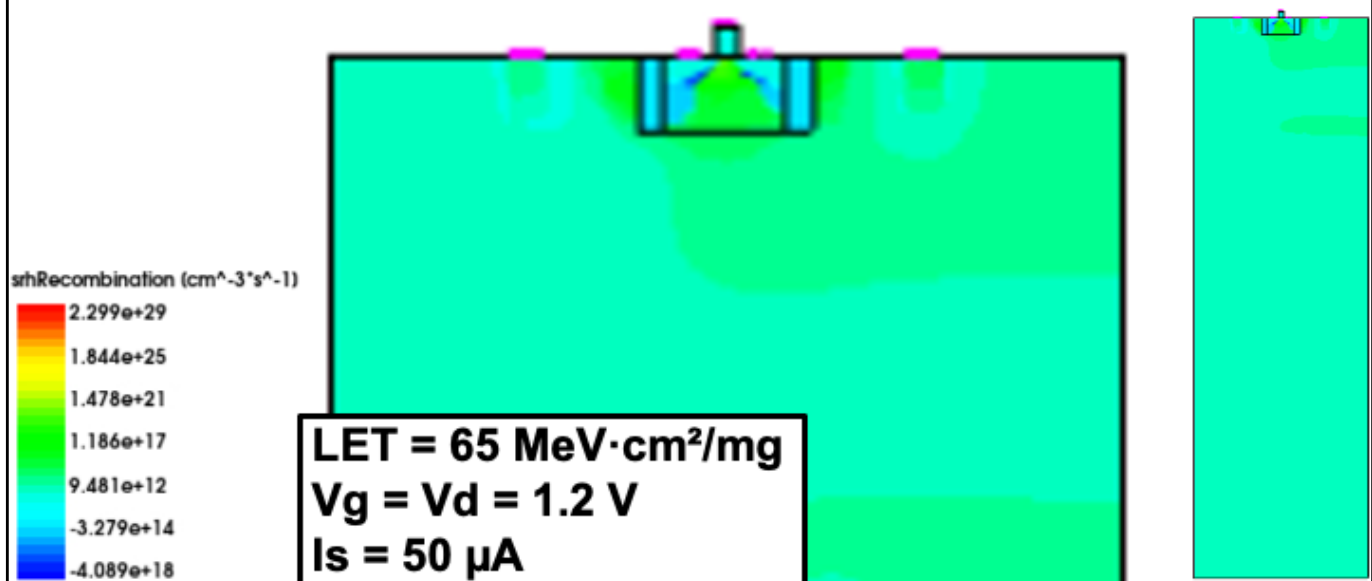
## NFET: HI Strike - TotalCurrentDensity



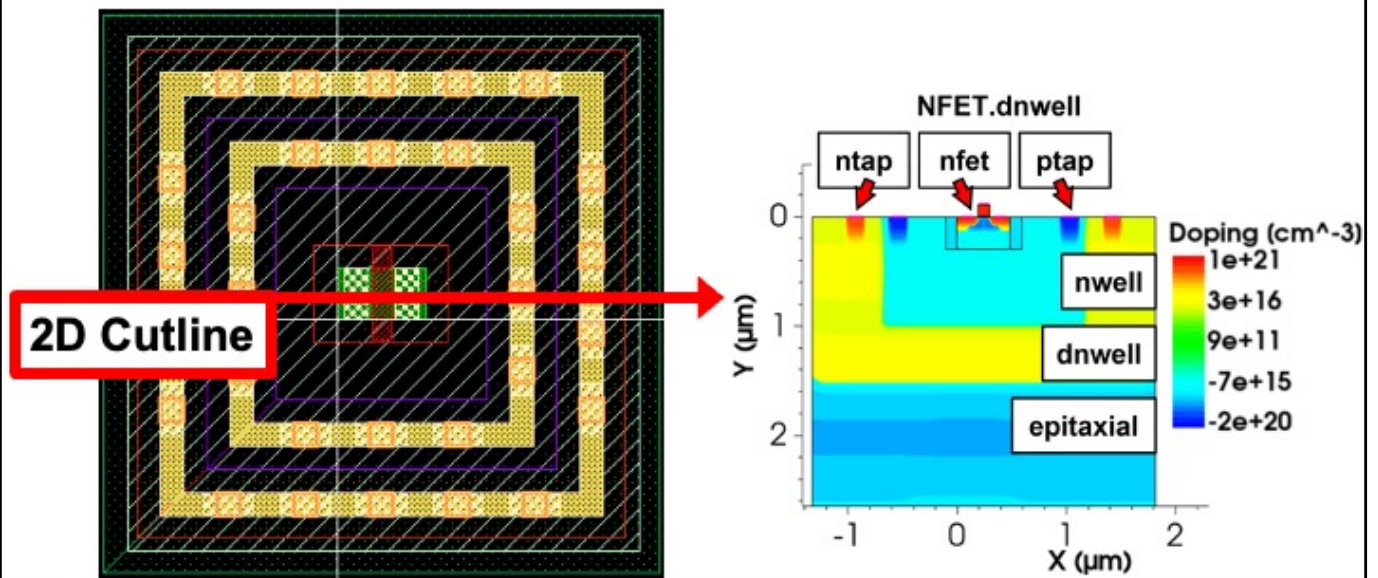
## NFET: HI Strike - Electrostatic Potential



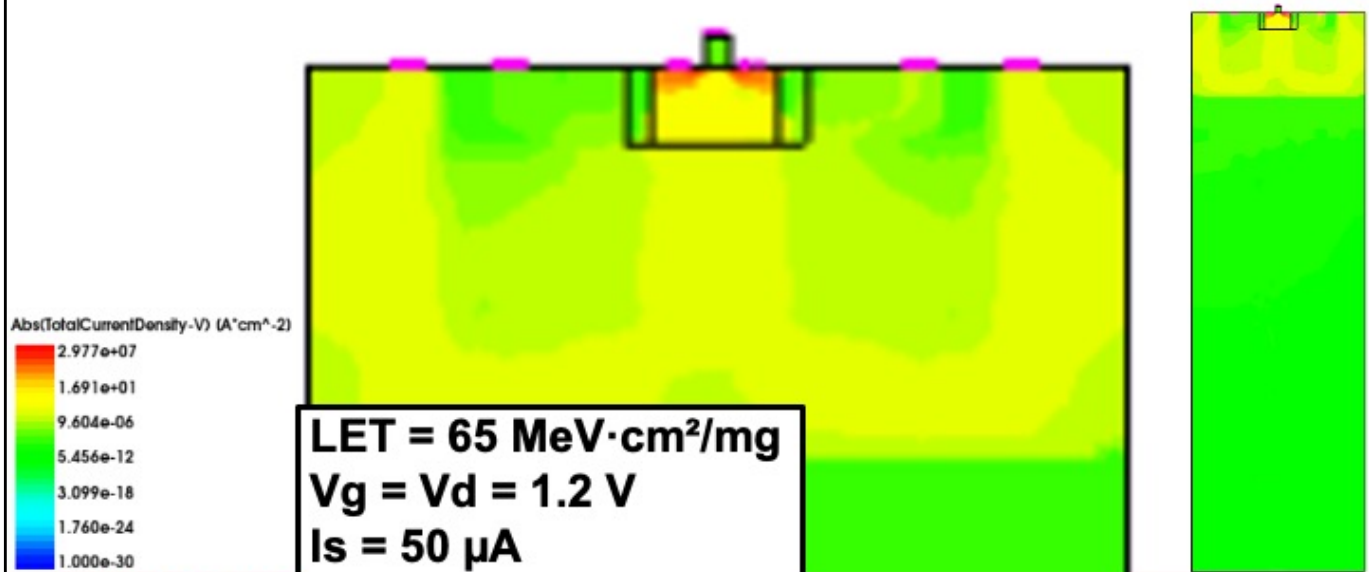
## NFET: HI Strike - srhRecombination



## Layout (left) & TCAD Model (right)

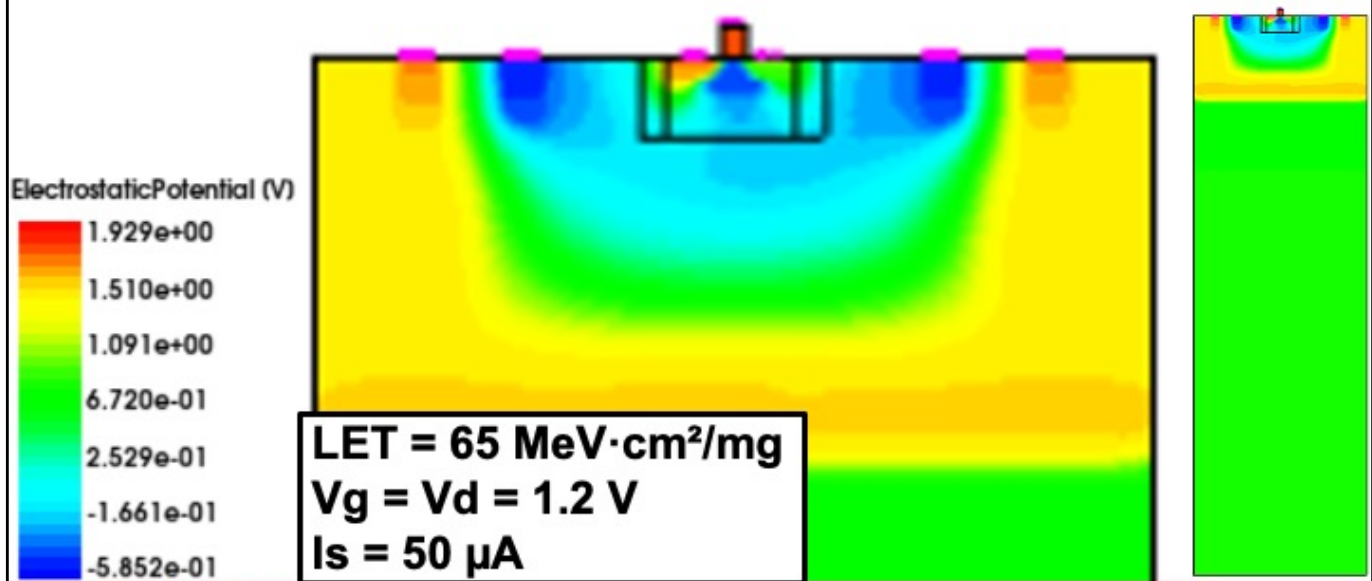


## NFET.dnwell: HI Strike - TotalCurrentDensity





## NFET.dnwell: HI Strike - ElectrostaticPotential



## NFET.dnwell: HI Strike - srhRecombination

