A Placement-Oriented Mitigation Technique for Single Event Effect in Monolithic 3D IC

Michael Blacconiere & Micah Robertson

Author Information

- Sarah Azimi
  - Assistant Professor – Polytechnic University of Turin (Politecnico di Torino)
    - Part of the Electronic CAD and Reliability Research group
  - 51 listed publications on IEEE (37 since 2020)
  - 766 total citations
- Corrado De Sio
  - Currently pursuing Ph.D. - Polytechnic University of Turin
  - 35 listed publications on IEEE (29 since 2020)
  - 546 total citations
- Luca Sterpone
  - Professor with Department of Control and Computer Engineering - Polytechnic University of Turin
    - Head of Department of Control and Computer Engineering
  - 190 listed publications on IEEE (46 since 2020)
  - 5521 total citations (2068 since 2020)

Lab/Group Information

- DAUIN at Polytechnic of Turin (Italy)
  - Department of Automation and Informatics
  - CAD Group
    - Electronic CAD & Reliability
  - 34 Person Lab
  - 1st and 3rd author are still in the lab
- Publishing on Single Event Upsets since at least 2008
- Focus a lot on FPGAs (Field Programmable Gate Arrays)
- Currently looking at SoC devices (Hardware Software Codesign) for space applications
- Publish Lots of papers – 70+ a year for the last 4 years
- Link to site

International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD)

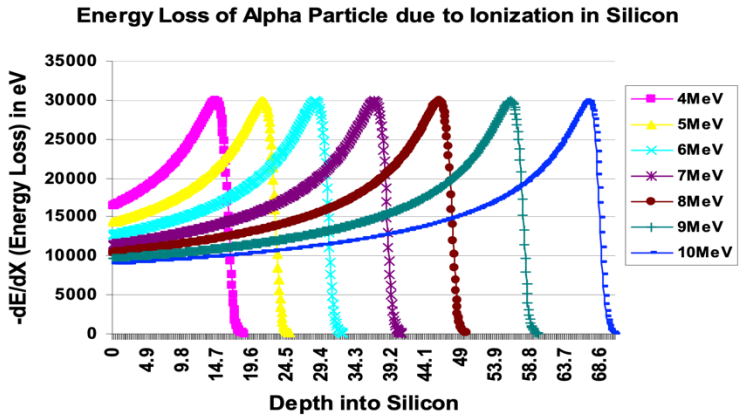
- From 1991 – 2006 (Biannual)
  - International Workshop on Symbolic Methods and Applications to Circuit Design (SMACD)
- From 2008-2010 (Biannual)
  - International Workshop on Symbolic and Numerical Methods, Modeling and Applications to Circuit Design (SMACD)
- 2012
  - Went back to original name
- 2015-2025 (Annual)
  - Modern Form

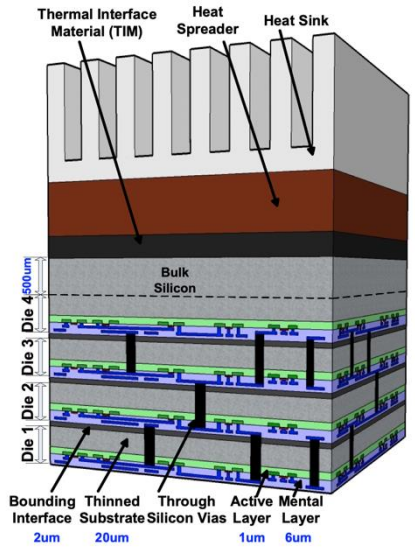
- 4 Page Limit Submission (Full Limit)
- Categories
  - Synthesis, Sizing and Optimization
  - Modeling
  - Simulation Verification and Test
  - CAD for emerging technologies
  - ML for CAD/EDA
  - Hardware security

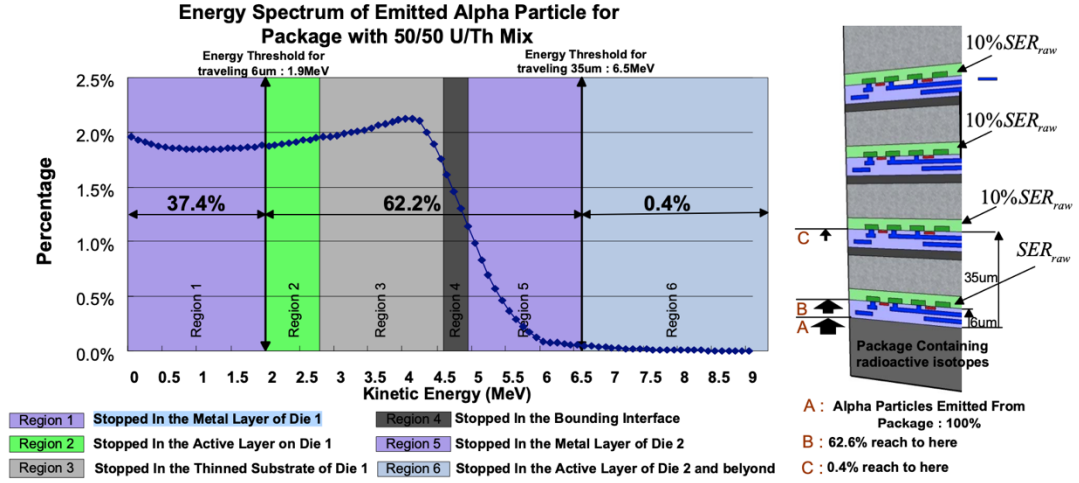
Background

- 3D ICs consists of stacked silicon layers utilizing connections between the layers to improve transistor density and performance
- The results are simulated since the manufacture and assembly of these chips are costly
  - Uses Monte Carlo Simulations[2]
- Allows for heterogenous technology types

- This paper builds on the findings out of “Microarchitecture Soft Error Vulnerability Characterization and Mitigation under 3D Integration Technology” by Wangyuan Zhang and Tao Li [3] (Important Figures Below)

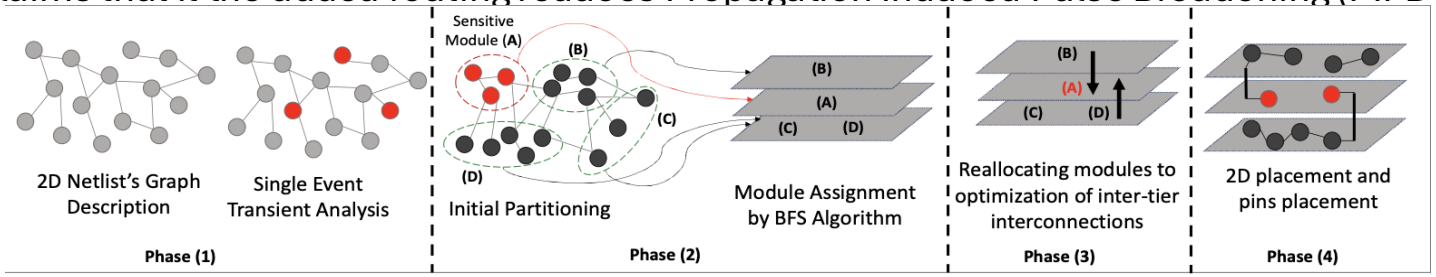






Summary

- Identifies sensitive sequential components
  - Analysis performed on 2D circuit layout, using physical design description graph
  - SET pulses are injected into circuit, and the propagation effects on each pulse are calculated
  - Examines which sequential nodes receive pulse and determines which are most sensitive
- Uses intrinsic attributes of the 3D Monolithic process to protect identified sensitive components from SEUs
  - 3D monolithic integrated circuits consist of multiple layers or tiers of 2D Integrated circuits
  - Allocates the susceptible sequential components to the inner tear to limit the probability of an SET resulting in an SEU
    - Outer tiers shield inner tiers
    - Added routing provides an RC filter
- Applies the methodology to a collection of three circuits
  - Claims the added 3D radiation protects against large SETs
  - Claims that it the added routing reduces Propagation Induced Pulse Broadening (PIPD



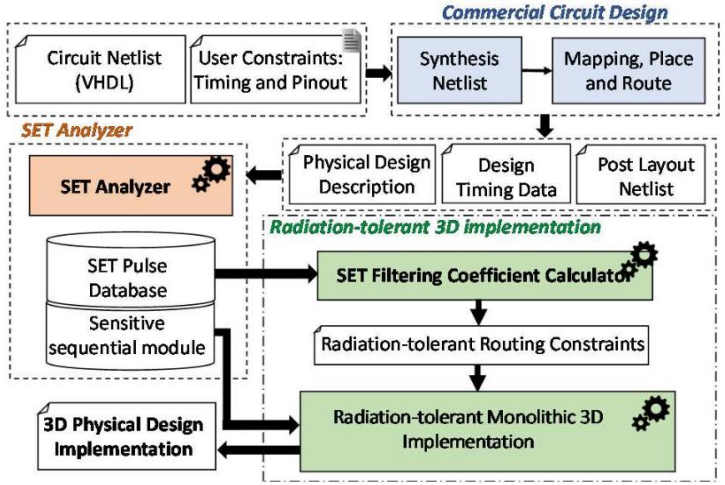
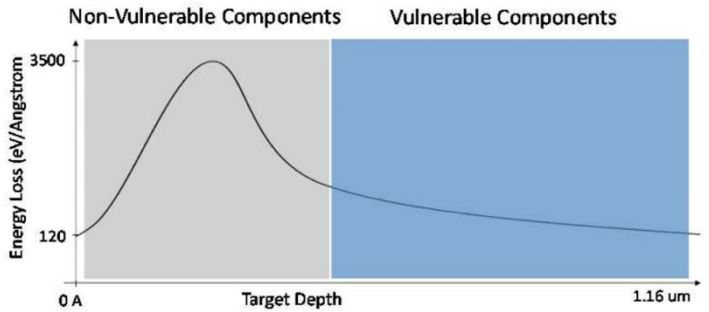


Fig. 1. The radiation-tolerant 3D implementation framework.

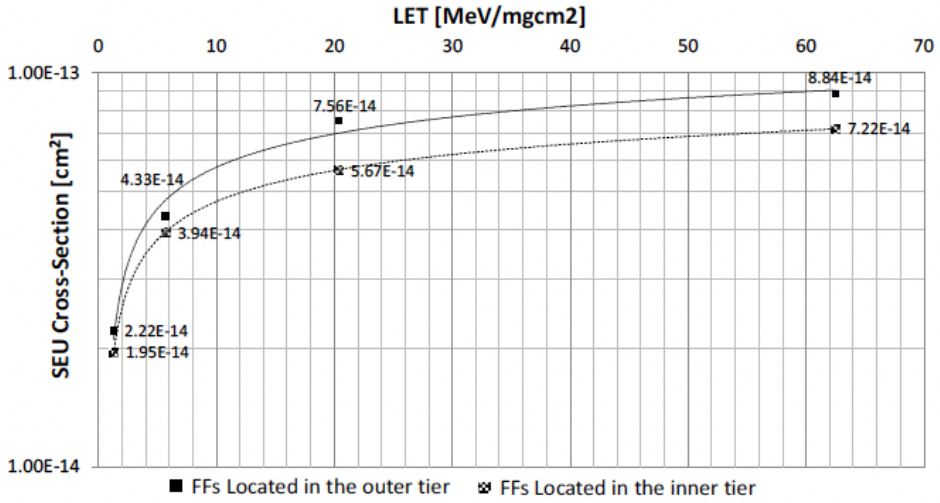


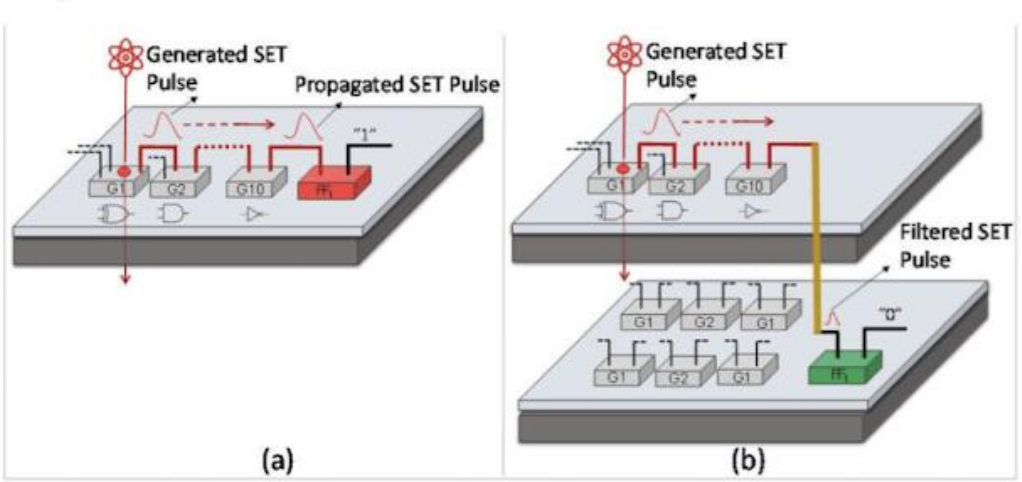
Sensitive Node Finding

- Circuit design is converted into Physical Design Description (PDD) graph
  - Intermediate nodes – Combinational Logic
  - Terminal nodes – I/O pins and sequential components
- SET Analyzer sends pulse through the input and output of each intermediate node
  - Duration and amplitude of each pulse modeled to match the expected radiation particle
  - Pulses propagate until they reach a terminal node
- Propagation Induced Pulse Broadening (PIPB) coefficient is calculated
  - Based on gate types and the routing interconnections of the circuit as described in the PDD
  - Effect on pulse duration reaching each terminal node is evaluated (identifies which pulses remain dangerous when they reach the terminal nodes)
- List of all sequential elements facing an SET pulse at the output is generated by the analyzer
  - Sensitive sequential modules are identified
  - Gives maximum duration/amplitude of the pulse that reaches each sequential node
- Analyzer on the 2D design is based only on logic of the circuit, not the layout or timing
  - Results are still valid in the 3D case, as only the physical layout changes, not the logic

Monolithic 3D Intrinsic Protection

- Inner layers are “shielded” by the outer layers from radiation events
  - Claims that for low-energy ions, the bulk of the energy is deposited into the outer layer
- Adding routing between layers creates an RC filter that removes or reduces SET pulses
  - Can be done in 2D but has less space overhead in 3D





Paper Conclusions

- Placement based SEE mitigation techniques are viable
  - Reduction of Propagation Induced Pulse Broadening (PIPB) coefficient
  - Lower duration of SET pulses

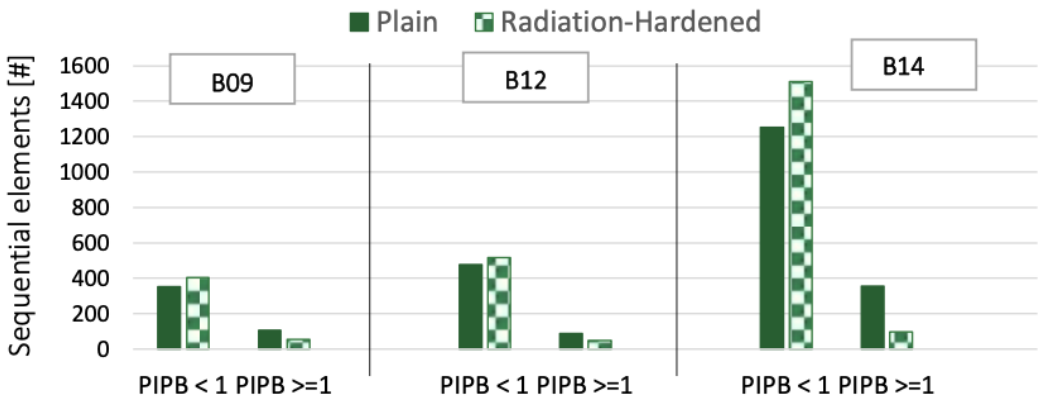


Fig. 7. PIPB distribution on Plain 2D and Radiation-hardened 3D implementation.

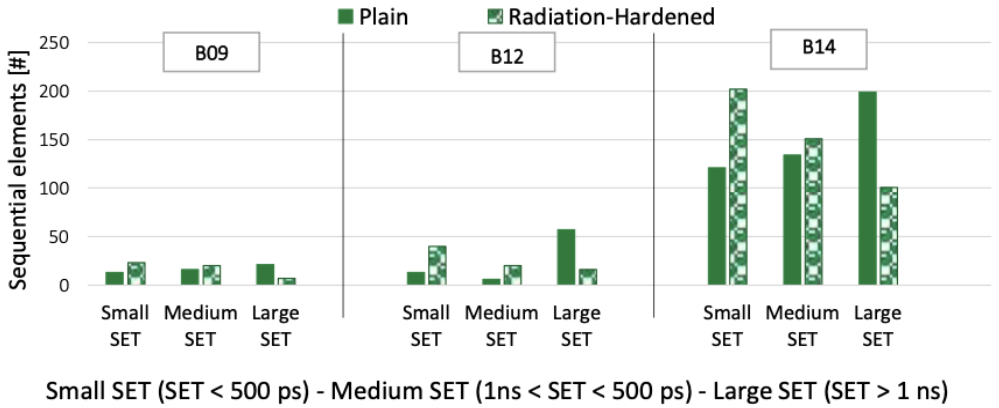


Fig. 6. SET distribution on Plain 2D and Radiation-hardened 3D implementation.

Discussion Questions

- Was the paper successful in presenting its goals and the methods used?
  - Did the authors clearly separate logical, SET-induced vulnerability from SEU-induced errors, or were the distinctions overly blurred?
- Were the justifications/results provided sufficient in supporting the conclusion?
- What do we think of the claim that inner layers are more protected from radiation than outer layers?
- How does the logic-level analysis used in this paper compare to device-level SEU modeling for identifying sensitive components?
  - Do we think the algorithm will find all sensitive node or are there ones in may miss?
  - What are the performance trade-offs from using this algorithm to separate out sensitive nodes?
- Is the placement based approach truly new, or is it mainly a recombination of known shielding and routing techniques applied to 3D ICs?
- What are the technical strengths of the methods used, and what parts of the analysis or modeling could be better?
- How well do the authors' benchmark circuit choices represent real-world digital systems?
  - Are simulation results alone enough to support their claims?
  - The results presented in this paper are simulation based, what other factors would need to be considered when testing this device in beam?
- Overall, is this a worthy paper to keep in your inventory?

References

- [1] S. Azimi, C. De Sio and L. Sterpone, "A Placement-Oriented Mitigation Technique for Single Event Effect in Monolithic 3D IC," 2022 18th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD), Villasimius, Italy, 2022, pp. 1-4, doi: 10.1109/SMACD55068.2022.9816235. keywords: {Analytical models;Solid modeling;Three-dimensional displays;Sensitivity;Single event upsets;Reliability engineering;Circuit synthesis;3D ICs;Reliability;Single Event Effects}
- [2] L. Sterpone, F. Luoni, S. Azimi and B. Du, "A 3-D Simulation-Based Approach to Analyze Heavy Ions-Induced SET on Digital Circuits," in IEEE Transactions on Nuclear Science, vol. 67, no. 9, pp. 2034-2041, Sept. 2020, doi: 10.1109/TNS.2020.3006997.keywords: {Mathematical model;Computational modeling;Public transportation;Urban areas;Batteries;Vehicles;Numerical models;3-D;heavy ions;layout;radiation effects;simulation;single-event transient (SET)}
- [3] Wangyuan Zhang and Tao Li, "Microarchitecture soft error vulnerability characterization and mitigation under 3D integration technology," 2008 41st IEEE/ACM International Symposium on Microarchitecture, Como, Italy, 2008, pp. 435-446, doi: 10.1109/MICRO.2008.4771811. keywords: {Microarchitecture;Integrated circuit reliability;CMOS technology;Silicon on insulator technology;Circuit faults;Microprocessors;Stacking;Semiconductor device reliability;CMOS process;Wire}