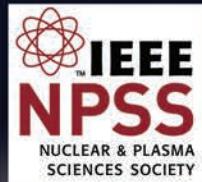


2021 Short Course Notebook

NSREC 2021 Virtual
July 16-19, 2021



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Short Course 2021

Introduction

This volume consists of notes to accompany the four lectures forming the Short Course, “Challenges and Opportunities for Radiation Hardening in Advanced Technologies,” presented at the 2021 IEEE Nuclear and Space Radiation Effects Conference.

The Short Course addressed the challenge of choosing suitable techniques to harden electronics against radiation. Finding the proper trade-off between protection and area/performance penalty is a crucial aspect for the design of space or safety-critical systems. Radiation hardening solutions for different types of electronic devices/circuits and different applications will be explored. The four lectures were given by subject matter experts who prepared these notes.

The lectures were:

Hardening Techniques for Digital Circuits, Dr. Balaji Narasimham, Broadcom

Hardening Techniques for Analog and Mixed-Signal Circuits, Dr. Daniel Loveless, University of Tennessee at Chattanooga

Hardening Techniques for Image Sensors, Dr. Vincent Goiffon, ISAE-SUPAERO, University of Toulouse

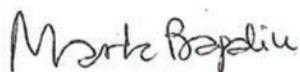
System-Level Hardening - What Could Go Wrong, and How to Make It Right, Kay Chesnut, Raytheon Technologies

This volume should be of value in studying these topics and for future reference.

It was my honor to serve as Chair for the 2021 IEEE Nuclear and Space Radiation Effects Short Course and I am indebted to the four individuals above for their patience and diligence in the preparation of this excellent set of notes.

I would also like to thank the RESG and NSREC conference committees for their invaluable support.

Short bio-sketches for the lecturers follow.



Marta Bagatin
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Dr. Balaji Narasimham, Broadcom



Balaji Narasimham received his Ph.D. in electrical engineering from Vanderbilt University, Nashville, TN, in 2008. He joined Broadcom, Irvine, CA in 2008 where he is currently a Master R&D Engineer and leads the reliability team. Dr. Narasimham's work focusses on CMOS circuit design, radiation effects, and reliability of semiconductor devices and circuits. He architects design reliability and soft error guidelines for Broadcom's diverse products. He has been instrumental in developing techniques to characterize and mitigate radiation effects in memory and logic circuits from planar to FinFET technologies enabling Broadcom products to achieve reliability targets at low performance overhead and has guided product designs in new satellite markets. He has authored or co-authored over 75 peer-reviewed papers related to his research, has authored a book chapter on single-event transients and has three US patents on efficient soft error mitigation. He was the recipient of the IEEE NSREC Outstanding Paper Award in 2013 and 2015 and the IEEE RADECS Conference Best Paper Award in 2007. He received the Broadcom President's Award for Excellence in 2013. He has served in the technical program committees and chaired sessions at both the IEEE NSREC and IEEE IRPS. He also serves as a reviewer for various IEEE journals. He is a Senior Member of the IEEE.

Dr. Daniel Loveless, University of Tennessee at Chattanooga



T. Daniel Loveless is a UC Foundation Associate Professor of Electrical Engineering at the University of Tennessee at Chattanooga (UTC). He received the B.S. degree in electrical engineering from the Georgia Institute of Technology in 2004 and the M.S. and Ph.D. degrees in electrical engineering from Vanderbilt University in 2007 and 2009, respectively. Prior to joining UTC, he was a Senior Engineer and Research Assistant Professor at the Vanderbilt University Institute for Space and Defense Electronics from 2009 to 2014, where he was involved in radiation effects research related to high-speed analog and mixed-signal circuits, and the modeling and design of integrated circuits for the evaluation of radiation effects in advanced CMOS technologies.

Dr. Loveless joined UTC in 2014 and established a microelectronics research program focused on radiation effects and reliability in electronic and photonic integrated circuits. Additionally, he founded the UTChattSat program focused on undergraduate and graduate research and education in small-satellites, space systems engineering, and radiation effects. Dr. Loveless has authored approximately 100 journal articles and conference papers. He is a Senior Member of the IEEE and serves as an Associate Editor of the IEEE Transactions on Nuclear Science. He has received five best conference paper awards, the 2019 Radiation Effects Early Achievement Award, and the IEEE Nuclear and Plasma Sciences Society (NPSS) Graduate Scholarship Award for his contributions to the fields of nuclear and plasma sciences.

Dr. Vincent Goiffon, ISAE-SUPAERO, University of Toulouse



Vincent Goiffon received his Ph.D. in EE from the University of Toulouse in 2008. The same year he joined the ISAE-SUPAERO Image Sensor Research group as Associate Professor and he has been a Full Professor of Electronics at the Institute since 2018. He has contributed to advance the understanding of radiation effects on solid-state image sensors, notably by identifying original degradation mechanisms in pinned photodiode pixels and by clarifying the role of interface and bulk defects in the mysterious dark current random telegraph signal phenomenon.

Besides his contributions to various space R&D projects, Vincent has been leading the development of radiation hardened CMOS image sensors (CIS) and cameras for nuclear fusion experiments (e.g. ITER and CEA Laser MegaJoule) and nuclear power plant safety.

Vincent Goiffon is the author of one book chapter and more than 90 publications, including more than 10 conference awards at NSREC, RADECS and IISW. He has been an associate editor of the IEEE Transactions on Nuclear Science since 2017 and has served the community as reviewer and session chair.

Kay Chesnut, Raytheon Technologies



Kay Chesnut, Engineering Fellow, Radiation Effects Engineering, Raytheon Intelligence & Space at Raytheon Technologies has worked on space systems and communication satellite hardware for over 40 years. She developed and delivered over 20 new systems over her career using new technologies that had to operate in harsh radiation environments including both nuclear and natural environments. Kay started extensively working with the radiation community in 1993, where collaboration on the then new technology insertion of a 500MHz digital GaAs direct digital synthesizer, formed a solid foundation for the proper mitigation approaches.

Kay has served as the Financial Chair for the IEEE's 2003 NSREC, Local Arrangements Chair for the 2005 NSREC, 2009 NSREC Short Course Instructor (with Dr. Kirk Kohnen), Conference Chair of the 2011 NSREC, 2008 Radiation Effects Steering Group Secretary, and the 2012-2015 Radiation Effects representative on the IEEE Nuclear Plasma Sciences Society AdCom.

Hardening Techniques for Digital Circuits

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1. Introduction

Innovations in semiconductor integrated circuits (IC) manufacturing has enabled technology scaling to nanometer dimensions. Device dimensions and operating voltages of ICs are constantly shrunk to satisfy an ever-increasing demand for reduced power and increased operating speeds of circuits. Scaling to feature sizes beyond sub-100-nanometer was made possible through innovations such as strained-Si technology, high-K metal gate, and transition from planar to tri-gate or FinFET device structures as well as extreme ultraviolet (EUV) lithography [Tsmc], [Le05], [Mi07], [Wi01], and [Ku12]. This has kept alive Moore's predictions of doubling transistor counts per IC every two years [Mo65]. Fig. 1 shows a chart of technology scaling as a function of year of first availability [Tsmc].

With decreasing feature sizes, reduced supply voltages, and increasing packing densities, digital circuits are ever more vulnerable to radiation induced upsets [Ba05], [Bu01], and [Do03]. Deep sub-micron devices show increased susceptibility to Single-Event Effects (SEEs), which constitute a particular category of radiation effects [Do03]. A Single-Event (SE) occurs when an energetic particle, such as a heavy ion or neutron, incident on a semiconductor region creates electron-hole pairs and causes a change in the device's normal operation. SEEs are not just a concern for space applications, but a threat to many terrestrial applications.

This short course will provide a brief overview of SEE and highlight effects in digital circuits. Hardening-by-design approaches used for overcoming SE in memories, latches and logic circuits will be reviewed. Error correction techniques for memories along with spatial- and time-redundancy based approaches for latches and logic circuits will be presented. Recent advancement in the radiation-tolerant design approaches that tradeoff performance with the extent of radiation tolerance to suit different applications will be discussed along with the performance penalty vs. radiation tolerance comparisons. Finally, the course will review scaling trends and bias dependence of single-event upset (SEU) rates from planar to FinFET processes with an emphasis on the opportunities and challenges for radiation hardening in highly scaled technologies. The focus of the course will primarily be based on advanced bulk-planar and bulk-FinFET circuits,

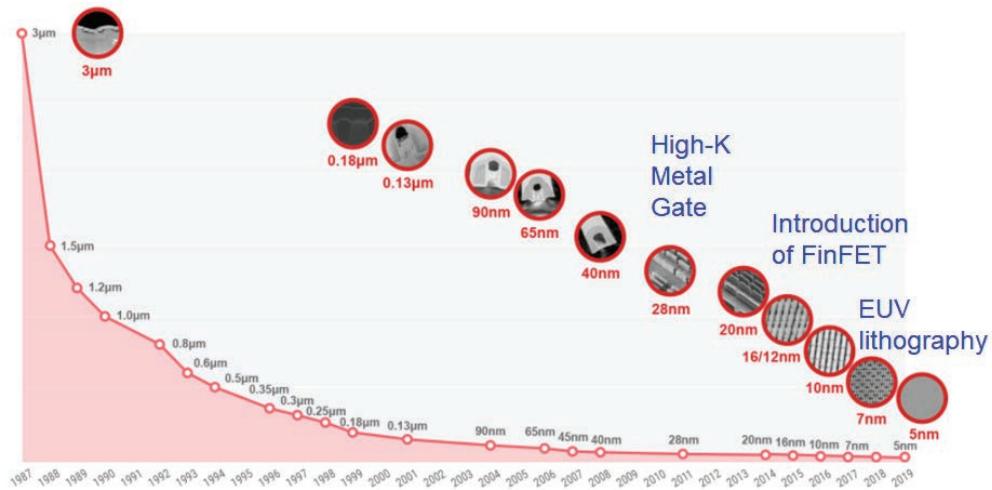


Fig. 1. Technology scaling as a function of year of first availability, after [Tsmc]

though most of the hardening-by-design concepts are also applicable to silicon-on-insulator (SOI) ICs.

2. Background on SEE

The category of SEEs encompasses a multitude of phenomena that have, as a common cause, the passage of an energetic particle through the semiconducting or insulating materials used in the manufacture of ICs. The common sources of SEEs are cosmic rays and heavy-ions for space applications, and neutrons (which produce SEEs indirectly through secondary particles emitted as a result of nuclear interactions) and alpha particles for terrestrial applications. As an energetic particle passes through the IC, it excites electrons from the valence band and leaves behind a track of electrons and holes. If the track passes through or near a reverse-biased semiconductor p-n junction, the high electric field present in the region can efficiently separate the particle-induced electrons and holes (Fig. 2).

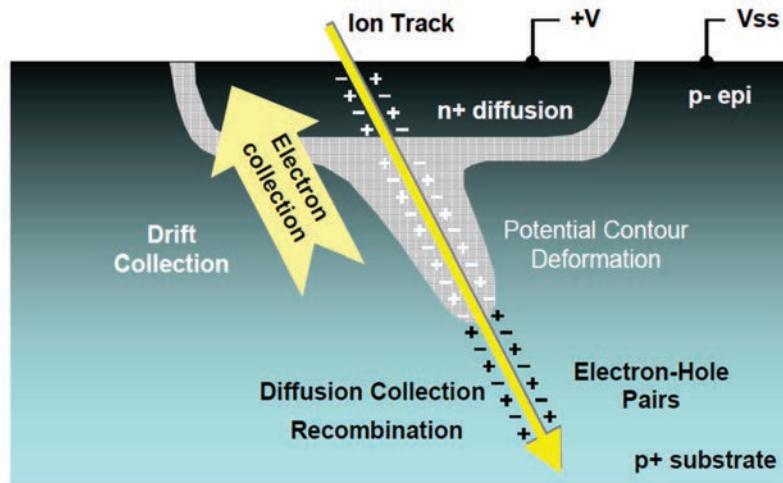


Fig. 2. Schematic of a reverse-biased n+/p junction struck by an ion indicating the deformation of the potential leading to the funnel. Electric field at the junction leads to initial rapid charge collection by drift followed by diffusion collection of charges, after [Ba05].

Carriers thus separated may be collected by a circuit node due to the nodal voltages present in the circuit, generating a current at the terminals of the semiconductor device. This drift charge collection is completed within tens of picoseconds in advanced processes. Deposited carriers can also diffuse from the bulk or substrate of the semiconductor into the vicinity of the depletion-region field where they may be collected by the circuit node, adding to the total charge collected. The diffusion charge collection happens over nanosecond timescales. Charge generated along the particle track can locally extend the junction electric field due to the highly conductive nature of the charge track, leading to a field funnel region [Hs81]. This funneling effect can increase charge collection at the struck node by extending the junction electric field further into the substrate, allowing charges deposited away from the junction to be collected efficiently through drift. In advanced complementary metal-oxide-semiconductor (CMOS) processes when electrons or holes released by a particle strike are confined within the well region in which a transistor exists, charge collection may be enhanced by a parasitic bipolar effect [Do03]. For example, for a p-type metal-

oxide-semiconductor field effect transistor (PMOSFET) in an n-well process, holes induced by the particle strike may be collected at the drain or substrate junctions. However, electrons left behind in the well region lower the well potential. This lowers the source-well potential barrier and may result in injection of holes into the well from the source, which can then be collected at the drain. This adds to the original particle-induced current and the effect is described as parasitic-bipolar charge collection. In sub-100 nanometer technologies the charge cloud from the ion strike can encompass multiple devices and well-contacts, and result in complex charge collection behavior across multiple devices [Da07].

2.1. Types of SEE

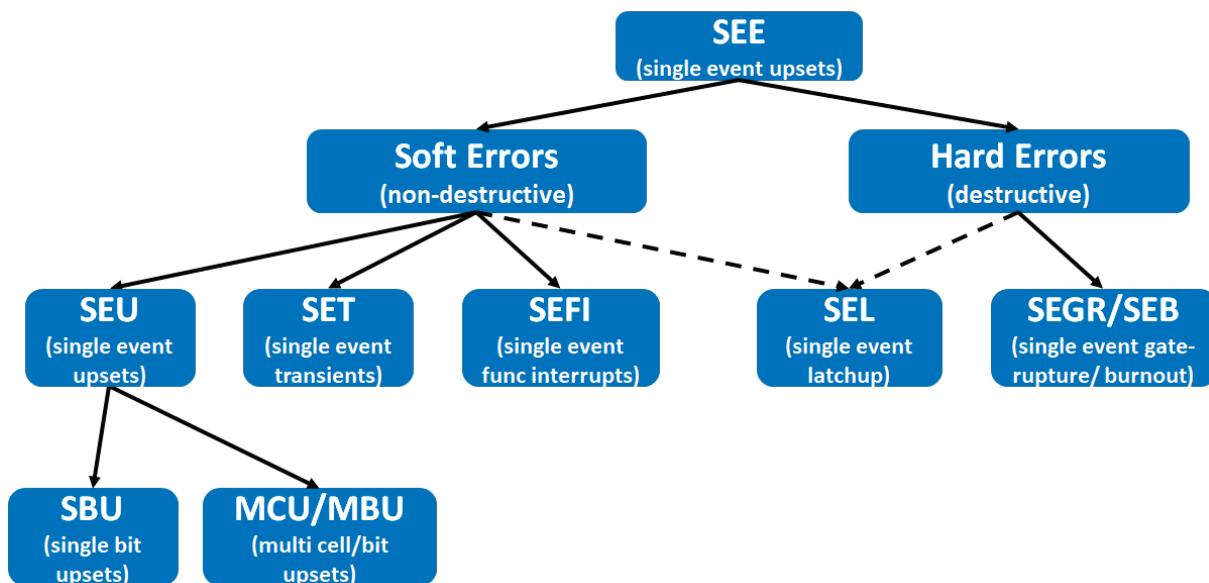


Fig. 3. Types of Single Event Effects

Single events can be broadly categorized as destructive and non-destructive SEEs depending on whether they result in a hard (or permanent) error vs. a soft error (no permanent damage). The major types of non-destructive SEE include Single-Event Upsets (SEU), Single-Event Transients (SET) and Single-Event Functional Interrupts (SEFI). An SEU is a static upset in storage cells such as Static Random Access Memory (SRAM) cells, latches and flip-flops. The upset rate due to such an event is largely independent of the clock frequency [Ba05]. Depending on the number of bits flipped due to a single particle strike event, SEUs can further be classified as Single-Bit Upsets (SBU) and Multi-Cell or Multi-Bit Upsets (MCU/MBU). MCUs typically refer to upsets along both bit-line and word-line directions in a memory array, while MBUs are used to refer to upsets strictly along the word-line direction (i.e. within the same word). While MCU/MBU are usually a small fraction of the overall SEUs, they may render error correction schemes less effective without appropriate memory interleaving to tackle such events. SEFI are SEUs that happen in a critical register and hence impact the device functionality. Such events typically require a reset or power cycling. For sequential CMOS ICs, an energetic particle strike may cause a transient voltage perturbation, called an SET, which propagates through the circuit and may

become stored as incorrect data, causing disruption of the circuit operation. An SET will result in an error if the SET pulse arrives at a storage node so as to get latched. For example, for a flip-flop, if an SET pulse arrives during the set-up-and-hold time of the primary latch, it will result in an error. Thus, upset rates due to SETs depend on the pulse width of the SET and the clock frequency [Bu01]. With increasing clock frequency, there are more latching clock edges to capture an SET [Bu01]. SETs in analog electronics are referred to as ASET while those in digital combinatorial logic are referred to as DSET.

Other types of SEE include Single-Event Latchup (SEL), Single-Event Burnout (SEB), and Single-Event Gate Rupture (SEGR), of which SEB and SEGR are typically destructive SEEs while SEL may or may not be destructive. Due to the proximity of semiconductor regions in CMOS transistors, they contain parasitic bipolar structures. An SEL happens when an ion strike triggers the parasitic PNPN structure present in CMOS devices creating a low resistance path between the power and ground [Br96]. A full chip power cycle is typically needed to recover from SEL. SEL is generally non-destructive with external resistances to limit the current. However, if enough current is drawn it can result in catastrophic damage to metallization and junctions leading to a hard error. SEB typically occurs in power devices where an ion strike could lead to destructive burnout due to high current conditions caused by junction breakdown and thermal runaway [Se03]. SEGR results in rupture of the gate dielectric due to high electric field created by an ion strike [Se03]. SEGR impacts power MOSFETs and non-volatile structures. Both SEB and SEGR are destructive events that lead to hard fails. Fig. 3 summarizes the different types of SEE.

This short course will focus on hardening techniques for non-destructive SEEs including SEUs (along with MCU/MBU), SETs, and SEL. In the next sections we will review these mechanisms in more detail along with hardening techniques to mitigate their impact.

2.2. Sources of SEEs

The natural space radiation environment consists of transient particles and particles trapped by planetary magnetospheres in “belts” [Ba03]. Transient radiation consists of galactic cosmic ray (GCR) particles and particles from solar events such as coronal mass ejections and flares and includes protons and heavy-ions of all elements of the periodic table (Fig. 4(a)). Trapped particles include protons, electrons, and heavier ions. For more details on the space radiation environment please refer to [Ba03].

Terrestrial radiation is created by cosmic rays and solar particles interacting with the Earth’s atmosphere which results in a “shower” of secondary particles such as protons, electrons, neutrons, heavy-ions, muons, and pions. Of these, neutrons are the most important product of the cosmic ray showers for terrestrial radiation effects [Ta95] (Fig. 4(b)). While high-energy neutrons (>1 MeV to several 100s of MeV) are not directly ionizing, they typically interact inelastically with nuclei of atoms present in an IC. During this interaction, the neutron is absorbed and is followed by ejection of nuclear fragments or spallation reaction products. The spallation reaction products deposit hundreds of femto-Coulombs (fC) of charge and cause SEE [Ba05]. Alpha particles emitted by trace uranium and thorium impurities in packaging materials (illustrated in Fig. 4(c)) are the next key source of radiation effects for terrestrial applications [Ma78]. The alpha particle is a doubly ionized helium atom emitted from nuclear decay of an unstable isotope such as ^{235}U and ^{232}Th . Most of the alpha particle emission is in the 4-6 MeV range. The third source of ionizing radiation for terrestrial applications are the low-energy or thermal neutrons ($\ll 1$ MeV). Boron-

10 has a high capture cross-section for thermal neutrons and it breaks into ionizing fragments (^7Li and alpha particle) shortly after absorbing the thermal neutron and these fragments are then capable of inducing soft errors. For further details on the sources of terrestrial radiation, please refer to [Ba05].

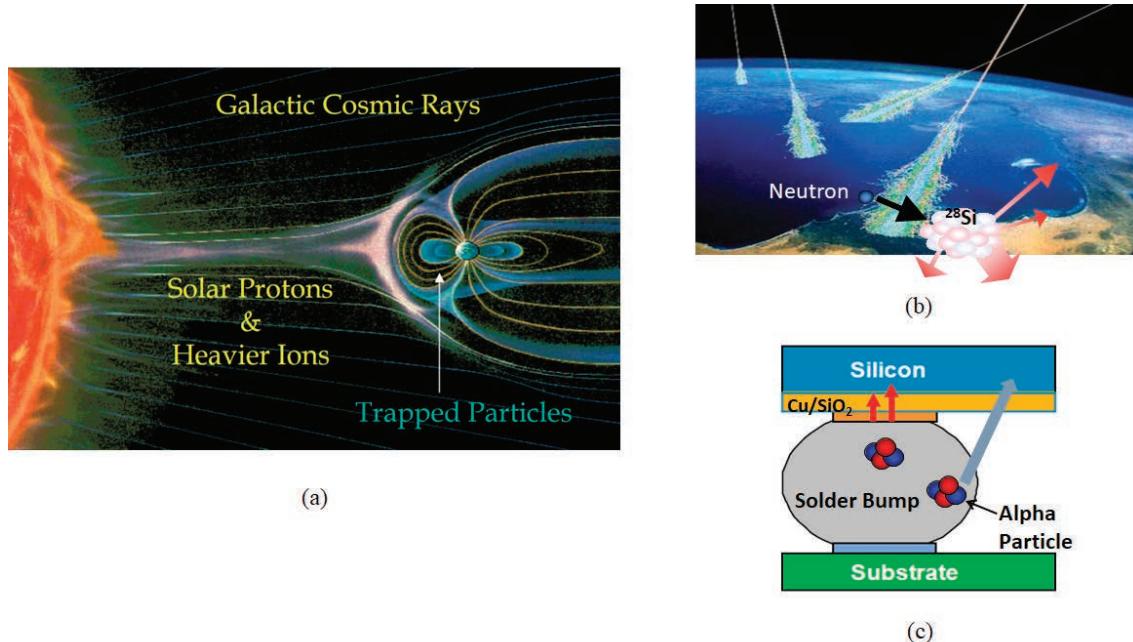


Fig. 4. (a) Illustration of the space radiation environment (image courtesy: Nikkei Science Inc and NASA), and illustration of the terrestrial radiation environment including (b) neutrons (produced by cosmic ray collisions with air molecules) and (c) alpha particles (emitted from impurities in the packaging material)

2.3. Definitions and Units

The amount of charge generated as an ionizing particle interacts with a material is determined by the energy loss per unit length and is known as the linear energy transfer (LET). This is typically given in units of MeV-cm²/mg.

Cross-section (σ) expresses the likelihood of an error due to an SEE and is determined by the ratio of the SE error count to the ion fluence (particles per unit area) that causes the errors. Cross-section has units of area. SE cross-section is typically charted as a function of LET and is used to estimate SE error rates. An example of heavy-ion SEU cross-section curve is shown in Fig. 5 [Ba05]. For proton and neutron testing, the x-axis of such a curve is plotted in terms of particle energy, since for a given particle energy a range of LETs are observed. These types of cross-section curves can be generated under accelerated test conditions. SE error rate can be calculated by integrating the device cross-section with the particle spectrum over the energies encountered in the actual environment. Threshold LET refers to the minimum LET at which the device begins to register SE errors and the threshold cross-section is the associated cross-section at threshold LET. The cross-section rises rapidly following threshold LET and eventually saturates at the limiting cross-section or only increases marginally with further increase in LET. The cross-section curve is usually fit to a cumulative Weibull form and serves as the input to SE error rate estimation routines.

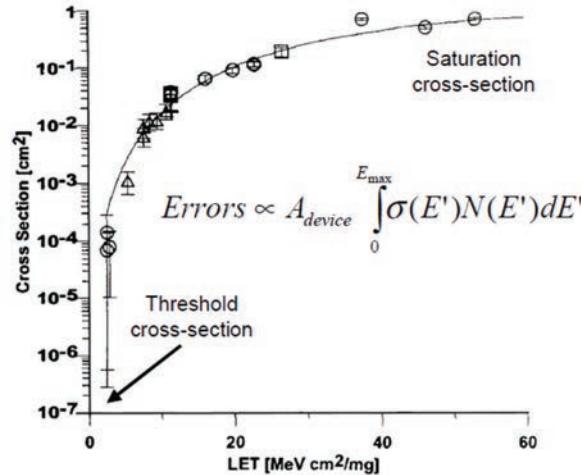
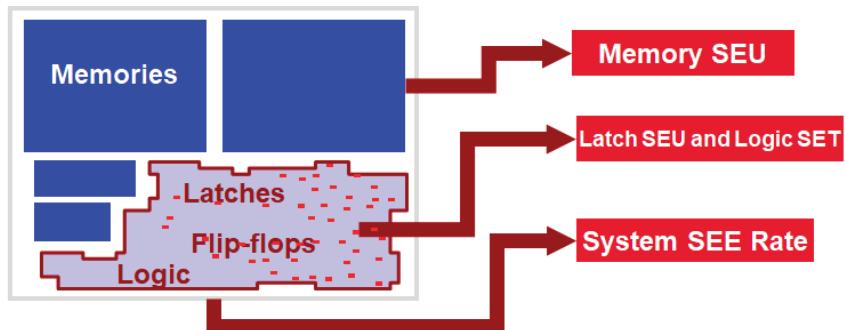


Fig. 5. An example heavy-ion cross-section curve for a device, after [Ba05]

SEUs are also referred to as soft errors in the commercial domain. The error is “soft” because the circuit/device itself is not permanently damaged by the radiation and the error can be corrected by writing new data. (In contrast, a “hard” error is manifested when the device is physically damaged and the operation loss is permanent.) Soft error rate (SER) is the rate at which a device encounters or is predicted to encounter soft errors. It is typically expressed as number of failures-in-time (FIT). One FIT equals one error per billion hours of device operation. In contrast to heavy-ion and mono-energetic sources, certain facilities offer “white” neutron spectra that closely mimic the terrestrial cosmic background spectrum, but with a much higher flux and allow accelerated experiments where the SER can be directly obtained once the difference in the beam flux and background neutron flux are accounted for [Ba05].

2.4. Digital Circuit Categories and Radiation Response



$$\text{SEE}_{\text{system}} = \delta_{\text{mem}} \text{SEU}_{\text{mem}} + \delta_{\text{Latch}} \text{SEU}_{\text{Latch}} + \delta_{\text{Logic}} \text{SET}_{\text{Logic}}$$

Fig. 6. Illustration of the overall SEE rate of digital circuits comprising of memory SEUs, latch (and flip-flop) SEUs and combinational logic SERs, after [Zh08]

Digital circuits include storage elements such as memory, latches and flip-flops as well as combinational logic gates. As discussed, particle strikes in memory lead to SBU and MCU/MBU. Latches and flip-flops are impacted by SEUs, while ion strikes in combinational logic gates result in SETs. The overall SE error rate of digital circuits is the sum of the upset rate of memories, latches and combinational logic gates, as shown in Fig. 6. In the following sections we will discuss radiation hardening approaches for each of these circuit categories in detail.

2.5. Importance of SE-Hardening

Before delving into the details of SE hardening techniques for digital circuits, let us briefly review the history of SE issues in space and terrestrial applications to further underscore the importance of SEE mitigation. SEUs have been the root cause of satellite failures to server failures. The first notable SEU happened back in 1975 when a Hughes satellite experienced communication loss attributed to cosmic ray upsets [Bi75]. Soon after in 1978, May and Woods published the first evidence of soft errors from alpha particles in packaging material which signified the possibility and threat of single events in terrestrial applications. Fast forward several years and soft errors were not just talked about in radiation effects community, but even in financial journals such as Forbes which published an article on cosmic-ray-induced soft errors in SRAMs causing server crashes [Forb]. In the following years, range of issues were getting attributed to soft errors – from network outage issues to anomalies in vote counting and malfunctioning of an airplane’s autopilot [Eti], [Inde]. These events undermine the credibility of the company manufacturing the product, result in loss of revenue and in some cases lead to loss of customers.

Advanced systems are built with hundreds if not thousands of ICs with each IC containing billions of transistors. Without appropriate SEE mitigation, the terrestrial SER of such a system could easily approach millions of FIT per system which translates to one SEE every few days. Such error rates may be unacceptable even for relatively less critical terrestrial applications such as mobile devices. ICs used in networking and server applications demand very stringent FIT requirements. Thus SEE mitigation is key to meet FIT requirements of many terrestrial applications. Due to the harsher particle environment, space applications typically require higher levels of SEE mitigation to meet SEU rates requirements. Thus, it is imperative to have robust hardening solutions to mitigate SEEs in ICs and is key to enabling critical space and terrestrial products.

3. Memory Hardening Techniques

Random access memory (RAM) is one of the most common type of memory used in IC designs. Static-RAM (SRAM) is a type of RAM that uses a latching circuit to store data, typically using back-to-back connected inverters. Dynamic RAM (DRAM) on the other hand stores each bit of data on a cell designed with a tiny capacitor and a transistor. The state of the capacitor, being either charged or discharged, represents the value of the bit stored, either 1 or 0. Since the charge on the capacitor leaks off, DRAMs require periodic refreshing of the data. Both these types of memory are volatile memories (i.e. requires power to maintain data storage). Other volatile memories include register files and content addressable memories (CAM). The core storage element of these designs are similar to the SRAM cell with additional circuitry. In this short course, we will focus on the design hardening and error correction schemes for SRAMs. The error correction techniques are mostly applicable to other memory types as well.

3.1. Design Hardening

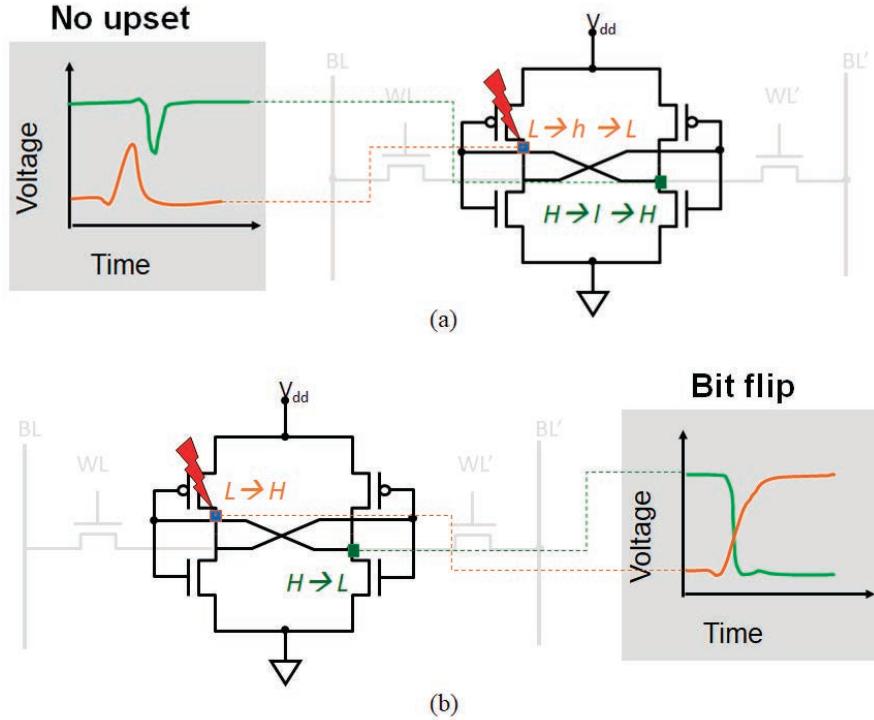


Fig. 7. Illustration of single-event strike in an SRAM bit-cell. In (a), the transient voltage pulse-width is shorter than the delay between the two inverters in the SRAM cell and hence the bit does not flip. In (b), the transient pulse-width is longer than the loop delay and hence results in the bit being flipped.

Fig. 7 shows the standard 6-transistor SRAM bit-cell and illustrates a radiation event on one of its transistors. The core storage element of this bit-cell is formed by two back-to-back connected inverters. When a memory cell holds a value, it has two transistors in “on” state and two transistors in “off” state. When the cell is holding a particular state, a radiation event on one of the off-state transistors within the storage element will cause a transient or glitch at that node. To a first degree, if the duration of this transient is shorter than the feedback loop delay of the cell, then the state of the SRAM will remain unchanged (no upset) as illustrated in Fig. 7(a). On the other hand, if the duration of this transient is longer than the feedback delay of the cell, then the state of the SRAM will flip as illustrated in Fig. 7(b). The minimum charge needed to flip the SRAM bit-cell is called the critical charge or Q_{crit} which is proportional to the product of the node capacitance and node voltage plus the restoring charge provided by the initially on-state device (which is proportional to the product of the restoring drive current from that device and the duration of the event or time to flip the cell) as given by equation 1. The SEU rate is proportional to the sensitive area of the bit-cell (drain-body junction area of off-state devices in the bit-cell) and is exponentially dependent on the ratio of the Q_{crit} and the collected charge due to a particle strike (Q_{coll}) as given by equation 2 [Ha00].

$$Q_{crit} = C_n \times V_{dd} + I_{restore} \times t_{flip} \dots \dots \dots (1)$$

$$SEU\ Rate \propto A_{sens} \times e^{-Q_{crit}/Q_{coll}} \dots \dots \dots (2)$$

Design techniques to harden the bit-cell involve increasing the storage capacitance of the node or using larger transistors to increase the drive strength. Fig. 8(a) shows an SRAM bit-cell hardened with additional capacitance [Sh08]. These techniques aim to increase the critical charge needed to flip the cell. The key drawback is that they make the cell slower and also increase the bit-cell size. Alternately, the feedback loop delay of the back-to-back connected inverters may be increased with additional resistors as shown in Fig. 8(b) [Ke88]. This aims to protect the cell by making the loop delay longer than the transient created at a node due to a radiation event, in which case the error will not be latched on and the cell will revert to its original state. The key drawback of this approach is that in addition to slowing the device and potentially increasing the bit-cell size, it also introduces a temperature sensitivity, as the value of the resistor varies with temperature [Ka07].

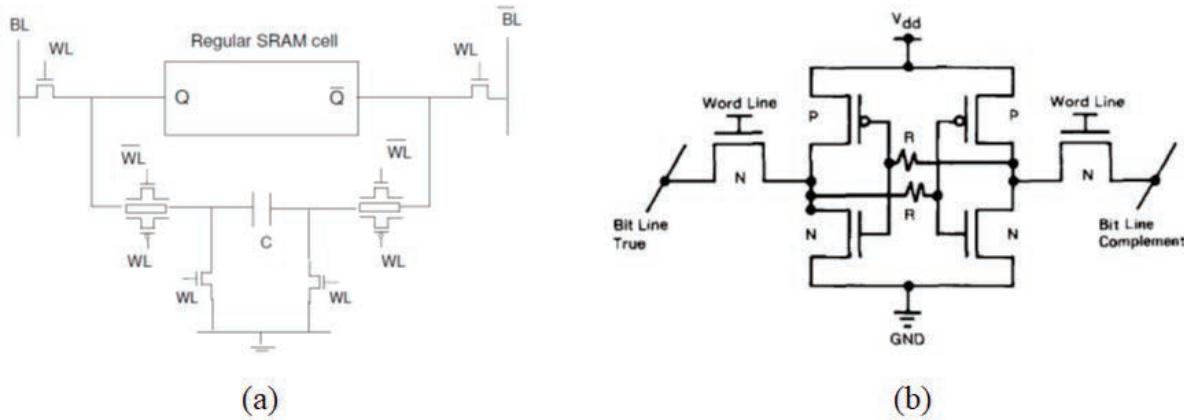


Fig. 8. (a) SRAM bit-cell hardened with additional capacitance, after [Sh08], and (b) SRAM bit-cell hardened with additional resistors, after [Ke88]

Other types of hardening the memory bit-cell involve adding additional transistors to increase the Q_{crit} or to provide redundant storage nodes. For example, the dual interlocked storage cell (DICE) based SRAM design uses four interconnected inverters to mitigate SEU as shown in Fig. 9(a) [Ca96]. The interlocked or interconnected nature of the design along with redundancy ensures that it is mostly immune to single node charge collection and requires radiation-induced charge to be collected by two nodes to cause a bit flip. [Ni08] proposes a hardened SRAM cell that uses blocking feedback transistors to mitigate SEUs as shown in Fig. 9(b). The advantage of DICE- and other redundancy-based designs are high SEU tolerance. However, such designs suffer from large area consumption and cell performance degradation. Moreover, in advanced process nodes with reduced feature sizes careful placement of the nodes and node separation will be required to mitigate multi-node charge collection and achieve high levels of immunity for most redundancy-based design approaches [Wa09].

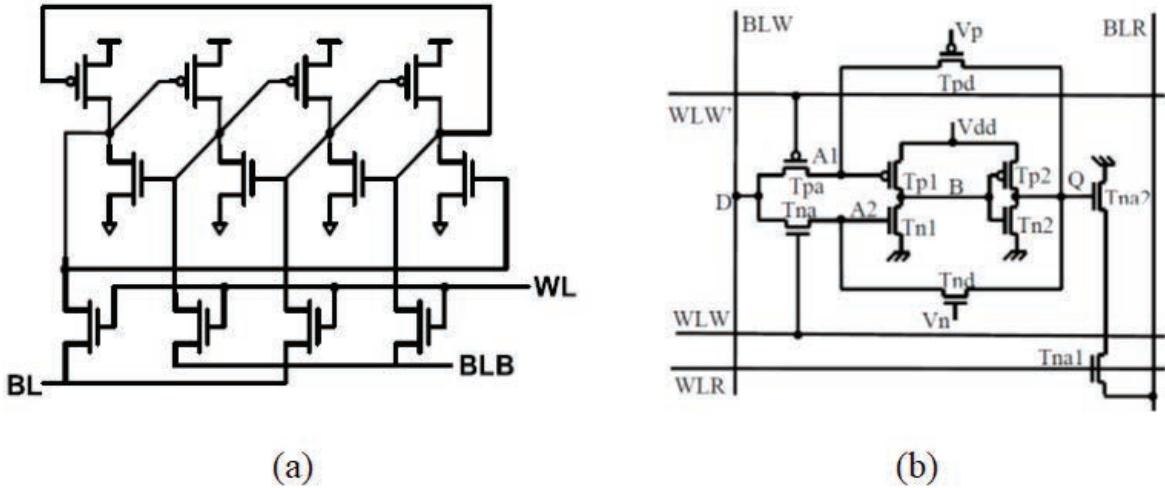


Fig. 9. (a) DICE-based SRAM bit-cell, after [Ca96], and (b) SRAM bit-cell hardened with blocking-feedback transistors, after [Ni08]

3.2. Error Correction Codes

Memory systems can be made fault tolerant with the use of error detection and correction codes which use information redundancy to detect and correct errors [Ch84]. In a system-based hardening approach, error correction code (ECC) is combined with periodic memory scrubbing (i.e., checking a memory for errors) to improve the effective bit-error-rate (BER) of the system. Bit interleaving is used to ensure physically adjacent bits map to different words to make the ECC schemes more effective in tackling multi-bit errors, as will be discussed in the next sub-section. Use of ECC, bit interleaving and memory scrubbing along with hardening by design approaches for the ECC and control circuitry have been proposed by many authors as the most effective method of dealing with soft errors in memory [Sa90], [Ba05b], [Sl05], [Ba07].

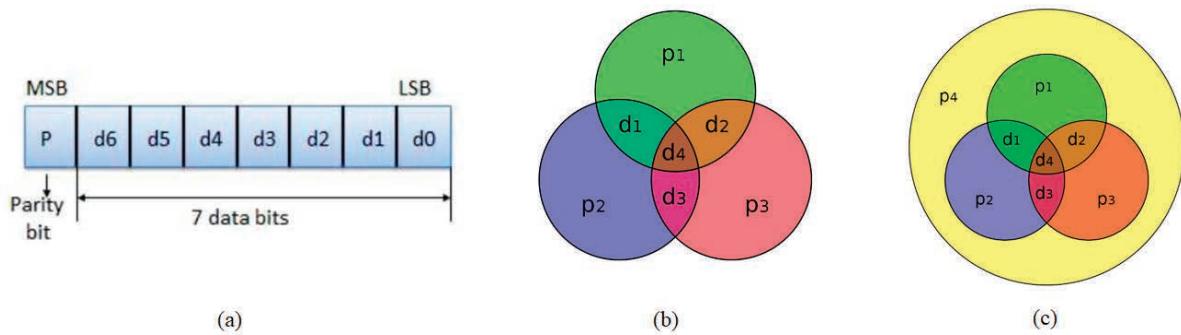


Fig. 10. (a) Illustration of parity bit used for error detection and (b) a (7,4) Hamming code used for error correction, and (c) (8,4) extended Hamming code (SEC-DED), after [Wik1]

Parity is the simplest form of error detection (Fig. 10(a)). The parity bit ensures that the total number of 1-bits in the string is even or odd. If the number of ones in given word including parity bit is even then it is termed even parity. Receiver can detect presence of error if parity of received

signal is different from expected parity. For some applications, detecting the presence of an error may be sufficient and the firmware or software can handle the error. The drawback of using higher-level systems to handle error is that it adds to the error recovery times or latency to correct the error.

For many applications, detecting the presence of an error is not sufficient. For such cases, ECC helps detect and correct the error [Ch84]. ECC are implemented with encoder and decoder blocks. The encoder block creates a set of check bits that will help identify the position of an error and the decoder block will be able to restore the correct value. While ECC can be implemented at the hardware or software level, hardware-based ECC have the advantage of low latency for error correction. The simplest ECC can correct single-bit error and detect double-bit errors, while more complex schemes can detect or correct multiple-bit errors. The key parameters of an ECC are denoted by (n, k) or (n, k, d) , where n is the total number of bits used, k is the number of data bits and d is the number of bit-differences between valid codewords within a code. The difference $n-k$ represents the amount of redundancy in a particular code. One of the simplest ECC is the Hamming code, named after R. W. Hamming who invented it in 1950 [Ha50]. Hamming codes belong to a family of linear error-correcting codes in which, for $r \geq 2$, $n = 2^r - 1$ and message length $k = 2r - r - 1$. Fig. 10(b) illustrates an example of a $(7, 4)$ Hamming code with 4 data bits and 3 check or parity bits that are based on different combinations of the data bits such that a single bit error in any of the 7 bits can be identified. With an additional parity bit, the code can correct a single bit error and detect a double bit error and is known as the extended Hamming code or single-error-correct/double-error-detect (SEC-DED) code. An $(8, 4)$ SEC-DED code is shown in Fig. 10(c).

A common code in computer memories is the $(72, 64, 4)$ SEC/DED code [Ch84], [Sh05], [Ta09]. It uses 72 total bits (9 bytes) to encode 64 bits (8 bytes), with a Hamming distance of four between codewords. A single-bit error can be correctly mapped back to its original codeword, or corrected, while a double-bit error can be detected but not uniquely mapped back to a valid codeword. Such codes can be implemented in the hardware using extra memory bits to store the check bits and encoding/decoding circuitry to compute and verify the check-bits.

Table I. Types of ECC schemes

Type of ECC	Method of Operation	Pros/Cons
Two- and Multi-Dimensional Parity Check Code	Message treated as multidimensional grid; Calculated parity digit for each row & column	High error correction, but considerable area/power overheads
Convolution Code	Generates parity via sliding application of a Boolean polynomial function to a data stream	Multiple groups of errors correctable, when relatively far apart; high area/power penalty
Reed-Solomon Codes	Operates on a block of data treated as a set of finite-field elements	Burst error correcting capability, but large area/power overheads
Adjacent Error Correction	Block codes that checks for adjacent errors in data or check bits	Low area/power penalty, but multi-bit errors outside detection range not correctable

Other types of error correction codes that can be used to protect memory against SEU include convolution code [Ra09], two-dimensional error code [Zh10], matrix code [Ar10], Reed Solomon code [Ne05], and Golay codes [Ba07]. The convolution code can correct double errors via sequential encoding and decoding. The two-dimensional error code has a high error correction capability, but at the cost of considerable area and power overheads. The matrix code can correct adjacent errors. The Reed Solomon code and the Golay code can deal with multiple errors, however, suffer from large area, power and delay overheads due to their complex encoding and decoding schemes. In [Sh12], the authors discuss an adjacent error correction code that can correct a single error, a double-adjacent error, and a triple-adjacent error caused by an SEU in high density memory at lower area, power and delay penalties, compared to some of the other ECC schemes. Table I summarizes the details of some of these ECC schemes. Table II provides a comparison of the area, speed, read delay, threshold LET and saturated cross-section [Sh12].

Table II. Performance and radiation-hardness comparison of different ECC schemes, after [Sh12]

	Area	Power	Read Delay	Threshold LET (MeV-cm ² /mg)	Saturated Cross-Section (cm ² /bit)
Adjacent error correction	1	1	1	12.0	7.6e-9
Hamming Code	0.88	0.78	0.92	8.2	5.1e-8
Convolution code	2.45	2.38	0.85	10.6	3.7e-8
Two-dimensional codes	1.27	1.21	1.06	11.7	9.3e-9

In many applications the memory may be in a hold mode for long durations. In such a situation the memory keeps accumulating radiation induced errors as the ECC schemes are activated only when the memory is actively read. Thus, gradually the number of errors in the memory can be more than the correctable and detectable threshold based on the ECC scheme employed. To overcome this, in [Si20] authors highlight the importance of maintaining the number of SEUs in a row within a threshold value set by the employed ECC algorithm and outline a self-refresh scheme that reads stored data periodically and corrects any errors (Fig. 11(a)). The self-refresh is only executed when the SRAM is in the hold mode. Results based on 39 MeV proton testing presented in [Si20] show significant reduction in the number of addresses with errors with the use of the self-refresh scheme as shown in Fig. 11(b).

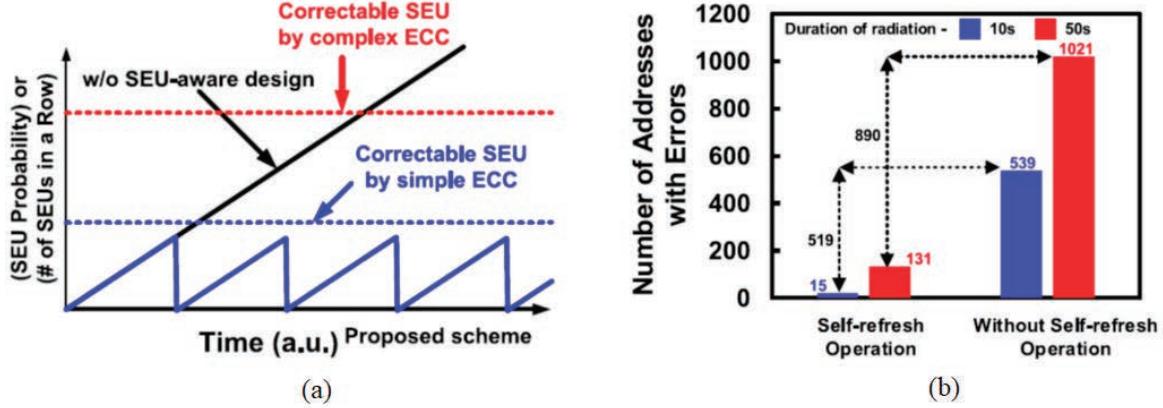


Fig. 11. (a) Self-refresh scheme for lowering # of SEU in idle memory, and (b) Proton test results showing measured number of errors with and without self-refresh for different radiation duration, after [Si20]

3.3. Multi-Bit Upsets

An SEU in memory could affect a single bit, termed as a single bit upset or SBU, or a group of bits could be affected, termed as a multiple-cell or multiple-bit upset (MCU/MBU) as mentioned earlier [Ba05], [Se06], [Ta15], [Fa16]. MCUs are typically produced by high LET events. The MCU fail pattern will typically be contiguous as a single event induces the MCU, but in some cases with different data state sensitivity, non-contiguous fail patterns may be observed. In addition, increasing the incident angle of ions (or protons/neutrons) has been shown to increase the number of cells that upset resulting in increased occurrence of MCUs as well as the number of affected cells in an MCU [Re97], [Ti08], [Ha12], and [Bl13]. This is because the amount of charge deposited per unit depth relative to the surface increases with the angle away from normal resulting in more charge being deposited within the well which spreads to more cells and could cause upsets in more cells. Furthermore, angular strikes increase the proximity of the generated charge to a range of collecting nodes which results in more collected charge in each of them.

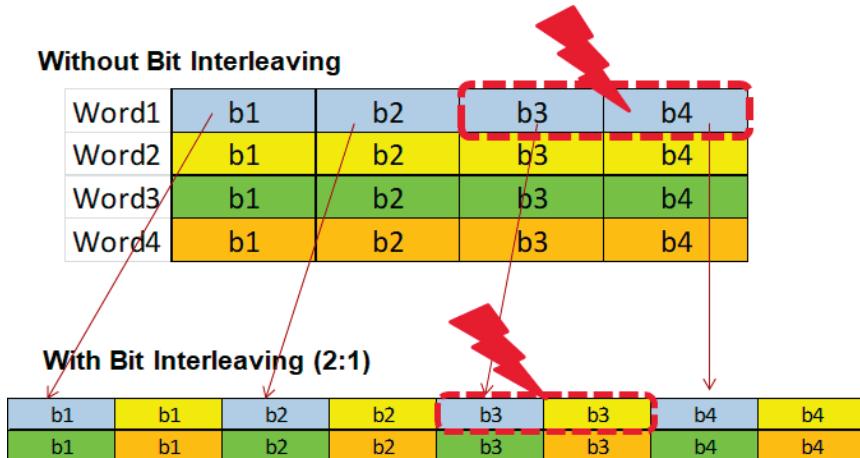


Fig. 12. Illustration of 2:1 bit interleaving scheme in a memory array

Most error correction codes are capable of correcting SBUs, while more complex codes are needed for correcting MCUs, as was seen in the previous section. In a memory array, MCU clusters may extend along word-line or bit-directions or both. MCUs along bit-line direction automatically map to different words and hence do not pose a threat from ECC perspective. MCUs along the word-line direction affect multiple bits within the same word rendering typical ECC schemes to be ineffective. To convert MCU along word-line into SBU across multiple words, bit-interleaving is used in memory design and layout. With bit interleaving, physically adjacent bits map to different words. Thus a contiguous MCU will map to SBU in different words which can be tackled by standard ECC schemes. Fig. 12 illustrates a simple 2:1 bit interleaving scheme on 4-bit words. Extensive radiation test data for the intended environment of operation is needed to understand the maximum extent of MCU events for different types of memories in a given process node.

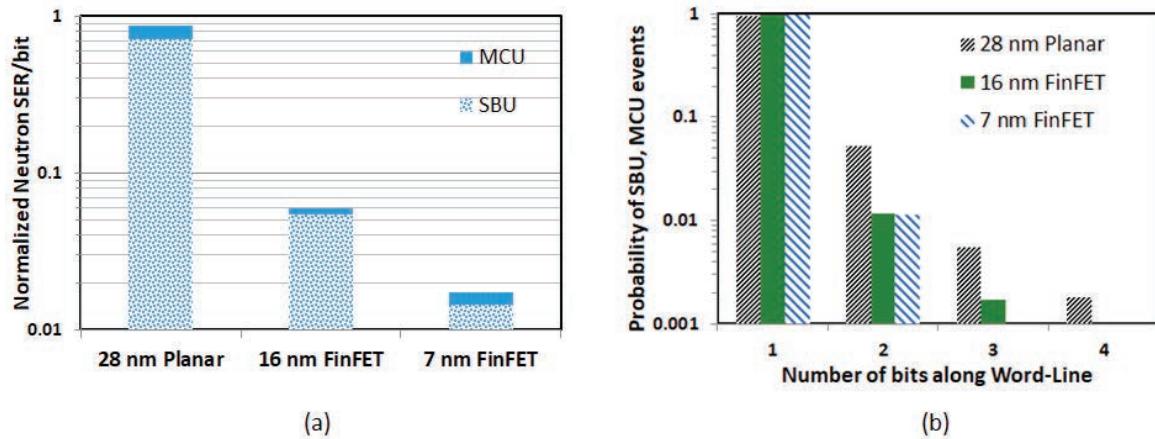


Fig. 13. (a) Normalized single-bit and multi-cell SER for neutron exposures for 28-nm planar, 16-nm FinFET and 7-nm FinFET processes (b) Probability of SBU, MCU events as a function of number of bit flips along the word-line direction, after [Na21]

Recent works have looked at MCU rates and sizes for planar and FinFET process nodes [Ta15], [Na21]. In [Ta15], authors discuss heavy-ion induced MCUs in 16-nm FinFET process and show that the maximum size of MCU is less than 4-bits along word-line direction at nominal operating voltages even at high LETs. In [Na21], authors discuss trends in MCUs from planar to FinFET process nodes based on neutron test results. Fig. 13(a) shows the SBU and overall MCU rates for the 28-nm planar and 16-nm and 7-nm FinFET processes for neutron exposures at the nominal supply voltage for the respective processes [Na21]. Due to the larger LET values of neutron reaction byproducts compared to alpha particles, neutrons exposures typically induce larger MCUs than alpha particles for terrestrial applications. The overall MCU rate includes MCUs in both bit-line and word-line directions. Compared to the planar process, the overall percentage of MCU is lower for the FinFET process nodes, though the 7-nm FinFET node MCU rate is marginally higher than that for the 16-nm FinFET node, as seen in Fig. 13(a). The probability of MCU upsets along the word-line direction which is the key factor that determines ECC efficacy is shown in Fig. 13(b). The 1-bit probability in this chart represents all the single-bit upsets as well as MCUs along the bit-line. As can be observed, ~99% of the upsets in both 16-nm FinFET and 7-nm FinFET processes were found to be SBU or MCUs along bit-line. In addition, the maximum size of MCU along the word-line also reduced from 4 bits in the 28-nm process to 3 bits in the 16-nm process

and to 2 bits in the 7-nm process at the respective nominal supply voltage. These results indicate that similar ECC schemes will be more efficient in FinFET process nodes than in planar process nodes in mitigating soft error threat.

4. Latch/Flip-Flop Hardening Techniques

A latch or flip-flop is the basic storage element in sequential circuits. Similar to memories, latches and flip-flops have two stable states and can be used to store state information. A latch captures data during either the clock-high or clock-low state (level-triggered), while a flip-flop, which is designed using two latches, is typically clock edge-triggered. Fig. 14 shows the design of a standard D-flip-flop circuit formed using two latches along with an illustration of an SEU in the second latch. As can be observed, each latch is designed using back-to-back connected inverters similar to the SRAM cell, while the key difference in the latch is that the feedback loop is controlled by the state of the clock. A latch is said to be in the hold state when the loop is closed. Similar to the memory cell, a latch in the hold state can be upset by a radiation event at one of the off-state devices in the latch, if the collected charge is greater than the critical charge (Q_{crit}) of the latch. In other words, a latch upset occurs when the voltage transient created by radiation strike is longer than the feedback loop delay of the latch.

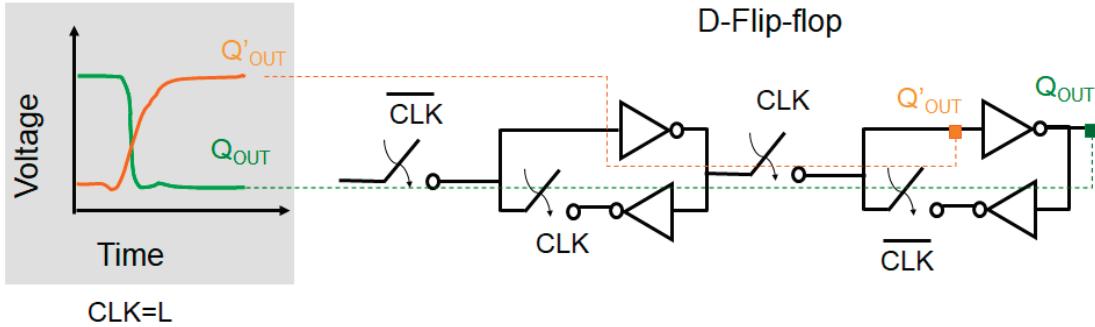


Fig. 14. Design of a standard D-flip-flop formed using two latches and illustration of SEU in the secondary latch

While arrayed memory cells can be protected with ECC schemes, such techniques are generally not applicable for latches and flip-flops, as they are not used in arrayed fashion in sequential logic circuits. Radiation hardening by design (RHBD) is needed to reduce the latch or flip-flops sensitivity to SEUs. Design hardening techniques target to increase the Q_{crit} , which in turn increases the feedback loop delay, or lower the Q_{coll} , which reduces the width of the single-event transient (SET) created by a radiation event. Alternately, redundancy based design techniques may be used to detect and correct SEUs. Different types of latch hardening techniques may be classified into traditional RHBD approaches and commercial or new-space hardening approaches. Table III compares aspects of these two approaches along with some examples. In the next sub-sections we will review some key designs from both these approaches.

Table III. Comparison of latch hardening approaches

	Traditional RHBD Approach	Commercial/New-Space Hardening Approach
Goal	Immune to SEU	Improved SEU; Help meet FIT budget
Examples	DICE-based, redundancy-based (TMR)	RCC-latch, BISER, Hysteresis, Charge-Steering
Target Environment	Traditional space applications	Terrestrial and commercial space
SER Vs. Performance	Best SER, large penalties are acceptable (area, speed or power)	Improved SER (not bullet-proof), moderate to low penalty

4.1. Traditional Hardening-by-Design Approaches for Latches and Flip-Flops

4.1.1. Spatial Redundancy

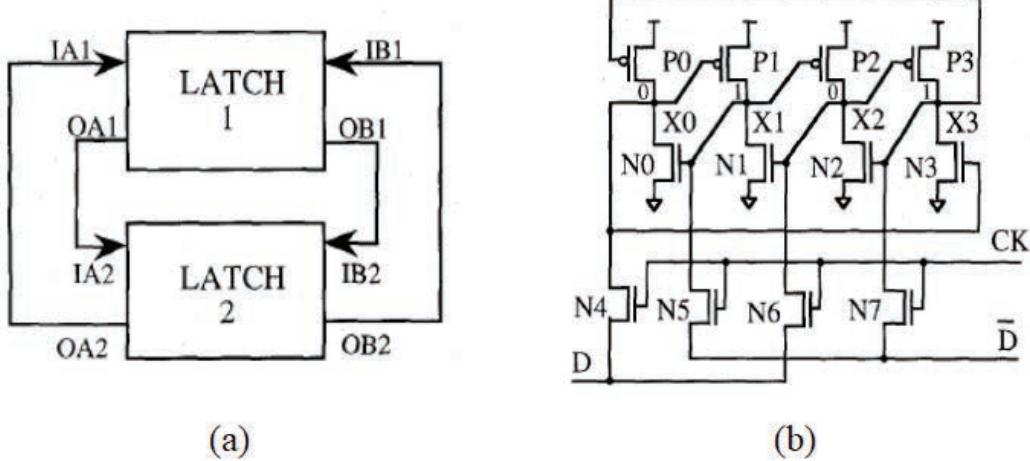


Fig. 15. (a) Design of a redundancy-based hardening with state restoring feedback, and (b) the Dual-Interlocked storage Cell (DICE) latch design, after [Ca96].

Traditional latch hardening involves spatial- and temporal- redundancy based approaches. In spatial redundancy, additional transistors and redundant storage nodes are added to the latch (or flip-flop) circuit. Redundancy in the storage circuit helps maintain a source of uncorrupted data after an SEU. Fig. 15(a) illustrates an example of such a design with two latches, L1 and L2, that store the same data. In addition, data in the uncorrupted section provides specific "state restoring" feedback to recover the corrupted data. In Fig. 15(a), the differential outputs OA, OB of each latch section are connected to the differential feedback inputs IA, IB of the opposite, dual latch section [Ca96]. An extension of such a design which also interleaves the storage nodes is the dual interlocked storage cell (DICE) based latch hardening [Ca96], a version of which was seen under

the design hardening methods for memory in the previous section. Fig. 15(b) shows the DICE latch design. Interleaving provides dual node feedback to each storage node, meaning that the logic state of each of the four nodes of the cell is controlled by two adjacent nodes that do not directly depend on one another. Such redundancy based techniques are generally not sensitive to single node charge collection and require charge collection at two different off-state nodes to flip the cell. While adding extra transistors also adds additional sensitive area, separating the sensitive nodes by a distance larger than the range of typical charge collection distance after a single event is needed to form a robust device. With decreasing feature size and increased packing density leading to increased multi-node charge collection, such redundancy based latch designs are susceptible to an upset.

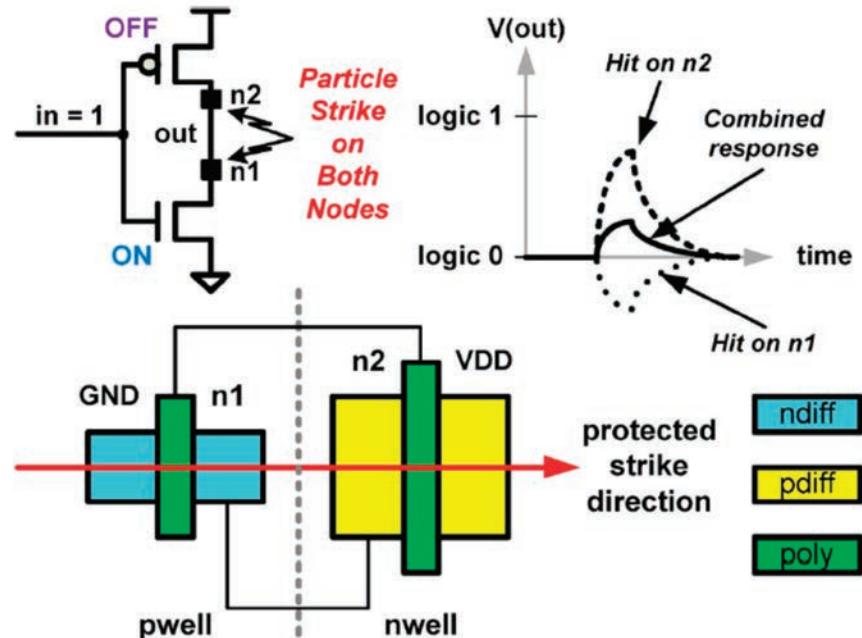


Fig. 16. Illustration of the LEAP principle for an inverter indicating reduced charge collection when single event particle hit covers both NMOS and PMOS drain nodes of an inverter; Transistor alignment in horizontal direction to reduce charge collection is also illustrated, after [Le11].

A variant of the DICE latch called LEAP-DICE was shown to help mitigate impact of multi-node charge collection in DICE design [Le10], [Le11]. LEAP stands for Layout Design through Error-Aware Transistor Positioning and is a layout principle for soft error resilience of digital circuits. LEAP looks at the circuit response to single event charge collection at each individual node, then places the transistors in such a way that during a particle strike, multiple diffusion nodes can act together to fully or partially cancel the overall effect of the single event on the circuit. Consider the case where the drain contact nodes of the PMOS and NMOS transistors in an inverter are simultaneously hit by a particle strike. In this inverter example, the positive charge collected by the PMOS transistor is offset by the negative charge collected by the NMOS transistor, resulting in lower total charge collection at the output node as illustrated in Fig. 16. Experimental results presented in [Ah10] confirm this type of circuit interaction.

Based on the above principle, the LEAP-DICE design was developed and implemented in a 180 nm CMOS process [Le10], [Le11]. Fig. 17(a) illustrates the positioning of the transistors in such design along with the DICE schematic. Fig. 17(b) shows the cross-sections of DICE and LEAP-DICE as a function of LET for select sensitive directions of incidence in each layout. The lowest LET upset threshold for LEAP-DICE is shown to be about an order of magnitude larger than the lowest LET upset threshold for DICE. In addition, the LEAP-DICE flip-flop has $\sim 5 \times$ lower SEU rate on average, compared to the reference DICE flip-flop.

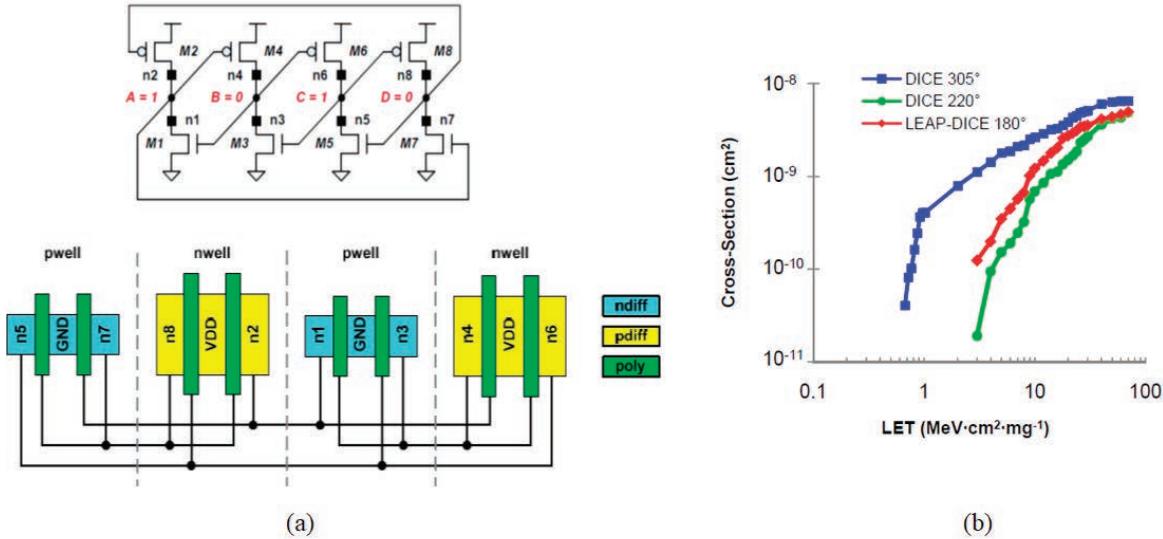


Fig. 17. (a) DICE latch schematic and the LEAP principle based layout positioning of the transistors, and (b) SEU cross-section of standard DICE and the LEAP-DICE designs as a function of LET for select sensitive directions, after [Le10].

Modular redundancy along with majority voters is another key type of traditional latch hardening technique. In n -modular redundancy, n redundant elements are used to detect and vote the correct output, where n is typically an odd number greater than or equal to three. The triple modular redundancy (TMR) is a form of the N -modular redundancy in which three modules

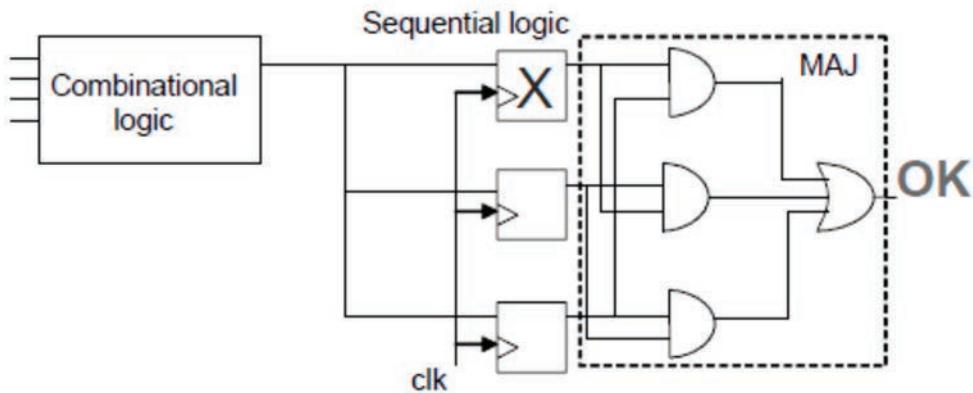


Fig. 18. Triple modular redundancy (TMR) in the sequential logic (flip-flops) along with a majority voter, after [Ka07].

perform a process and a majority voter is used to vote the correct output. If any one of the systems fail, the other two systems along with the majority voter will correct the fault. Fig. 18 illustrates the TMR design for flip-flops along with a majority voter.

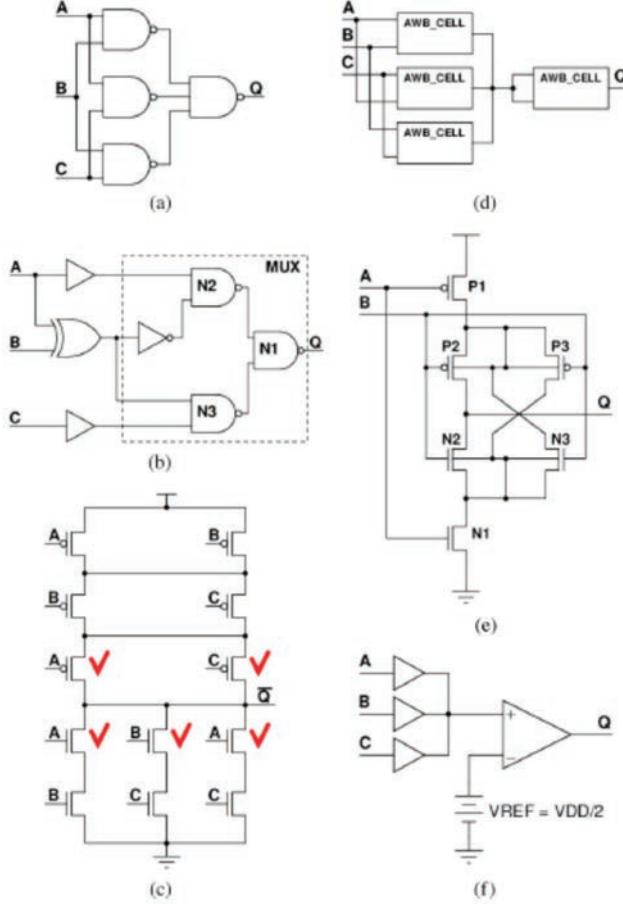


Fig. 19. Majority voter designs investigated in [Da14]. (a) “NAND” logical scheme; (b) “MUX” logical scheme; (c) “12TI” transistor-level implementation; (d) “AWB” logical scheme; (e) AWB_CELL transistor-level implementation; (f) “ACOMP” logical scheme.

The TMR design for flip-flops shown in Fig. 18 has two key drawbacks. Any upsets to the combinational logic will be stored in all three copies of flip-flops and hence will lead to an erroneous output. The next drawback is related to single events on the voter circuitry which can lead to an erroneous signal that propagates and gets latched in the next stage. Full TMR design triplicates the combinational logic and the voter circuitry to overcome these issues and will be reviewed in the next section on combinational logic SE hardening techniques.

Single event tolerance of different types of voter circuitry was studied in [Da14]. The studied designs included a NAND-gates based implementation of voter function, MUX based voter, “12TI” or 12-transistor implementation of voting function, “AWB” which uses actively biased, isolated well transistors and “ACOMP” which is an analog majority voter using a comparator (Fig. 19). Based on the relative area of each of the design and the heavy-ion saturated cross-section area, both relative to that of the NAND based voter design, a relative efficiency factor was presented in

[Da14]. Table IV shows these data indicating that the 12TI design has the best overall relative efficiency.

Table IV. Relative efficiency of different voter design, after [Da14]

Voter	Input	δ_σ	δ_S	δ_{EFF}
NAND	0	1.00	1.00	1.00
	1	1.00		1.00
MUX	0	1.89	1.13	0.47
	1	2.09		0.42
12TI	0	1.14	0.46	1.91
	1	1.40		1.55
AWB	0	3.80	7.78	0.03
	1	5.63		0.02
ACOMP	0	4.34	1.94	0.12
	1	2.58		0.20

4.1.2. Temporal Redundancy

Temporal redundancy techniques process the data at different instances of time, which allows detection of transients that are shorter than the sampling interval. Any SETs that are shorter than the delay between sampling instances will be filtered by such design. A temporal dual feedback (TDF) D-flip-flop design, shown in Fig. 20, was presented in [Ha15] and [Ha16]. Each of the latches in the TDF DFF is protected from SETs on the input and in the feedback by the inverter based delay elements δ_{in} and δ_{fb} , respectively. The signal appearing on the input of the delay element is compared with the signal at the output of the delay element. Thereby, any SET with pulse width shorter than δ_{in} will be filtered out by the redundant inputs as inputs must be equal in order to allow the signal to propagate. If the SET pulse width is longer than δ_{in} , the SET will propagate to node Z_m and will have to be filtered out by δ_{fb} . Any SET with pulse width shorter than δ_{fb} will be filtered out by the guard-gates (GG1 and GG2) (also known as C-elements), as the GG inputs need to be equal in order to allow signal propagation. In order to be tolerant to single node hits on one of the guard-gates, the TDF utilizes dual feedback paths. As discussed in [Ha16], the drawback with temporal redundancy is however that it adds a performance penalty in terms of increased setup time and clock-to-Q delay for each of the latches.

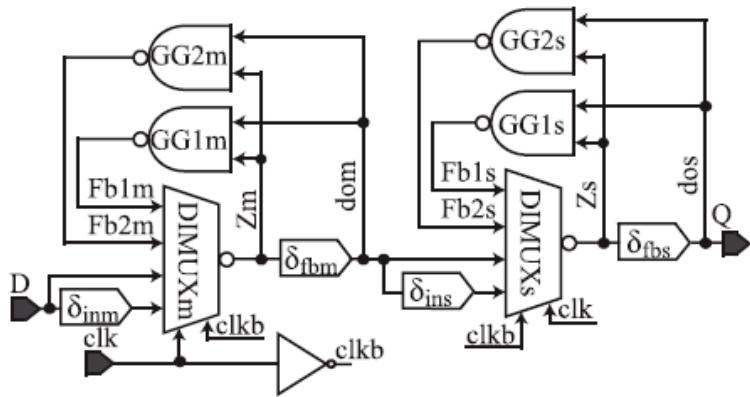


Fig. 20. Schematic of a temporal dual feedback (TDF) DFF, after [Ha15].

The SEU performance of the TDF DFF along with spatial redundancy based designs including DICE and TMR DFF implemented in a 65-nm bulk CMOS process was compared in [Ha16]. Different versions of the TDF, including current starved and low-threshold voltage designs were implemented and tested. Fig. 21 shows one of the dataset presented in this paper, comparing the SEU cross-section for different designs at normal incidence and 45 degree tile angles at LET of 68.8 MeV-cm²/mg and V_{DD} of 0.5 V. Data shows that the baseline TDF SEU performance is comparable to that of the TMR design even at angular strikes. While the DICE SEU performance is good at normal incidence, its SEU increases significantly at angular incidence as probability of multi-node charge collection increases with angular strikes. The TDF design using a current-starved inverter-based delay element instead of multiple inverter based delay elements along with a low threshold voltage transistor based design were also tested in this work. These designs help save area and improve drive currents.

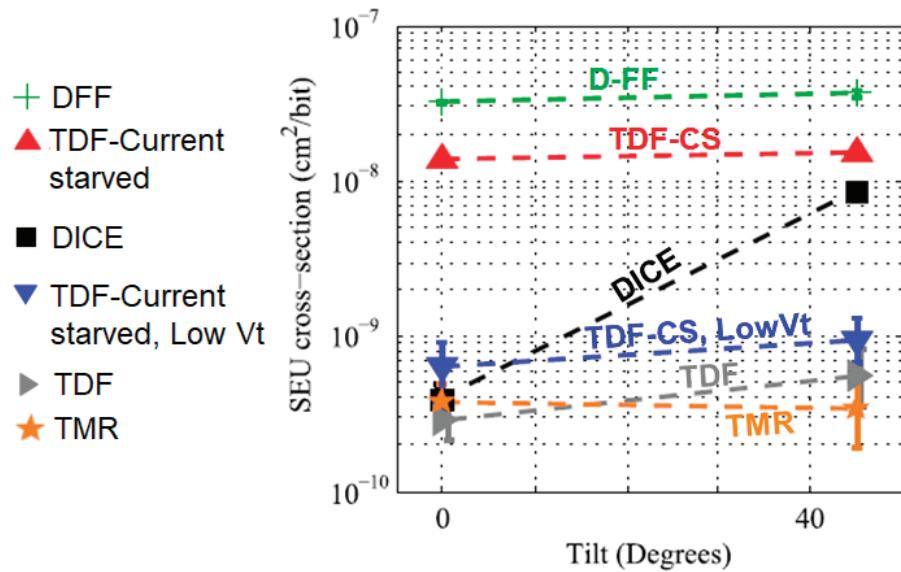


Fig. 21. Heavy-ion SEU comparison TDF and other flip-flop designs at 0 and 45 degree tilt angles of incidence. Data collected at V_{DD} = 0.5V, and LET of 68.8 MeV-cm²/mg, after [Ha15].

4.2. Commercial and New-Space Latch Hardening Approaches

With millions of latch and flip-flop (FF) cells on an integrated circuit, upsets to unhardened latch and FF cells dominate the terrestrial IC-level SE error rates, necessitating hardening them against SEUs for many commercial terrestrial applications. On the other hand, with such a large number of latch and FF cells on an IC, any increase in area or power to improve SE hardness of individual cells results in significant IC-level performance penalties. As a result, SE-tolerant latch and FF cells with minimal performance penalty are highly sought after by the semiconductor industry for commercial as well as for new-space designs.

Over the past couple of decades many different performance-efficient design-hardening techniques have been developed for improving the SEU hardness of latch designs. In this short course we will review a few of these techniques, including built-in soft error resilience (BISER)-based FF [Mi05], reinforcing charge collection (RCC)-based FF [Se10], hysteresis-based FF

[Na12], charge-steering based FF [Na17], and pulsed-DICE design [Na19]. Such designs provide an improvement of up to an order of magnitude in the cell-level SER.

4.2.1. BISER

BISER is based on redundancy wherein the output of the primary latch is compared with data from a secondary or redundant latch using a C-element, as shown in Fig. 22. The cost associated with the redundant latch is minimized by the reusing on-chip resources such as scan for multiple functions at various stages of manufacturing and field use [Mi05]. During normal operation, when the clock signal is high, the latch input is strongly driven by the combinational logic and the latch is not susceptible to SEUs. When clock is low, C-out already has the correct value and any SEU in either latch will result in a situation where the logic value on A will not agree with B. As a result, the error will not propagate to C-OUT and the correct logic value will be held at C-OUT by the keeper. In [Mi05], authors indicate that the BISER technique helps achieve more than an order of magnitude improvement in the SER with minimal area impact (since the redundant latch is a scan-reuse latch), and less than 10% power and performance impact.

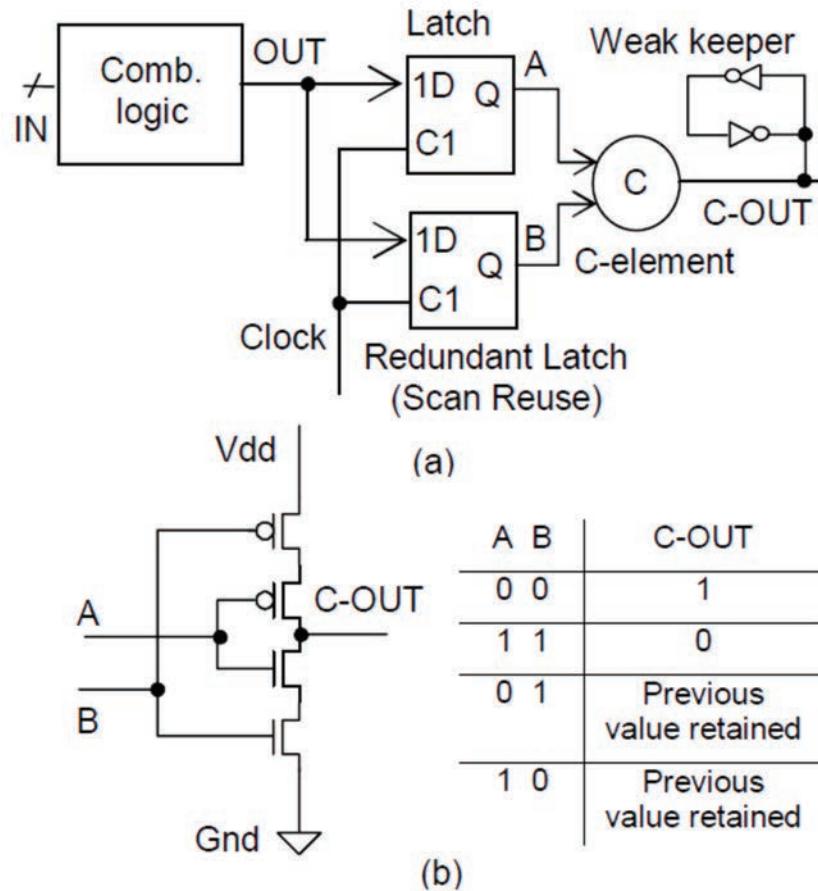


Fig. 22. (a) BISER based latch hardening design and (b) design of C-element, after [Mi05].

4.2.2. Reinforcing Charge Collection (RCC)

The RCC technique is similar to the LEAP-DICE technique seen earlier whereby the transistors are placed in such a way that during a particle strike, multiple diffusion nodes can act together to fully or partially cancel the overall effect of the single event on the circuit. As discussed earlier, a latch circuit typically consists of a pair of cross-coupled inverters and in each inverter the off-state device's diffusion (referred to as victim diffusion) is vulnerable to collecting ionizing-particle-induced charge that can disrupt the stored state. The on-state device's diffusion (referred here as reinforcing diffusion), on the other hand, collects charge that reinforces the stored state. RCC technique is based on the principle that if the charge generated by a particle strike can be collected in both the victim and reinforcing diffusions (charge sharing), the Q_{crit} needed to upset the stored state can be increased, thus reducing the SEU rate.

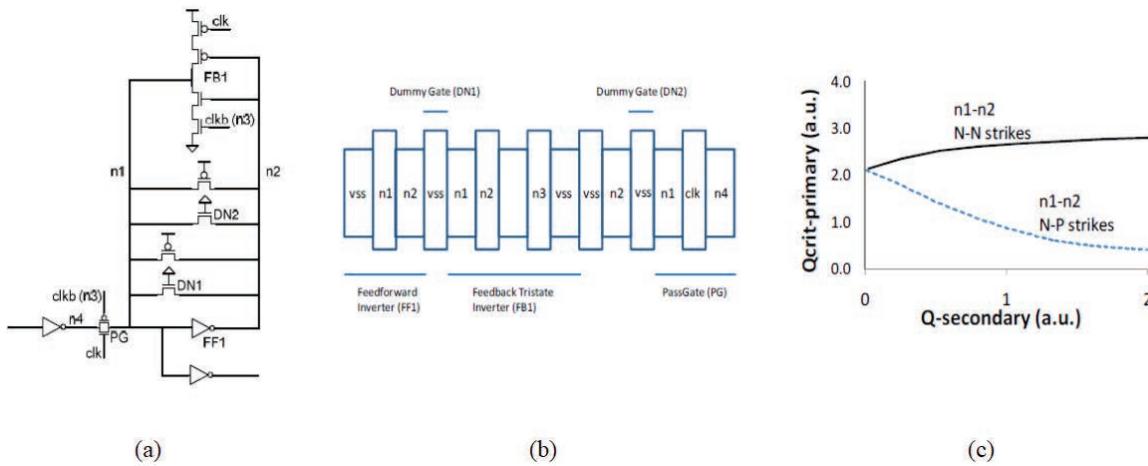


Fig. 23. (a) RCC latch schematic, (b) Layout placement for the N-type diffusions illustrating how the victim and reinforcing nodes are brought together and (c) Q_{crit} simulations showing charge collection for N-N and N-P nodes, after [Se10].

In [Se10], authors explain that the victim diffusion is fully reverse biased making it an efficient collector of the particle-induced charge, while the reinforcing diffusion initially has no externally applied reverse bias, but has only the built-in potential, making it a weak collector. However, even this weak collection serves to increase Q_{crit} . Furthermore, once the victim diffusion begins collecting charge, the electric field across the victim diffusion's depletion region quickly collapses. Simultaneously, since the reverse bias across the reinforcing diffusion increases, its depletion region widens and the charge collection efficiency increases. To improve the charge sharing between victim and reinforcing nodes, these need to be placed close to each other. In [Se10], authors show that if these nodes are within a minimum design rule dimension of each other, the closer proximity leads to a significant SER reduction. This was achieved through use of “dummy” gates (OFF transistors) that helped to bring the diffusions of the same type within one poly dimension, greatly increasing the probability that charge generated by a particle will be collected by both diffusions and thus reducing SER. Fig. 23(a) shows a RCC latch schematic with two pairs of dummy devices that are OFF, and whose sole purpose is to minimize victim-to-reinforcing diffusion separation. One pair allows charge sharing between victim and reinforcing diffusions of the cross-coupled inverters and the other pair allows charge sharing between the input pass gate

diffusion and its complement node. Fig. 23(b) shows the layout stick diagram for such an arrangement for just the N-type diffusions. Fig. 23(c) shows the critical charge simulations, indicating that for N-N strikes (which denote NMOS strikes in nodes n1 and n2) the Q_{crit} increases (and hence SER decreases), while for N-P strikes (which denote strikes where charge is collected in the OFF NMOS on one side and the OFF PMOS on the other side) a decrease in the Q_{crit} occurs (and hence an increase in SER). Table V summarizes neutron and proton test results for RCC type latch designs [Se10]. Results indicate $\sim 3 \times$ lower neutron SER for certain RCC latch designs.

Table V. Neutron and Proton SER test results for RCC type devices, after [Se10]

Device	V _{cc} [V]	Neutron measured SER reduction	Neutron simulated SER reduction (no RCC)	Proton measured SER reduction	
				27 MeV	198 MeV
RCC1	0.7	3.8x ± 30%	1.2x	2.0x ± 10%	2.5x ± 10%
RCC2	0.7	1.1x ± 30%	1.0x	1.1x ± 10%	1.3x ± 10%
RCC1	1.0	NA		NA	3.2x ± 10%
RCC2	1.0	NA		NA	1.3x ± 10%

4.2.3. Hysteresis-based latch hardening

The hysteresis-based latch hardening technique is based on increasing the critical charge of a node without increasing the sensitive area [Na12]. For the same sensitive cell area, a higher critical charge will help lower the SEU rate. Although there are many approaches to increasing the critical charge, many of them also result in increasing the sensitive area, thus negating the overall impact on the SEU rate. For example, it was shown that simply doubling the transistor size (which helps improve the drive current, capacitance and hence the critical charge) does not provide any significant improvement in the overall SER [Le11]. Critical charge is also directly related to the switching threshold (among other parameters, such as nodal capacitance, transistor drive currents, etc.) of individual gates. A higher switching threshold will require higher voltage swings, resulting in increased critical charge and forms the basis of the hysteresis based hardening approach.

Fig. 24(a) shows the hysteresis-based D-latch design. In the hysteresis latch, the storage nodes of the standard latch are each connected to a secondary cross-coupled inverter pair (or ‘hysteresis’ inverters) with a weaker drive. The ‘hysteresis’ inverters lead to shifting the switching threshold voltage of the latch and increasing the noise margin. In addition, the hysteresis inverters are gated by the clock, which helps improve the speed and power performance. This gating was shown to be a key advantage of the hysteresis approach over designs based on the Schmitt-trigger latch [Sa06]. It selectively applies hysteresis only during the hold mode of the latch and not during the write operation. Furthermore, with the use of clocked inverters, the pass-gates in the hysteresis inverter loop can be combined with the pass-gate in the main latch inverter loop. Along with the

smaller size of the hysteresis inverters and reduced routing complexity, this helps lower the area impact for the hysteresis-based D-latch design.

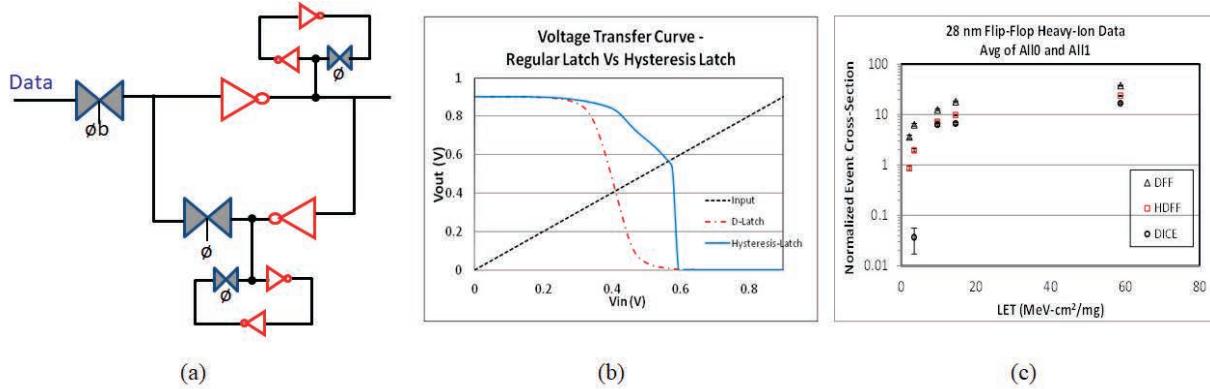


Fig. 24. (a) Schematic of the hysteresis-based D-latch, (b) Voltage transfer curves for the standard D-latch and the hysteresis latch showing the higher switching threshold for the latter design and (c) Normalized heavy-ion SEU cross-section as a function of the LET of the ion for DFF, HDFF, and DICE designs. After [Na12].

Fig. 24(b) shows the voltage transfer curves for a D-latch and the hysteresis latch based on 28-nm CMOS process. As can be seen from Fig. 24(b), the hysteresis latch has a switching threshold voltage that is about 200 mV higher than the standard D-latch for the case of the input transitioning from low-to-high. A similar increase in the switching threshold is present for the high-to-low transition as well. Thus the overall hysteresis for HDFF is \sim 400 mV. The increased switching threshold along with the increased node capacitance and cell delay results in increasing the critical charge needed to upset the hysteresis latch. In addition, short transients created due to single-event hits are more easily masked by the hysteresis latch. Although the ‘hysteresis’ inverters help improve the critical charge, they do not significantly affect the sensitive cell area of the latch. Because the ‘hysteresis’ inverter has a weaker drive compared to the inverter in the main latch (by a factor of two or more), an upset to the ‘hysteresis’ inverters does not force the main latch to change state.

In [Na12], it was shown that the average critical charge for the hysteresis DFF (or HDFF) is more than $3\times$ greater than the critical charge for DFF, whereas the area penalty (increase in cell area required) is about 55% lower than that of the DICE design. Although the HDFF cell has a similar number of transistors as that of a DICE FF design, the smaller size requirement for the ‘hysteresis’ inverters and the reduced routing complexity of the HDFF make its cell area significantly smaller than that of the DICE. In addition, the cell delay and power are lower for the HDFF cell compared to the DICE design. Fig. 24(c) shows the normalized heavy-ion cross-section as a function of particle LET for the DFF, HDFF, and DICE FF based on test results from a 28-nm test chip [Na12]. At very low particle LETs, the DICE FF is much harder than the HDFF or DFF. The soft error performance of DICE FF, however, degrades with increasing LET of the ion. The HDFF design provides about $3\times$ improvement in the SEU cross-section compared to the DFF indicating that the HDFF can be used to gain improved SEU performance at a lower performance penalty.

4.2.4 Charge-Steering latch hardening

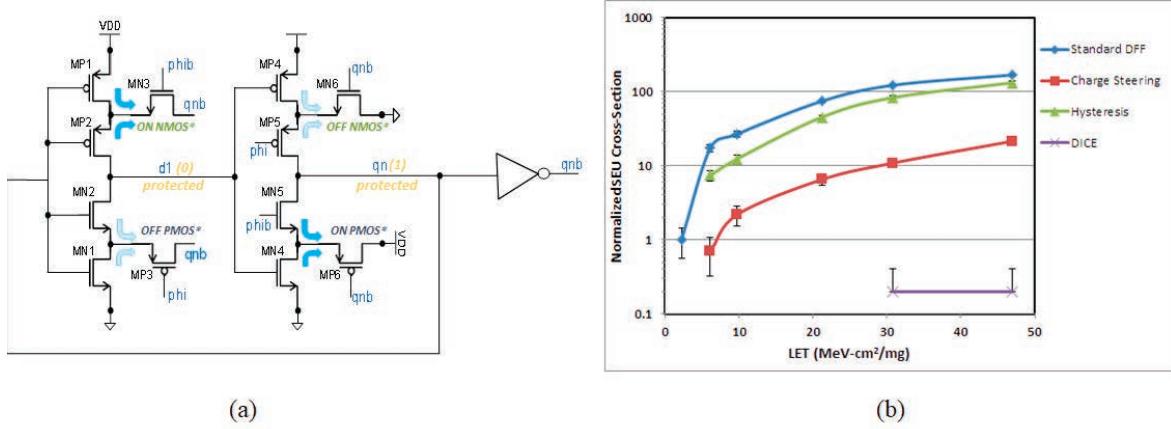


Fig. 25. (a) Schematic of the charge-steering D-latch, and (b) Normalized heavy-ion SEU cross-section as a function of the LET of the ion for standard DFF, hysteresis DFF, charge-steering and DICE designs for 16-nm FinFET technology. After [Na17].

The charge-steering latch improves the SEU tolerance by providing an alternate low impedance path for excess carriers generated during an ionizing particle strike [Na17]. Charge steering is achieved through the use of guard transistors, which are connected to the latch internal nodes to steer excess carriers generated by the single event away from the storage nodes. This is equivalent to providing additional restoring current drive at the hit node. The combined effect of the Q_{coll} decrease at the sensitive node (due to excess carriers being steered away from it) along with the Q_{crit} increase that comes from the additional parasitic capacitances, results in a significant improvement in the SEU performance.

Fig. 25(a) shows the schematic design of the charge-steering latch, where NMOS transistors MN3 and MN6 are used to steer charge away from ion hits on PMOS transistors MP1/MP2 and MP4/MP5, respectively [Na17]. Likewise, PMOS transistors (MP3 and MP6) are used to steer charge away from ion hits on NMOS transistors. During normal operation, if the input signal to the charge-steering latch is “high”, the signal level at node d1 is 0 V because MP1 and MP2 are turned off, and MN1 and MN2 are turned on. When the input signal is “high”, and the latch is in hold state (i.e., phi is “low”), charge-steering transistor MN3 is strongly ON. Both the source and drain of MP2 see a “low” voltage and hence the source-body and drain-body junctions are reverse biased. It should be noted that an ion hit (and the subsequent charge collection) on the drain of MP1 alone will not affect the storage node voltage because MP2 will remain OFF during this period. During an ionizing particle strike event on MP2, the reverse-biased source-body junction of MP2 (or drain-body junction of MP1) offers an additional low resistance path to remove the excess charges through MN3, which provides a low resistance path for the carriers, and steers it away from the sensitive node. Due to the close proximity of the source and drain nodes of a transistor in such advanced technology nodes, charge sharing is easily initiated between the source and drain of MP2 and the excess charges will tend to flow through the path with the lowest impedance. For charge collection at MP2, the impedance of the MN3 path was found to be about 1.5× to 2× lower than the impedance of the latch output path (since the charge steering transistors

were designed to have larger fin count than the latch transistors). This helps reduce the SEU susceptibility of the cell by steering charges away from the latch storage nodes. Similarly, MP6 helps protect MN4/MN5 nodes in the second inverter for this input condition. For the opposite input condition, MP3 and MN6 protect the respective sensitive nodes. It should be noted that only one charge steering transistor is ON per stacked inverter and hence there is no contention during hold state. As discussed in [Na17], the effective critical charge for the charge-steering latch was found to be more than $4\times$ greater than the critical charge for DFF. The charge steering design was also shown to have lower performance penalties compared to the hysteresis and DICE FF designs.

Fig. 25(b) shows the normalized heavy-ion data for the standard DFF, hysteresis, charge-steering and DICE designs based on test results from a 16-nm FinFET test chip [Na17]. While the hysteresis design shows marginally better performance compared to the standard DFF, the charge-steering FF design shows more than an order-of-magnitude SEU cross-section improvement across LETs compared to the DFF.

4.2.5. Pulsed-DICE latch

As discussed earlier, a latch captures data during either the clock-high or clock-low state while a flip-flop is designed using two latches to obtain clock edge-triggered operation. A pulsed latch is designed with only a single latch, but uses a pulsed clock to trigger it [Ko96]. This synchronizes the pulsed latch to the clock in a similar fashion to the edge-triggered flip-flop, since the rising and falling edges are identical in terms of timing. The pulsed latch requires a pulse generator to generate pulses with a source clock. With such a pulsed clock, the latch operates like an edge-triggered flip-flop. Since the pulsed latch operates like a flip-flop using only a single latch, it is inherently faster and more power efficient than a conventional flip-flop design (which requires two latch stages).

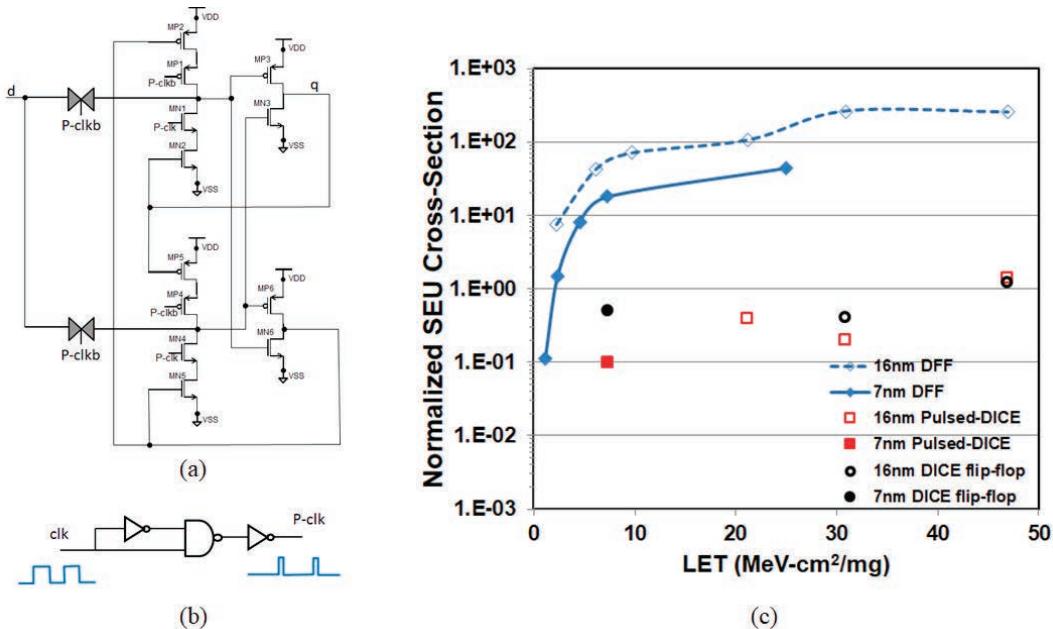


Fig. 26. (a) Schematic of the pulsed-DICE latch, (b) circuit to generate pulsed clock and (c) Normalized heavy-ion SEU cross-section as a function of the LET of the ion for standard DFF, pulsed-DICE, and conventional DICE designs. After [Na19].

In [Na19], a pulsed-DICE latch, a conventional DICE flip-flop and the standard DFF were implemented in both a 16-nm FinFET and 7-nm FinFET bulk CMOS processes. Fig. 26(a) shows the schematic of the pulsed-DICE latch and Fig. 26(b) shows the pulse generator circuitry. The pulsed-DICE latch was found to be about 60% faster (based on setup time + clock-to-Q delay) with an area overhead that is ~30% lower compared to a conventional DICE-FF design. Fig. 26(c) shows the normalized heavy-ion data for the standard DFF, pulsed-DICE and the conventional DICE designs. These results were based on testing at reduced bias of 0.55 V. Results indicate that, even at the reduced bias condition, the LET-threshold for the pulsed-DICE design is >7 MeV-cm 2 /mg at normal incidence and the cross-sections are ~ two orders of magnitude lower than that for the standard D-FF above that LET. The SEU performance of the pulsed-DICE latch and the conventional DICE FF were comparable (within error bars).

Table VI provides a comparison of the cell area, neutron (or proton) SER and the saturated heavy-ion SEU cross-section of various flip-flop designs relative to that of the standard DFF. While TMR based FF design offers the lowest SEU vulnerability, alternatives such as the charge-steering and pulsed-DICE provide significant SER and SEU reduction at much lower area penalty making such designs attractive option for many terrestrial and certain space applications.

Table VI. Area and SEU performance comparison of various flip-flop designs relative to the standard DFF

Flip-Flop Type	Area (n.u.)	Neutron/Proton SER (n.u.)	Saturated Heavy-Ion Cross-Section (n.u.)
D-Flip-Flop	1	1	1
Hysteresis D-FF	1.7	0.05	0.5
Charge Steering D-FF	1.26	0.014	0.13
DICE	$\sim 2x$	0.01	<0.1
Pulsed-DICE	1.33x	0.01	<0.1
TMR	$>3x$	<0.001	<0.001

5. Combinational Logic SET Hardening Techniques

In a combinational logic circuit, charge collection due to a single-event strike on a particular node will generate a low-to-high or high-to-low voltage transition or a transient called the SET. The collection of charge first results in a current spike. This current spike may momentarily flip the state of the output node, thus causing a “glitch” or transient to propagate along the combinational logic chain. The ability of this noise pulse to propagate depends not only on its magnitude, but also on the active logic paths from the node existing at that instant in time. An example of this is shown in Fig. 27.

As long as an active path exists for the propagation of the SET pulse, its capture as an error by a latch depends on the width of the transient and on the clock frequency. An error in this context is defined as latching an incorrect logic value. Depending upon the magnitude of charge collected, the width of this transient voltage pulse varies. The pulse width of the transient (along with clock frequency) thus determines the vulnerability of the circuit to SETs [Do-03, Bu-01]. In advanced

technologies with lower propagation delays and higher clock frequencies, the SET can more easily traverse many logic gates, and the probability that it is latched increases [Ba-05].

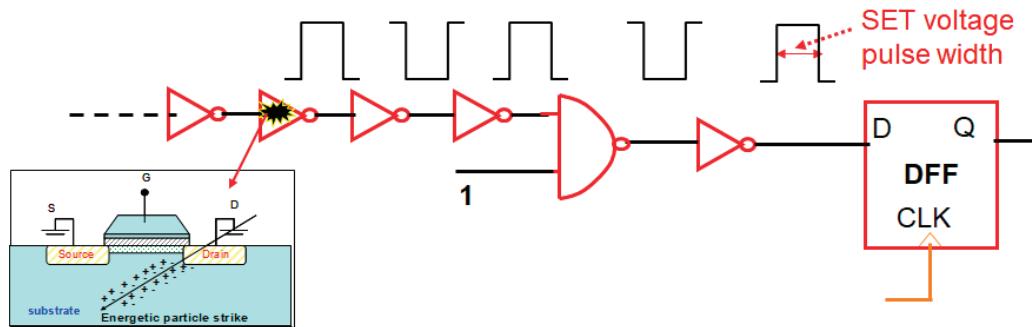


Fig. 27. Single event transient (SET) propagation through a combination logic chain

Traditional approaches to combinational logic SET hardening involve RHBD techniques to reduce the width of the SET. This includes use of guard drains and guard bans to reduce the Q_{coll} at a node which in turn helps reduce the SET pulse width making it harder to be latched as an error. Redundancy-based approaches including temporal- and spatial- redundancy are other popular techniques to mitigate SETs. We will review these approaches in this section along with a commercial low-cost approach based on targeted-hardening.

5.1. Traditional Combinational Logic SET Hardening Techniques

5.1.1. SET Pulse Quenching

A layout approach to mitigate charge collection at a node and charge sharing between nodes is by surrounding the device with guard rings or guard drains [Na08], [Bl05]. The reduction in Q_{coll} helps reduce SET pulse width in turn reducing probability of latching an SET as an error. A guard ring is an n+ (or p+) diffusion region surrounding a device in the n-well (or p-substrate). Guard drains are reversed biased diodes placed near the drain regions in order to minimize the charge collected by the hit device (see Fig. 28).

Guard rings have been shown to be effective for PMOS devices in the n-well, but they have not been as effective for NMOS devices in the p-substrate [Na08]. This is because guard rings help maintain the well potential and hence limit secondary charge collection from parasitic bipolar effect in PMOS devices residing in the n-well. However for NMOS devices in the p-substrate, charge collection is not enhanced by the parasitic bipolar transistor and guard rings are less efficient. Whereas guard drains were shown to be better at reducing drift and diffusion charge collections in NMOS transistors. The guard drain regions act as a secondary charge collection region and collect some of the deposited charges thus reducing the charge available for collection by the hit device. TCAD simulations presented in [Na08] show the effectiveness of guard rings and guard drains in reducing the collected charge in a 130-nm bulk-CMOS process (Fig. 29).

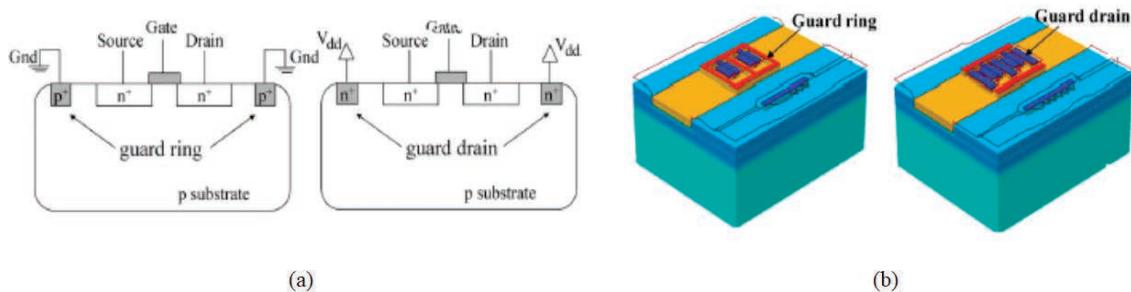


Fig. 28. (a) NMOS cross-section and (b) 3D-TCAD structures of PMOS devices depicting layout with guard rings and guard drains. After [Na08]

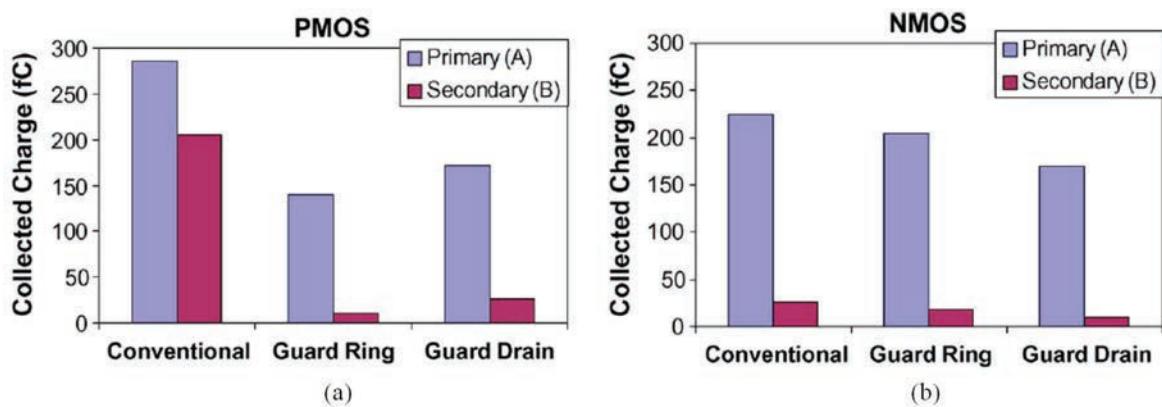


Fig. 29. Charge collection in TCAD structures depicting a conventional layout, layout with guard rings and layout with guard drains for (a) PMOS and (b) NMOS devices. After [Na08]

Experimental results based on a 130-nm bulk CMOS process also showed that guard rings help reduce the maximum SET pulse width, which corresponds to the maximum amount of charge collected, by about 20% (Fig. 30) while the event cross section reduces by about 42%. On the other hand, guard drains were found to be about 30% more efficient in reducing error rates than guard rings.

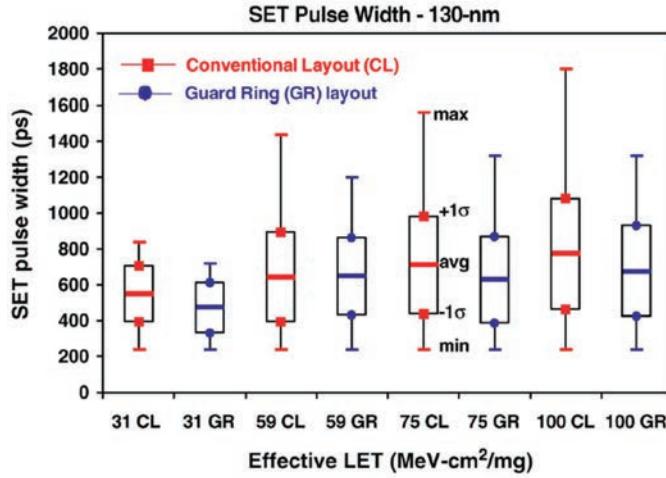


Fig. 30. Heavy-ion test results showing the average, minimum, maximum and ± 1 standard deviation in SET pulse widths for conventional and guard ring layouts, after [Na08]

5.1.2. Spatial Redundancy

Spatial redundancy for combinational logic SET mitigation involves using two or more copies of the logic and latch circuitry. Using two copies of the logic and latch circuitry will allow detection of errors in any one path. As discussed in the case of the BISER technique, using a C-element at the output of the two paths, as shown in Fig. 31(a), will mask any error in one of the paths from propagating [Mi05].

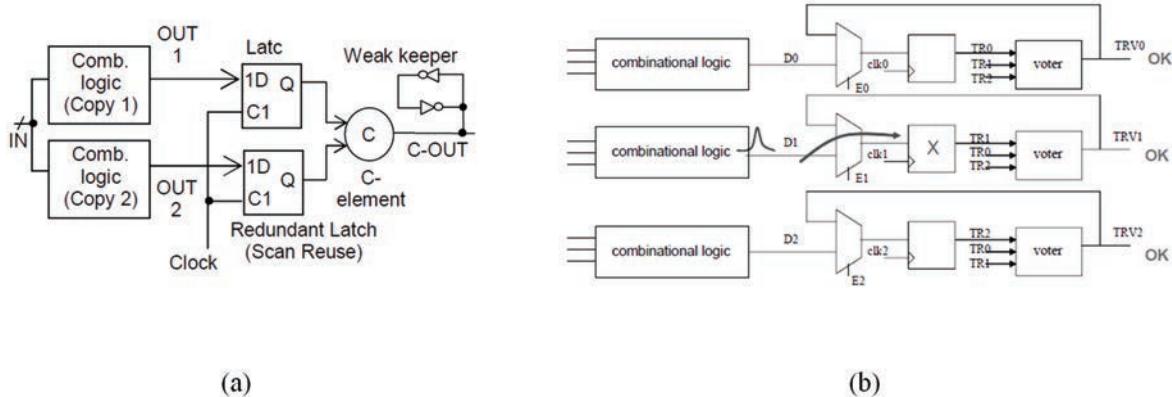


Fig. 31. Spatial redundancy based combinational logic SET hardening using (a) two copies of logic and latch circuitry along with C-element, after [Mi05] and (b) full TMR based design, after [Ka07]

The more popular approach is the triple modular redundancy (TMR) which in the case of combinational logic SET mitigation involves the use of three copies of the logic and latch circuitry [Ka07]. Along with a majority voter this can correct the errors in any one path. To mitigate direct upsets to the voter circuit, the voter is also triplicated as shown in Fig. 31(b). The key drawback

dual or triple modular redundancy is the significant power and area penalties associated with this approach.

5.1.3. Temporal Redundancy

Temporal redundancy techniques rely on sampling the data at different time intervals which allows the detection of faults that are shorter than the sampling delay [Ka07], [Mi05]. Use of two copies of flip-flops which are controlled by a clock and a delayed clock will allow for the detection of an SET, while three copies allow for error correction. The delay (d) should be longer than the longest SET pulse width that must be detected. Another option is to sample the combinational logic output and a delayed version of the output using the same clock as shown in Fig. 32(a). Once again, the use of a C-element helps with masking errors in any one of the paths. Fig. 32(b) shows the implementation using 3 copies of flip-flops. While time redundancy reduces the area and power penalties associated with duplicating the logic circuitry, the clock distribution gets more complicated and the frequency of operation is lowered to account for the arrival of the delayed signals.

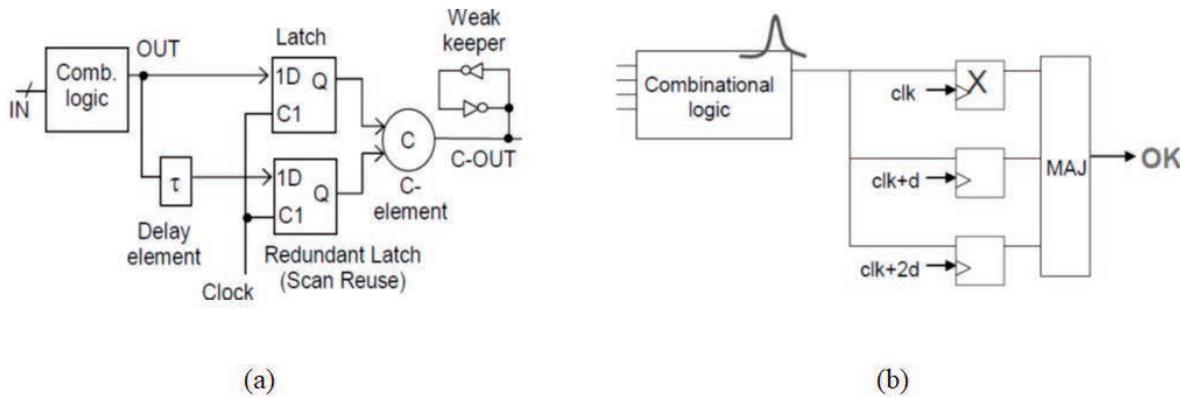


Fig. 32. Temporal redundancy based combinational logic SET hardening (a) using two copies of latch one of which receives the direct output of the logic circuit and the other the delayed output, after [Mi05] and (b) using three copies of latch circuit with delayed clock signals, after [Ka07]

The above approaches highlight that combinational logic SET hardening is more expensive in terms of area, power and performance penalty compared with memory and latch hardening techniques. On the other hand, studies have showed that combinational logic SEU rates are a small fraction of the latch or FF SEU rates even at high frequencies of operation [Ha09], [Se15]. Heavy-ion test results presented in [Ha09] show that the SET cross-section per gate is about an order of magnitude lower than the standard FF SEU cross-section per bit. In [Se15], the authors indicate that the combinational SER per minimum-sized, nominal N/P ratioed inverter is about 1% of the receiver FF SER at 1 GHz based on neutron test results (while the ratio is closer to 10% for skewed N/P ratioed inverters that were designed to enhance SET propagation). In other words, for each nominally designed inverter in the fan-in cone of a FF, the combinational SER increases by 1% of the receiving FF SER at 1 GHz indicating that their contribution to the overall SER remains less than that of sequential elements. Fig. 33 plots the ratio of the combinational logic SER per inverter

for skewed (denoted by “S6”) and nominal (denoted by “N6”) N/P ratio inverters as a fraction of the FF SER.

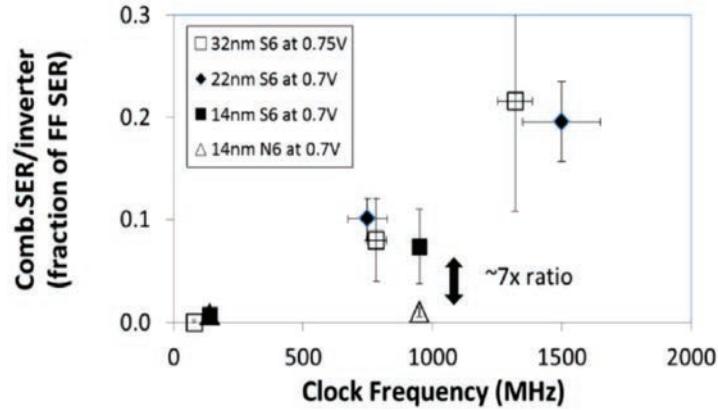


Fig. 33. Measured combinational logic SER per inverter as a fraction of the FF SER for nominal and skewed inverter designs, after [Se15]

5.2. Commercial and New-Space SEU and SET Mitigation – Targeted Hardening

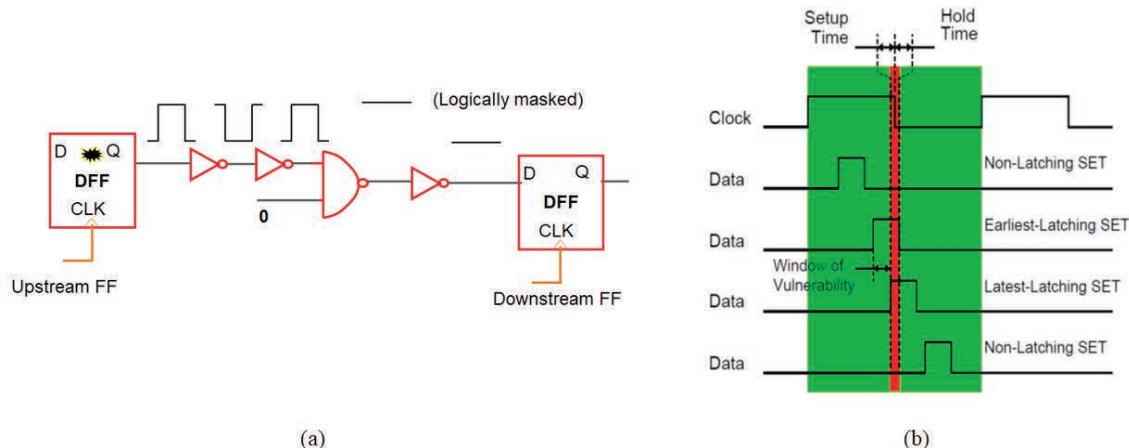


Fig. 34. (a) Illustration of logic masking and (b) temporal relationship for latching an SET as an error, after [Ma02]

Targeted hardening is based on the fact that not all logic or FF upsets propagate to the output of the system due to various masking effects such as logic masking and timing masking [Na13]. If the locations of the majority of critical logic paths and FFs in a design can be identified, then targeted hardening can be applied to efficiently mitigate logic SEU and to minimize the area, speed, and power penalties. Logic or functional masking occurs when an error at a node does not propagate due to the logic state of the system or does not affect system output (Fig. 34(a)). Timing masking happens when an error at a node does not reach the downstream logic within the setup and hold time requirements as illustrated by Fig. 34(b) [Ma02], [Se04]. The overall chip-level logic SEU rate is the product of the raw SEU rate times these masking factors.

$$SER_{net} = SER_{raw} \times Logic\ Masking\ Factor \times Timing\ Masking\ Factor \dots\dots\dots (3)$$

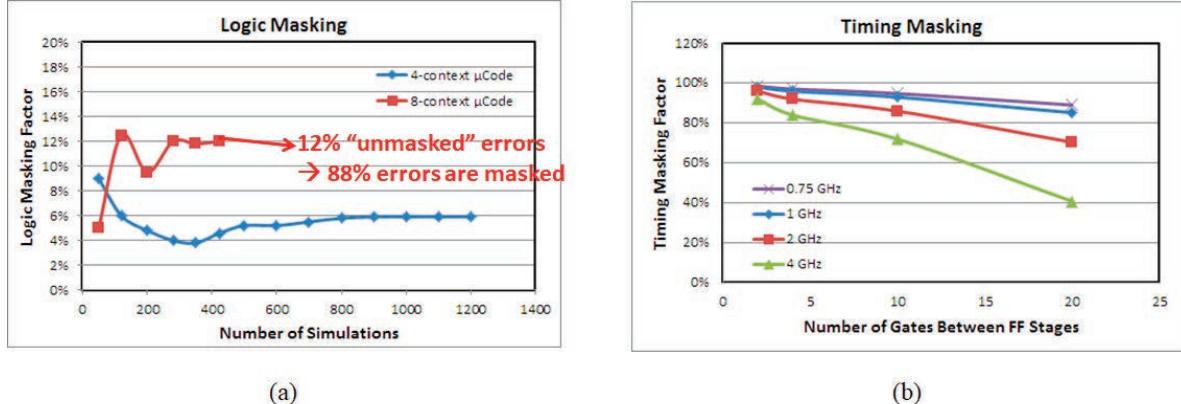


Fig. 35. (a) Logic masking factors for a network processor design for different operating modes (8-context represents max processor load) and (b) timing masking factors based on FO-4 gates between upstream and downstream FF, after [Na13].

In [Na13], a network processor design with millions of flip-flops was simulated to identify the masking factors. Timing masking factor (TMF) is a measure of the fraction of time a circuit is sensitive to upsets [Se04]. Timing masking was simulated on a linear chain of fan-out-4 inverter stages between an upstream and downstream flip-flop in [Na13]. The timing masking factor was extracted for different operating frequencies and number of gates between flip-flops. With increasing pipeline depth, the propagation delay through the combinational logic increases, which results in reducing the TMF and, in turn, the net SER. Similarly, increasing clock frequency also reduces the TMF. The timing masking factor was found to be ~93% for an average pipeline depth of 10 gates between flip-flops used in the network processor design running at 1 GHz frequency as shown in Fig. 35(b).

The logic masking factors were analyzed for different functional blocks of a network processor design with the use of a statistical fault injection model. Analysis of these results indicated that a majority (~88–94%) of these errors are logically masked as shown in Fig. 35(a), and that most errors originate from a few functional blocks. Fig. 36(a) shows a simplified block diagram of the network processor highlighting the key functional blocks. Fig. 36(b) shows the percentage of unmasked errors for each functional block. The secondary y-axis of Fig. 36(b) shows the number of flip-flop cells in each functional block. The analysis indicates that the instruction controller and pipeline (“instruct” functional block) propagated the most errors (~28%), while many of the other blocks either did not propagate errors or have <5% error factors. Furthermore, the instruction controller and pipeline accounts for ~55% of the overall errors and, hence, hardening the logic gates and flip-flops in this block can help eliminate these errors. This functional block has about 174K flip-flops which constitutes ~10% of the total flip-flop count of 1.75M. Thus targeted hardening of a small fraction of the overall design can result in a significant improvement in the overall SER.

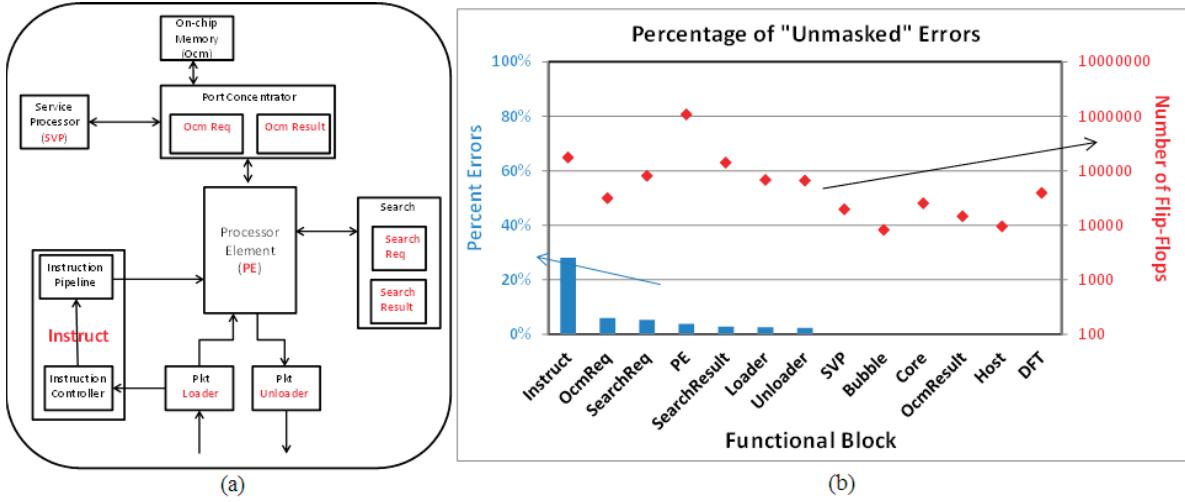


Fig. 36. (a) Simplified block diagram of the network processor highlighting the key functional blocks. (b) Percentage of unmasked errors (primary y-axis) and the number of flip-flops (secondary y-axis) per functional block, after [Na13]

In [Na13], the relative SER was presented for the unhardened processor using standard DFF, and for two cases of targeted hardening using either the hysteresis DFF or the DICE FF for the instruction pipeline (which has ~10% of the overall flip-flops but accounts for ~55% of the overall unmasked errors). Table VII summarizes these results, indicating that with a mere 7% increase in the overall flip-flop area, the overall flip-flop SER can further be reduced by a factor of ~2× with the targeted use of hysteresis DFF. The targeted use of DICE offers only marginally better SER compared to the hysteresis DFF, while the area penalty is about 2× higher. The overall processor speed is determined by the longest path or pipeline depth in addition to the flip-flop delay. With the targeted use of the hysteresis DFF, the overall processor speed is estimated to reduce by about 8% and the power increases by about 3% compared to the unhardened processor. The speed and power penalties are marginally larger with the targeted use of DICE FF, as shown in Table VII. The targeted hardening approach can easily be extended to hardening the logic gates in the instruction pipeline to mitigate the logic SET contribution, in addition to the FF SEU contribution. With different applications having different SEU mitigation requirements, such targeted hardening can help meet the overall error rate budget with lower area, speed and power penalties.

Table VII. Raw and derated FF SER along with the overall FF area, speed, and power comparison for the unhardened and ‘targeted’ hardened processor, after [Na13].

Category	Overall FF Area (n.u.)	Overall Processor Speed (n.u.)	Overall FF Power (n.u.)	Overall Raw FF SER (n.u.)	Overall Derated FF SER (n.u.)
Unhardened Processor	1	1	1	1	0.112
Processor with Targeted Hardening using Hyst-DFF	1.07	0.92	1.03	0.54	0.060
Processor with Targeted Hardening using DICE	1.15	0.88	1.08	0.51	0.057

6. Single-Event Latchup Hardening Techniques

In this section we will briefly look at some of the SEL hardening approaches. For additional details, request readers to refer to chapters II and IV of this years' short course where rad-hard by design and system-level SEL mitigation approaches are discussed. As mentioned earlier, an SEL happens when an ion strike triggers the parasitic PNPN structure present in CMOS devices creating a low resistance path between the power and ground and is especially a significant concern for CMOS circuits in space radiation environment [Jo96], [Br96].

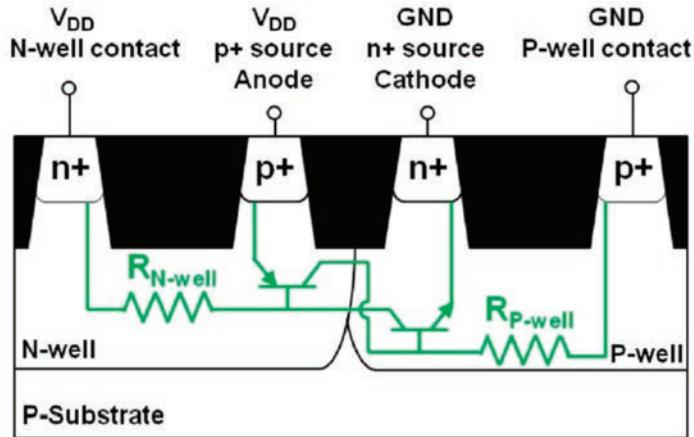


Fig. 37. Cross-section of a dual well bulk CMOS technology showing parasitic resistors and bipolar transistors, after [Do10]

Latchup can be triggered in dual well technologies when the parasitic *pnp* transistor, formed by the p source/N-well/P-well, and the parasitic *npn* transistor, formed by the n source/P-well/N-well, are in a positive feedback loop, such that the output (collector) of each transistor is connected to the input (base) of the other, as shown in the overlaid equivalent circuit in Fig. 37 [Do12]. The positive feedback loop allows a large current to flow from power to ground, which persists until either power is removed or thermal damage occurs.

The key parameters that influence SEL susceptibility are the well and substrate resistance and the current gains of the parasitic bipolar NPN and PNP transistors. Lower resistances make it more difficult to forward bias the parasitic emitter-base junctions and hence makes it more difficult to activate the parasitic bipolar transistors. Reducing the gains of the bipolar transistors makes it difficult to sustain a latchup event, while completely decoupling the parasitic transistors ensures no PNPN path exists and thereby inhibits the SEL.

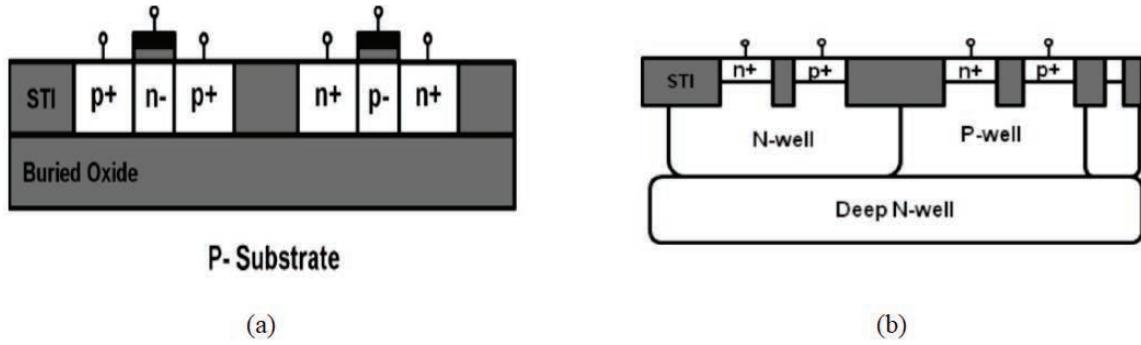


Fig. 38. (a) Cross-section of a floating-body CMOS SOI technology where the PMOS and NMOS transistors are dielectrically isolated from one another and hence is immune to latchup, and (b) cross-section of a triple well technology that has been shown to improve SEL hardness, after [Do12]

In SOI technology, the PMOS and NMOS transistors are dielectrically isolated from one another by the shallow trench isolation (STI) and the buried oxide and thus have been reported to be completely immune to latchup due to the absence of PNPN path [Mu96], [Sc03]. Fig. 38(a) shows a cross-section of a floating body SOI technology. However, it should be noted that there are other SOI processes such as the BiCMOS SOI which use deep trench isolation and hence the PMOS and NMOS devices are not dielectrically isolated (as the digital devices are typically separated by STI or LOCOS that does not extend down to the buried oxide) [Do12].

Triple well technology is another approach that has been shown to improve SEL hardening [Ga07] (Fig. 38(b)). Since most devices are fabricated in a p- substrate, triple well is often referenced as an n buried layer or a deep N-well (DNW). The introduction of the DNW reduces the PNP base resistance and hence is claimed to improve SEL robustness [Ga07]. This reduction can be significant as DNWs tend to have much lower sheet resistances than standard N-wells and because a blanket DNW provides parallel paths to many N-well contacts. However, other works claim that, depending on the test conditions under which the processes are compared, either dual well or triple well structures can be more susceptible to electrically-induced latchup [Ko06]. This is because, while DNW decreases the base resistance and the gain of the PNP transistor, which promotes latchup robustness, it also increases the base resistance and the gain of the NPN transistor, which promotes latchup susceptibility [Ko06], [Do12]. In [Do12], neutron-induced SEL in dual and triple-well SRAMs fabricated in a 130-nm process were compared and it was shown that the triple-well SRAMs were much more robust to SEL. Furthermore, the authors of [Do12] claim that immunity to neutron-induced SEL will likely be achieved at room temperature in any triple-well IC that is fabricated in a 130 nm or newer technology node with $V_{DD} \leq 1.2$ V and substrate resistivity ≤ 8 ohm-cm as process-level latchup robustness has improved in CMOS since the 180 nm technology node [Bo05] and since latchup becomes less problematic as supply voltages shrink and as substrate resistivity decreases. It should be noted that more recent studies have indicated that the switch to a 3-D geometry for bulk FinFETs in advanced technology nodes has resulted in increased parasitic BJT gain products, re-establishing electrical- and radiation-induced latchup as a significant reliability concern [Da17], [Ka18], and [Ba21]. It remains to be seen how effective triple-well will be in advanced bulk FinFET processes.

Another widely used latchup mitigation technique is the increased frequency and density of well-contacts thereby reducing well resistances. By keeping these resistances low, transient

currents will not be able to produce a potential drop large enough to activate the parasitic BJT and thus mitigate SEL [Do10]. In [Do10], radiation-induced SEL was studied on SRAMs fabricated in a 45-nm CMOS process with two different well contact densities. In one case (1X) the standard N-well and P-well contact densities were used and in another (8X) contacts were selectively removed, so that the highest resistance to the contacts is eight times larger than it is in the 1X SRAM. Heavy ion SEL response of the circuits at 80 °C is shown in Fig. 39(a). As can be observed from Fig. 39(a), the 8X SRAM is far more susceptible to SEL and has a much lower LET threshold for SEL than the 1X SRAM, highlighting that ICs with more densely contacted wells are less susceptible to SEL [Do10].

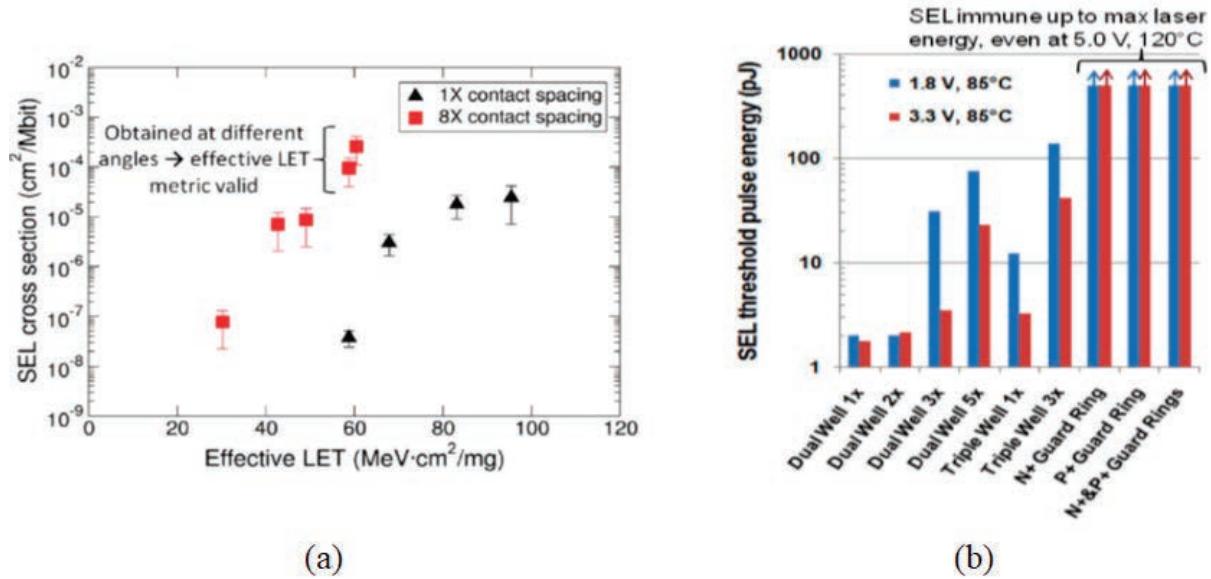


Fig. 39. (a) Heavy ion SEL cross sections of the 1X and 8X contact spacing SRAMs at 80 °C. The 8X SRAM, which has fewer N-well and P-well contacts, is far more susceptible to SEL., after [Do10] and (b) SEL threshold pulse energies at the strike location for several layout/process variations of test structures; “1X” represents the minimum allowable n⁺ to p⁺ source spacing, after [Do12]

Guard rings is another commonly used approach to overcome SEL. They reduce the risk of latchup through increased electrical and spatial isolation and are very effective at keeping the wells pinned to the appropriate potentials thus reducing or eliminating the probability of the parasitic BJT to turn ON. In [Do12], test structures with n⁺ guard rings surrounding p⁺ sources, p⁺ guard rings surrounding n⁺ sources and a third structure with both n⁺ and p⁺ guard rings were implemented in a 180-nm CMOS process and studied using pulsed laser tests. Pulsed laser testing is an optical method of radiation testing that uses pico-Joule or nano-Joule energy lasers to generate electron-hole pairs. This type of testing can help identify the mechanisms responsible for SEEs by injecting charge into specific SEE-sensitive nodes (as the laser light can be focused to a spot with a diameter less than 1 μm) and then observing the circuit or device response [Bu13]. All guard ring structures were shown to be immune to the maximum laser energy (equivalent to > 100 MeV-cm²/mg) at 120 °C. Fig. 39(b) summarizes these results.

7. Challenges and Opportunities for SEE Hardening

7.1 Scaling Trends

In this section we will review some of the challenges and opportunities for SEE hardening with technology scaling and briefly discuss the future outlook. The critical charge needed to flip a memory bit reduced by $\sim 30\%$ per generation in older technologies, while in sub-100-nm the reduction in Q_{crit} started to slow down [Se15], [Ko21]. This can be attributed to reduction in the voltage scaling as well as the performance gains achieved by innovations such as strained Si, high-K metal gate, and FinFET technologies that helped increase the drive strength, limiting degradation in Q_{crit} . Fig. 40(a) shows the evolution of Q_{crit} as a function of channel length (l) indicating a slowdown in the Q_{crit} scaling around 0.5 fC [Ko21]. The solid and dashed lines in Fig. 40(a) are based on trends predicted by Peterson [Pe82] and Pickett [Pi82] in 1982. On the other hand, the bit-cell area and hence the sensitive area continues to reduce with technology as shown in Fig. 40(b). The combined effect of these trends results in the per-bit SER and the per-bit saturated SEU cross-section to reduce with technology scaling. The reduction in the per-bit SER is proportional to the bit-cell area scaling within planar nodes. Technology scaling from planar to FinFETs resulted in large reductions in the SEU sensitivities as the transistor structure changed from planar to finFET [Se12], [Le15], [Se15], [Na15], [Fa16], [Na18], [Na21]. This has been attributed to a reduction in the sensitive cross-section area of individual transistors in the FinFET process, resulting in improved per-bit SEU performance, especially for nominal supply voltage operation. Subsequent work showed that scaling within FinFET processes from the 16-nm FinFET node to the 7-nm FinFET node resulted in SER reduction proportional to the bit-cell area scaling [Na18]. For all process nodes up to the 7-nm FinFET node, scaling has resulted in a decrease in per-bit SER.

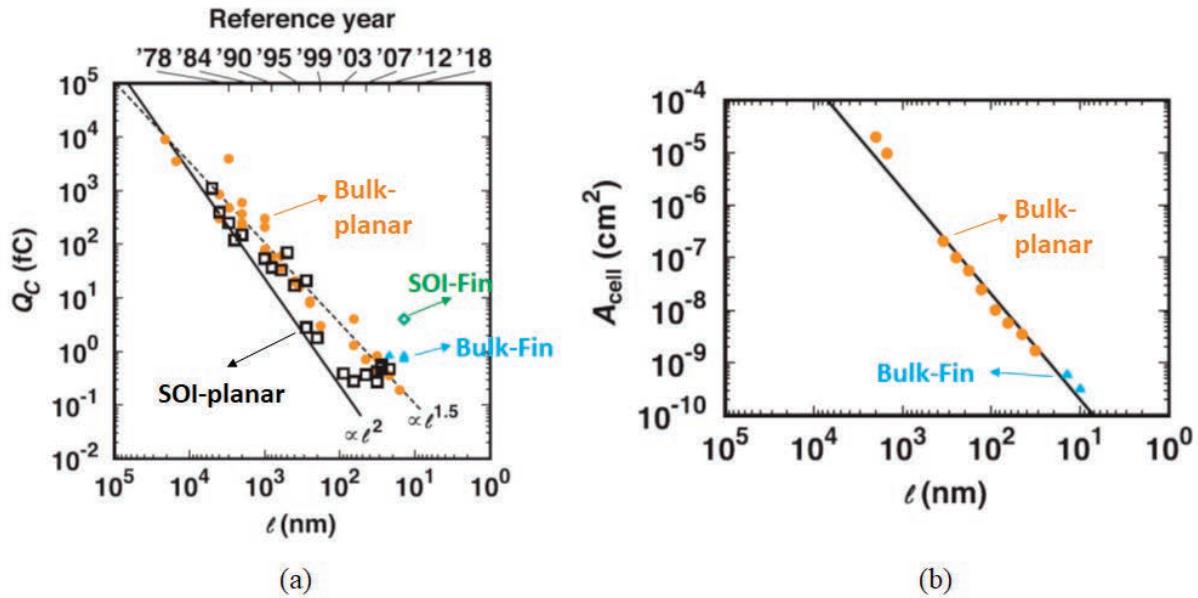


Fig. 40. (a) Scaling of Q_{crit} , and (b) SRAM bit-cell area scaling, after [Ko21]

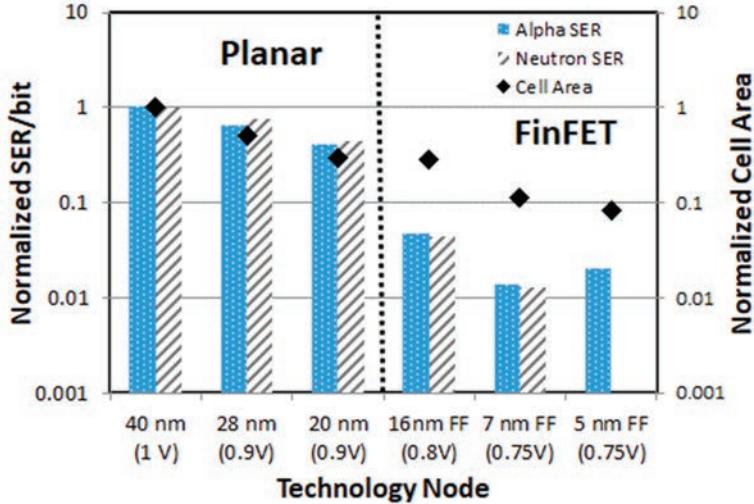


Fig. 41. Normalized scaling trends in the per-bit alpha and neutron SER of SRAMs as a function of technology node; Secondary y-axis shows the normalized SRAM bit cell area comparison, after [Na21].

Fig. 41 plots the normalized per-bit alpha and neutron SER of SRAMs from planar nodes down to the 5-nm FinFET node [Na21]. Alpha and neutron SER data of every process node is normalized to the neutron SER of the 40-nm process. Alpha SER data for each node was calculated for a package alpha emission rate of 0.002 cph/cm² and neutron SER is based on sea-level NYC neutron flux of 14 nph/cm². The secondary y-axis shows the normalized bit-cell area with technology scaling. As can be observed from Fig. 41, scaling from planar to FinFET processes offered a significant improvement in the per-bit SER as the geometry changed from planar to 3-D FinFET that helped reduce the sensitive cross-section area due to the narrow fin structure while keeping the nodal capacitances comparable. Within the planar processes, the SER reduction was approximately proportional to the bit-cell area reduction. Similar trend is observed when scaling from the 16-nm FinFET process to the 7-nm FinFET process. This trend is due to the scaling of sensitive area within the bit-cell in proportion to the overall bit-cell area. However, scaling from the 7-nm FinFET node to the 5-nm FinFET node, the per-bit alpha SER shows an increase for the first time. In [Na21], authors attribute this to a reduction in the Q_{crit} of the 5-nm FinFET process relative to 7-nm FinFET. The result highlights that variations in Fin geometries and doping profiles could alter the node capacitances and drive strength of the transistors which affect the Q_{crit} and hence the SER scaling trends in advanced FinFET processes. Mitigation techniques will need to account for such changes in SEU trends for different digital circuits, as the classical trend of an improvement in the per-bit SEU rate with each new process generation may no longer hold true.

Fig. 42 plots the scaling trends in the saturated per-bit SRAM SEU cross-section (denoted by σ_∞) as a function of the channel length (l) for bulk-planar, bulk SOI and bulk finFET devices [Ko21]. As can be observed, the SRAM SEU cross-section reduction with scaling follows the bit-cell area scaling trend (represented by the solid line in Fig. 42). The saturated SEU cross-section of bulk-planar SRAMs, especially in the sub 100-nm nodes, exceeds the cell area trend line and in [Ko21] this is attributed to the increase in MCU rates in bulk-planar devices. On the other hand, the saturated cross-section of SOI SRAMs are largely within the cell area bound across generations. This is attributed to the fact that the buried oxide in SOI keeps transistors electrically

isolated, minimizing charge sharing and mitigating MCUs. The buried oxide in SOI also helps limit the charge collection at the struck node. Thus SEU rates of SOI SRAM at the same process geometry are typically better than those of bulk devices as can be observed in Fig. 42. On the other hand, bulk-finFETs have provided significant reduction in the SEU rates relative to bulk-planar as discussed earlier and the bulk-Fin data point in Fig. 42 was observed to have a saturated SEU cross-section lower than the bit-cell area and is in line with conventional SOI SRAM trends. In [Ko21], the author indicates that this SOI-like response of bulk-Fin is likely due to the narrow-fin effect which helps increase the transistor-substrate resistance and helps mitigate substrate charge sharing, thereby reducing probability of MCUs (as was also observed in data presented earlier in this chapter under memory SEU hardening section).

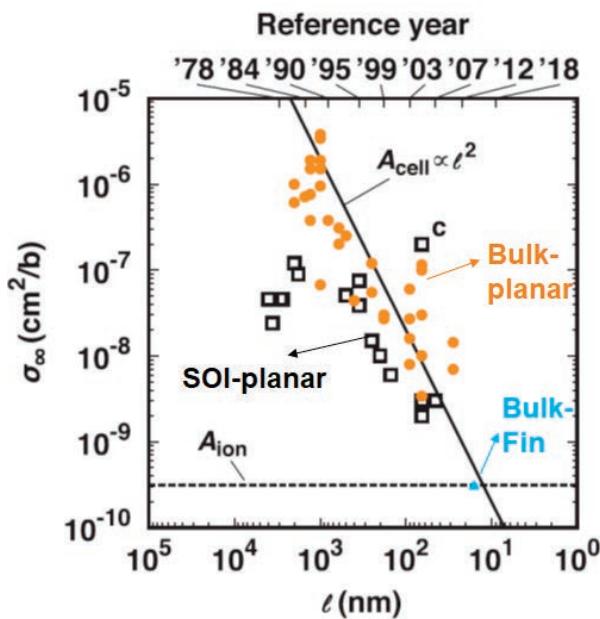


Fig. 42. Saturated per-bit SEU cross-section with scaling, after [Ko21]. Solid line represents the SRAM cell area scaling and the dotted line represents the area of an ion track.

7.2 Bias Dependence of SEU

One of the major design challenge for the electronic industry is the overall power dissipation of ICs. The Semiconductor Industry Association (SIA) roadmap and the recent 2020 International Roadmap for Devices and Systems (IRDS) have identified power dissipation as one of the key reliability concerns for electronic systems [IRDS]. Since power dissipation is proportional to V_{DD}^2 , system-level designers have resorted to reducing the supply voltage to reduce power. On the other hand, compared to planar technologies, FinFET technology has better stability and current drive at reduced supply voltages as the gate controls the channel from three-sides. This has enabled FinFET transistors to have stable operation at low voltages, which is essential for many power sensitive applications. Thus it is important to understand the SEU sensitivities at low voltages especially for FinFET processes.

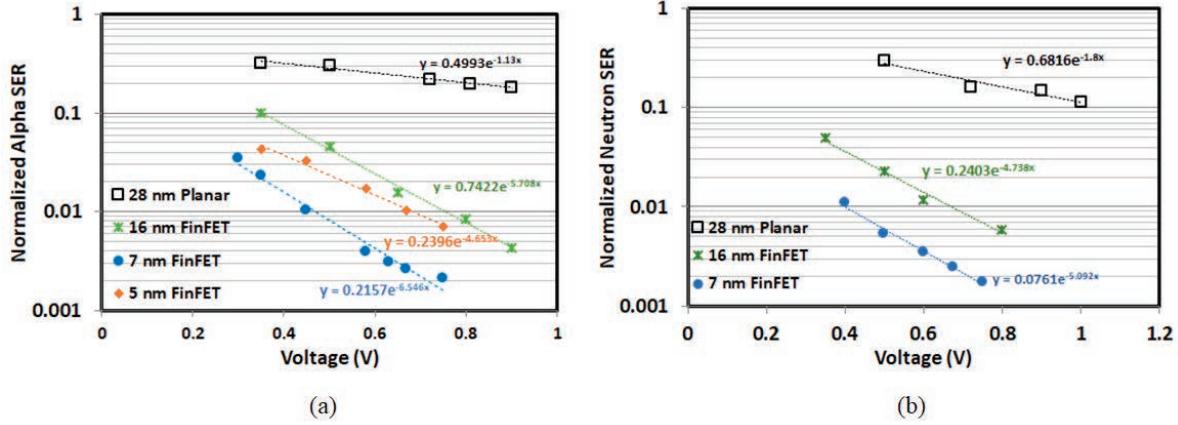


Fig. 43. Bias dependence of the (a) per-bit alpha particle SRAM SER and (b) per-bit neutron SRAM SER, for planar and FinFET processes, after [Na21]

Fig. 43(a) plots the bias dependence in the per-bit alpha particle SER of SRAMs as a function of supply voltage for 28-nm planar, 16-nm FinFET, 7-nm FinFET and the 5-nm FinFET processes [Na21]. Note that the y-axis of Fig. 43(a) is in log scale. As can be observed, SER for all FinFET processes exhibit a strong exponential dependence on the supply voltage, while the planar process node exhibits a weak exponential dependence that may also be modeled by a linear trend line. (FinFET processes' SER data do not fit a linear trend line.) This indicates that the single-event mechanisms are similar for FinFET processes but different from that of planar processes. Differences in Q_{crit} and Q_{coll} trends between planar and FinFET processes have been shown to result in the strong exponential dependence of SEU on the supply voltage for FinFET processes [Na15], [Na18], [Na21].

Fig. 43(b) shows the bias dependence of the neutron SRAM SER for the 28-nm planar process along with 16-nm and 7-nm FinFET processes. Similar to the alpha-particle data, the FinFET processes are observed to have a stronger exponential bias dependence compared to that for the planar process node which has a weak exponential, or linear, trend. The data indicates that for FinFET technologies, SER assessment and mitigation approaches must take into consideration the lowest operating bias for the given application.

7.3. Implications for System-Level SEU Rates

While the per-bit SER has largely shown an improvement with technology scaling to FinFET processes, as more functionality is added, the density and size of chip designs continue to increase which tend to offset the per-bit SEU improvements. Fig. 44(a) illustrates the normalized per-bit SER trend as a function of technology node along with the chip or system-level SER trends assuming a 2 \times and 4 \times increase in the density at each new generation. This clearly shows that at the system-level the benefits of per-bit SEU improvement with scaling will be diminished. For example, assuming a 4 \times increase in the density of memory per node, the system-level SER of 28-nm planar is comparable to that of the 16-nm FinFET at their respective nominal operating voltage. Furthermore, the stronger SEU bias dependence of FinFET processes could exacerbate the system-level SER difference at low voltage operation. For instance, the system-level SER of a 16-nm FinFET process increases by ~2 \times with a 20% reduction in operating voltage, while that of a 28-nm planar increases only by ~15% for a similar rate of supply voltage reduction as shown in Fig.

44(b). Such trends may pose a challenge for SEU hardening as hardening techniques need to account for the lowest operating and standby voltage for the intended application including supply tolerance.

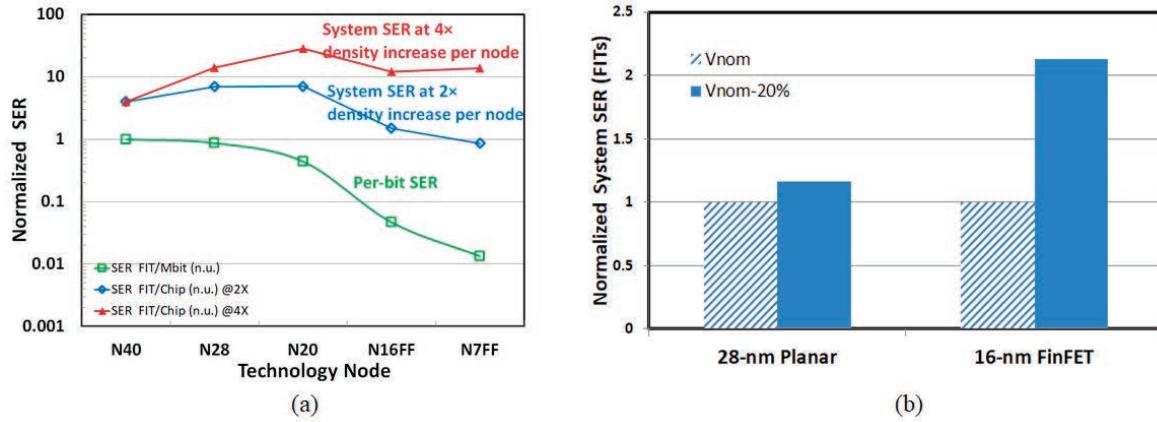


Fig. 44. (a) Illustration of the per-bit and system-level SER trends and (b) normalized system-level SER at nominal and 20% below nominal V_{DD} for 28-nm planar and 16-nm FinFET processes

7.4. Future Outlook

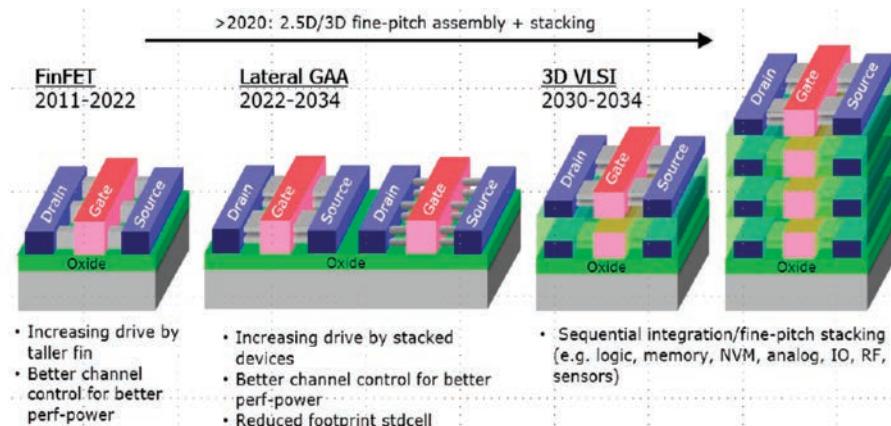


Fig. 45. Evolution of device architecture based on the 2020 IRDS More Moore Roadmap, after [IRDS]

The 2020 IRDS More Moore Roadmap [IRDS] projects technology scaling to an equivalent feature size of 0.7-nm in 2034 with gate-all-around (GAA) and 3D device stacking as illustrated in Fig. 45. The roadmap also indicates muon-induced SER to be one of the long term reliability challenges with scaling. The recent 5-nm FinFET SER data showed that technology scaling may no longer provide the expected reduction in the per-bit SEU rate and further reductions in Q_{crit} may make circuits more sensitive to very low-LET particles, including muons. With chip power scaling continuing to be the number one key reliability challenge, and with GAA devices providing better gate control of the channel potentially allowing for lower voltage operation compared to current generation of technologies, system-level SEU rates could see an increase. SEU hardening techniques will thus continue to be an important design aspect for not just space applications but

for most terrestrial applications as well. On the other hand, GAA and 3D stacking may pave the way for novel SEU hardening approaches that may not have been possible in the current processes.

8. Summary

In this short course we reviewed a wide range of traditional and novel SE hardening-by-design approaches for digital circuits including memory, latches, and logic. The choice of the hardening technique will depend on many factors such as the intended application, environment of operation, operating voltage range and the target SEU rate. ECC techniques are effective protection for most memories when combined with appropriate bit interleaving and scrubbing techniques. Traditional redundancy-based approaches for latch and logic circuits such as DICE and TMR provide best SEU rates though the performance penalties are relatively high. Novel hardening schemes such as hysteresis, charge-steering latch designs as well as targeted hardening of critical blocks have low performance penalty with good SEU rate improvements. These are attractive alternatives for terrestrial and select commercial space designs. Guard rings as well as certain SOI processes are effective in mitigating the threat of SEL. Technology scaling from planar processes to FinFETs provides good per-bit SEU rate reduction at nominal operating voltage, while FinFETs exhibit an exponential SEU increase at lower operating voltages. SEU hardening techniques should hence account for the lowest operating voltage for the intended application. The SEU improvements with scaling may get diminished at the system level with increase in density and size of the IC.

9. Acknowledgements

I thank Prof. Bharat Bhuva, Prof. Ronald Schrimpf, Prof. Robert Reed and all the Professors at Vanderbilt University's Radiation Effects and Reliability group with whom I have had the privilege of collaborating on many SEE topics over the past decade and had many useful discussions on radiation effects. I would also like to thank all my colleagues at Broadcom for their invaluable help and support.

10. References

- [Ah10] J. R. Ahlbin *et al.*, "Effect of multiple-transistor charge collection on SET pulse widths," *IEEE International Reliability Physics Symposium*, pp. 198-202, 2010.
- [Ar10] C. A. Argyrides, P. Reviriego, D. K. Pradhan, and J. A. Maestro, "Matrix-based codes for adjacent error correction," *IEEE Trans. Nucl. Sci.*, vol. 57, no. 4, pp. 2106–2111, 2010.
- [Ba03] J. L. Barth, C. S. Dyer and E. G. Stassinopoulos, "Space, atmospheric, and terrestrial radiation environments," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 3, pp. 466-482, June 2003.
- [Ba05a] R. C. Baumann, "Single event effects in advanced CMOS Technology," in *Proc. IEEE Nuclear and Space Radiation Effects Conf. Short Course Text*, 2005.
- [Ba05b] R. C. Baumann, "Radiation-induced soft errors in advanced semiconductor technologies," *IEEE Trans. Device Mater. Reliab.*, vol. 5, no. 3, pp. 305–316, Sep. 2005.
- [Ba07] M. A. Bajura *et al.*, "Models and Algorithmic Limits for an ECC-Based Approach to Hardening Sub-100-nm SRAMs," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 4, pp. 935-945, Aug. 2007.

- [Ba21] D. R. Ball *et al.*, "Single-Event Latchup in a 7-nm Bulk FinFET Technology," *IEEE Trans. Nucl. Sci.*, 2021 (pre-print).
- [Bi75] D. Binder, E. C. Smith and A. B. Holman, "Satellite Anomalies from Galactic Cosmic Rays," *IEEE Trans. Nucl. Sci.*, vol. 22, no. 6, pp. 2675-2680, Dec. 1975.
- [Bl05] J. D. Black, A. L. Sternberg, M. L. Alles, A. F. Witulski, B. L. Bhuva, L. W. Massengill, J. M. Benedetto, M. P. Baze, J. L. Wert, and M. G. Hubert, "HBD layout isolation techniques for multiple node charge collection mitigation," *IEEE Trans. Nucl. Sci.*, vol. 52, no. 6, pp. 2536-2541, Dec. 2005.
- [Bl13] J. D. Black, P. E. Dodd and K. M. Warren, "Physics of Multiple-Node Charge Collection and Impacts on Single-Event Characterization and Soft Error Rate Prediction," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 3, pp. 1836-1851, June 2013.
- [Bo05] G. Boselli, V. Reddy, and C. Duvvury, "Latch-up in 65 nm CMOS technology: A scaling perspective," in *Proc. Int. Reliab. Phys. Symp.*, pp. 137-144, Apr. 2005.
- [Br96] G. Bruguier and J-M. Palau, "Single Particle-Induced Latchup," *IEEE Trans. Nucl. Sci.*, vol. 43, pp. 522-532, April 1996.
- [Bu01] S. Buchner and M. Baze, "Single-event transients in fast electronic circuits," in *Proc. IEEE Nuclear and Space Radiation Effects Conf. Short Course Text*, 2001.
- [Bu13] S. P. Buchner, F. Miller, V. Pouget and D. P. McMorrow, "Pulsed-Laser Testing for Single-Event Effects Investigations," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 3, pp. 1852-1875, June 2013.
- [Ca96] T. Calin, M. Nicolaidis and R. Velazco, "Upset hardened memory design for submicron CMOS technology," *IEEE Trans. Nucl. Sci.*, vol. 43, no. 6, pp. 2874-2878, Dec. 1996.
- [Ch84] C. L. Chen and M. Y. Hsiao, "Error-Correcting Codes for Semiconductor Memory Applications: A State-of-the-Art Review," *IBM Journal of Research and Development*, vol. 28, no. 2, pp. 124-134, March 1984.
- [Da07] S. DasGupta, A. F. Witulski, B. L. Bhuva, M. L. Alles, R. A. Reed, O. A. Amusan, J. R. Ahlbin, R. D. Schrimpf, L. W. Massengill, "Effect of Well and Substrate Potential Modulation on Single Event Pulse Shape in Deep Submicron CMOS," *IEEE Trans. Nucl. Sci.*, vol. 54, pp. 2407-2412, Dec. 2007.
- [Da14] I. A. Danilov, M. S. Gorbunov and A. A. Antonov, "SET Tolerance of 65 nm CMOS Majority Voters: A Comparative Study," *IEEE Trans. Nucl. Sci.*, vol. 61, no. 4, pp. 1597-1602, Aug. 2014.
- [Da17] C.-T. Dai, S.-H. Chen, D. Linten, M. Scholz, G. Hellings, R. Boschke, J. Karp, M. Hart, G. Groeseneken, M.-D. Ker, A. Mocuta, and N. Horiguchi, "Latchup in Bulk FinFET Technology," *Proc. IEEE Int. Rel. Symp. (IRPS)*, pp. EL-1.1-EL1.3, Apr. 2017.
- [Do03] P. E. Dodd and L. W. Massengill, "Basic Mechanisms and Modeling of Single-Event Upset in Digital Microelectronics," *IEEE Trans. Nucl. Sci.*, vol. 50, pp. 583-602, 2003.
- [Do10] N. A. Dodds *et al.*, "Selection of Well Contact Densities for Latchup-Immune Minimal-Area ICs," *IEEE Trans. Nucl. Sci.*, vol. 57, no. 6, pp. 3575-3581, Dec. 2010.
- [Do12] N. A. Dodds *et al.*, "Effectiveness of SEL Hardening Strategies and the Latchup Domino Effect," *IEEE Trans. Nucl. Sci.*, vol. 59, no. 6, pp. 2642-2650, Dec. 2012.
- [Eeti] Soft errors cause network outage. <https://www.eetimes.com/sram-soft-errors-cause-hard-network-problems/#>
- [Fa16] Y. Fang and A. S. Oates, "Characterization of Single Bit and Multiple Cell Soft Error Events in Planar and FinFET SRAMs," *IEEE Trans. Dev. Mat. Rel.*, vol. 16, no. 2, pp. 132-137, June 2016.

- [Forb] Cosmic-ray induced upsets in Servers.
<https://www.forbes.com/forbes/2000/1113/6613068a.html?sh=47c655726162>
- [Ga07] G. Gasiot, D. Giot, and P. Roche, "Multiple cell upsets as the key contribution to the total SER of 65 nm CMOS SRAMs and its dependence on well engineering," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, pp. 2468–2473, Dec. 2007.
- [Ha50] R. W. Hamming, "Error detecting and error correcting codes," *Bell System Technical Journal*, 29 (2): 147–160, 1950.
- [Ha00] P. Hazucha and C. Svensson, "Impact of CMOS Technology Scaling on the Atmospheric Neutron Soft Error Rate," *IEEE Tran. Nucl. Sci.*, vol. 47, no. 6, pp. 2586–2594, Dec. 2000.
- [Ha09] D. L. Hansen *et al.*, "Clock, Flip-Flop, and Combinatorial Logic Contributions to the SEU Cross Section in 90 nm ASIC Technology," *IEEE Trans. Nucl. Sci.*, vol. 56, no. 6, pp. 3542-3550, Dec. 2009.
- [Ha12] R. Harada, S. Abe, H. Fuketa, T. Uemura, M. Hashimoto and Y. Watanabe, "Angular Dependency of Neutron-Induced Multiple Cell Upsets in 65-nm 10T Subthreshold SRAM," *IEEE Trans. Nucl. Sci.*, vol. 59, no. 6, pp. 2791-2795, Dec. 2012.
- [Ha15] A. Hasanbegovic and S. Aunet, "Supply Voltage Dependency on the Single Event Upset Susceptibility of Temporal Dual-Feedback Flip-Flops in a 90 nm Bulk CMOS Process," *IEEE Trans. Nucl. Sci.*, vol. 62, no. 4, pp. 1888-1897, Aug. 2015.
- [Ha16] A. Hasanbegović and S. Aunet, "Heavy Ion Characterization of Temporal-, Dual- and Triple Redundant Flip-Flops Across a Wide Supply Voltage Range in a 65 nm Bulk CMOS Process," *IEEE Trans. Nucl. Sci.*, vol. 63, no. 6, pp. 2962-2970, Dec. 2016.
- [Hi00] D. Hisamoto et al., "FinFET-a self-aligned double-gate MOSFET scalable to 20 nm," *IEEE Trans. Elec. Dev.*, vol. 47, no. 12, pp. 2320-2325, Dec 2000.
- [Hs81] C. M. Hsieh, P. C. Murley, and R. R. O'Brien, "A field-funneling effect on the collection of alpha-particle-generated carriers in silicon devices," *IEEE Elec. Dev. Let.*, vol. 2, pp. 103–105, Dec. 1981.
- [Inde] Cosmic ray upsets causing election and plane autopilot issues.
<https://www.independent.co.uk/news/science/subatomic-particles-cosmic-rays-computers-change-elections-planes-autopilot-a7584616.html>
- [IRDS] The International Roadmap for Devices and Systems (IRDS) More Moore Roadmap, 2020.
- [Jo96] A. H. Johnston, "The influence of VLSI technology evolution on radiation-induced latchup in space systems," *IEEE Trans. Nucl. Sci.*, vol. 43, no. 2, pp. 505–521, Apr. 1996.
- [Ka07] F. L. Kastensmidt, "SEE Mitigation Strategies for Digital Circuit Design Applicable to ASIC and FPGAs," in *Proc. IEEE Nuclear and Space Radiation Effects Conf. Short Course Text*, 2007.
- [Ka18] J. Karp, M.J. Hart, P. Maillard, G. Hellings, and D. Linten, "Single-Event Latchup : Increased Sensitivity from Planar to FinFET," *IEEE Trans. Nucl. Sci.*, vol. 65, no. 1, pp. 217-222, Jan. 2018.
- [Ke88] S. E. Kerns *et al.*, "The design of radiation-hardened ICs for space: a compendium of approaches," *Proc. of the IEEE*, vol. 76, no. 11, pp. 1470-1509, Nov. 1988.
- [Ko96] S. Kozu, M. Daito, Y. Sugiyama, H. Suzuki, H. Morita, M. Nomura, K. Nadehara, S. Ishibuchi, M. Tokuda, Y. Inoue, T. Nakayama, H. Harigai, Y. Yano, "A 100MHz, 0.4W RISC Processor with 200MHt Multiply-Adder, using Pulse Register Technique," Proc. IEEE ISSCC, pp. 140-141, 1996.

- [Ko06] D. Kontos, K. Domanski, R. Gauthier, K. Chatty, M. Muhammad, C. Seguin, R. Halbach, C. Russ, and D. Alvarez, "Investigation of external latchup robustness of dual and triple well designs in 65 nm bulk CMOS technology," in *Proc. Int. Reliab. Phys. Symp.*, pp. 145–150, 2006.
- [Ko21] D. Kobayashi, "Scaling Trends of Digital Single-Event Effects: A Survey of SEU and SET Parameters and Comparison With Transistor Performance," *IEEE Trans. Nucl. Sci.*, vol. 68, no. 2, pp. 124-148, Feb. 2021.
- [Ku12] K. J. Kuhn, "Considerations for Ultimate CMOS Scaling," *IEEE Trans. Elec. Dev.*, vol. 59, no. 7, pp. 1813-1828, July 2012.
- [Le05] M. L. Lee, E. A. Fitzgerald, M. T. Bulsara, M. T. Currie, and A. Lochtefeld, "Strained Si, SiGe, and Ge channels for high mobility MOSFETs," *J. Appl. Phys.*, vol. 97, no. 1, Jan 2005.
- [Le10] H. K. Lee et al., "LEAP: Layout design through error-aware transistor positioning for soft-error-resilient sequential cell design," *IEEE Int. Reliability Physics Symp.*, pp. 203–212, 2010.
- [Le11] H. K. Lee, K. Lilja, M. Bounasser, I. Linscott and U. Inan, "Design Framework for Soft-Error-Resilient Sequential Cells," *IEEE Transactions on Nuclear Science*, vol. 58, no. 6, pp. 3026-3032, Dec. 2011.
- [Le15] S. Lee, I. Kim, S. Ha, C. Yu, J. Noh, S. Pae, and J. Parket, "Radiation-Induced Soft Error Rate Analyses for 14 nm FinFET SRAM Devices," *IEEE Intl. Rel. Phy. Sym.*, pp. 4B1.1-4B1.4, 2015.
- [Ma78] T. C. May and M. H. Woods, "A New Physical Mechanism for Soft Errors in Dynamic Memories," *IEEE Intl. Rel. Phys. Symp.*, pp. 33-40, 1978.
- [Ma02] D. G. Mavis and P. H. Eaton, "Soft error rate mitigation techniques for modern microcircuits," *IEEE Intl. Rel. Phys. Symp. Proc.*, pp. 216-225, 2002.
- [Mi05] S. Mitra, N. Seifert, M. Zhang, Q. Shi and K. S. Kim, "Robust system design with built-in soft-error resilience," *IEEE Computer*, vol. 38, no. 2, pp. 43-52, Feb. 2005.
- [Mi07] K. Mistry et al., "A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free Packaging," *Proc. IEEE Intl. Electron Devices Mtg*, pp. 247-250, 2007.
- [Mo65] G. E. Moore, "Cramming more components onto integrated circuits," *Electronics*, vol 38, no. 8, pp. 114-117, Apr. 1965.
- [Mu96] O. Musseau, "Single-event effects in SOI technologies and devices," *IEEE Trans. Nucl. Sci.*, vol. 43, no. 2, pp. 603–613, Apr. 1996.
- [Na08] B. Narasimham, J. W. Gambles, R. L. Shuler, B. L. Bhuva and L. W. Massengill, "Quantifying the Effect of Guard Rings and Guard Drains in Mitigating Charge Collection and Charge Spread," *IEEE Trans. Nucl. Sci.*, vol. 55, no. 6, pp. 3456-3460, Dec. 2008.
- [Na12] B. Narasimham et al., "A Hysteresis-Based D-Flip-Flop Design in 28 nm CMOS for Improved SER Hardness at Low Performance Overhead," *IEEE Trans. Nucl. Sci.*, vol. 59, no. 6, pp. 2847-2851, Dec. 2012.
- [Na13] B. Narasimham et al., "Evaluation of logic SER for a network processor and the use of targeted hardening to improve system SER performance," *IEEE Intl Rel Phys Symp (IRPS)*, pp. 3D.2.1-3D.2.5, 2013.
- [Na15] B. Narasimham, S. Hatami, A. Anvar, D. M. Harris, A. Lin, J. K. Wang, I. Chatterjee, K. Ni, B. L. Bhuva, R. D. Schrimpf, R. A. Reed, M. W. McCurdy, "Bias Dependence of Single-Event Upsets in 16 nm FinFET D-Flip-Flops," *IEEE Trans. Nucl. Sci.*, vol. 62, pp. 2578-2584, 2015.

- [Na17] B. Narasimham, K. Chandrasekharan, J. K. Wang, K. Ni, B. L. Bhuva and R. D. Schrimpf, "Charge-Steering Latch Design in 16 nm FinFET Technology for Improved Soft Error Hardness," *IEEE Trans. Nucl. Sci.*, vol. 64, no. 1, pp. 353–358, Jan. 2017.
- [Na18] B. Narasimham, S. Gupta, D. Reed, J. K. Wang, N. Hendrickson, H. Taufique, "Scaling Trends and Bias Dependence of the Soft Error Rate of 16 nm and 7 nm FinFET SRAMs," *IEEE Intl Rel Phys Symp*, 2018.
- [Na19] B. Narasimham, K. Chandrasekharan, J. K. Wang and B. L. Bhuva, "Soft Error Performance of High-Speed Pulsed-DICE-Latch Design in 16 nm and 7 nm FinFET Processes," *IEEE Intl. Rel. Phys. Symp.*, pp. 1-4, 2019.
- [Na21] B. Narasimham et al., "Scaling Trends in the Soft Error Rate of SRAMs from Planar to 5-nm FinFET," *IEEE Intl. Rel. Phys. Symp.*, 2021.
- [Ne05] G. Neuberger, F. de Lima, L. Carro, and R. Reis, "An automatic technique for optimizing reed-solomon codes to improve fault tolerance in memories," *IEEE Design Test of Comput.*, vol. 22, no. 1, pp. 50–58, Jan. 2005.
- [Ni08] M. Nicolaidis, R. Perez and D. Alexandrescu, "Low-Cost Highly-Robust Hardened Cells Using Blocking Feedback Transistors," *IEEE VLSI Test Symposium*, pp. 371-376, 2008.
- [Nu05] G. Neuberger, F. de Lima, L. Carro, and R. Reis, "An automatic technique for optimizing reed-solomon codes to improve fault tolerance in memories," *IEEE Design Test of Comput.*, vol. 22, no. 1, pp. 50–58, 2005.
- [Pe82] E. L. Petersen, P. Shapiro, J. H. Adams, and E. A. Burke, "Calculation of cosmic-ray induced soft upsets and scaling in VLSI devices," *IEEE Trans. Nucl. Sci.*, vol. NS-29, no. 6, pp. 2055–2063, Dec. 1982.
- [Pi82] J. C. Pickel, "Effect of CMOS miniaturization on cosmic-ray-induced error rate," *IEEE Trans. Nucl. Sci.*, vol. NS-29, no. 6, pp. 2049–2054, Dec. 1982.
- [Ra09] A. Rastogi, M. Agarawal and B. Gupta, "SEU MITIGATION-using 1/3 rate convolution coding," *IEEE Intl. Conf. Comp. Sci. and Inf. Tech.*, pp. 180-183, 2009.
- [Re97] R. A. Reed *et al.*, "Heavy ion and proton-induced single event multiple upset," *IEEE Trans. Nucl. Sci.*, vol. 44, no. 6, pp. 2224-2229, Dec. 1997.
- [Sa90] A. M. Saleh, J. J. Serrano, and J. H. Patel, "Reliability of scrubbing recovery-techniques for memory systems," *IEEE Trans. Reliab.*, vol. 39, no. 1, pp. 114–122, Apr. 1990.
- [Sa06] Y. Sasaki, K. Namba, H. Ito, "Soft Error Masking Circuit and Latch Using Schmitt Trigger Circuit," *IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, pp. 327-335, 2006.
- [Sc03] J. R. Schwank, V. Ferlet-Cavrois, M. R. Shaneyfelt, P. Paillet, and P. E. Dodd, "Radiation effects in SOI technologies," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 3, pp. 522–538, Jun. 2003.
- [Se03] F. W. Sexton, "Destructive single-event effects in semiconductor devices and ICs," *IEEE Trans. Nucl. Sci.*, vol. 50, pp. 603 – 621, June 2003.
- [Se04] N. Seifert, and N. Tam, "Timing Vulnerability Factors of Sequential," *IEEE Trans. Dev. and Mat. Rel.*, pp. 516-522, 2004.
- [Se06] N. Seifert *et al.*, "Radiation-Induced Soft Error Rates of Advanced CMOS Bulk Devices," *IEEE Intl. Rel. Phy. Symp. Proc.*, pp. 217-225, 2006.
- [Se10] N. Seifert *et al.*, "On the radiation-induced soft error performance of hardened sequential elements in advanced bulk CMOS technologies," *IEEE Intl. Rel. Phys. Symp.*, pp. 188-197, 2010.

- [Se12] N. Seifert, B. Gill, S. Jahanuzzaman, J. Basile, V. Ambrose, Q. Shi, R. Allmon, A. Bramnik, "Soft Error Susceptibilities of 22 nm Tri-Gate Devices," *IEEE Trans. Nucl. Sci.*, vol. 59, no. 6, pp. 2666–2673, Dec. 2012.
- [Se15] N. Seifert *et al.*, "Soft Error Rate Improvements in 14-nm Technology Featuring Second-Generation 3D Tri-Gate Transistors," *IEEE Trans. Nucl. Sci.*, vol. 62, no. 6, pp. 2570–2577, Dec. 2015.
- [Sh05] J. L. Shin, B. Petrick, M. Singh, and A. S. Leon, "Design and implementation of an embedded 512-kb level-2 cache subsystem," *IEEE J. Solid-State Circuits*, vol. 40, no. 9, pp. 1815–1820, Sep. 2005.
- [Sh08] Y. Shiyanovskii, F. Wolff and C. Papachristou, "SRAM Cell Design Protected from SEU Upsets," *IEEE International On-Line Testing Symposium*, pp. 169-170, 2008.
- [Sh12] X. She, N. Li and D. W. Jensen, "SEU Tolerant Memory Using Error Correction Code," *IEEE Trans. Nucl. Sci.*, vol. 59, no. 1, pp. 205-210, Feb. 2012.
- [Si20] M. S. M. Siddiqui, S. Ruchi, L. Van Le, T. Yoo, I. Chang and T. T. Kim, "SRAM Radiation Hardening Through Self-Refresh Operation and Error Correction," *IEEE Trans. Dev. Mat. Rel.*, vol. 20, no. 2, pp. 468-474, June 2020.
- [Sl05] C. W. Slayman, "Cache and memory error detection, correction, and reduction techniques for terrestrial servers and workstations," *IEEE Trans. Device Mater. Reliab.*, vol. 5, no. 3, pp. 397–404, Sep. 2005.
- [Ta95] A. H. Taber and E. Normand, "Investigation and characterization of SEU effects and hardening strategies in avionics," DNA-TR-94-123, Defense Nuclear Agency, Alexandria, VA, February 1995.
- [Ta09] H. J. Tausch, "Simplified birthday statistics and hamming EDAC," *IEEE Trans. Nucl. Sci.*, vol. 56, no. 2, pp. 474–478, Apr. 2009.
- [Ta15] N. Tam *et al.*, "Multi-cell soft errors at the 16-nm FinFET technology node," *IEEE Int'l. Rel. Phys. Symp. Proc.*, pp. 4B.3.1-4B.3.5, 2015.
- [Ti08] A. D. Tipton *et al.*, "Device-Orientation Effects on Multiple-Bit Upset in 65 nm SRAMs," *IEEE Trans. Nucl. Sci.*, vol. 55, no. 6, pp. 2880-2885, Dec. 2008.
- [Tsmc] Technology Scaling. https://www.tsmc.com/english/dedicatedFoundry/technology/logic/1_5nm
- [Wa09] K. M. Warren *et al.*, "Heavy Ion Testing and Single Event Upset Rate Prediction Considerations for a DICE Flip-Flop," *IEEE Trans. Nucl. Sci.*, vol. 56, no. 6, pp. 3130-3137, Dec. 2009.
- [Wi01] G. D. Wilk, R. M. Wallace, J. M. Anthony, "High- κ gate dielectrics: Current status and materials properties considerations," *J. Appl. Phys.*, vol. 89, no.10, May 2001.
- [Wik1] Hamming Code. https://en.wikipedia.org/wiki/Hamming_code
- [Zh08] X. Zhu, "Logic SER Characterization," *IEEE Int'l. Rel. Phys. Symp. Tutorial*, 2008.
- [Zh10] M. Zhu, L. Xiao, S. Li, and Y. Zhang, "Efficient two-dimensional error codes for multiple bit upsets mitigation in memory," *Proc. IEEE Int. Symp. Defect Fault Tolerance VLSI Syst.*, pp. 129–135, 2010.

Hardening Techniques for Analog and Mixed-Signal Circuits

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1.0 Introduction: Analog and Mixed-Signal Electronics in Space Avionics

Unwavering advancements in IC technology make fabrication processes very suitable and desirable for digital designs. Market requirements demand small-area and low-voltage strategies. Further, fully digital systems can be more easily redesigned and scaled with process changes or fully synthesized with reprogrammable technologies. Nevertheless, analog and mixed-signal (AMS) circuits are widely used for commercial terrestrial systems and space systems. According to Allied Market Research, mixed-signal integrated circuits (*i.e.*, mixed analog and digital circuits) account for the largest segment within the global semiconductor integrated circuit (IC) market. They are expected to grow by an additional 7% by 2027 [1]. The AMS market growth is primarily fueled by the demand for low-power integrated systems-on-chip (SoC) with telecommunications capabilities. This demand holds in all market sectors, including for space and defense systems. The continued and growing need for hybrid analog and digital systems arises from the performance advantages of some critical and commonplace analog components and the rise of integrated three-dimensional IC technologies that can combine multiple technology nodes within a single chip package.

All SoC applications require precision clocking and data communication interfaces, and most require analog/digital interfaces. Some example AMS circuit blocks used for these applications include:

- Clock generators/synthesizers.
- Voltage converters and regulators.
- Analog-to-digital converters (ADCs).
- Digital-to-analog converters (DACs).
- Sampling circuits.

Common to these circuit blocks is the need for the minimum area, low power, and reliable operation under extreme thermal conditions, and exposure to ionizing radiation.

This short course will overview radiation effects in AMS circuits and discuss primary, and state-of-the-art mitigation approaches for total ionizing dose (TID) and single-event effects (SEE). The short course will identify the critical requirements for hardening any circuit and present strategies based on modifying the process, layout, or circuit. Mitigation strategies will

be organized based on fundamental hardening mechanisms rather than based on circuit type, though several examples will be provided for the aforementioned AMS circuits.

2.0 Radiation Effects in Analog and Mixed-Signal Electronics

2.1 General Trends in Radiation Effects with Technology Scaling

Ionizing radiation – energetic particles which can penetrate semiconductor material, leaving ionized charge in their wake – can cause information corruption and transient system failure. The radiation is ubiquitous, existing in the environment external to a circuit and emanating from processing and packaging material integral to a circuit. Once only the concern of space-bound systems where increased susceptibilities to single-event effects (SEEs) have been reported as device feature sizes decrease and operating frequencies increase, IC density and power scaling have propelled this issue to the forefront of reliability concerns at current technology nodes in ground-based and space-deployed electronic systems [2][3].

The increased susceptibility to SEE in advanced Complementary Metal-Oxide Semiconductors (CMOS) can be attributed primarily to factors associated with device scaling trends [4][5]. Early scaling theories through the 1970s and 1980s followed two basic approaches: constant-voltage scaling and constant-field scaling [6][7]. However, in recent years, the higher currents necessary for greater operating frequencies, combined with the need for higher packing densities, require the semiconductor devices to have shorter channel lengths and widths with higher oxide breakdown fields [8]. These scaling pressures are principally constrained by the acceptable leakage currents when the transistors are “off,” and many works have focused on more complicated scaling algorithms and device structures to counteract these scaling tradeoffs [5]. Ultimately, the fast-paced scaling trends in MOS technologies, consequently decreasing nodal capacitances [6], results in increased single-event (SE) vulnerabilities by reducing the minimum amount of charge (*i.e.*, critical charge) required to alter the state of a circuit node [9].

TID effects, on the other hand, are often assumed to decrease with each technology node. This trend is due to the reduction in the thicknesses of critical dielectric layers driven by Moore’s law scaling [10]. However, the TID response of MOS devices with advanced gate stacks is often

more complex than for MOS devices with SiO_2 gate oxides [10]. TID challenges remain for linear bipolar technologies and CMOS technologies suitable for high-performance analog and RF functionality [10]-[13].

The following sections overview TID and SEE in AMS circuits.

2.2 Total Ionizing Dose Effects in AMS Circuits

Barnaby provided a comprehensive review of TID in [14]. Here, a summary of TID and the implications for AMS circuits is discussed.

2.2.1 Physical Processes of TID

The interaction of ionizing particles (*i.e.*, protons, electrons, or energetic heavy ions) with the atoms of a semiconductor material results in the generation of electron-hole-pairs (ehps) along the ionization track and secondary electrons emitted via photon-material interactions [15]. The density of ehps generated along the tracks of charged particles is proportional to the energy transferred to the target material [16]. Stopping power or linear energy transfer (LET) describes the energy loss per unit length (dE/dx) of a particle. It is a function of the mass and energy of the particle as well as the target material density [17]. The units of LET are commonly expressed as $\text{MeV}\cdot\text{cm}^2/\text{g}$. TID refers to the total amount of energy deposited by a particle that results in ehp production and has a typical unit of the rad, which denotes the energy absorbed per unit mass of a material [14].

Figure 1 [18] illustrates the primary physical processes that lead to TID damage, including:

- Generation of ehps.
- Prompt recombination of a fraction of the generated ehps.
- Transport of free carriers remaining in the oxide.
- Formation of trapped charge via hole trapping in defect sites (N_{ot}) or the appearance of interface traps (N_{it}) via reactions involving hydrogen [19].

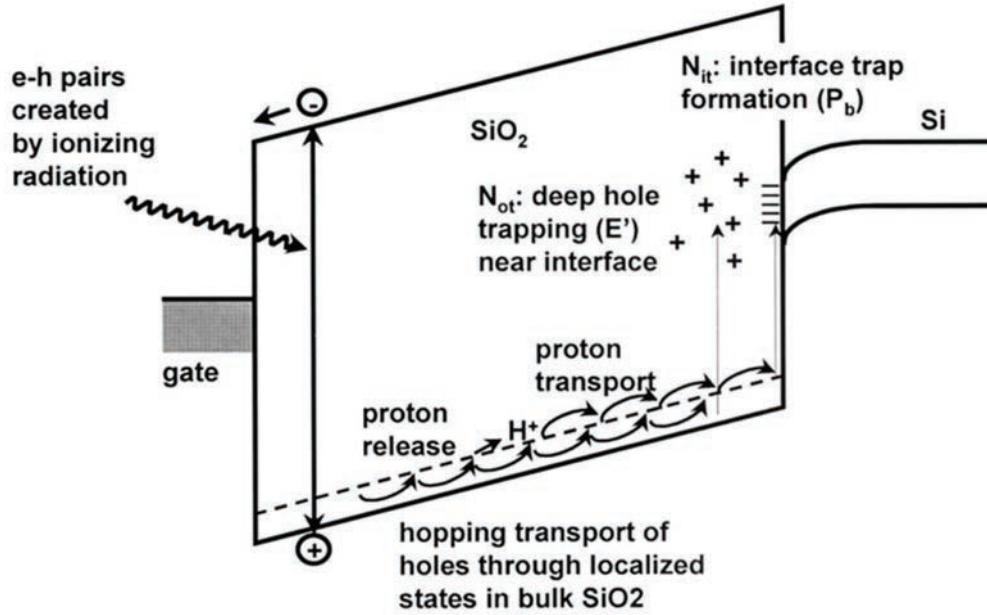


Figure 1: Summary of the primary physical processes that lead to TID damage [18].

2.2.2 Bipolar Junction Transistors

In bipolar junction transistors (BJTs), TID damage to oxide dielectrics leads to:

- Excess base current via enhanced recombination with traps.
- Increased collector current in *npn* devices due to increased emitter area (via surface inversion from N_{ot}).
- Increased reversed leakage current from collector to base (CB) due to increased carrier generation (via traps) in CB junction.

Primarily affecting lateral *pnp* transistors, more significant TID effects can also be observed at low dose rates, referred to as enhanced low-dose-rate sensitivity (ELDRS) [20].

A Gummel plot showing collector (I_C) and base (I_B) current versus base-emitter voltage (V_{BE}) for a BJT technology is provided in Figure 2 [21]. Significant increases in base current with TID are observed, resulting in degradation in the current gain (β), as seen in Figure 3 [21]. The degradation can also be measured in transconductance (g_m) when referring to the input as the base-emitter voltage (V_{BE}) rather than I_B, as seen in Figure 4 for a SiGe heterojunction bipolar (HBT) transistor [22]. Increases in I_B and the resulting β degradation are particularly problematic for AMS and RF circuits because they can degrade AC parameters

and mismatch due to varying bias conditions. For example, as seen in Figure 5, the degradation in input bias current of an LM139 differential comparator is worse when the inputs are biased than when grounded, resulting in amplification of offset error [23]. Issues related to input bias current degradation, mismatch, and offset voltage are detailed in [24].

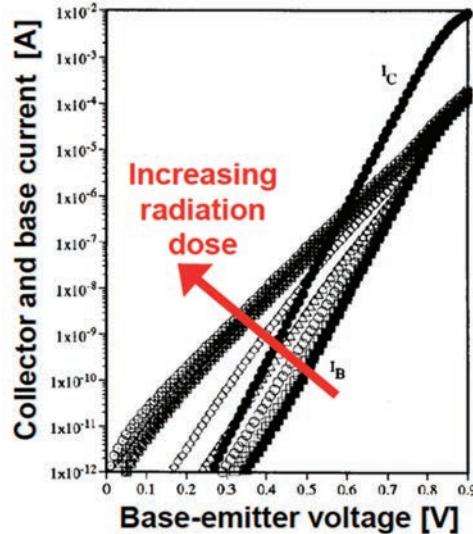


Figure 2: Gummel plot showing increases in base current of a BJT with increasing TID (after [21]).

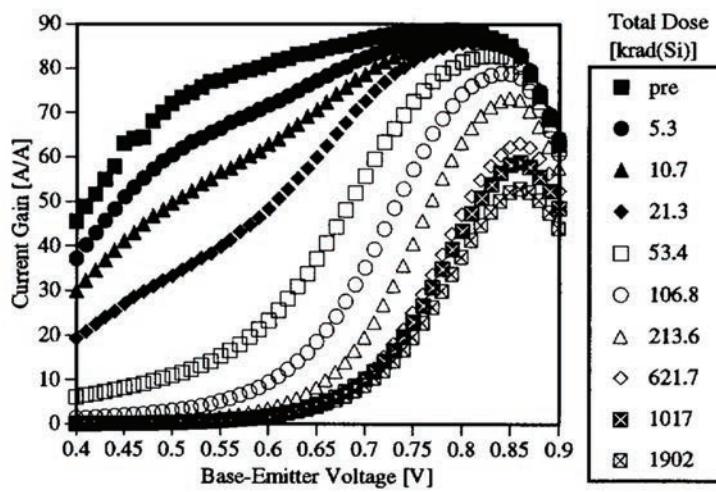


Figure 3: Current gain (β) of BJT shown in Figure 2 with respect to TID [21].

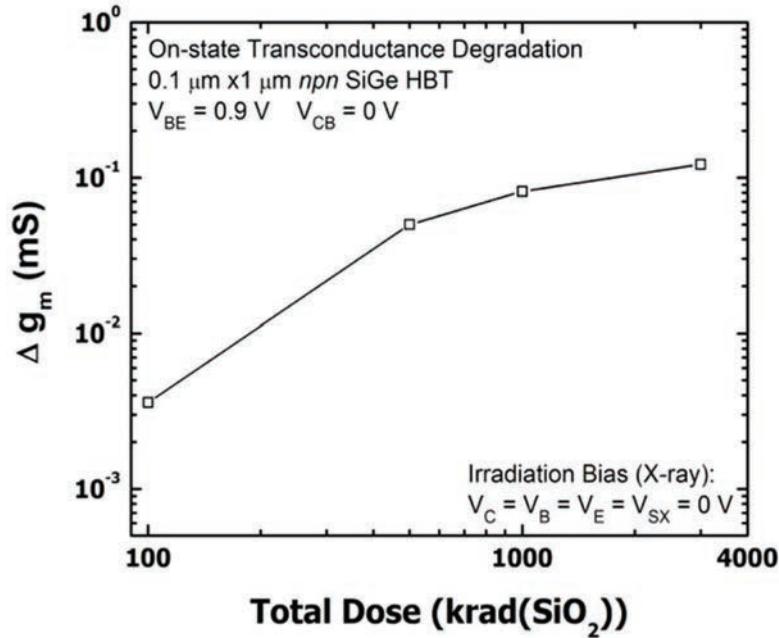


Figure 4: Transconductance (g_m) of a SiGe HBT with respect to TID [22].

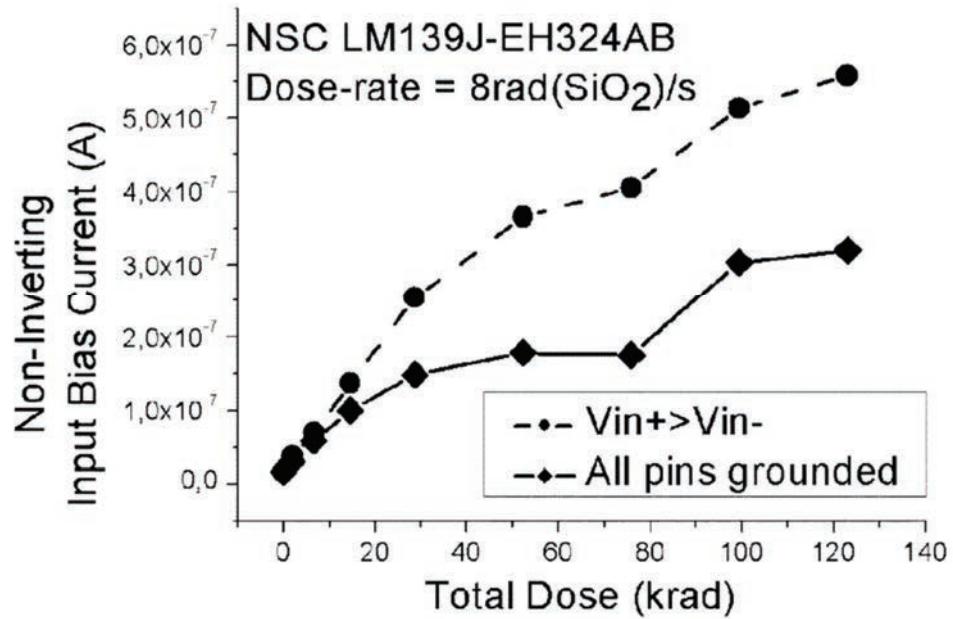


Figure 5: Input bias current at the non-inverting input terminal of the LM139 comparator with respect to TID [23].

2.2.3 MOS Transistors

In CMOS technologies, TID damage to oxide dielectrics leads to:

- Threshold voltage (V_{TH}) shifts, sub-threshold slope reduction, and mobility (μ) degradation.
- Increase intra-device (edge) leakage in n-channel MOS (nMOS) transistors.
- Increased inter-device leakage in parasitic nMOS devices.
- Increased static supply current.

Figure 6 shows the pre-irradiation and post-irradiation drain current versus gate voltage (I_{DS} - V_{GS}) characteristics of nMOS transistors in a 45 nm bulk CMOS process. Data is shown for both room (25°C) and elevated (100°C) temperatures and illustrates an increase in sub-threshold leakage current with TID at both temperatures. The increase in leakage is attributed to the positive charge trapped in the shallow trench isolation (STI), causing leakage along the sidewalls between the drain and source. Additionally, the on-state slope of the I_{DS} - V_{GS} characteristics decreases with dose, showing TID-induced degradation in the on-state drain current [25]. There was no increase in sub-threshold leakage for p-channel (pMOS) transistors in the same technology and minimal degradation in on-state current.

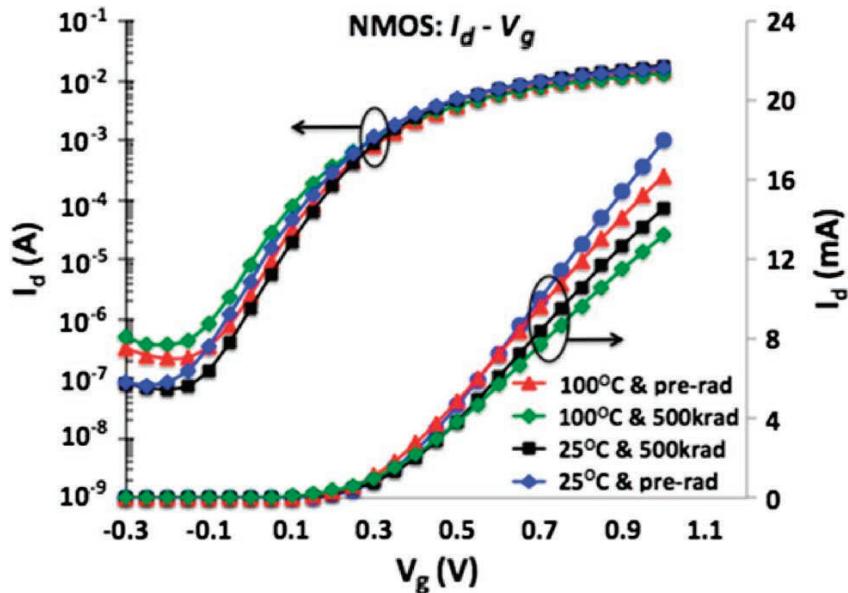


Figure 6: I_{DS} vs V_{GS} curves for an nMOS transistor in a 45 nm bulk CMOS technology before irradiation and at 500 krad (SiO_2) [25].

Increases in leakage current and decreases in on-state current decrease the g_m of CMOS transistors. Similar to the behavior of the degradation in BJT devices, g_m is seen to shift downward and to the right with increasing TID (see Figure 7). Degradation in g_m will enhance device mismatch and degrade gain. In Jagannathan *et al.* [25], the importance of temperature in AMS and RF designs is noted. Interestingly, the study in [25] was conducted with a 45 nm CMOS process tailored to RF technologies. The 45 nm node is generally thought tolerant to TID for most digital designs. However, minor TID degradation appears to be enhanced at elevated temperatures, potentially impacting design margins. In the same study [25] and additional works in [26] and [27], TID sensitivity was shown to cause reductions in frequency, amplitude, and phase noise in high-frequency voltage-controlled oscillators (VCO).

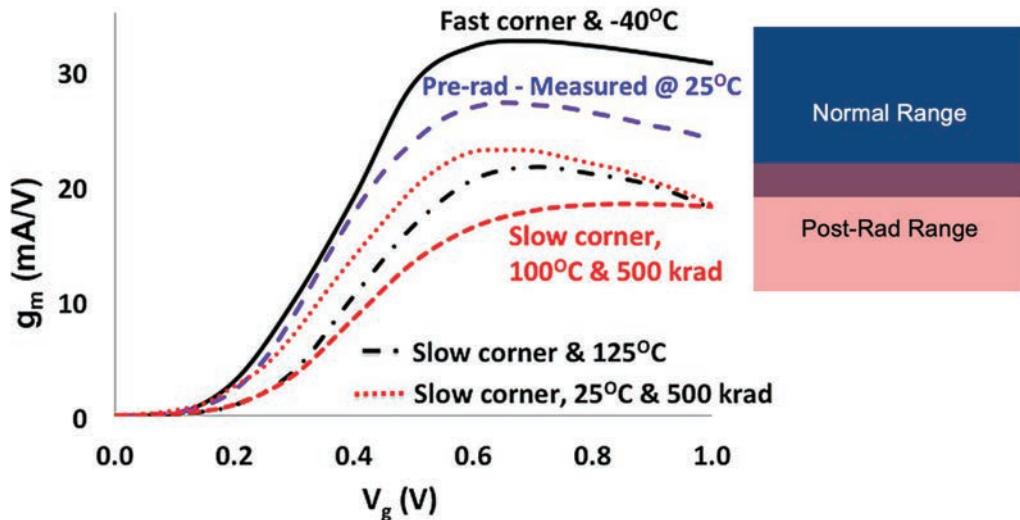


Figure 7: Simulated and measured g_m vs V_{GS} curves for an nMOS transistor in a 45 nm bulk CMOS technology before irradiation and at 500 krad(SiO_2). Simulations show the expected range of operation with variations in process parameters and temperature. Measured post-rad data at elevated temperature falls outside of the expected operating range (after [25]).

2.3 Single Event Effects in AMS Circuits

Single-Event Effects (SEE) result from the interaction of a single energetic particle with semiconductor material. SEE are determined by:

- Energy deposition and charge (ehp) generation in the semiconductor material.
- Charge collection at a metallurgical junction.
- Response of the circuit and system to erroneous charge.

Most SEE are non-destructive and transient. However, some SEEs are destructive, such as single-event latchup (SEL), and can lead to catastrophic system failures. This short course focuses on non-destructive single-event transients (SET), single-event upsets (SEU), and multiple-bit upsets (MBU) as they pertain to AMS design. Hardening strategies for the mitigation of SEL are also discussed.

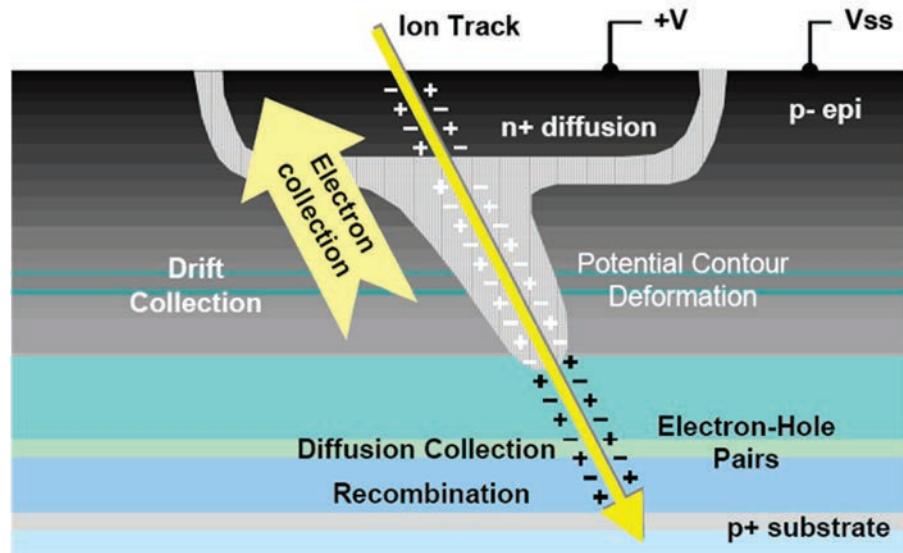


Figure 8: Illustration of an ion strike on a reverse-biased n+/p junction [28].

2.3.1 Charge Generation and Collection

Electron-hole pairs (ehp) generated from the interaction of a single energetic particle with a circuit's semiconductor material can be collected at a metallurgical junction. In this case, the event can manifest as a spurious transient signal within the circuit. Figure 8 illustrates the charge collected through drift and diffusion processes in a reverse-biased n+/p junction [28]. The initial

charge collection is due to field-assisted drift, followed by the collection of charge diffused through the substrate.

A consequence of charge generation and collection within a semiconductor device is radiation-induced photocurrents at the device terminals. The shape of the current pulse is related to the time derivative of the collected charge. As seen in Figure 9, an initial spike of current occurs due to drift collection, followed by a slow decrease in current due to diffusion collection [29]. The current pulse is most often modeled as a double exponential with empirical fitting parameters. This approach allows for comparative studies of circuit sensitivity to SEE and appears more valid for analog circuit analysis than for digital circuit analysis. The responses of analog circuits to single event phenomena tend to be dominated by circuit timing and gain parameters, thus shaping the overall behavior. In contrast, digital circuits are acutely sensitive to SET time constants [30]. Additional approaches for modeling single event photocurrent are described in [31].

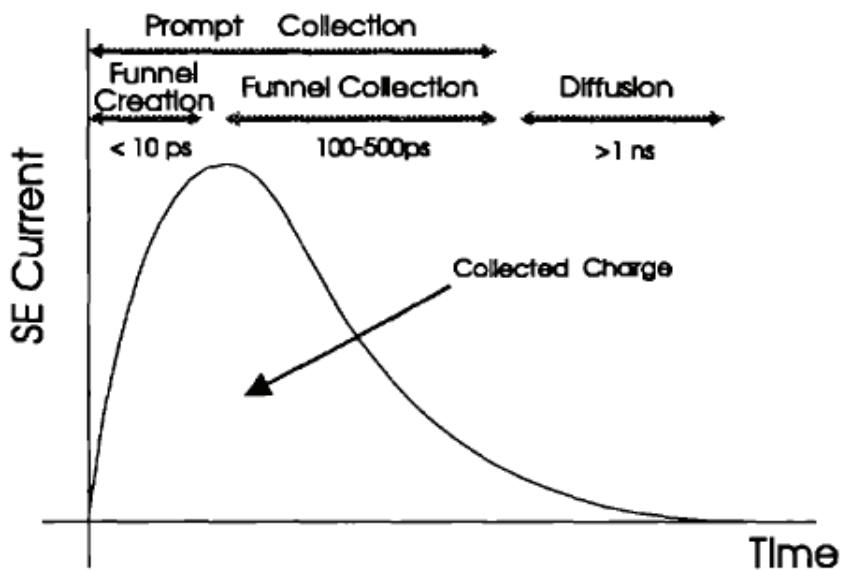


Figure 9: Typical shape of the SE current at a junction. The total collected charge corresponds to the integral of the current pulse [29].

2.3.2 Multiple Node Charge Collection

Another phenomenon increasingly more critical as modern electronics scale to nanometer dimensions is multiple-node charge collection. Due to the decreased feature sizes and increased

packing densities, the plasma track of free carriers generated from an ion strike may span multiple device junctions, allowing for charge collection by drift and diffusion processes at multiple device terminals. Figure 10, for example, illustrates the relative range of the ehp's created by a single-ion strike in a 1 μ m CMOS technology and a 90 nm CMOS technology [32]. The diameter of the electron-hole plasma track can generally be assumed to be technology-independent (note that it depends on the ion energy, mass, and material system). In the notional drawing shown in Figure 10, the electron-hole plasma spans multiple charge collection terminals in the 90 nm technology, resulting in the disturbance of many junctions and current transients at numerous locations.

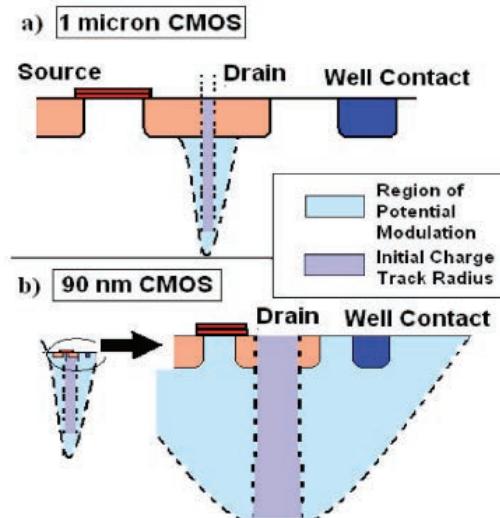


Figure 10: Relative range of the ehp cloud in a 1 μ m and a 90 nm technology. (a) The ehp track creating a potential perturbation on a small portion of the drain. (b) A strike with the same radius covering the source, drain and well contact [32].

An additional mechanism that can result in multiple node charge collection is illustrated in Figure 11. A proton is shown to collide with a single sensitive volume of bulk Si, producing secondary particles including a 14 MeV oxygen ion, a proton, gamma rays, and alpha particles. In this case, the heavy oxygen ion continues to transverse six additional sensitive volumes of silicon, depositing between 30 fC and 40 fC of charge within each volume [33]. This type of multiple node collection is expected to increase with scaling and is progressively more important for complete characterization.

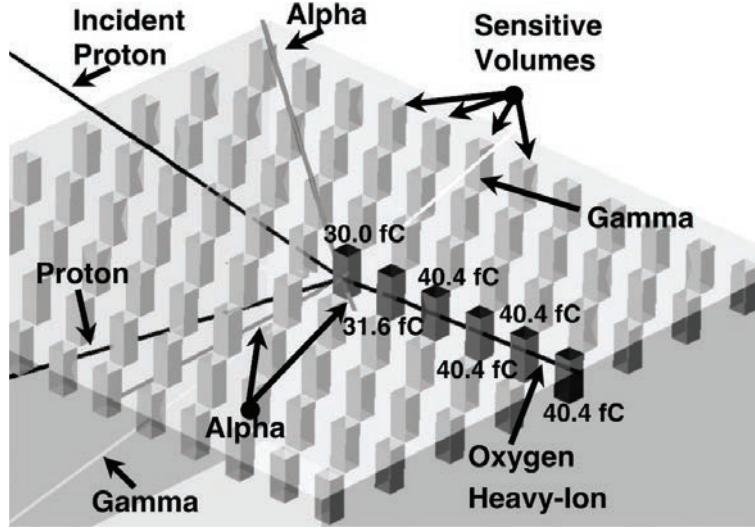


Figure 11: Simulated nuclear event with a 63 MeV incident proton. Proton interacts with a silicon nucleus producing secondary particles including a 14 MeV oxygen ion, a proton, gamma rays, and alpha particles. The heavy oxygen ion transverses six sensitive volumes, which collect between 30 fC and 40 fC each [33].

2.3.3 Circuit Response

While the meaning of a soft error in a digital circuit, *i.e.*, a corrupt memory or logic state, is relatively straightforward, there exists no standard metric for soft errors in AMS. An SEE in an AMS system depends on the:

- Initial charge generation and collection processes.
- Type of circuit (function).
- Circuit topology (schematic).
- Circuit layout.
- Operating mode.

Unlike TID, the effect of an SE is transient and does not alter the operation of a circuit, except for cases where the event is destructive or modifies the configuration (*e.g.*, functional interrupts).

Since spacecraft malfunctions (NASA's TOPEX/Poseidon satellite in 1992) were first attributed to analog SETs [34], the SET phenomenon has been widely researched through both experimental and simulation efforts. Koga *et al.* noted in [34] that SETs generated within the analog circuits were likely coupled into digital components within the spacecraft, thus identifying

the core issue with all mixed-signal electronics systems today. The increased interest in SETs in recent years can be attributed to three main factors:

- The LET threshold (minimum LET for which SETs can be observed) for SET generation is low. Heavy-ions with an LET as low as 1 MeV-cm²/mg can generate SETs in specific analog circuit configurations, thus allowing for many heavy-ions capable of creating SETs [35].
- SETs have been observed with amplitudes spanning the power supply rails (or greater) and durations as long as milliseconds [36].
- The energy threshold (minimum particle energy required for SET generation) is low; protons and even alpha particles have been shown capable of generating SETs in advanced CMOS electronics [37], [38].

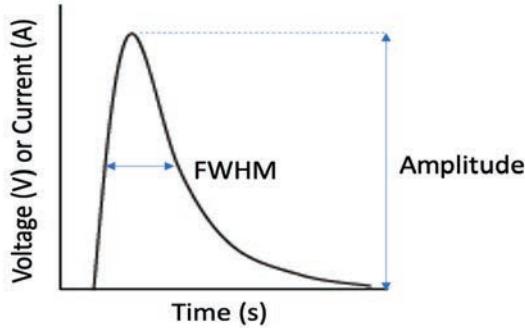


Figure 12: Single-event transient with the typical quantifiable measures of amplitude and pulse width (time width) measured full width at half maximum (FWHM).

Transients like those first observed in [34] are often described by their amplitude and pulse width, as seen in Figure 12. The pulse width may be quantified in various ways, the most common being the time width at half of the maximum amplitude, *i.e.*, full width at half maximum (FWHM). Amplitude is simply the change in voltage or current from the nominal state. The pulse width may be described as the amount of time the transient exceeds a threshold value. Thresholding is most commonly seen when a specific error level is identified but is otherwise arbitrary.

Using the voltage amplitude versus time-width (FWHM) method described by Figure 12, Figure 13 illustrates a scatter plot of SET pulses that are possible at the output of an LM124

operational amplifier [39]. These SETs were measured under heavy-ion broad beam exposure (specifically 100 MeV Br, 150 MeV Mg, and 210 MeV Cl ions). A variety of positive and negative-going transients were observed in the experiment with both long and short durations. The type of transient observed at the circuit output can be attributed to the location of the initial ion strike within the circuit.

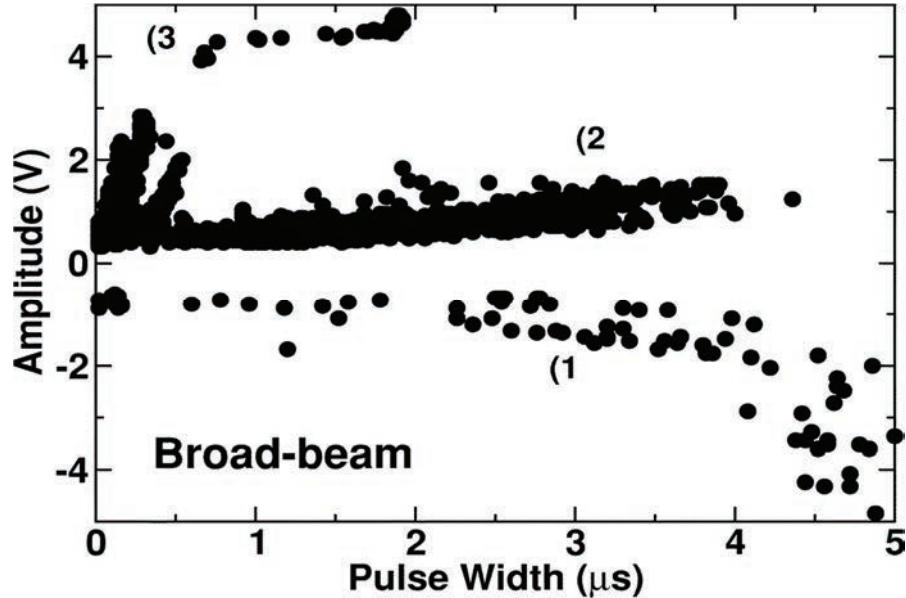


Figure 13: Amplitude versus time-width (measured full-width at half-maximum of amplitude) of single-event transients at the output of an LM124 operational amplifier under heavy-ion exposure (100 MeV Br, 150 MeV Mg, and 210 MeV Cl ions) [39].

SETs such as those observed in [34] and [39] illustrate the wide range of possible responses within a given circuit topology – these works focus on operational amplifiers. As mixed-signal circuits are required to bridge analog and digital domains, SETs in AMS circuits are often subject to various response mechanisms due to complex component interactions. Figure 14 and Figure 15 illustrate examples of SETs in AMS circuits [40]-[42]. Figure 14 shows (a) two voltage SETs within a phase-locked loop (PLL) [40] that results in (b) frequency perturbations [41]. Figure 15 illustrates current transients within a SiGe HBT low-noise amplifier (LNA), resulting in errors in the modulated data via 16-symbol (4-bit) quadrature amplitude modulation (QAM) [42]. The SETs result in errors as indicated by a shifting of the decoded symbols within the constellation diagram.

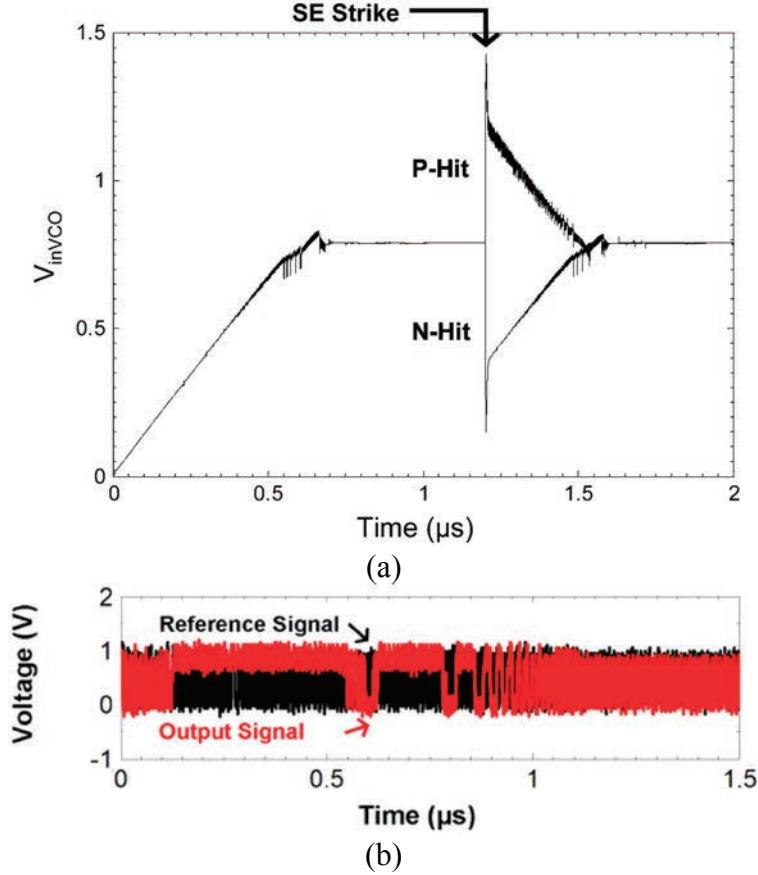


Figure 14: (a) Simulations of SETs on an internal node within a PLL [40]. (b) Measured SET in a PLL designed in 130 nm CMOS, showing in output frequency modulation. The event was captured using laser two-photon absorption (TPA) at the Naval Research Laboratory [41].

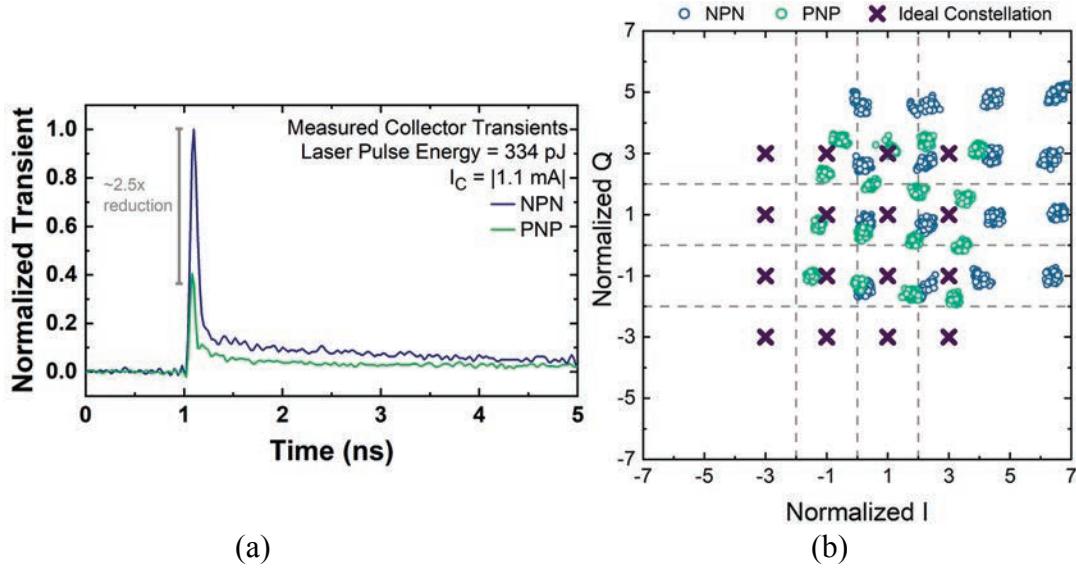


Figure 15: (a) Example measured SETs resulting from strikes to *npn* and *pnp* transistors in a SiGe HBT technology. (b) Constellation diagrams for 16-QAM-modulated data on *npn* and *pnp* LNAs for an LET of 10 MeV·cm²/mg [42].

2.3.4 Techniques for Measuring and Quantifying SEE

Though there are no standard error metrics for SEE in AMS circuits, several practical analysis techniques are commonplace. One experimental approach beneficial for interrogating specific circuit vulnerabilities and for comparative radiation-hardened-by-design (RHBD) studies is laser-induced carrier generation for SEE applications. Laser excitation of ehp can be accomplished via single-photon absorption (SPA) or two-photon absorption (TPA) using high peak power femtosecond pulses at sub-bandgap optical wavelengths [43][44].

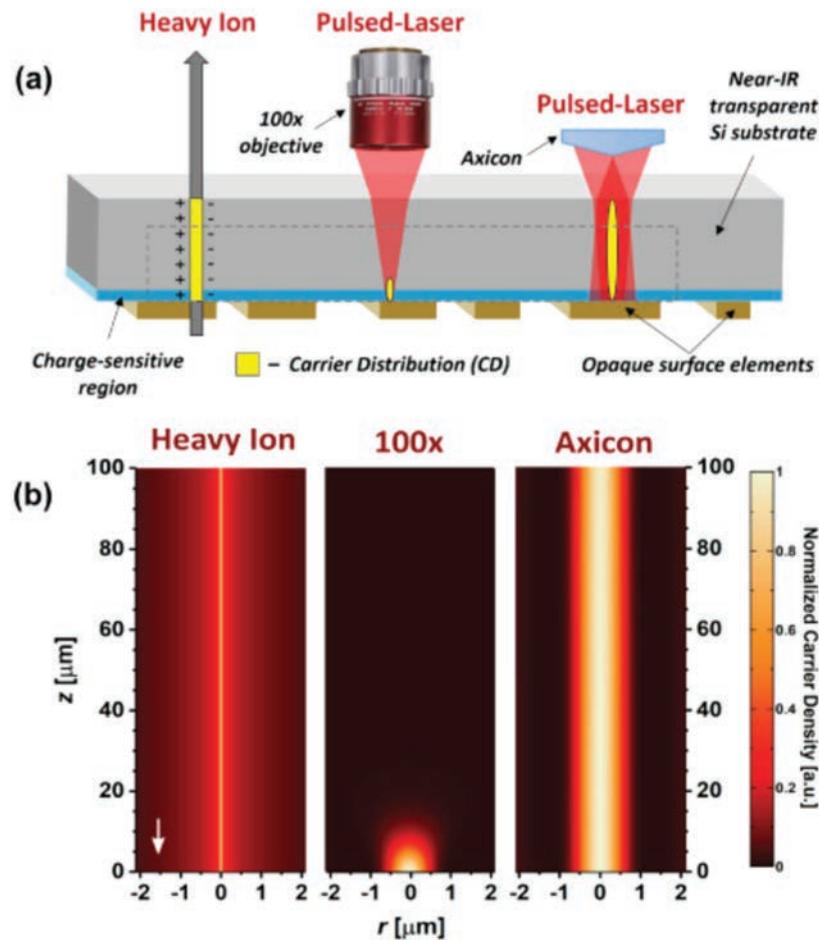


Figure 16: Depiction of the carrier generation processes in a device or circuit (a). The region denoted by the dashed line represents the axial region in (b) where the carrier distributions (CDs) produced by each irradiation source are shown [45].

The TPA SEE technique is particularly useful for SEE analysis due its ability to interrogate SEE phenomena through the wafer using backside irradiation. TPA eliminates

interference from the metallization layer stacks prevalent in modern devices and circumvents many of the testing issues associated with flip-chip-mounted parts. The typical TPA SEE experimental setup is described in [43][44]. A device under test (DUT) is mounted on a motorized *xyz* translation platform. Optical pulses are focused through the wafer onto the front surface of the DUT (see Figure 16 [45]), resulting in a near-Gaussian beam profile with a typical diameter of between 1-1.6 μm at focus [43]. Figure 16 also illustrates the differences in carrier generation processes between heavy-ion and pulsed-laser approaches. By scanning the laser over a defined region of interest and recording responses at each *x-y* location, vulnerable circuit nodes can be identified, aiding in vulnerability analyses and RHBD comparisons. Additional laser-based SEE testing approaches can be found in [46] and [47].

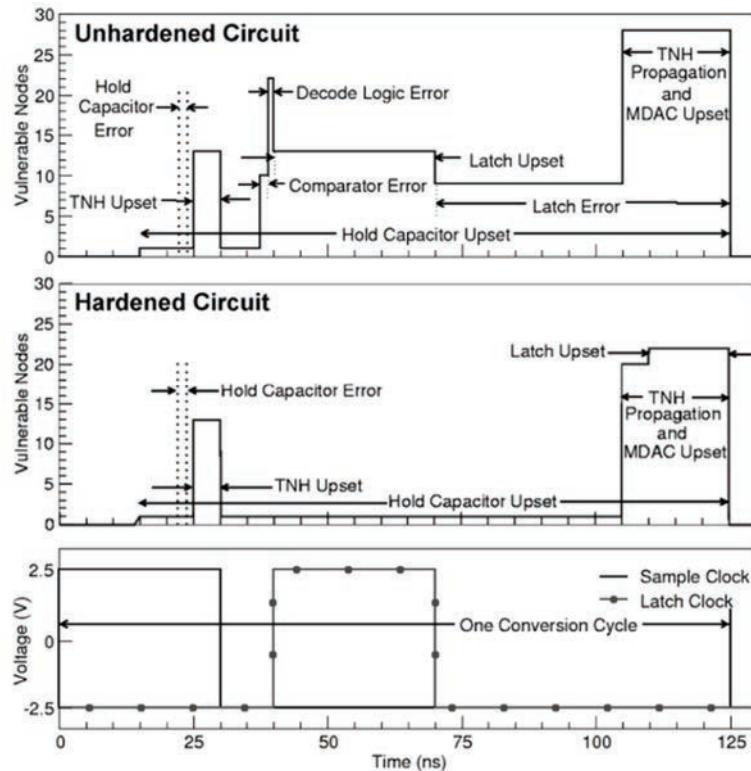


Figure 17. Windows of vulnerability for unhardened (top) and hardened (middle) 2-bit flash ADC circuits with respect to the clock (bottom) for one conversion cycle.

Whether through laser interrogation, simulation, modeling, or other various experimental techniques, the identification of the radiation vulnerabilities is perhaps the most time consuming yet critical activity in the development of RHBD strategies. The window of

vulnerability is a well-known concept in the digital design community and describes the amount of time during a clock cycle that a circuit is vulnerable to SEU. Generally, reducing the window of vulnerability improves the SEU performance. Kauppila *et al.* use the concept to determine the sub-circuits of a flash ADC vulnerable to single events within a single conversion cycle (Figure 17) [48]. The knowledge from this type of analysis was helpful for targeted hardening solutions.

Also, the concept has also been employed to examine the relative SE sensitivities of SerDes and PLL sub-circuits through what was termed “phase-dependent” single-event analysis [49]. Asynchronous laser injections were used to deposit energy into the circuits at random time within the clock cycles. Figure 18 shows the number of errors versus signal phase for laser strikes in a pre-emphasis amplifier in a 2 Gbps SerDes (left) and for laser strikes in the output switches in the charge pump of a 200 MHz PLL (right). While errors occur during the entire clock period, they tend to be concentrated about the rising and falling clock edges [49].

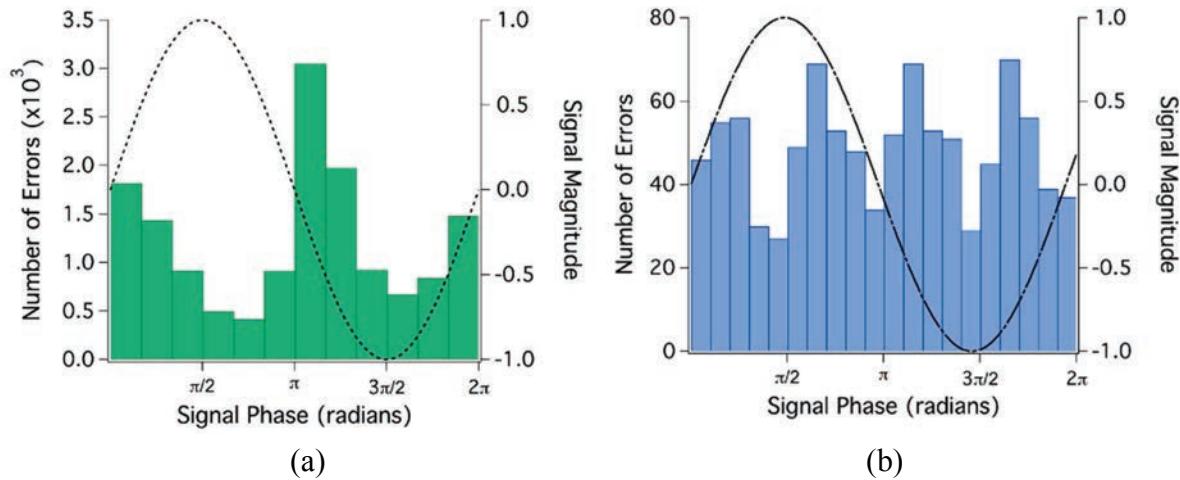
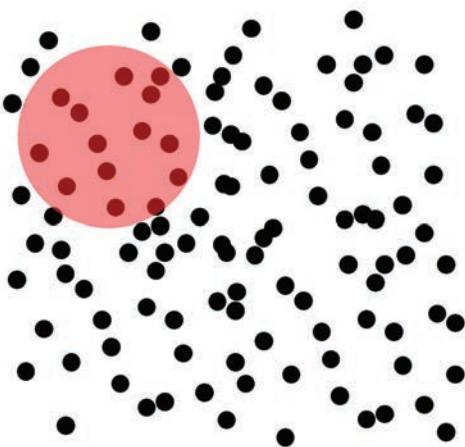


Figure 18: Number of errors versus signal phase for laser strikes in a pre-emphasis amplifier in a 2 Gbps SerDes (a) and for laser strikes in the output switches in the charge pump of a 200 MHz PLL (b). While errors occur during the entire clock period, they tend to be concentrated about the rising and falling clock edges [49].

The most common method for quantifying the overall vulnerability to SEE is through heavy ion exposure via a particle accelerator. Testing standards and an overview of the types of beam facilities most commonly used for SEE testing are provided in [50]. SEU recorded during

these experiments are quantified by the cross-sectional area (σ) reporting upsets versus the LET. The process for determining the σ of a DUT following radiation exposure is depicted in Figure 19. Typically, the radiation test engineer sets the desired particle flux (particles per unit area per unit time) and exposes the DUT until the desired number of events (N) is recorded or for a predetermined length of time [51]. The length of exposure time determines the total fluence (F), or the number of particles that impact the DUT per unit area. Then σ is determined by Equation (1) and is typically expressed in units of cm^2 . Thus, σ can be thought of as the area of the DUT that is sensitive to SEU at a particular LET. These measured cross-sections are then plotted with respect to the LET, as shown in Figure 20. The primary goal of RHBD is to reduce SEU error rates by increasing the threshold to upset (LET threshold or LET_{TH}) and decreasing the limiting or saturation cross-section (σ_{lim}).



Calculation of Cross-Section

Known Arial Density of Ions (i.e., fluence)
Ex. 10 ions/ cm^2

Number of shots that hit an unknown target
Ex. 14 ions hit target (i.e., SEU)

$$\text{Cross-section} = \frac{14 \text{ SEUs}}{10 \text{ ions}/\text{cm}^2} = 1.4 \text{ cm}^2/\text{target}$$

Figure 19: Simplified process for determining the heavy-ion cross-section of a DUT.

$$\sigma = \frac{N}{F} (\text{cm}^2) \quad (1)$$

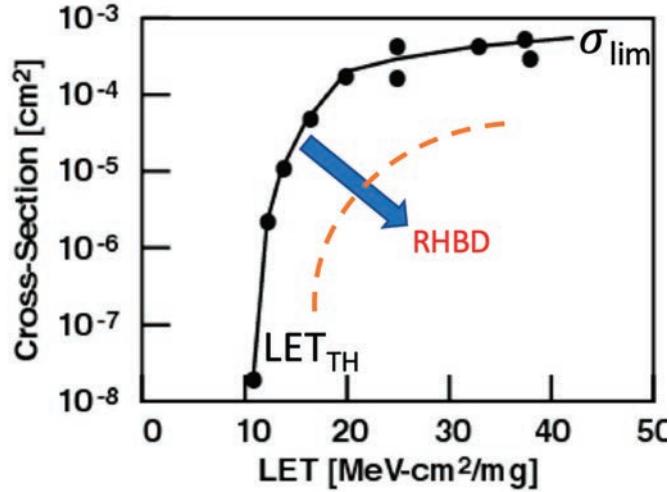


Figure 20: Illustration of SEU cross-section versus LET and notional depiction of radiation hardening by design.

2.3.5 Single-Event Latchup

Single-event latchup (SEL) is one of the most problematic and well-known of the destructive SEE [52]-[55]. SEL is a consequence of a parasitic thyristor (*pnpn*) that is formed in adjacent *n*-type and *p*-type regions in CMOS circuits (Figure 21). The parasitic thyristor is composed of *pnp* and *npn* BJTs, where the collector of each BJT is connected to the base of the opposing, creating a potential positive feedback loop. The parasitic circuit is dormant under normal operating conditions when all of the relevant *pn* junctions are reverse biased. However, an IC can be triggered into latchup by electrical conditions or by the radiation environment if the product of the current gains of the *pnp* and *npn* transistors is greater than 1. While these stimuli start the latchup process in different ways, the equilibrium conditions such as the holding voltage and holding current are the same [52].

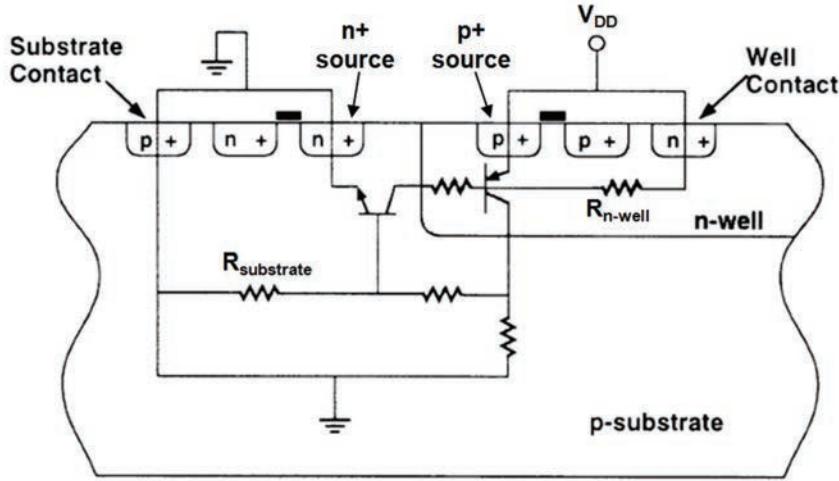


Figure 21: Cross-section of typical CMOS technology showing parasitic thyristor that can be triggered into low impedance state [54].

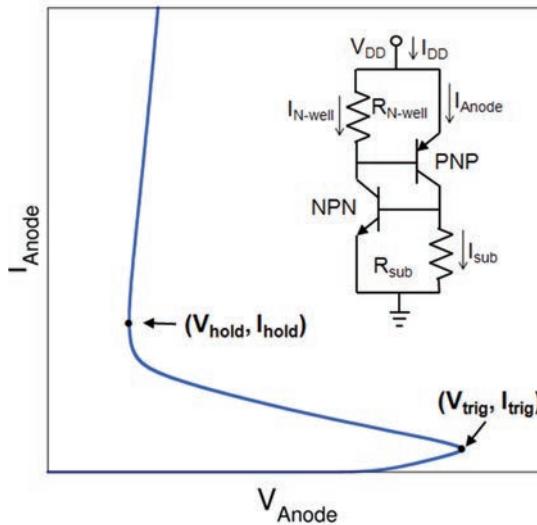


Figure 22: Typical I - V curve generated via positive current injection into the anode, indicating the latchup conditions [54].

Figure 22 illustrates the typical I - V characteristics produced via positive current injection [54]. Current is forced into the anode, causing the anode voltage (*i.e.*, the p -source) to increase. Once the p -source-to- n -well junction is forward biased, current is injected into the base of the npn (*i.e.*, the p -substrate), turning on the parasitic npn . The npn then injects current into the base of the pnp , reinforcing the active parasitic structure. This is called the trigger point and is labeled in Figure 22. With both BJTs turned on, there is a low impedance path

between V_{DD} and V_{SS} , causing an increase in current even as the anode voltage decreases. The thyristor structure is then said to be latched because it will remain in a high current state until the p -source voltage is decreased below a critical level, termed the holding voltage (V_{hold}) [54].

3.0 Approaches to TID Mitigation

3.1 Radiation Hardening by Process (RHBP)

Historically, a common and potentially expensive approach to realizing radiation-tolerant ICs was radiation-hardening by process (RHBP), where extra steps were added to a fabrication process to increase the intrinsic tolerance of devices [56]-[64]. In general, all oxide regions with a thickness of 10 nm or greater, not hardened by design (discussed in subsequent sections), need to be processed to minimize the number of hole traps or use deep electron traps and recombination centers to produce as little net positive charge as possible [61]. While process hardening recipes are typically proprietary, techniques such as ion implantation and layered films for controlling the location of trapped charges are effective in hardening oxide regions [61].

Strained-enhanced SiGe HBT technology (graded Ge layer in the base of a Si transistor) has emerged as an excellent choice for TID-robust RF circuits, potentially accomplished without the use of additional process modifications [62]. Figure 23 illustrates a cross-section of a SiGe HBT transistor, highlighting various important features [63]. The multi-Mrad TID tolerance of the technology has been attributed to (1) the thin emitter-base (EB) spacer contained within a heavily doped region of the epitaxial base, (2) the thin heavily doped base, and (3) the thin shallow trench isolation (STI) in the collector–base (CB) junction that is well away from the core transport path of the transistor. These features exist to allow for a strained SiGe alloy inside the base region of a BJT to enable RF operation but are a serendipitously effective combination for TID tolerance [62]. Figure 24 shows the forward-mode Gummel characteristics of a SiGe HBT fabricated in the IBM 9HP technology node with TID. Moderate damage (note the Mrad tolerance) is seen through the increase in off-state base current, which is attributed to the classical BJT response due to the generation of traps along the interface of the EB spacer oxide [22].

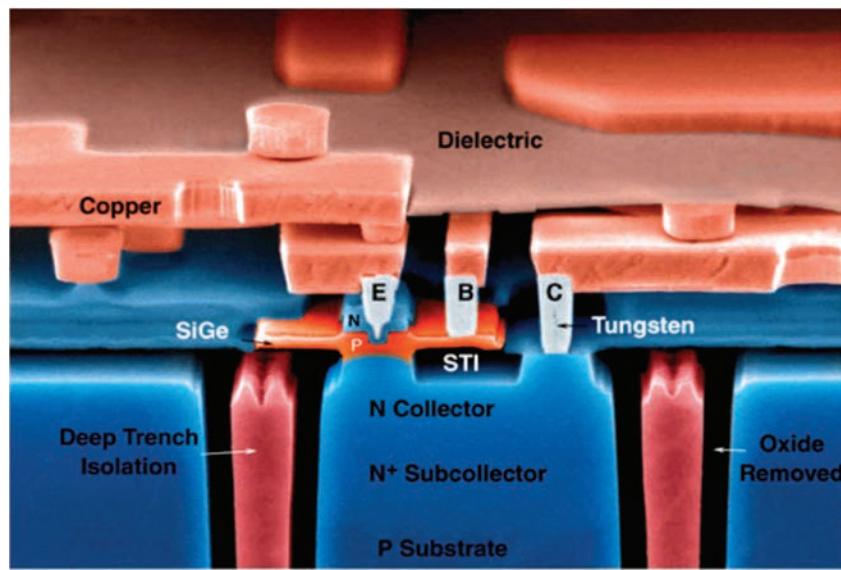


Figure 23: Cross-section of a SiGe BT transistor [63].

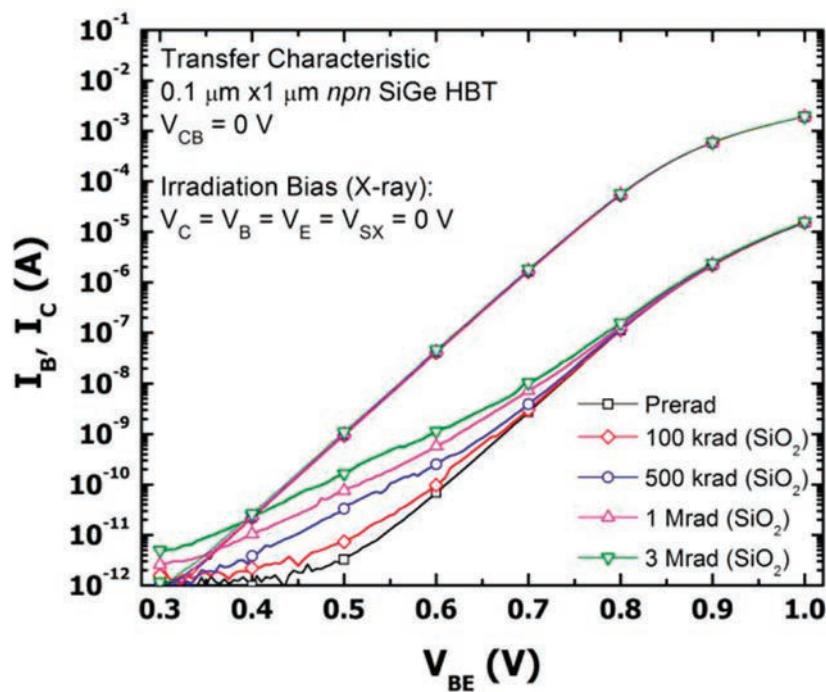


Figure 24: Forward-mode Gummel characteristics of a SiGe HBT fabricated in the IBM 9HP technology node with respect to TID [22].

3.2 Radiation Hardening by Design (RHBD) via Transistor Layout

The relative robustness of modern CMOS technologies to TID, primarily due to thin gate oxides, has led to RHBD circuits through individual transistor layout. Edgeless (or enclosed/annular) transistor layout eliminates the radiation-induced sidewall channel leakage in nMOS transistors. It reduces trapped charge in the field oxide bordering the channel, contributing to shifts in threshold voltage. An edgeless transistor is constructed with the drain surrounded by the gate, which is in turn surrounded by the source. This layout eliminates the sidewall edge leakage path between source and drain, thereby making the transistor immune to radiation-induced leakage [35].

Additional layouts methods to eliminate sidewall leakage in nMOS transistors include a two-poly process [65], an enclosed-drain layout in which the gate surrounds the drain with the source on a single side [66], and the use of p^+ guard rings to combat the surface inversion of the p -substrate that leads to nMOS-to-nMOS and nMOS-to- n -well leakage currents [14], [66]-[69].

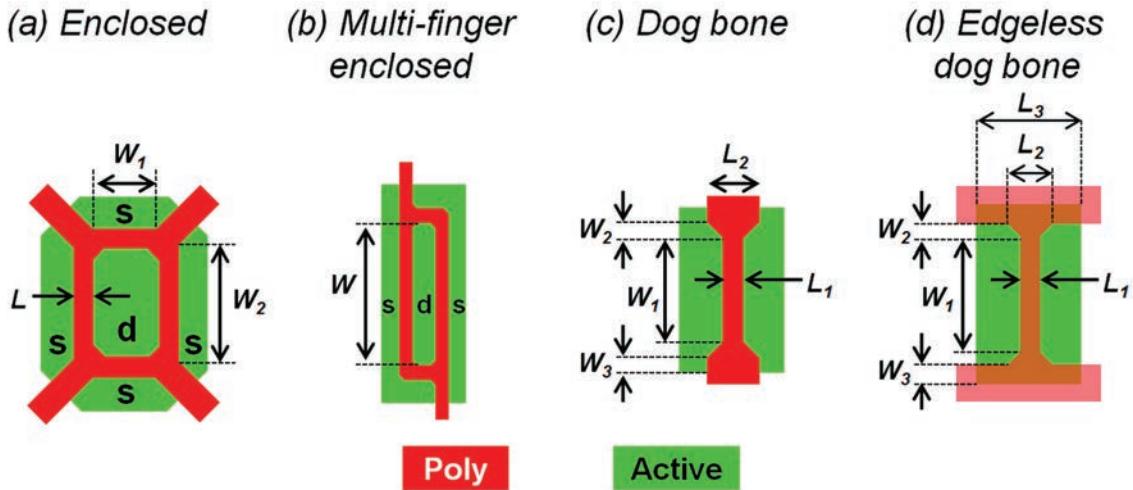


Figure 25: Variants of edgeless transistor design to eliminate sidewall leakage between the drain and the source, including (a) single-finger enclosed, (b) multi-finger enclosed, (c) classic dog bone, and (d) edgeless dog bone [35].

While an edgeless layout is highly effective at mitigating TID leakage, the layout generally requires design waivers from the manufacturer and creates asymmetry, which can be problematic for analog designs. Figure 25 illustrates four edgeless transistor layouts, including the (a) single- and (b) multi-finger enclosed approaches and simplified “dog-bone” edgeless designs in (c) and (d). The dog bone layout of Figure 25 (c) is the classic approach to avoiding the source-drain asymmetry of enclosed designs. By increasing the poly length at the transistor edge, the effect of the radiation-induced channel can be somewhat mitigated [70]. The main drawback of this geometry is the effect the more extended section of the gate has on the aspect ratio of the transistor. Figure 25 (d) illustrates a solution to this problem by extending the poly horizontally, effectively eliminating the edge of the transistor [35].

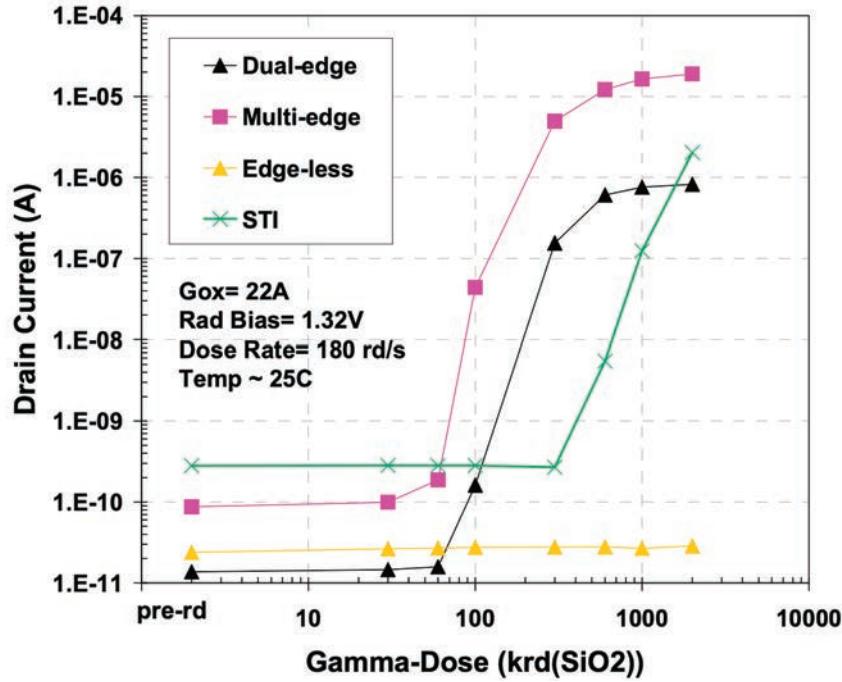


Figure 26: Gamma-ray (^{60}Co) TID evaluation of transistor structures in a commercial 90 nm CMOS process [71].

Concentric edgeless layout techniques are highly effective at eliminating trapped charge in the STI responsible for increased leakage with TID. Figure 26 shows a Gamma-ray (^{60}Co) TID evaluation of transistor structures in a commercial 90 nm CMOS process [71]. Edgeless transistors in this technology showed no increase in leakage current with TID. It was

noted in [71] that any circuit not designed with an edgeless transistor must be investigated for potential TID-induced failures, including AMS circuits designed with symmetry in mind.

While a concentric edgeless transistor layout is highly effective at mitigating TID, an edgeless layout cannot be applied to some transistor configurations. For example, Dynamic Threshold Voltage MOSFETs (DTMOS) have appeared as an option for very-low-voltage design [72]-[74]. Figure 27 shows (a) the layout of a DTMOS transistor (b) applied to transistors M_1 and M_2 in a bandgap current reference [35]. In a typical bandgap reference, *npn* BJTs or nMOS transistors will be used in place of reference transistors M_1 and M_2 . In a DTMOS design, the matched current references are pMOS transistors with the gate, drain, and body grounded, while voltage is applied to the source. The forward biased source-body junction causes reductions in the threshold voltage via the body-bias effect.

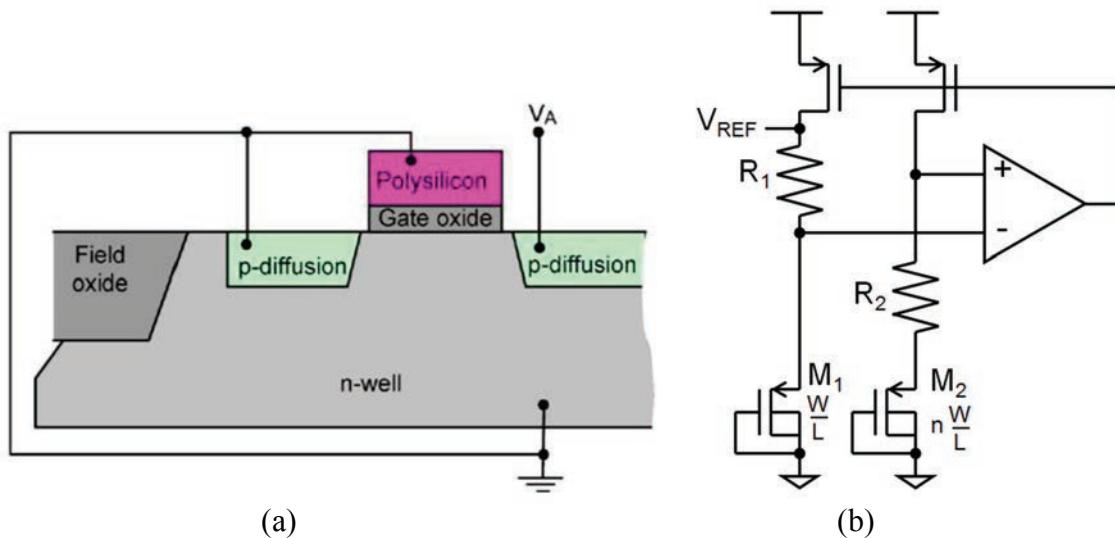


Figure 27: (a) DTMOS transistor with the gate, drain, and body grounded, while voltage is applied to the source. (b) DTMOS-based bandgap reference [35].

DTMOS transistors exhibit exponential current-voltage characteristics over the voltage range of weak inversion in the channel. Further, the voltage across the DTMOS transistor has a negative temperature coefficient, making it a suitable replacement for the *pn* junction in the bandgap reference [35], [75]. In this operating region, the forward-biased source-body junction

contributes negligibly to current consumption, and channel conduction dominates device operation.

The DTMOS-based bandgap reference exhibits excellent electrical performance and shows superior TID performance when compared to nMOS-based designs. However, the configuration is still moderately vulnerable to TID, primarily due to the induced mismatch [35]. Further, an edgeless layout does not aid in TID mitigation for DTMOS transistors because they are constructed using pMOS transistors, as shown by the results in Figure 28 where the TID response of the standard and edgeless versions of the (a) DTMOS-based and (b) nMOS-based references designed in a 180 nm bulk CMOS technology are compared. The edgeless transistor layout makes a marked difference in the TID response for the nMOS-based reference. Still, it does not impact the DTMOS design, reinforcing that the TID degradation is primarily due to STI leakage in the diode-connected nMOS transistors [35].

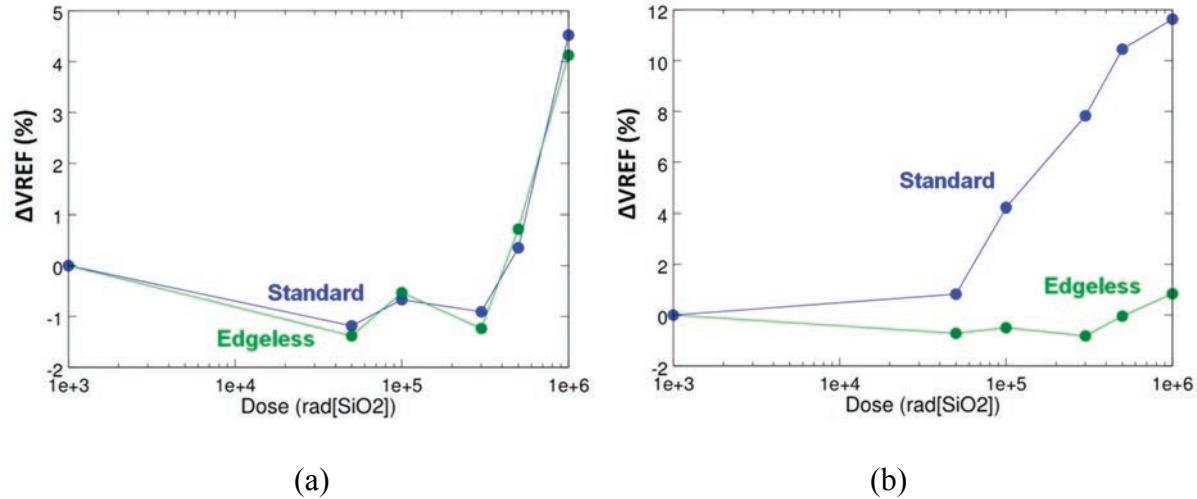


Figure 28: TID response of the standard and edgeless versions of the (a) DTMOS-based and (b) nMOS-based references [35].

3.3 Radiation Hardening by Design (RHBD) via Circuit Topology

In the event that process and device layout strategies do not result in the necessary TID performance or when process and device changes are not possible, circuit design choices can be effective in mitigating TID. This section briefly reviews TID mitigation techniques for continuous-time and discrete-time circuits and notes some system-level considerations.

3.3.1 Continuous-Time Circuits

Continuous-time circuits represent a broad class of analog electronics, most commonly designed around the operational transconductance amplifier (OTA) because resistors, inductors, integrators, multipliers, voltage regulators, buffers, and filters can all be designed with OTAs and capacitors. The primary issues with TID in continuous-time circuits are increases in input bias current [76]-[79]. These increases in bias current can induce input-referred offset voltages in OTA components, current mirror mismatch, and increased noise gain [35].

Chopper stabilization (CHS) is a modulation technique often employed in continuous-time circuits to reduce the input-referred DC offset voltage as well as the effects of $1/f$ and thermal noise [80]. CHS was introduced in 1948 using a vacuum tube and mechanical relay [81], later being realized in integrated electronics [82], [83]. Essentially, CHS applies modulation to transpose a signal to a higher frequency where there is no $1/f$ noise, demodulating the signal after amplification.

Figure 29 illustrates the CHS concept [84]. The modulation and demodulation are accomplished via the switches shown in Figure 29 (a) and Figure 29 (b) that operate on non-overlapping clocks 1 and 2. The switches act to toggle the two inputs between the inverting and non-inverting inputs of the OTA. By periodically reversing the polarity of the signal, the chopper modulates the signal to the chopping frequency, f_c , and acts to cancel any offset between the two inputs. With sufficient filtering, the amplitude of the square wave at V_F is reduced such that the output is near the ideal value [84]. This technique was applied to the voltage reference circuit shown in Figure 27 (b), and the hardened version is given in Figure

30 [84]. As seen in Figure 31, CHS is shown to completely remove TID-induced offset voltage [35][84].

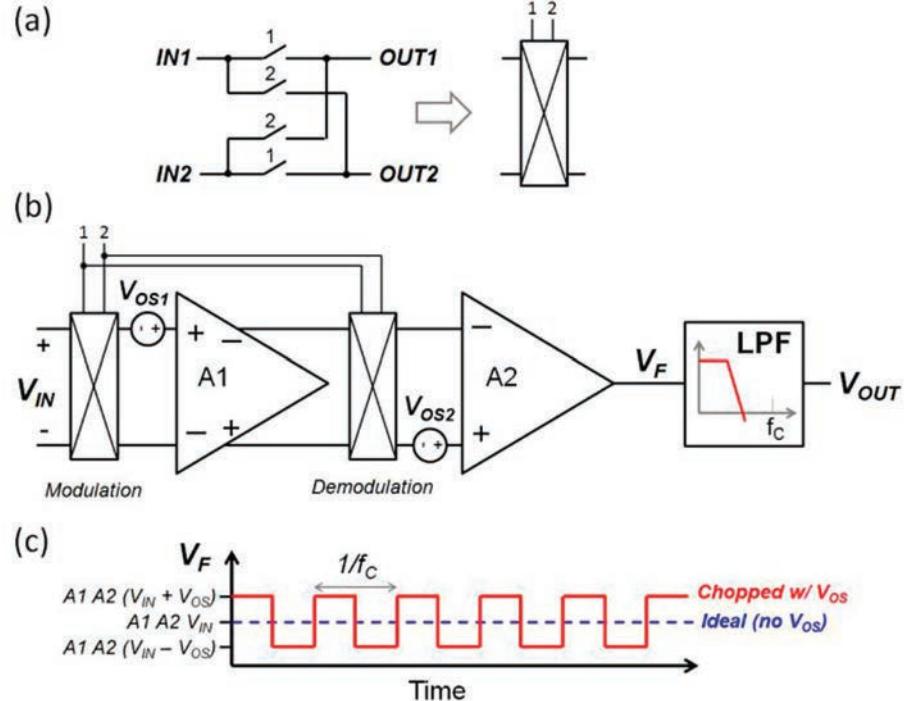


Figure 29: CHS concept illustrating the (a) chopper schematic symbol, (b) chopper amplifier followed by a low-pass filter (LPF), and the (c) output at the unfiltered output V_F [84].

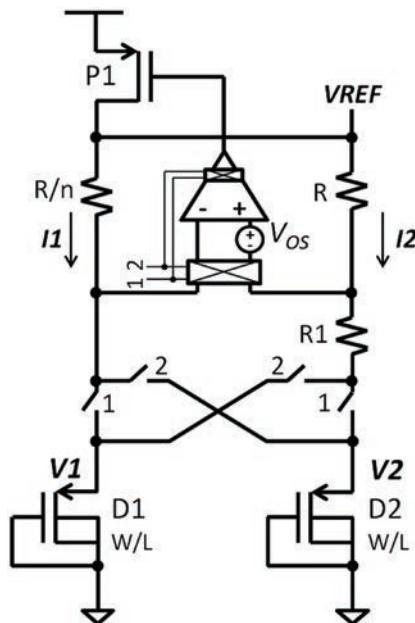


Figure 30: Radiation hardened voltage reference design employing CHS [84].

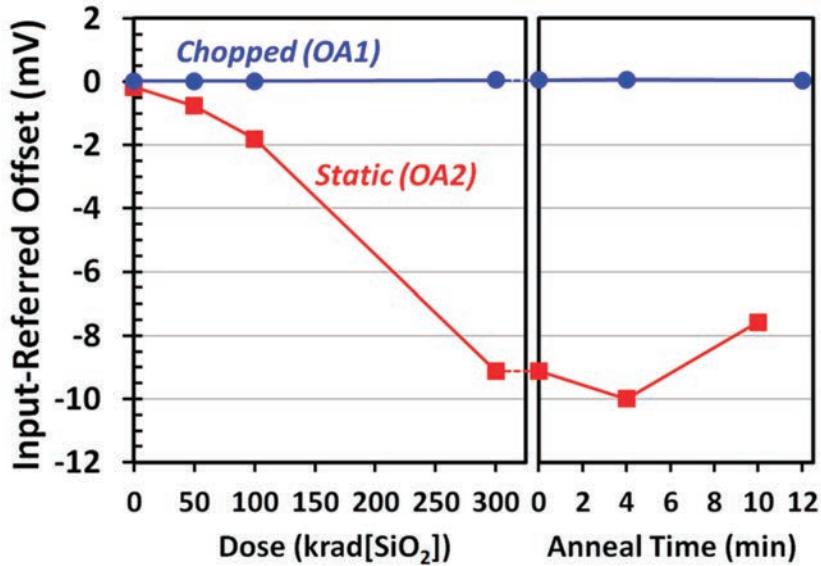


Figure 31: Input-referred offset voltage with TID for OTAs with and without CHS [35].

3.3.2 Discrete-Time Circuits

Other dynamic offset cancellation techniques applicable to discrete-time circuits include auto-zeroed amplifiers and correlated double sampling [35], [85], [86], though these works do not report TID data, focusing on the use of these techniques for the mitigation of SEE (See Section 4.0). It is not clear based on current literature if the techniques are effective against TID, but they are certainly discrete-time alternatives to CHS.

3.3.3 System-Level Considerations

While this document is focused on mitigation strategies at the device and circuit levels, it is worth noting that there are many system-level TID mitigation strategies that have been successfully realized. Some of these strategies are discussed in detail in part IV of the 2021 NSREC short course [87]. However, some system-level strategies can impact IC design choices. For example, Nicolaidis *et al.* proposed the use of current sensors at the board level to detect the excessive current induced by the SEL [55]. In this case, the system should be designed to reduce the V_{DD} of the affected device or sub-circuit and reestablish power after a predetermined period of time. Therefore, it was proposed to modify the power distribution structures to create isolated and tunable V_{DD} and V_{ss} lines.

4.0 Approaches to SEE Mitigation

The mitigation of SEE in AMS components can generally be accomplished through a “brute force” approach; that is, area, power, and bandwidth are sacrificed through the increase of capacitance, device size, and current drive to dimension the amplitude and length of SETs [88]-[91]. The challenge of radiation-hardened AMS circuit design is to develop techniques for mitigating SETs while minimizing these design penalties. This challenge is particularly daunting with state-of-the-art chip systems contain billions of transistors, integrated analog and digital, three-dimensional (3D) IC stacks, and multiple voltage domains. The critical charge to upset a device can be just a few fC.

Further complicating SEE mitigation are the effects of “charge sharing” in highly scaled nodes [92]. The historical assumption is that SEEs disturb a single sensitive volume in the semiconductor material. Reports in the literature generally indicate that the “single sensitive volume approximation” breaks down somewhere between the 130 nm and 90 nm planar technology nodes (*i.e.*, the effects of “charge sharing” between multiple sensitive volumes is not a dominant factor for 130 nm feature sizes and greater) [89], [92], [93]. The impacts of charge sharing phenomena and novel device structures (such as non-planar FETs) in the generation and propagation of SETs must be considered in more advanced integrated circuit processes.

SET mitigation, whether achieved through “brute force” or another sophisticated design approach, can be implemented at the various levels of abstraction described in Figure 32:

- Technology process level (through physical process changes).
- Device/transistor layout level (through device structural changes).
- Circuit level (through schematic/topological changes or layout changes).
- System level (through architectural changes).

While there are many circuit-specific techniques for SEE mitigation, there are essentially two strategies, irrespective of the technology and abstraction level [88]:

- Reduce the amount of collected charge (Q_{coll}) at a metallurgical junction (refer to section 4.1).

- Increase the critical charge (Q_{crit}) required to generate an SEE (refer to section 4.2).

As described in Figure 32, process-level and device layout-level abstraction levels are generally used to reduce Q_{coll} , whereas circuit topology, circuit layout, and system approaches are designed to increase Q_{crit} .

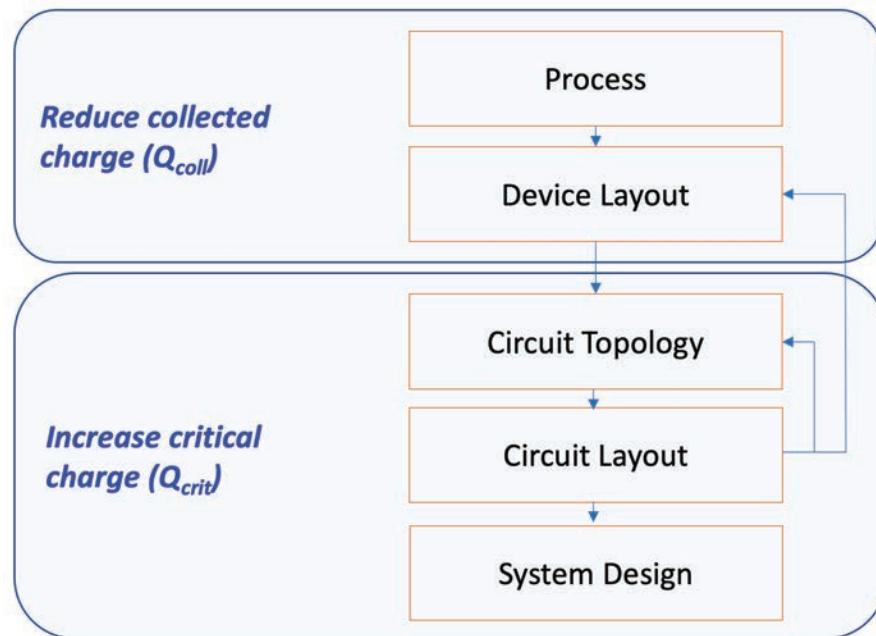


Figure 32: General SEE hardening flow including radiation-hardening by process (RHBP) and radiation-hardening by design (RHBD) via device layout for reducing the collected charge, and RHBD via circuit topology and circuit layout and radiation-hardening by system for increasing the critical charge to upset.

4.1 Reducing the Collected Charge (Q_{coll})

4.1.1 RHBP: Substrate Engineering

The reduction of Q_{coll} at a critical node of an IC requires a fundamental alteration of the technology process or the device implementation. One technology-level method for performing this reduction is substrate engineering. For example, the use of charge blocking layers in the substrate can be effective for controlling delayed charge collection from events. Figure 33 shows simulation results of the charge collected following the interaction with 36 MeV ^{16}O ions in a SiGe HBT device (5HP) [94]. The peak charge collection occurs for

strikes within the deep trench isolation (DTI), and the tails represent charge collection from events outside the DTI. Three versions of the *p*-type charge blocking layer were utilized: 10^{16} , 10^{17} , and 10^{18} cm^{-3} . Increasing the doping of the blocking layer limits the charge collection from outside the DTI [94].

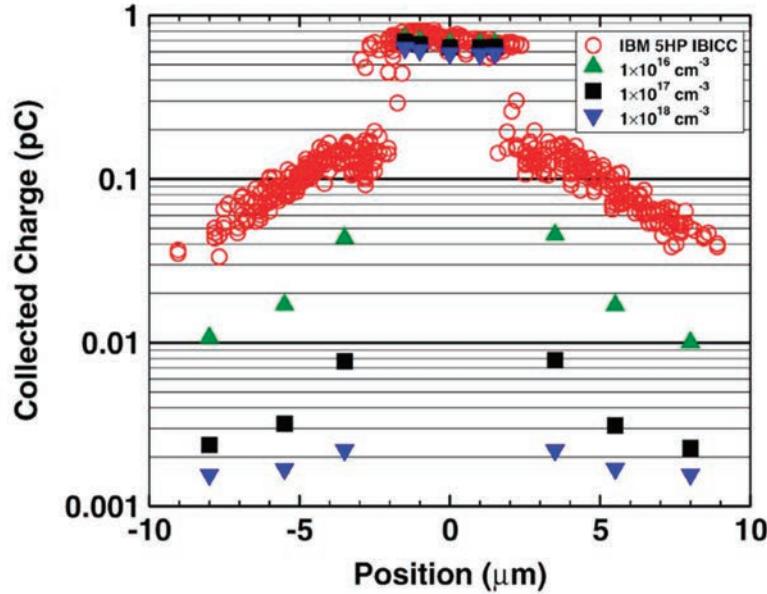


Figure 33: Simulation results showing the charge collection (following the interaction with 36 MeV ^{16}O ions) of a SiGe HBT device. The peak charge collection occurs for strikes within the DTI and the tails represent charge collection from events outside the DTI. Three versions of the *p*-type charge blocking layer were utilized: 10^{16} , 10^{17} , and 10^{18} cm^{-3} [94].

An additional example of substrate engineering is using a thin silicon layer to limit the collection volume (*e.g.*, silicon-on-insulator (SOI)) [95]. The dielectric isolation of transistors has allowed SOI technologies to be prevalent in space and military applications for over 50 years as it prevents SEL [95]. In recent years with the shrinking of gate oxide thickness due to technology scaling, modern sub-100 nm SOI devices have seen a reduction in TID effects, prompting additional interest in using the technology for space applications. Some challenges associated with design in SOI technologies include parasitic elements not present in bulk technologies [95], floating-body and history effects [96], and higher likelihoods of wave-shaping effects (*i.e.*, pulse propagation, attenuation, and broadening) [97], [98]. These circuit-level challenges with SOI generally complicate the analysis of the SE sensitivities of the

technology. However, the smaller (and inherently more isolated) sensitive volumes compared to similarly-sized bulk devices (*i.e.*, Q_{coll} is generally less for SOI than for bulk in similar feature size technologies) generally means shorter SET durations and smaller SE cross-sections [99]-[104].

4.1.2 RHBD: Layout-level Mitigation

A reduction in Q_{coll} may also be obtained through layout-level mitigation techniques. Layout-level mitigation generally involves transistor- or circuit-level modification of layout cell arrangements for reducing the amount of collected charge at critical device junctions.

4.1.2.a. Guard Rings

The historical assumption is that SEEs affect a single sensitive volume in the semiconductor material. Reports in the literature generally indicate that the “single sensitive volume approximation” breaks down somewhere between the 130 nm and 90 nm planar technology nodes (*i.e.*, the effects of “charge sharing” between multiple sensitive volumes is not a dominant factor for 130 nm feature sizes and greater) [92]-[93]. The impacts of charge sharing phenomena and novel device structures (such as non-planar FETs) on the generation and propagation of SETs must be considered in more advanced integrated circuit processes. This is often referred to as multiple-node charge collection and can result in multiple-bit and multiple cell upsets in memory circuits.

Guard rings ([105]-[108]), guard drains [108], and diodes [89] around bulk MOS devices (sometimes called guard contacts) are some common solutions to reduce multiple node charge collection and to allow for quicker recovery of the well potentials (in bulk CMOS). The isolation created between neighboring sensitive volumes is especially pronounced in pMOS devices that exhibit a propensity for parasitic bipolar enhancement. Figure 34 illustrates the layout of a typical structure that includes guard contacts between each pMOS and nMOS device (adapted from [105]). The guard contacts are formed from the same diffusion as the N-well and P-substrate contacts. They have been shown to limit the charge collection at the neighboring circuit diffusions ([105][107][108]), though at an area penalty (~30%).

Similar to guard rings, drains, and diodes for MOS technologies, the use of *n*-rings [109], substrate-tap rings [110], and nested minority-carrier guard rings [111] may be utilized in bipolar structures. Additional techniques for HBT devices (analogous to the guard rings, drains, and diodes mentioned earlier for CMOS) include the addition of dummy collectors for charge collection in HBT devices [112] and the increase in the substrate and well contacts (for a reduction in substrate and well impedances) [106], [113]-[115].

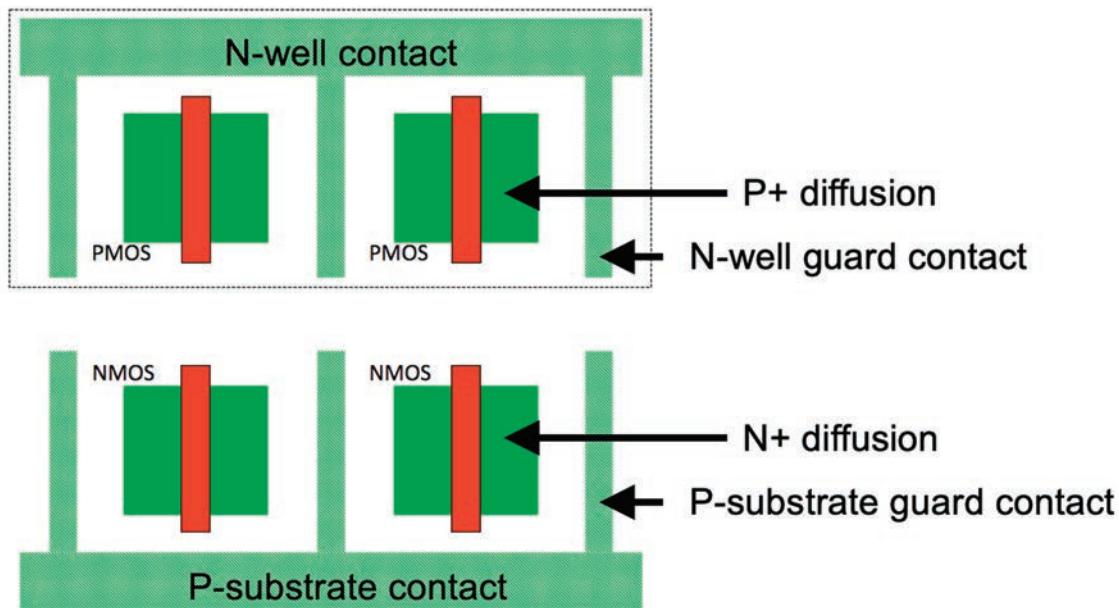


Figure 34: Generic layout that includes guard contacts between each pMOS and nMOS device (adapted from [105]).

Guard rings are also commonly used to mitigate SEL, as they can break the feedback loop between the parasitic cross-coupled BJTs. The sensitivity of a component to SEL depends on the (1) parasitic BJT gains (the product of the current gains must exceed a value of one) and (2) the distributed diffusion, well, and substrate resistances. Mitigation of SEL involves making adjustments to the process, geometry, density and spacing of wells, sources, source-to-well contacts, and source-to-source contacts in order to:

- Reduce of parasitic BJT current gain through process engineering. For example, the gain depends on channel doping, silicide proximity, and strain.

- Decouple the parasitic BJTs or increase the coupling resistance between the parasitic paths.
- Decrease the resistances from the BJTs to the well and substrate contacts.

While device layout-level approaches can reduce Q_{coll} of microelectronic devices, the methods are typically dictated by choice in technology (*i.e.*, the specific implementation is dependent on the technology or requires a fundamental change in technology parameters). Technology dependencies can be problematic in a rapidly changing technological environment (with newly developed technologies and new challenges). It should be noted that at the present time, the 5 nm to 16 nm technology nodes, developed in fully-depleted SOI (FDSOI) and bulk and SOI FinFET technologies, are in commercial development phases. Many works are evaluating the impact of this paradigm shift on the radiation vulnerability of systems ([5], [116]-[118]).

4.1.2.b. Nodal Separation

Charge sharing (*i.e.*, the collection of charge by two or more *pn* junctions following a single event) is due to the diffusion of the carriers through a semiconductor material. The reduction in nodal spacing can increase the charge collection at nodes other than the primary struck node. For older generation technologies (greater than 130 nm gate lengths as a general rule of thumb, though not a hard limit), the distances between the hit and adjacent devices are large enough to collect most of the charge at the hit node. However, for advanced technologies, the proximity of devices results in the diffusion of charge to nodes other than the hit node. With the small amount of charge required to represent a logic-HIGH state (shown to be less than one fC in 45 nm SOI [119]), the charge collected due to diffusion at an adjacent node may be significant. Figure 35 illustrates a cross-section of two adjacent nMOS devices in a bulk CMOS technology. The active node is the original ‘hit’ node, whereas the passive node refers to any adjacent node that collects charge [92].

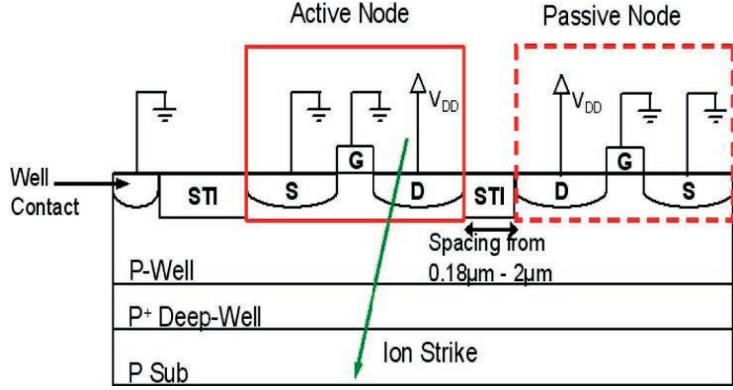


Figure 35: Cross-section of two adjacent nMOS devices in a bulk CMOS technology. The active node is referred to as the original ‘hit’ node whereas the passive node or device refers to any adjacent device that collects charge [92].

One solution for mitigating the amount of charge “shared” between adjacent nodes is nodal separation [92], [113]. Figure 36 illustrates the charge collected on the passive device versus the LET of the incident ion on the active device as a function of nodal separation. Both pMOS-to-pMOS and nMOS-to-nMOS charge sharing are illustrated and show decreased charge collection with an increase in distance between devices. Although effective, nodal separation is not a practical solution when considering the demands for higher packing densities and increased speeds.

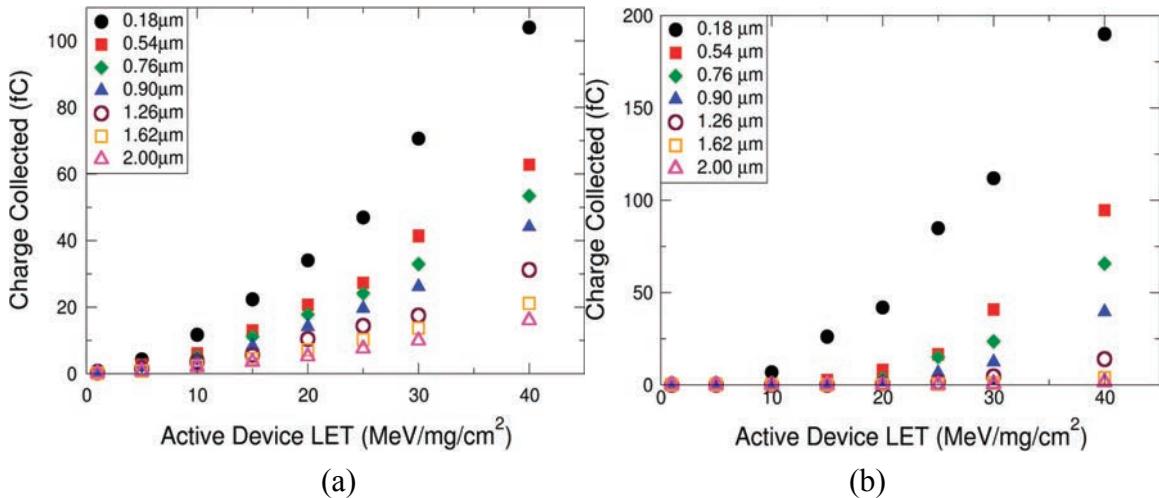


Figure 36: (a) Nodal separation of two pMOS devices: passive pMOS device shows a decrease in charge collection with increase in distance. (b) Nodal separation of two nMOS devices: passive nMOS device shows a decrease in charge collection with increase in distance [92].

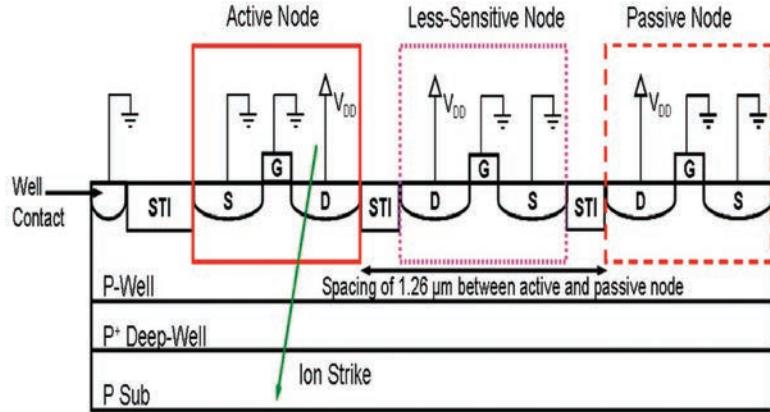


Figure 37: Cross section showing active and passive nMOS devices. The less-sensitive node is placed between the active and passive devices in interleaved designs [92].

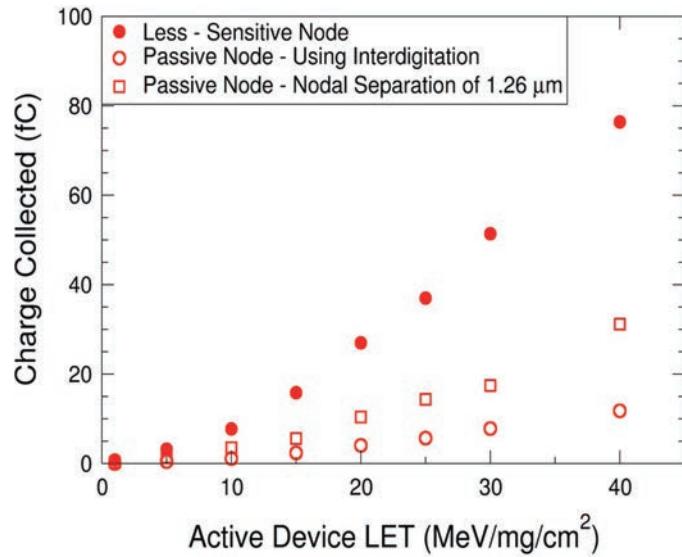


Figure 38: Charge collected on passive device with and without interdigititation [92].

4.1.2.c. Interleaving / Interdigititation

Interdigititation, or interleaved layout, is a technique that takes advantage of the benefits of nodal separation and guard contacts while maintaining device density requirements. Provided that the designer has knowledge of the sensitive circuit nodes as well as those that pose less of a threat, the less sensitive transistors can be placed between pairs of sensitive devices (Figure 37), and the nodal spacing between critical devices can be increased while maximizing density [92]. This method has been successfully implemented in dual interlocked

cell (DICE) and other redundancy-based designs [120]-[124]. Figure 38 illustrates simulation results showing the charge collected on neighboring, passive devices with and without interdigitation. Interdigitation lowers the charge collected on the passive device, even when compared to equivalent nodal spacing. The less-sensitive node place between the sensitive pair acts as a guard ring, further reducing the collected charge.

4.1.2.d. Hardening via Charge Sharing

Given the challenge of providing sufficient nodal separation to mitigate the effects of charge sharing, another hardening method takes a very different approach by encouraging the charge sharing phenomenon in differential circuit topologies. The “Hardening via Charge Sharing” techniques (HCS) bridge between RHBD via layout modifications and RHBD via circuit modifications, most often relying on the careful interplay between the two levels of abstraction.

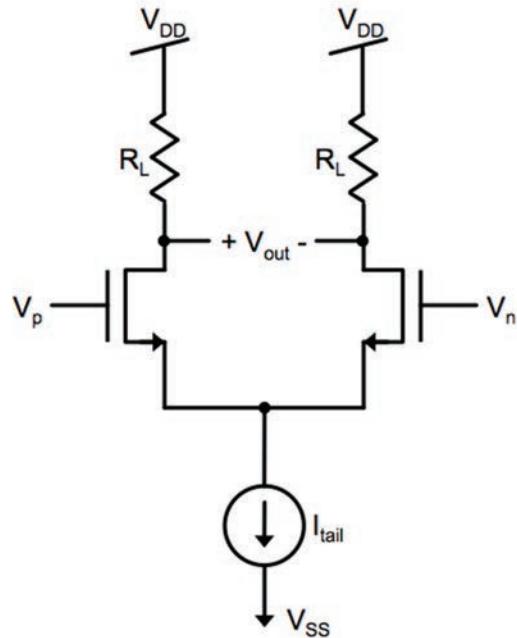


Figure 39: Basic schematic of a differential pair.

Differential circuits are commonly used in high-performance analog design due to their improved dynamic output range and better noise rejection over their single-ended counterparts. Figure 39 depicts a differential pair, often used as an input to an integrated amplifier. Two

transistors are connected such that any differential voltage applied to the inputs ($V_{id} = V_p - V_n$) is amplified, and any common-mode voltage (*i.e.*, a voltage applied to both V_p and V_n) applied to the inputs is rejected. However, an SEE occurring in circuitry feeding one of the input gates of the differential pair or in one of the devices in the differential pair can perturb the voltage at the input. This voltage perturbation, not common to both inputs, will result in a transient output voltage.

While the differential topology is inherently a circuit-level approach, various layout-level strategies can improve the SE performance over single-ended designs. Hypothesized in [125] and shown for the first time through simulations in [126] and experiments in [127], the layout of matched transistors in a differential data path can be modified to exploit the charge-sharing phenomenon, thereby causing any SET to be rejected as a common-mode perturbation. Almost simultaneously, the use of charge sharing was exploited in digital design in [128] and is termed “pulse quenching.” Since discovering pulse quenching, many digital design techniques have employed the concept for improving the SE performance [129].

HCS is fundamentally different from typical methods for reducing Q_{coll} as HCS does not attempt to limit Q_{coll} at a single node but instead the differential Q_{coll} between two nodes. The layout of critical device pairs may be modified to maximize charge sharing. One such technique, termed *differential charge cancellation* (DCC) [126], minimizes the distance between the drains of matched devices in the differential pair and maximizes the likelihood of an ion strike affecting both sides of the differential pair through the common-centroid layout. It should be noted that the common centroid technique is typical for differential design to improve transistor matching but does not require that the distance between the drains in the differential pair be minimized as in DCC layout.

Figure 40 illustrates two layout variations of the differential pair, including devices A and B before and after DCC layout for maximizing charge sharing. Each transistor in the DCC configuration is split into two devices and placed diagonally. The device pairs should be arranged in a shared well with drains located as close as possible to promote common-mode charge rejection.

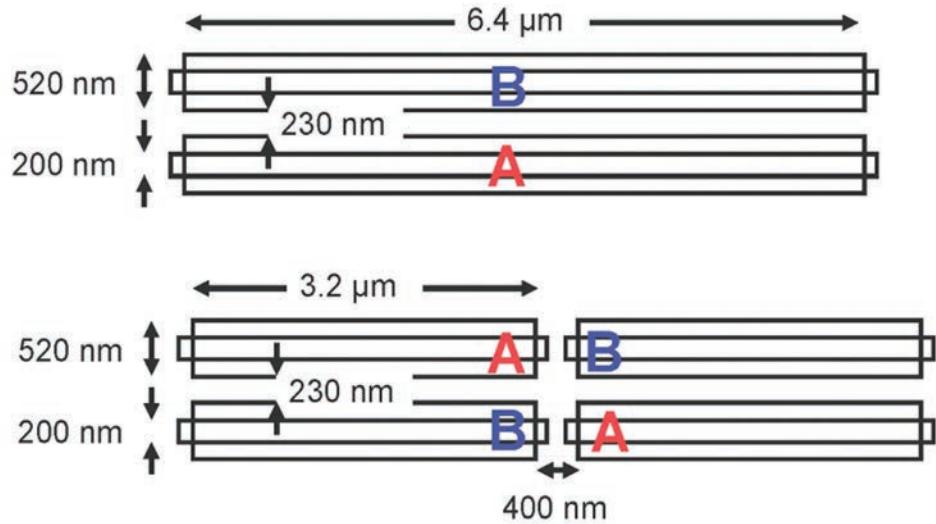


Figure 40: Differential pair including devices A and B before (single pair or SX) (top) and after DCC layout (parallel unit cell or PX) (bottom) for maximizing charge sharing [127].

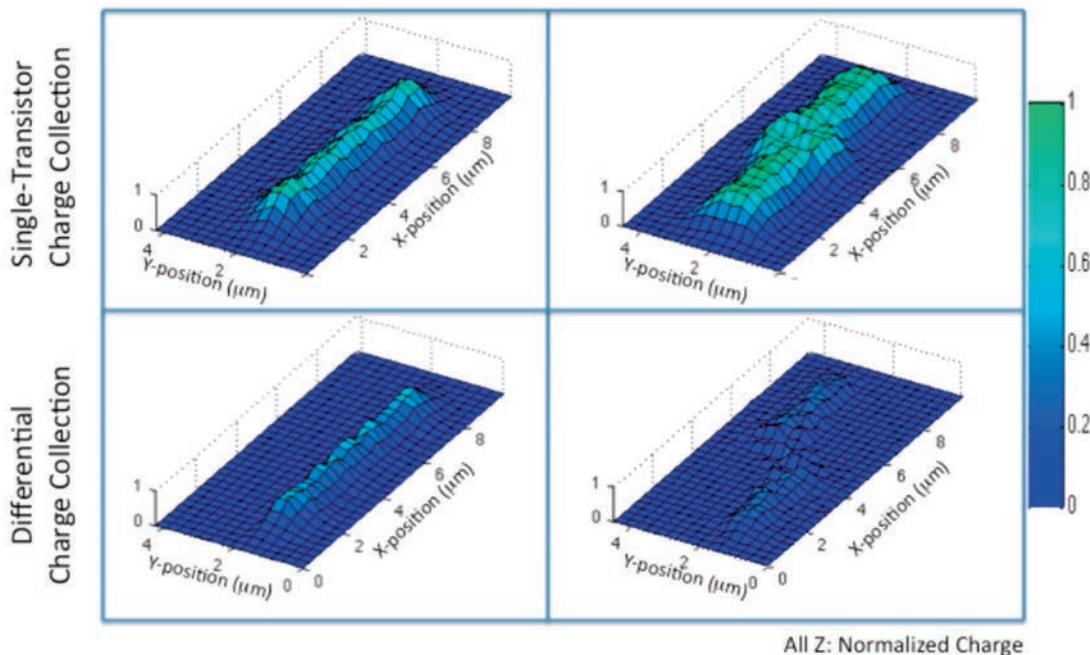


Figure 41. Surface plots of experimentally measured charge collected at points in the die scan for transistor A of the differential pair. The charge was injected using a laser two-photon absorption technique. Single-transistor charge collection is shown in the top row for the two-device configuration (left) and common-centroid layout (right). The differential charge is shown in the bottom row [127].

The devices in Figure 40 were fabricated in a commercial 65 nm technology, and laser TPA was used to deposit ehp in localized spots within the devices [127]. The resulting collected

charge measurements are shown in Figure 41, depicted as surface plots. Each pixel represents the relative collected charge at points in the die scan for transistor A of the differential pair. Single-transistor charge collection is shown in the top row for the two-device configuration (left) and DCC layout (right). The differential charge is shown in the bottom row. The DCC layout configuration is shown to decrease the sensitive area by over 90%. The performance advantage can be quantified by integrating over the surface area of the sensitive transistors. Figure 42 illustrates the distribution of Q_{coll} versus the device area for the baseline single transistor (BLSX) (top left in Figure 41), baseline differential unit cell (BLPX) (top right in Figure 41), and DCC single transistor (Differential SX) (bottom left in Figure 41) and DCC differential unit cell (Differential PX) (bottom right in Figure 41).

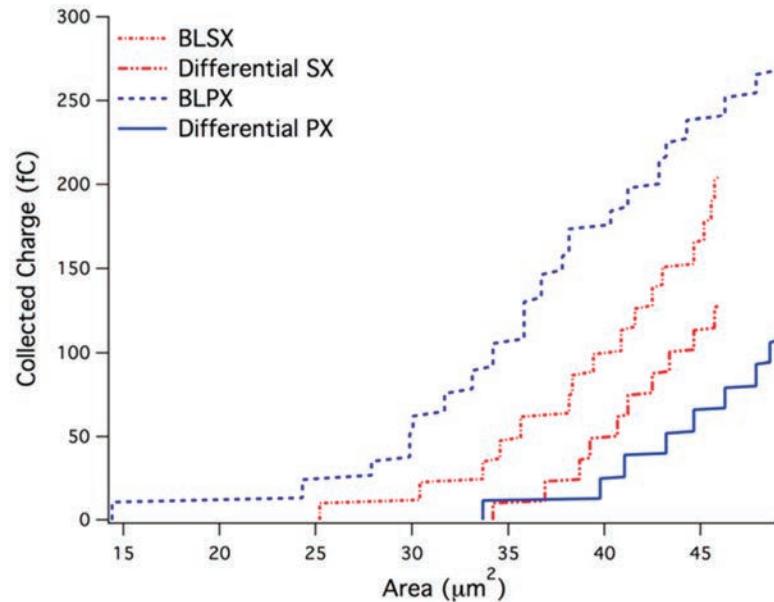


Figure 42. Cumulative distributions of collected charge versus device area for each of the four scenarios from [127].

Since a DCC layout is essentially a variation of a common-centroid layout used to improve matching in analog circuits, its use in differential input stages results in minimal layout penalty for the designer. In many cases, a DCC layout requires only minor changes in one or two metal layers of a standard analog layout. Furthermore, the DCC layout technique can be extended anywhere along symmetrical differential signal paths.

The DCC hardened layout technique takes advantage of charge sharing between adjacent transistors by using common-mode cancellation in differential signal paths. The HCS concept can be extended beyond layouts alone and exploited at the circuit level in AMS designs by using a combination of DCC layouts and appropriate analog circuit topologies [130].

Figure 43 illustrates one HCS technique termed sensitive node active charge cancellation (SNACC) that exploits charge sharing to create a compensation source for mitigating extraneous charge [130]-[132]. SNACC can be used to harden critical nodes that have a global effect on a larger circuit, *e.g.* the output node of a bias circuit for an op amp, or the reference circuit of a data converter. SNACC works by balancing out collected charge with an equal but opposite amount of charge at a critical node, with a net charge (ideally) of zero at the affected node.

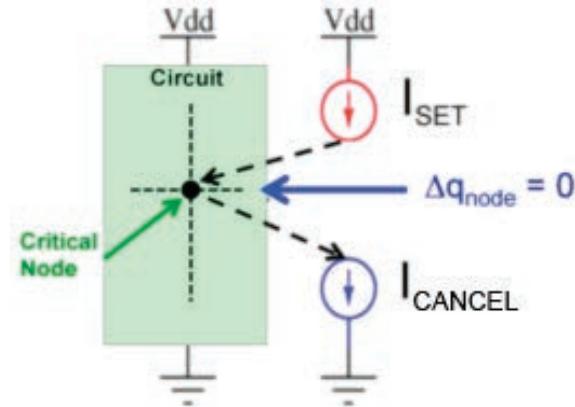


Figure 43: The sensitive node active charge cancellation (SNACC) hardening technique [130].

Figure 44 shows a complementary folded cascade op amp design, with transistors M27 through M30 forming a bias circuit for the amplifier. Any single-event transients that perturb bias voltages V_p , V_n , or V_{np} will affect the entire amplifier circuit. To prevent this, several additional transistors can be added to the bias circuit as shown in Figure 45. Transistors S1 through S8 form the SNACC circuit. The following transistor pairs have DCC layouts: M27-S1, M28-S2, M29-S7, and M30-S8. Collected charge on a sensitive junction in M28 through M30 is shared with its DCC “twin”, resulting in an equal but opposite current pulse being coupled into the bias circuit nodes through the S3-S4 or S5-S6 current mirrors. The

cancellation will not be perfect due to the different time constants of the two propagation paths, but the amplitude and duration of SETs can be reduced by more than 60% [132].

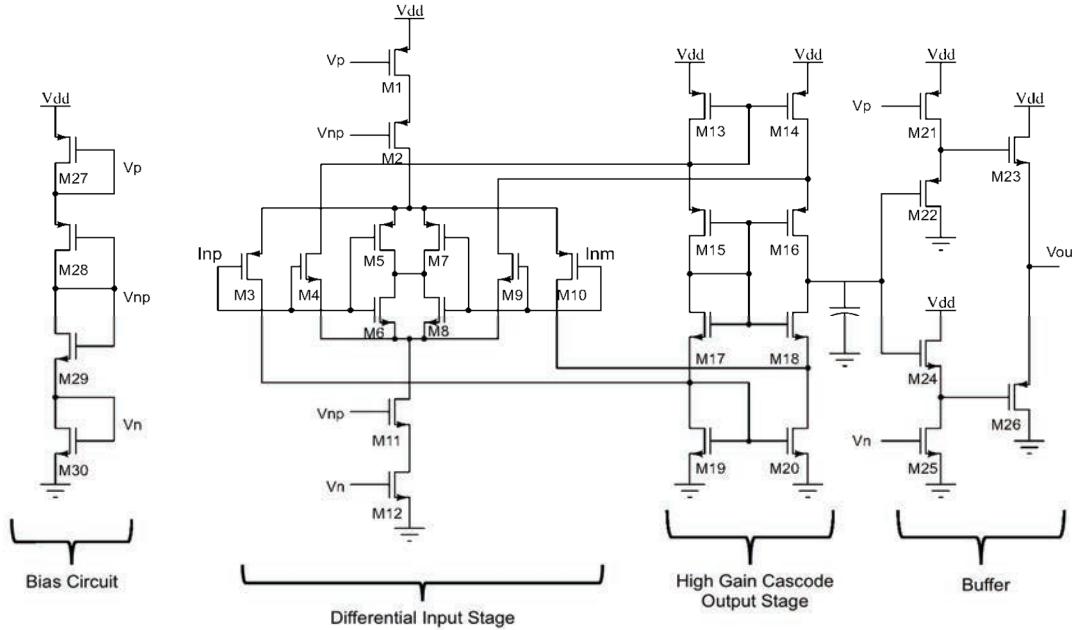


Figure 44: A complementary folded cascode op amp that is suitable for hardening using SNACC [132].

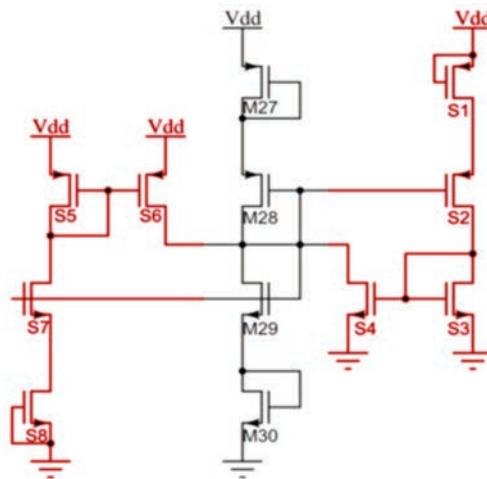


Figure 45: A SNACC-hardened op amp bias circuit with SNACC transistors highlighted in red [132].

Figure 46 shows the simulated response illustrated using error energy (an integral function of the SET) in conjunction with cumulative distribution function (CDF) plots. For a sampling of a random variable, a CDF describes the probability of observing a given value or smaller. The CDF plots show an output error energy X versus the probability that the observed error energy value will be X or smaller. In all cases the error energies were measured at the output node of the op amp configured in unity gain mode and biased with a common-mode input voltage of $V_{DD}/2$ [132].

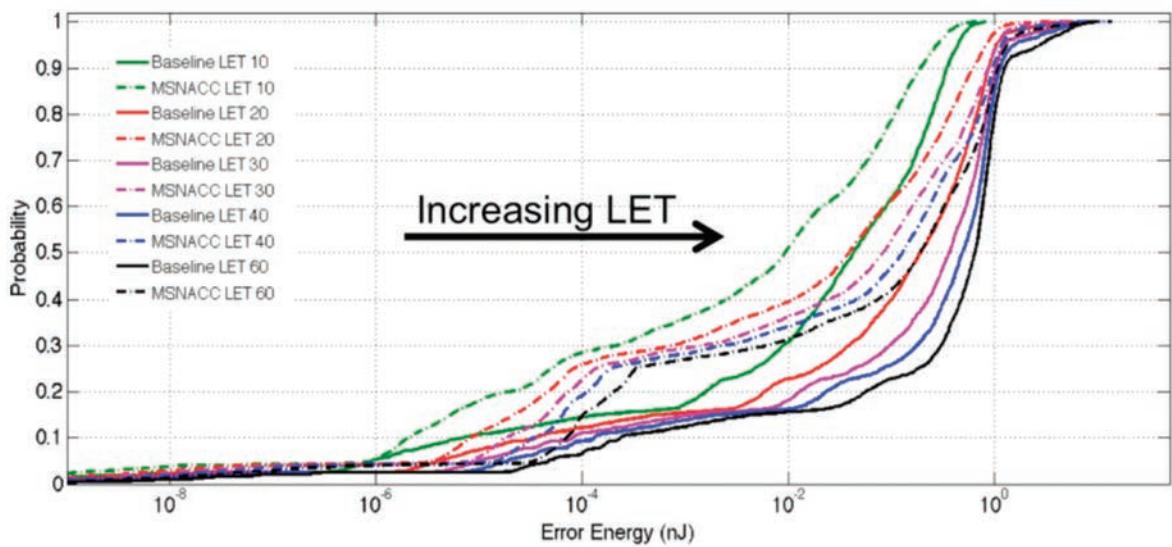


Figure 46: Cumulative distribution functions showing the probabilities of upset for energies originating in the operational amplifier's bias circuit with and without SNACC hardening following normal incidence strike for varying LET.[132].

It is not necessary for the SNACC transistors to have the same width-to-length ratios as the transistors they protect; the sizes of S1 through S8 can be scaled proportionally to save area, with the shared charge amplified by the SNACC current mirrors. Furthermore, strikes on the SNACC transistors do not affect the bias circuit, since charge sharing and cancellation also take place in a path from the SNACC transistors to the bias circuit transistors. The SNACC transistors have a negligible effect on the circuit's power consumption, since they are customarily biased off. The main design penalty is increased layout area, but SNACC is only needed for a few critical nodes. In the case of the op amp in Figure 44, the increase in area was only 7%.

In some circuits, the SNACC concept can be implemented without adding additional transistors. For example, consider the high gain cascade output stage of the op amp in Figure 44. If transistor pairs M13-M14, M15-M16, M17-M18, or M19-M20 are laid out in DCC configuration, collected charge on any of these devices will be shared, mirrored, and cancelled at the output node (the drains of M16 and M18) of the stage, with a mitigation mechanism essentially identical to that of the SNACC bias circuit. As this example illustrates, AMS circuits with symmetrical sub-circuit topologies are obvious candidates for the implementation of HCS techniques. The main drawback of HCS is that it cannot be used in IC fabrication processes such as silicon-on-insulator (SOI), where charge sharing is minimal or non-existent. For bulk processes, however, HCS techniques can be very effective in mitigating SETs.

4.2 Increasing the Critical Charge via Circuit and Layout Modifications

Methods for increasing Q_{crit} of a device or circuit may seem at first glance (at least from a circuit designer's point of view) to be more straightforward. In other words, a designer may operate under the assumption that the physical process (thus the amount of collected charge) cannot change, thus requiring creative solutions to limit the impact on the circuit. Conventional, perhaps "brute force" methodology, all designed to counteract extra charge, include [39]: increasing the transistor sizes (buffering) [90], [91], raising the drive currents [39], increasing the supply voltage [39], increasing capacitor sizes [39], and implementing redundancy [133].

Additionally, various mitigation techniques for AMS circuits can be found in the literature covering a wide range of topologies. Some common AMS circuits discussed in this section include OTA, LNAs, bandgap voltage references, VCOs, injection-locked oscillators (ILOs), PLLs, SerDes, comparators, and ADCs. Although many circuit-level mitigation techniques seem to be topology-specific, the fundamental hardening mechanisms have much in common. The remainder of the section presents an overview of the current state-of-the-art in SEE mitigation in AMS circuits. It organizes the techniques based on the root cause mechanisms.

4.2.1 Redundancy

While more common in digital circuits, triple modular redundancy (TMR) has been successfully used in mixed-signal circuits with digital output signatures, such as the voltage comparator. This approach was adopted in [133] where a single comparator was replaced by three parallel comparators driving a CMOS majority-voting circuit. The voting circuit was hardened by over-sizing the transistors.

Olson *et al.* [134] further evaluate tradeoffs of comparator redundancy when implemented in a pipelined ADC. While TMR effectively mitigates transients in the comparators, SE improvement reaches a point of diminishing returns after TMR is applied to the first half of the pipeline (*i.e.*, improvement is maximized when redundancy is implemented on the most significant bit or MSB). As seen in Figure 47, the signal-to-noise ratio (SNR) metric was used to compare the SE hardness of different circuit designs. By randomly injecting upsets into the circuit (via simulation) and analyzing the response in the frequency domain, the SNR indicates the impact of the SEs on the overall response of the circuit. The error rate referred to in the analysis corresponds to the probability of an event appearing within a conversion cycle, and not a radiation environment rate. While this technique assumes a simulated SE rate that is much too high to ever occur in an actual circuit, it does allow for hardness comparisons between different designs.

Figure 47 shows the SNR for increasing use of comparator TMR in a 10-bit pipelined ADC. Results shown are for a model with an individual comparator upset probability of 0.1% and 100%. The application of comparator TMR to the first half of the 10-bit pipelined ADC produces the best tradeoff in decreasing single event vulnerability versus increasing area and power. Note that even assuming extremely high comparator upset rates, comparator TMR is most effective when applied to the first 50% to 70% of the total number of stages. Similar results are shown regardless of ADC resolution [134].

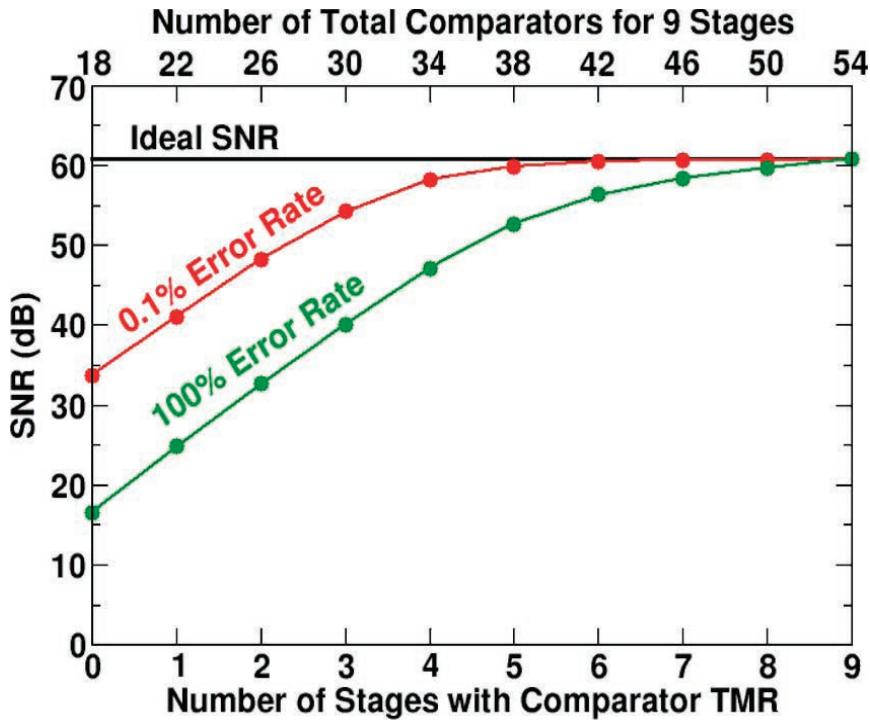


Figure 47: Signal-to-noise ratio improvement for increasing use of comparator TMR in a 10-bit pipelined ADC. The results shown are for a model with an individual comparator upset probability of 0.1% and 100% and are compared to the ideal SNR [134].

Redundancy has been applied to VCO and PLL topologies in several ways: (1) dual redundancy [135], (2) selective TMR, for example in the biasing circuitry [136], and more commonly by (3) replicating the VCO [137]-[141]. The designs are all shown to reduce the output phase displacement following ion strikes at varying area, power, and noise penalties based on TMR selectivity.

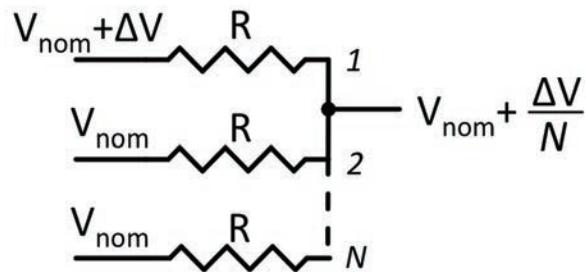


Figure 48: Analog averaging through the use of N identical resistors, R . A perturbation (ΔV) due to an SE strike on any one copy of the circuit is reduced to $\Delta V/N$ [142].

4.2.2 Averaging (Analog Redundancy)

Analog averaging is a form of hardware redundancy for the reduction of spurious transients. The averaging of an analog voltage can be accomplished by replicating and parallelizing a circuit N times and connecting the replicated nodes through parallel resistors to a common node, as seen in Figure 48 [142]. A perturbation (ΔV) due to an SE on any one copy of the circuit is reduced to $\Delta V/N$. This technique has been offered to solve the observed vulnerability of a charge pump for PLLs by implementing in the bias circuitry of the VCO [137]. Kumar *et al.* propose a similar approach to harden the charge pump and VCO blocks of a PLL by including two independent CP/LPF blocks controlling two cross-coupled VCO circuits [143]. This type of strategic redundancy can limit area and power penalties.

4.2.3 Node Splitting

One of the most versatile and practical methodologies for hardening AMS circuits is that of *node splitting* or HNS. HNS can be used in both discrete-time (*e.g.*, switched capacitor) and continuous-time circuits, for any integrated circuit process, and in many cases has almost negligible impact on circuit performance, layout area, or power dissipation [144]-[149]. HNS hardening is a form of redundancy in its simplest, as shown in Figure 49. The idea is to divide a circuit into two or more parallel signal paths, such that an ion strike on one path does not affect the other path(s). However, the key difference is that the parallel paths may be reduced gain paths, partial computations, or split (peeled) layouts, such that the sum of all paths is equivalent to the original function. Examples of HNS include dual- ([144], [145]) and quad-path [146] switching capacitor circuits, and peeled layouts ([148]) in operational amplifiers and comparators. It is also important to note that HNS is not purely a circuit-level mitigation strategy and requires careful consideration in the layout domain.

Ideally, the struck path will be disabled, so that the remaining path(s) will maintain signal integrity. However, even if the struck path is not disabled, the remaining signal path(s) will still tend to mitigate the amplitude and duration of the SET. Although HNS techniques are well suited to differential circuit topologies, they can be applied to single-ended circuit topologies as well.

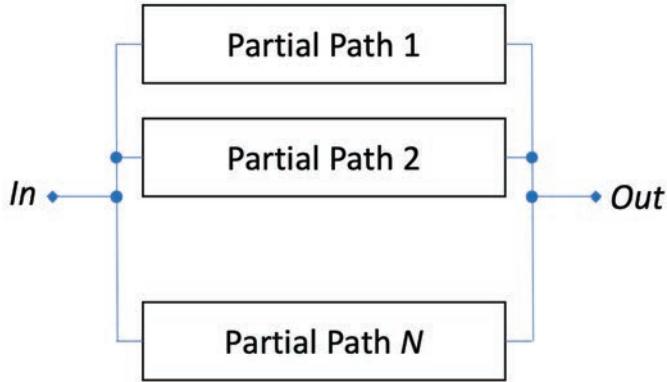


Figure 49: An illustration of the concept of hardening via node splitting.

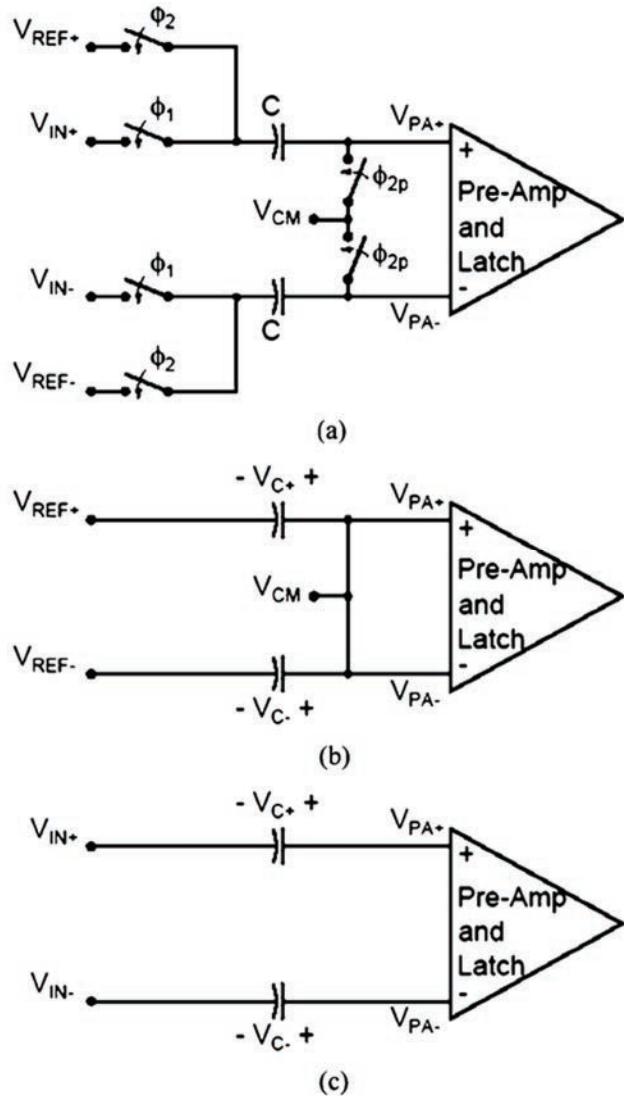


Figure 50: (a) The switched-capacitor comparator operates in two phases: (b) reset phase and (c) evaluation phase. The clocked switches are realized by nMOS transistors [145].

Dual path hardening was developed to significantly reduce the SET vulnerability of differential switched-capacitor circuits [144]-[146]. Due to the floating (high impedance) capacitive node, switched capacitors are notoriously sensitive to SEE and are typically avoided. The principle of the technique is to split the input nodes into separate parallel signal paths to provide significant immunity to a voltage perturbation on any single floating node of a switched-capacitor signal paths. This technique is applicable to any differential switched capacitor circuit and has been used with OTAs and comparators in [144] and [145].

Figure 50 illustrates a standard switched-capacitor comparator design as commonly used in pipelined ADCs [145]. The comparator operates in two phases: the reset phase when the common-mode voltage is applied to both inputs, and the evaluation phase when the two inputs are compared. A voltage perturbation in the differential data path of the comparator (due to an ion strike on a nMOS switching transistor) may cause erroneous data to be latched at the comparator output if a floating capacitor node is affected (in other words, no path exists for dissipating the collected charge).

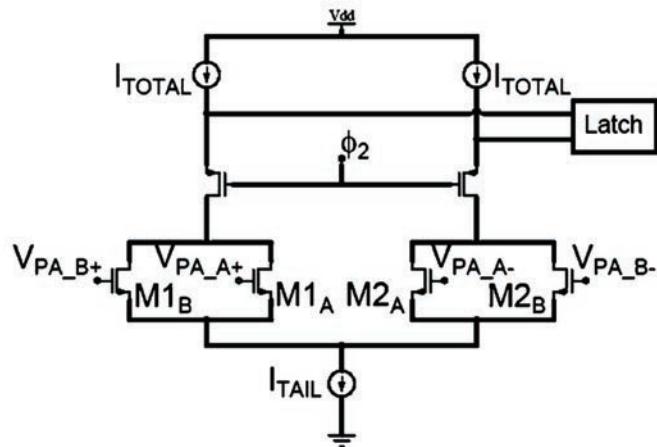


Figure 51: Simplified circuit schematic of the differential amplifier showing the split input paths [145].

Dual signal path hardening can be applied to prevent the majority of such errors from generating an erroneous latched value. Figure 51 shows the comparator with dual inputs employed in the differential input stage. Input transistors M1 and M2 are each split into two identical transistors connected in parallel such that the width-to-length ratio of each parallel

device is one-half the width-to-length ratio of the original transistor. If the gates of M1A and M1B are shorted together, the configuration is identical to a standard differential amplifier. The switched-capacitor differential input network is also duplicated, as shown in Figure 52.

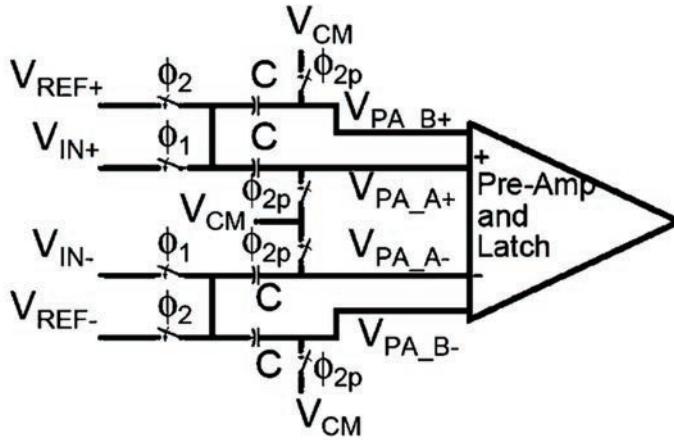


Figure 52: The switched-capacitor comparator with split differential amplifier input paths to harden the floating nodes against single-event upsets [145].

If one of the two signal paths is struck by an ion, the result is that the struck path is disabled, and the remaining path maintains signal integrity. Simulation and experimental results indicate significant improvement in single-event performance. Figure 53 illustrates results from laser TPA experiments on comparators designed in the AMI 0.5 μm bulk CMOS process with and without dual-path hardening [149]. The amplitude of the voltage error of the switched capacitor network follows the charge-to-voltage law ($Q = CV$) but saturates to values correctable by standard digital error correction. This is accomplished without any area, power, or performance penalties, as the capacitors and switches were all halved in size when duplicated. The main drawback is the increased complexity in layout. The technique was also successfully applied to the MDAC circuit within an ADC [149].

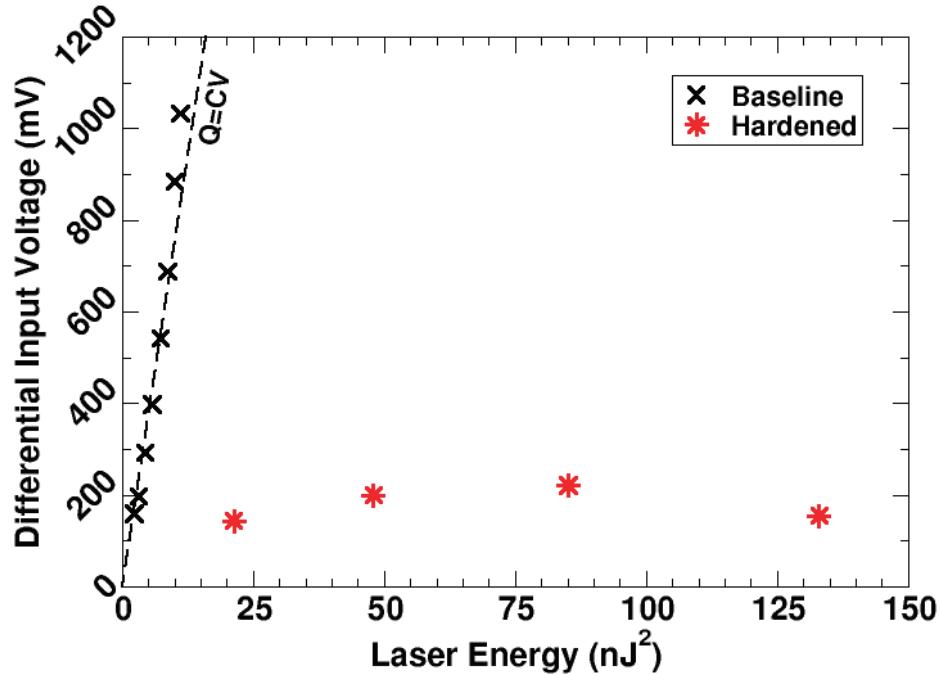


Figure 53: Results from laser TPA experiments on comparators designed and fabricated in the $0.5\text{ }\mu\text{m}$ bulk CMOS process with and without dual-path hardening [149].

The primary drawback of dual-path hardening is that the transistor switches must be the same type as the input transistors, *i.e.*, nMOS switches with nMOS inputs (or pMOS switches with pMOS inputs). This requirement ensures that the struck path will be disabled (*e.g.*, an ion strike on an nMOS switch pulls the gate of the nMOS input transistor to ground and shuts it off), but also limits dynamic input range, which makes dual-path hardening impractical for low voltage circuits. To address this limitation, quad-path hardened designs have also been developed with parallel nMOS-to-nMOS and pMOS-to-pMOS signal paths, as shown in Figure 54. Quad-path hardening has been proven to be even more effective than dual-path hardening in mitigating SETs, at the added cost of increased layout complexity.

Dual-path and quad-path hardening have minimal design penalties beyond added layout complexity. In terms of noise, power dissipation, and frequency response, dual- and quad-path hardened switched-capacitor circuits perform essentially identically to their unhardened counterparts. The additional area required by the split signal paths is almost negligible compared to the area of the capacitors, making these HNS techniques very attractive for high-performance AMS systems.

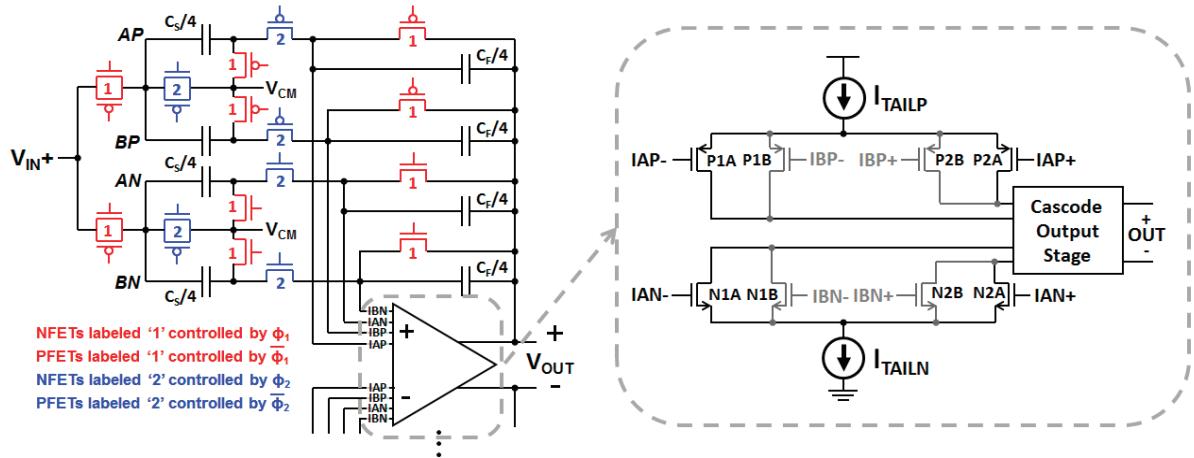


Figure 54: Schematic showing half of the quad-path S/H amp topology (negative half is identical) and simplified schematic of modified quad-input complementary folded-cascode OTA.

Hardening via peeled layouts is a form of HNS applicable to continuous-time circuits. In a peeled circuit, the layout is split or “peeled” into two halves, limiting the charge collection volumes to half of the original circuit. Figure 55 shows this concept applied to the input stage of an OTA [147]. The SET mitigation is accomplished by the separation of internal nodes between the two peeled paths, with the input and outputs effectively “wired-ORed” together. This technique will not reduce the SEE cross-section but will reduce the severity of the SETs, as shown via simulation of the baseline and peeled input stages in Figure 56 where a scatter plot of the maximum perturbation in voltage is plotted versus the settling time for strikes in every node within the OTA input stage. In Figure 56, the dark gray symbols represent strikes in the peeled input stage, whereas the light gray symbols represent strikes in the traditional input stage. The amplitude is attenuated in most cases.

As with dual-path and quad-path layouts, continuous-time peeled layouts have almost negligible effect on electrical performance, but in terms of overall SET mitigation they are not nearly as effective. However, recent works have attempted to improve the effectiveness of layout peeling with massively peeled layouts and strategic “smart” peeling of select and highly vulnerable sub-circuits [147], [148].

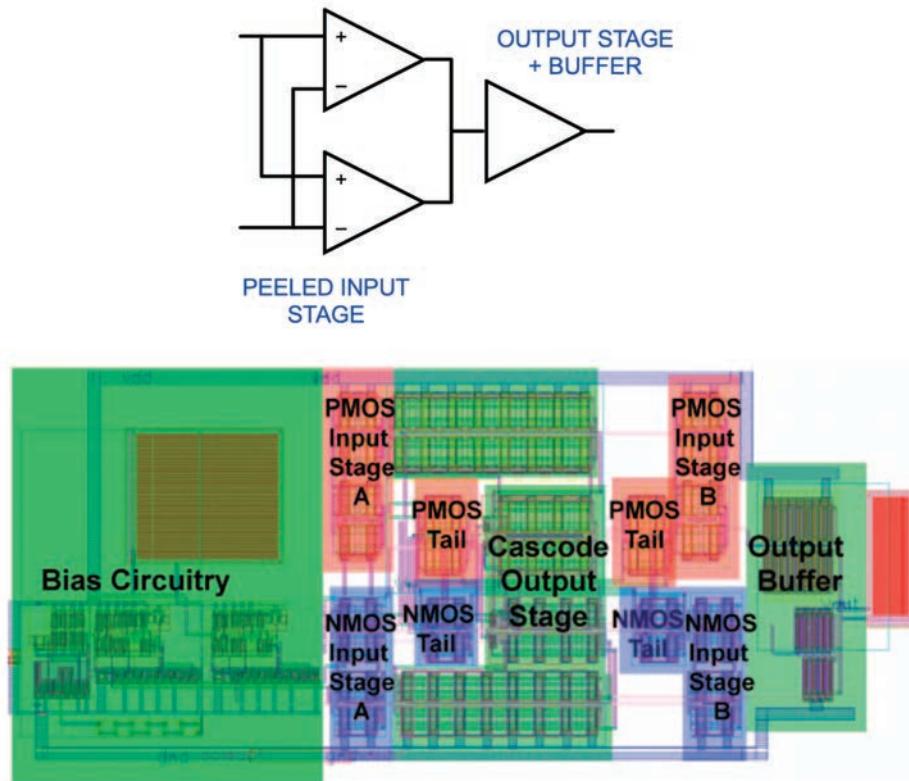


Figure 55: A peeled layout in an operational amplifier. The peeled input stage is shown in red and blue [147].

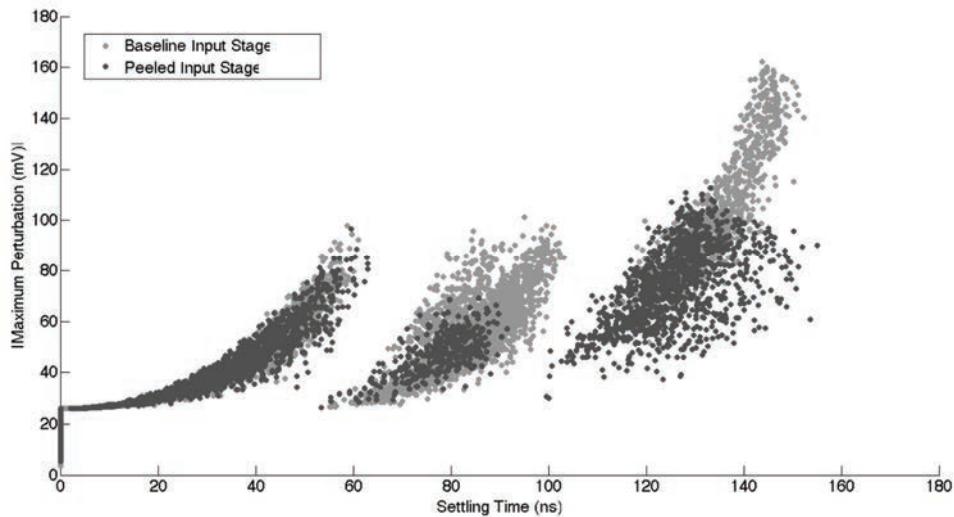


Figure 56: A peeled layout in an operational amplifier. The peeled input stage is shown in red and blue [147].

4.2.4 Dynamic Offset Cancellation

Dynamic offset cancellation techniques (see section 3.3.2 for TID mitigation) can also be effective at limiting the severity of SEE. Auto-zeroed CMOS comparators, which involve sampling and resetting the comparator's initial state each clock cycle, can limit the length of an SET to a single clock period [150]. Auto-zeroed amplifiers have also been implemented with dual-path hardening in [151], though no radiation results are reported.

4.2.5 Resistive Decoupling

Resistive decoupling was first published in 1982 as a technique for hardening memory cells [152], [153]. Series resistors are introduced in the cross-coupling lines of the inverter pairs in a static memory or a flip-flop. The resistors effectively increase the time constant seen by the two storage nodes and limit the maximum change in voltage during an SET, thus increasing the Q_{crit} required to change the state of the cell.

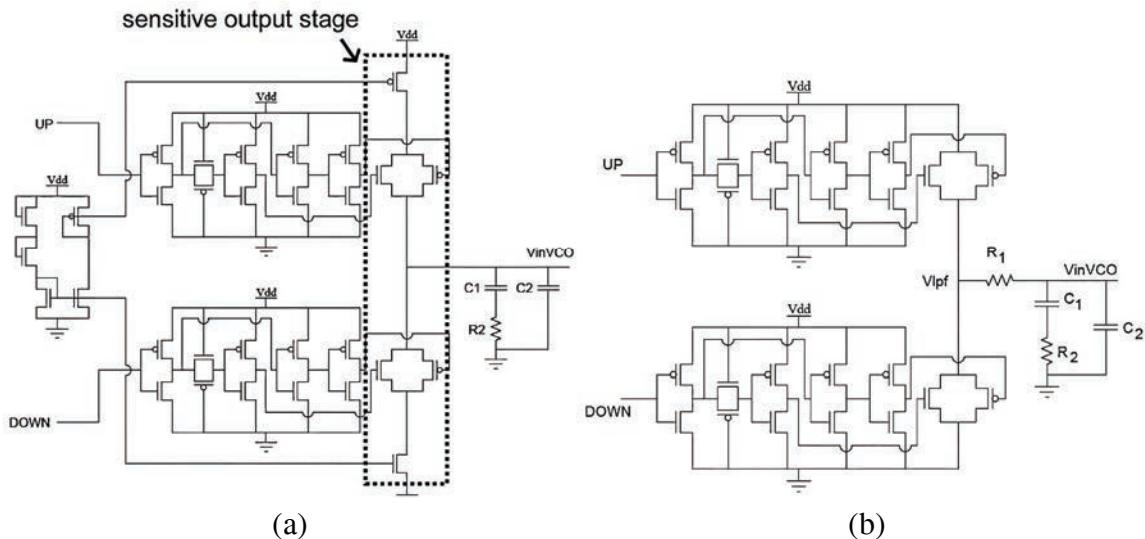


Figure 57: (a) A standard current-based charge pump configuration for PLL circuits. The sensitive output stage (high-impedance tri-state configuration) is directly coupled to the control voltage of the VCO. (b) Single-event hardened voltage-based charge pump configuration. The hardening mechanism relies on the high gain of the charge pump and the resistor R_1 to decouple the charge pump switches from the capacitive output node [40].

The resistive decoupling technique is also used in AMS circuits for hardening digital latches, such as those present at the output of voltage comparators in an ADC [154]. A similar technique may be used to filter high-frequency transients by decoupling nodes sensitive to

analog single-event transients (ASETs) and introducing a time constant through a series resistor or low-pass filter. This was shown in [40] and [41], where the high-impedance output of a charge pump circuit was decoupled from the capacitive input to a VCO. As seen in Figure 57, the number of sensitive nodes present in the output stage of the charge pump (Figure 57 (a)) may be reduced and subsequently decoupled from the VCO control voltage, V_{inVCO} (Figure 57 (b)).

Results from laser TPA excitation in standard and RHBD PLLs can be seen in Figure 58, where (a) the laser cross-section (sensitive area determined through a two-dimensional (2D) raster scan) of PLL sub-circuits is plotted versus the square of laser energy (proportional to deposited charge [43]) and (b) the number of erroneous clock pulses is plotted versus operating frequency at an incident laser energy of 30 nJ [41]. The hardening mechanism relies on the high gain of the charge pump (with lower output impedance when compared to the standard approach in Figure 57 (a)), and the resistor R_1 to decouple the charge pump switches from the capacitive output node [40]. The importance of the high impedance nodes will be discussed further in section 4.2.8.

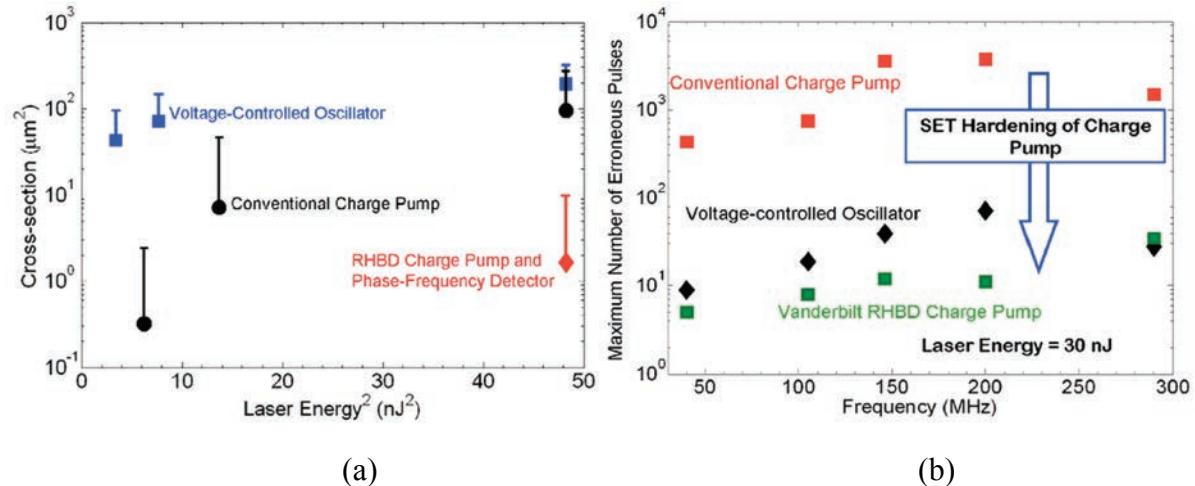


Figure 58: (a) The laser cross-section (sensitive area determined through a 2D raster scan) of PLL sub-circuits is plotted versus the square of laser energy (proportional to deposited charge [43]) and (b) the number of erroneous clock pulses is plotted versus operating frequency at an incident laser energy of 30 nJ. Approximately 2 orders of magnitude improvement in both the laser cross-section and number of erroneous pulses seen through the use of the hardened charge pump circuit [41].

4.2.6 Filtering

Filtering is a standard method for reducing the amplitude and duration of SETs at circuit- and system-levels, and a logical progression from the use of resistors to decouple sensitive nodes. Low-pass or bandpass filters may be added to critical nodes in order to suppress fast SETs, where the value of the filter depends on the circuit or system bandwidth [36]. Through computer-assisted system-level analysis, Boulghassoul *et al.* studied the SET response on an analog power-monitoring network. As seen in Figure 59, slight modifications to the passive component networks (*i.e.*, adjustments to the bandwidth) can reduce both the amplitude and duration of SETs with no change to steady-state bias conditions [155]. The approach has also shown effective in suppressing high frequency noise and SETs generated from the charge pump sub-component of a PLL ([40], [41]) and in hardening the bias nodes of a SerDes [156]. The use of LPFs for the mitigation of SETs in advanced CMOS memory circuits is also shown feasible for suppressing transients ≤ 50 ps [157].

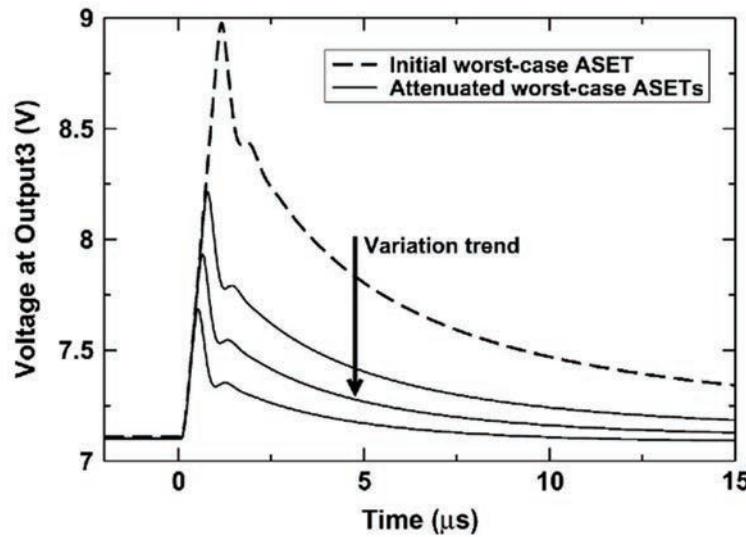


Figure 59: Simulated output voltage transients in a power monitoring network for various resistor values in the op amp feedback networks. Lowering of the resistance has the effect of reducing the amplitude and duration of transients [155].

Increasing the capacitance at nodes vulnerable to SEs can also reduce the amplitudes of the resulting SETs by increasing the amount of required charge to induce a voltage perturbation. This is often used when the performance specifications are not adversely affected [158]. The increase of nodal capacitance often alters characteristic parameters such as gain and

bandwidth. The subsequent section will discuss mitigation techniques when such characteristics are paramount.

4.2.7 *Modifications in Bandwidth, Gain, Operating Speed, and Current Drive*

No matter the chosen circuit-level mitigation approach, all choices function through the modification of characteristic circuit parameters such as gain, bandwidth, frequency, and drive strength. Each technique may require special attention in compromising performance tradeoffs (most AMS circuits already have stringent design requirements with little room for modification). One effective way to reduce the circuit's sensitivity to SETs is to reduce the part's bandwidth, thereby suppressing all transients outside of the frequency band. This rule of thumb can be thought generally applicable to analog topologies that can be expressed as closed-loop amplifier structures. It has been shown applicable in various studies on OTAs [36], [155], [158] and PLLs [159], [160], both of which can be represented as a closed-loop amplifier. However, Boulghassoul *et al.* [155] and Sternberg *et al.* [158] also discuss the importance of examining the severity of an SET with respect to the circuit application. For example, the threshold for an application is typically determined by both SET amplitude and duration. Sternberg *et al.* have pointed out that, depending on the origin of the SET, the duration of the pulse may increase as modifications are placed to decrease the amplitude. Therefore, specific consequences regarding the size of the resistors, compensation capacitors, and stage gains may occur and require special attention. In general, as seen by Loveless *et al.* regarding PLLs [160] and Sternberg *et al.* regarding OTAs [158], it appears that maximizing speed and minimizing the open- and closed-loop gains may improve the SET response.

Operating speed plays an interesting role in determining the SET response of analog circuits. As previously mentioned, analog circuits have been shown to exhibit reduced SET vulnerability for increased operating frequency [158], [160]. This is contrary to that typically observed in digital systems, where increasing error cross sections as a result of SETs induced in combinational logic have been observed for increasing operating frequency [161]. In digital circuits, an SET can result in an SEU and lead to a circuit error if the corrupted data propagates throughout the circuit and is observable at the output. The ability of the SEU to reach the circuit output depends on the logical and electrical masking as well as the window of vulnerability

(latch window masking). The result of latch window masking is that for equivalent SET pulse widths, faster circuits have a higher probability of being latched into memory. In analog electronics, however, increased speed is often accompanied by increased drive current and an improved ability to dissipate the deposited energy, making the circuit less vulnerable. It is thus essential to attribute the improvement to either speed or drive strength, as increased bias current is a well-known technique and is often used in AMS circuits for improved SET performance [156]. The enhanced performance may or may not be as a result of increased speed, but rather subtle changes in the individual device operating conditions such as bias, current drive, and load.

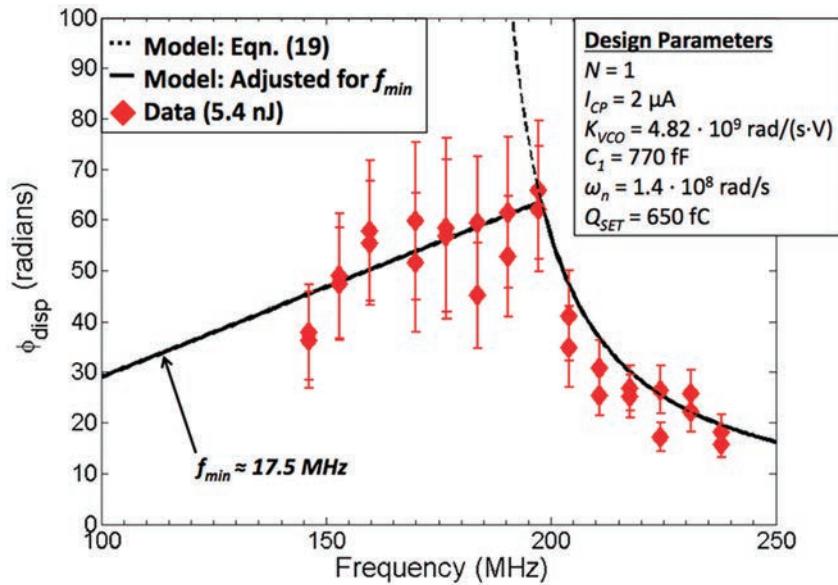


Figure 60: Average phase displacement versus lock frequency within the PLL's operating region for incident laser energy of 5.4 nJ plotted against the model shown in [160].

The importance of device operating conditions as separate from operating speed is discussed in regard to SET mitigation of mixed-signal PLL circuits in [160]. For a particular oscillator design, for example, it is shown that the operating frequency should be maximized within the designed bandwidth (consistent with that shown in [158] for OTAs). On the other hand, the natural frequency of the PLL (analogous to the response time of the closed-loop PLL and not to be confused with the output frequency) is found to amplify transients in the PLL resulting from ionizing radiation and thus should be reduced to improve the SET response of the PLL. Figure 60 illustrates this effect by plotting the results output phase displacement of a

PLL versus the operating frequency. Data were obtained through TPA experiments and plotted alongside an analytical expression for determining an upper bound for good radiation performance [160]. The phase displacement is observed to decrease with increasing frequency due to a complex interaction of the drive strength, natural frequency, and loop gain. The error (phase displacement) decreases with decreasing frequency in the low frequency regime (< 200 MHz in this case) because the VCO following the strike reaches the designed minimum frequency of operation [160].

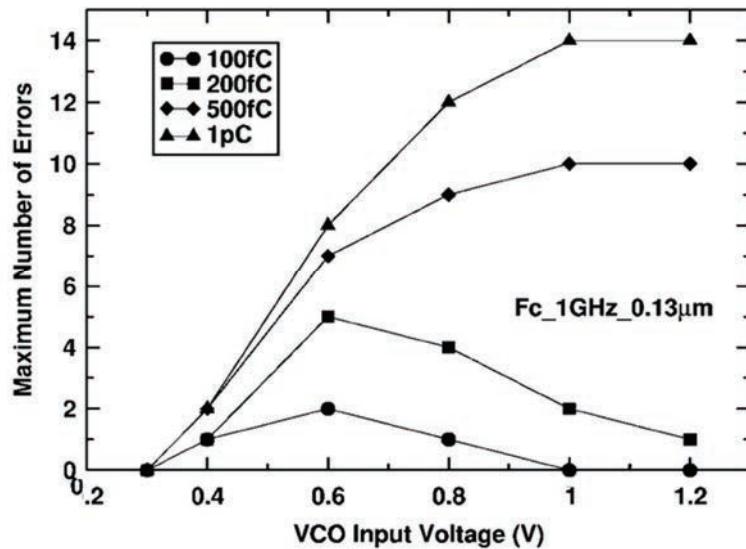


Figure 61: The simulated maximum number of errors generated by ion strikes as a function of the VCO input voltage. The VCO was designed in a 130 nm CMOS process and has a center frequency of operation of 1 GHz [162].

The coupling between drive strength and frequency can be also observed for a VCO as a stand-alone sub-circuit, though for different reasons. Figure 61 illustrates the simulated maximum number of errors generated by single ion strikes (total injected charges of between 100 fC to 1 pC) as a function of the VCO input voltage (which is proportional to drive strength and frequency) [162]. The VCO was designed in a 130 nm CMOS process and has a center frequency of operation of 1 GHz. For injected charges less than or equal to 200 fC, the number of errors increases then decreases with increasing input voltage. The eventual decrease (and in some cases, elimination) of the number of errors is due to the increasing drive currents with increasing input voltage. Stronger drive currents will restore the nominal bias conditions faster, thus compensating for the current perturbation. For injected charges greater than or equal to

500 fC, the maximum number of errors increases with increasing input voltage. This is due to the increase in oscillating frequency, resulting in a greater number of cycles with the characteristic time of the charge collection [162], [142].

Chung *et al.* show that the magnitude of the error response to transient perturbations in the PLL increases for increasing bandwidth, further indicating the importance of bandwidth in determining the SET response of the topology [159]. Figure 62 illustrates the simulated error response (in units of radians) of the PLL versus time for various PLL bandwidths. Increasing the PLL bandwidth is often accompanied by decreases in lock time (improved speed) and increased jitter (can be considered as noise for practical purposes). Tradeoffs in operating speed, jitter, settling time, bandwidth, and SET performance should be carefully considered.

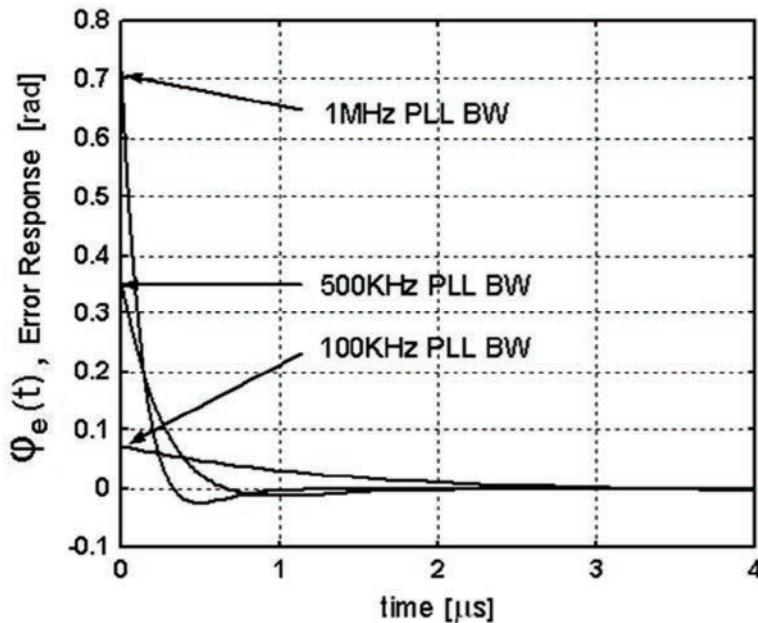


Figure 62: Transient PLL error response as a function of PLL bandwidth (BW) [159].

Through the efforts of Boulghassoul *et al.* in understanding the effects of scaling on the SET sensitivity of high-speed RF circuits, it is shown that the SET performance is not merely set by the bandwidth, but the gain-bandwidth product. For a given bandwidth, large gains result in degraded SET performance. Additionally, for the VCO circuits described, the optimum operating ranges are technology specific; the topologies discussed perform worse than a circuit in the same technology but with a smaller gain-bandwidth product, or worse than

a circuit in an older technology at comparable speeds. More importantly, de-rating the frequency in a state-of-the-art technology node does not compensate for the increases in radiation vulnerabilities at that node [162].

4.2.8 Reduction of High Impedance Nodes

One powerful technique for reducing the nodal sensitivity of AMS circuits is to reduce or eliminate high impedance nodes, thus improving the recovery times of the circuit following ion strikes. Similar approaches are often employed for reducing noise, by created low-impedance paths to shunt harmonic power out of a circuit [163], [164]. W. Chen *et al.* applied this to SEE mitigation through circuit modification of a cross-coupled differential and voltage-controlled Colpitts oscillator [165]. Through additional pMOS cross-coupled switching pairs at the oscillator output and decoupling the tail current source, output low impedance nodes were created and significantly improve the SET performance. Lapuyade *et al.* implemented a similar approach in an ILO designed using a SiGe BiCMOS process [166]. First, a pMOS cross-coupled pair is utilized to increase the transconductance. Further, the length of SETs is shown to decrease when operating in the injection locked mode. In general, free running oscillators tend to exhibit poor SET performance when compared to synchronized oscillators such as the ILO and VCO implemented in a negative feedback loop such as a PLL [40], [41], [136], [166], and [167],

Sutton *et al.* provide a technique for creating a low impedance path within a SiGe HBT device, designed to shunt charge away from the collector terminal. The path is realized by including an additional reverse biased *pn* junction formed between the *p*-substrate and guard ring (*n*-ring) resulting in a secondary electric field [109].

5.0 A Look to the Future of RHBD

State-of-the-art chip systems contain billions of transistors, integrated analog and digital, 3D IC stacks, and multiple voltage domains. Consequently, the development of future hardened electronics systems will likely experience many new challenges.

5.1 Unknown Radiation Effects in Emerging Devices

The disruption of technology scaling, moving from planar MOS to FDSOI and multi-gate structures, as seen in Figure 63, has allowed for better electrostatic control of the gate stack, allowing continued reduction in effective gate lengths [168]. However, as seen in Figure 64, the technology disruption can result in new radiation vulnerabilities and additional process and operating condition variation [169]-[171]. The historical trend of improving TID and worsening SEE with technology node may not be valid moving forward. TID and SEE mitigation strategies must be interwoven, especially for AMS circuits that may have acute sensitivities to TID through analog components and SET vulnerabilities.

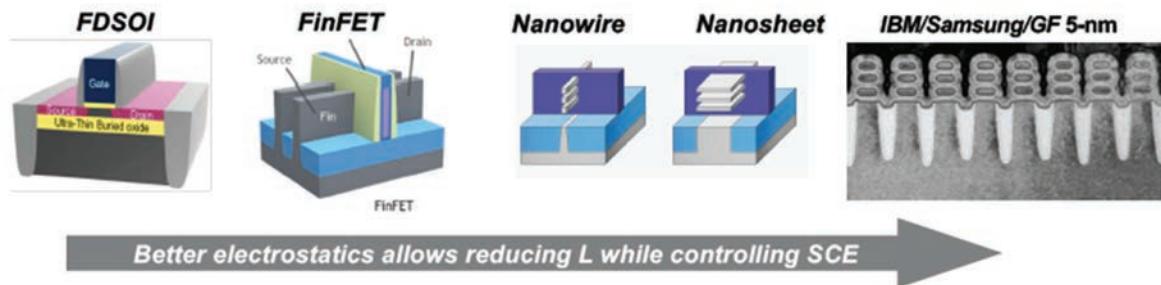


Figure 63: Semiconductor technology development post planar CMOS [168].

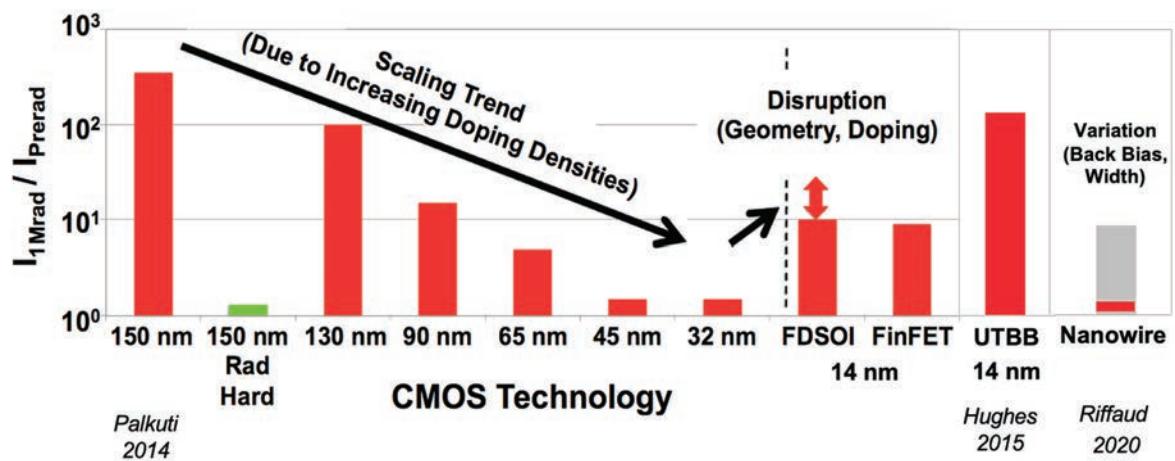


Figure 64: Ratio of post-rad (1 Mrad(SiO_2)) to pre-rad leakage current versus CMOS technology. Data from [169], [170], and [171].

5.2 Critical Charge will be a Fraction of a fC

Regardless of the uncertainties arising due to the post-Moore device disruptions [5], advanced IC technologies are seeing smaller and smaller critical charge values. Figure 65 illustrates the equivalent deposited energy to create an SEU versus year of technology release [172]. Low-energy protons, alpha particles, and muons may become increasingly problematic for managing SEE sensitivity. The general increase in SEE sensitivity will create additional challenges with:

- The development of RHBD libraries with restricted manufacturing options.
- Integrated modeling, simulation and experimental analysis methodologies for advanced technology ICs.

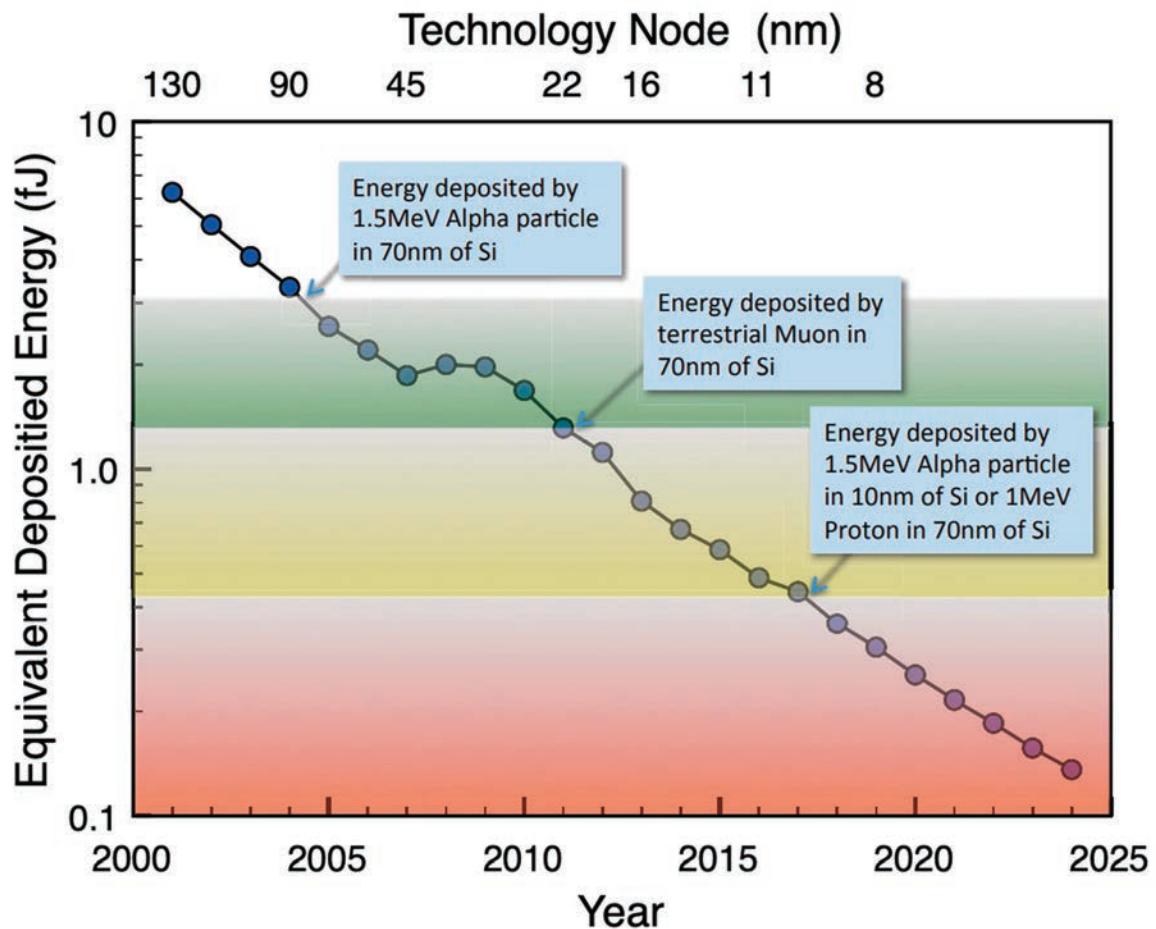


Figure 65: Equivalent deposited energy to create an SEU versus year of technology release [172].

5.3 Multi-Dimensional Integrated Technologies

The ability to integrate analog, digital, optical, memory, sensing, programmable, and RF technologies into a single-wafer and multi-tiered stacked wafers has allowed for incredible advancements in SoC applications. Figure 66 shows a 3D IC developed at Stanford with an integrated sensor layer, embedded resistive-RAM, and carbon nanotube FET technology with an embedded classification accelerator for machine learning (ML) [173]. Radiation hardness assurance for such technologies present unexplored challenges, yet new opportunities in RHBD (refer to section 5.5).

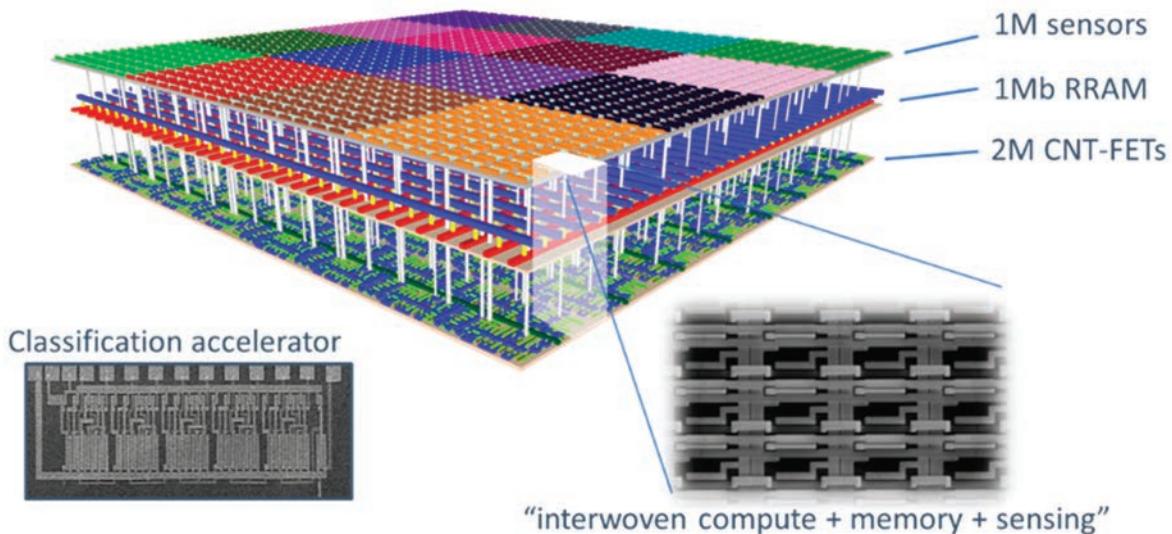


Figure 66: Three-dimensional (3D) IC developed at Stanford with an integrated sensor layer, embedded resistive-RAM, and carbon nanotube FET technology with an embedded classification accelerator for machine learning [173].

Radiation effects studies in these 3D stacked technologies [174]-[177] indicate that there is a growing need to understand the fundamental failure mechanisms and contributions of these configurations on radiation effects. The complexities of vertical integration present great difficulties in analyzing SEE and will require the study of novel component integration schemes with interleaving modeling and high-energy experimental approaches. Specific needs are:

- The effects of multi-tier charge-sharing presents previously unexplored challenges.

- There is a need for integrated process, layout, topology, and system-level RHBD approaches.
- New radiation effects testing methods and increased use of high-energy beam capabilities may be required.

5.4 Increased Use of Commercial-Off-the-Shelf (COTS) Components

The increased use of commercial-off-the-shelf (COTS) components demands new multi-scale modeling [79] and high-level RHBD approaches [178]. Hardening of COTS components may involve the introduction of radiation-hardened modules with unhardened intellectual property (IP) prior to fabrication, or system approaches to mitigating radiation effects without modification of any individual component.

In [178], an on-chip digital dosimeter [179] was integrated with an ARM Cortex-R4F processor and a body-bias generator circuit prior to fabrication, as seen in Figure 67. The SoC allows for modification of threshold voltages through body-biasing based on accumulated dose and has the effect of reducing TID-induced power increases. The compensation technique was shown to increase the TID tolerance from 50 krad(Si) to 700 krad(Si).

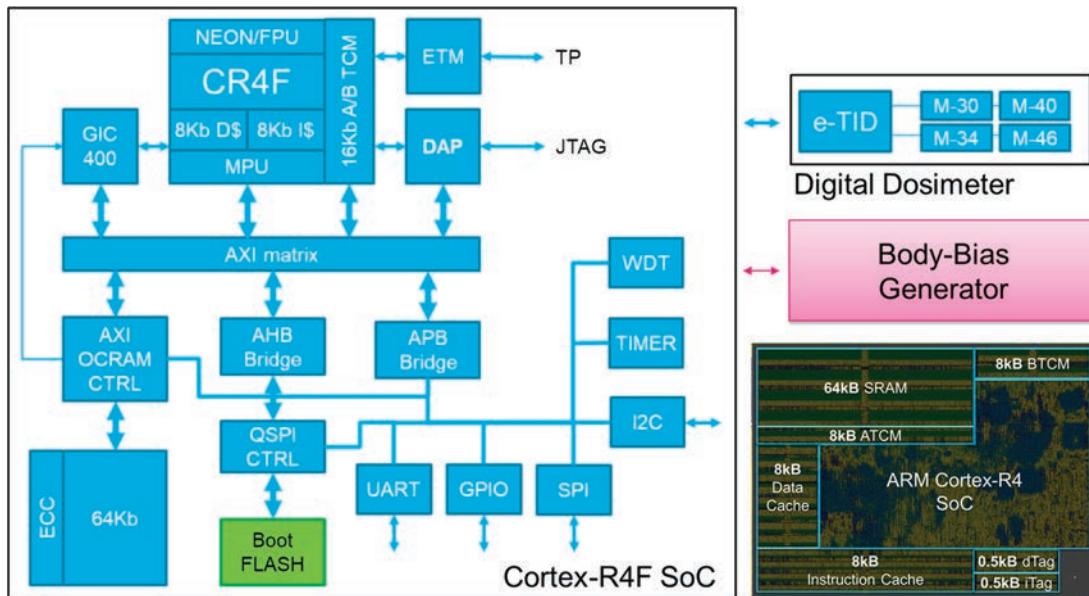


Figure 67: Radiation Hardened ARM Cortex-R4F processor architecture [178].

Other approaches allow for coupling of experimental data, TCAD, SPICE, analytical modeling with methods such as Monte Carlo and Bayesian statistics, and may allow for a “virtual” qualification of COTS parts [79], [180], [181]. These approaches are promising as they may reduce the overall radiation testing requirements by providing estimates of radiation response through a device-to-systems modeling strategy.

5.5 Artificial Intelligence in Design

As abundant as artificial intelligence (AI) has become in everyday life, it wasn’t until recently that AI found its way into orbit [182]. This recent achievement is owed to advancements such as the device seen in Figure 66 [173]. Various works have evaluated SEE in neuromorphic architectures and indicate promise for the development of hardened processors [183]-[190]. All of these efforts indicate that neuromorphic architectures may be inherently robust to SEEs.

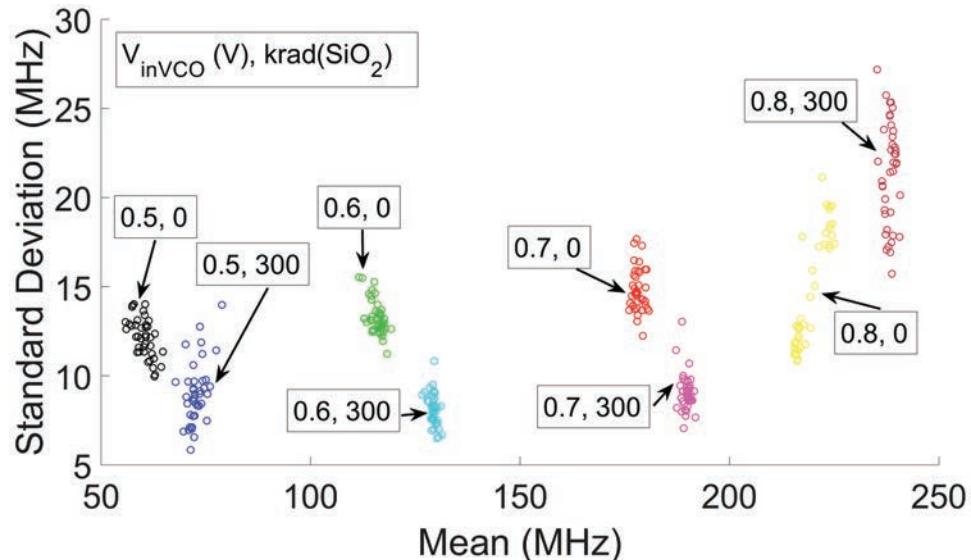


Figure 68: Scatter plot of the standard deviation versus the mean of the instantaneous frequency for a PLL designed and fabricated in a 130 nm CMOS technology node pre- and post-irradiation (300 krad(SiO_2) [191].

Recent works go further and suggest the possibility of Radiation-Hardening-by-AI by using ML to evaluate and adjust operating parameters of other integrated components *in situ* [191]-[193]. As seen in Figure 68 statistical features of a PLL circuit (such as the standard

deviation and mean of the frequency or phase) designed in a 130 nm CMOS technology were used to illustrate behavior clusters that change with TID [191]. These data were used to design a ML model based on the k-nearest neighbors (kNN) algorithm. The model was able to identify the TID of the PLL circuit regardless of the operating bias point over 95% of the time [191].

The statistical measurement technique shown in [191] was further described in [192] and applied to analyze SEE. The technique, termed Ionizing Radiation Effects Spectroscopy (IRES), uses statistical measurements of an arbitrary waveform to identify transient anomalies. The technique was designed to be independent of the data type, instead organizing the statistical parameters of an arbitrary measurement, such as the skewness (γ), kurtosis (κ), variance (σ^2), standard deviation (σ), and mean (μ), to detect transient anomalies. The technique is explained for an SET in the output waveform of a PLL circuit in Figure 69 [193]. The work further reports SETs measured at the output of a 130 nm CMOS PLL captured via laser TPA, quantifying the transients using various signal transformations (e.g., cycle-to-cycle phase jitter or $c2c$, cycle-to-mean phase jitter or $c2m$, and frequency or f) and up to eight statistical moment generating functions. These data were used to create ML models using kNN. The classification accuracy is illustrated in Figure 70 where the True Positive (TP) and True Negative (TN) values are quantified as the percent correctly identified versus the number of sample sets used to train the kNN models for various signal transformations [193]. Significant data to form the training sets may be necessary for such techniques, which may present the ultimate limitation in practice, but the amount of required data is clearly application dependent and may be optimized.

In the future, RHBD solutions may be realized through AI-based approaches for the detection and analysis of radiation-induced anomalies or degradation, which can then activate compensation techniques such as that shown in Figure 67 or through circuit and system reconfiguration.

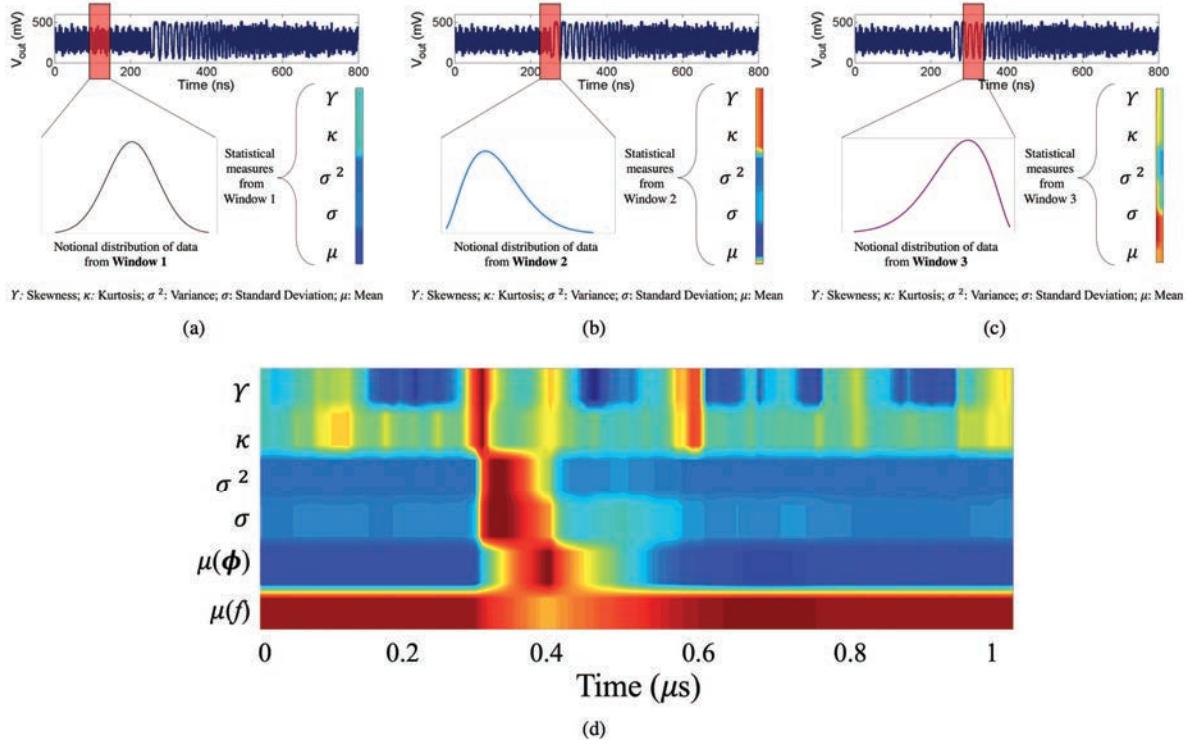


Figure 69: Illustration of the Ionizing Radiation Effects Spectroscopy (IRES) technique. IRES organizes statistical parameters, such as the skewness (γ), kurtosis (κ), variance (σ^2), standard deviation (σ), and mean (μ) of an arbitrary measurement, to detect transient anomalies. The technique can be applied to any data type and is illustrated for an SET in the output waveform of a PLL circuit [193].

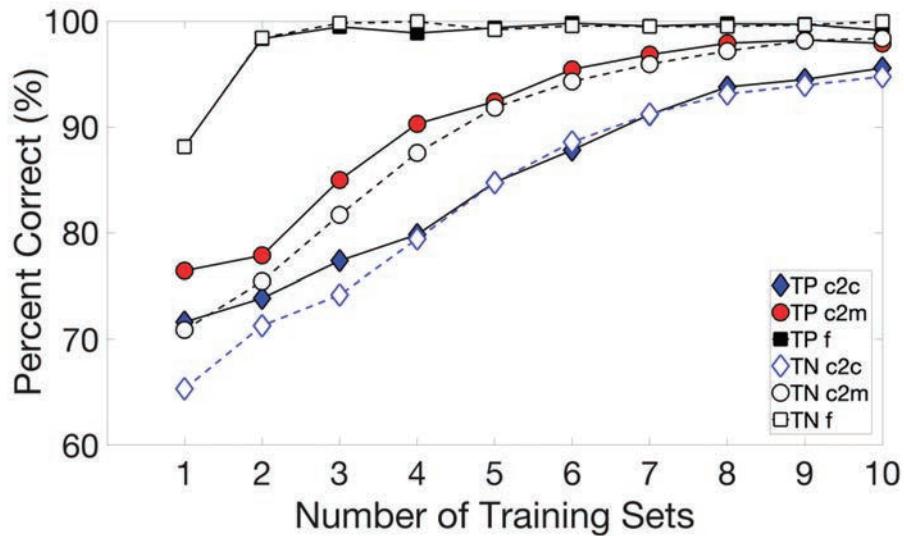


Figure 70: SET classification accuracy showing the True Positive (TP) and True Negative (TN) values. SETs in a 130 nm CMOS PLL captured via TPA at the Naval Research Lab are quantified as the percent correctly identified versus the number of sample sets used to train the kNN models for various signal transformations [193].

6.0 Summary

There are unique challenges in the hardening of AMS circuits as the effect of a radiation is dependent on the circuit topology, type of circuit (function), and the operating mode.

TID mitigation can be implemented at various levels of abstraction and involves one or both of the following:

- Reduction of positive hole trapping or reduction of the influence of positive hole trapping in oxides.
- Reduction of the sensitivity to TID degradation and mismatch.

TID mitigation can occur via Radiation Hardening by Process (RHBP) (refer to section 3.1), Radiation Hardening by Design (RHBD) through Transistor Layout (refer to section 3.2), and Radiation Hardening by Design (RHBD) via Circuit Topology (refer to section 3.3). RHBD techniques were discussed for continuous-time and discrete-time circuits and systems.

As with digital components, SEE mitigation in AMS components can generally be accomplished through a “brute force” approach; that is, area, power, and bandwidth are sacrificed through the increase of capacitance, device size, and current drive, in order to increase the critical charge required to generate SETs. The challenge of radiation hardened AMS circuit design is to develop techniques for mitigating radiation effects while minimizing these design penalties, whether achieved through “brute force” or a multifaceted design approach. SEE mitigation can be implemented at various levels of abstraction and fundamentally involves one or both of the following, irrespective of the technology and abstraction level:

- The reduction in the amount of collected charge (Q_{coll}) at a metallurgical junction (refer to section 4.1).
- The increase in the critical charge (Q_{crit}) required to generate an ASET (refer to section 4.2).

Similar to TID mitigation, SEE mitigation strategies can be implemented at process, layout, circuit and system abstraction levels. This short course overviewed basic and state-of-the-art mitigation approaches and provided some examples of hardened AMS circuits through:

- The reduction of Q_{coll} :
 - Substrate engineering (refer to section 4.1.1).
 - Layout-level mitigation (refer to section 4.1.2).
 - Guard Rings
 - Nodal Separation
 - Interleaving / Interdigitation
 - Hardening via Charge Sharing
- The increase of Q_{crit} :
 - Redundancy (refer to section 4.2.1).
 - Averaging (refer to section 4.2.2).
 - Node Splitting (refer to section 4.2.3).
 - Dynamic Offset Cancellation (refer to section 4.2.4).
 - Resistive Decoupling (refer to section 4.2.5).
 - Filtering (refer to section 4.2.6).
 - Modifications in Bandwidth, Gain, Speed, and Drive Strength (refer to section 4.2.7).
 - Reduction of High Impedance Nodes (refer to section 4.2.8).

Finally, new challenges in RHBD were discussed, including the implications of evolving and disruptive technologies, the increased use of COTS components, and the emergence of AI.

7.0 Acknowledgements

I greatly appreciate the helpful comments from Balaji Narasimham, Vincent Goiffon, Kay Chesnut, Pascale Gouker, Jeff Black, Dan Fleetwood, Allan Johnston, and Mary Loveless, and for the leadership provided by Marta Bagatin. I am also thankful for the collaborations with Tim Holman, Lloyd Massengill, Jeff Kauppila, Dale McMorrow, and Don Reising that helped shape many of the RHBD studies presented in this short course. Support provided by the Defense Threat Reduction Agency (DTRA), the Air Force Research Laboratory (AFRL), the Office of Naval Research (ONR), and the National Science Foundation (NSF) made this work possible. I am also grateful for the research students of the Reliable Electronics and Systems Laboratory (RES) at the University of Tennessee at Chattanooga (UTC).

8.0 References

- [1] S. Wankhede, “Mixed Signal IC Market by Type (Mixed Signal SoC, Microcontroller, and Data Converter) and End Use (Consumer Electronics, Medical & Healthcare, Telecommunication, Automotive, and Military & Defense): Global Opportunity Analysis and Industry Forecast, 2020–2027,” Allied Market Research, Jan. 2021. [Online]. Available: <https://www.alliedmarketresearch.com/mixed-signal-ic-market>
- [2] S. Buchner and M. Baze, “Single-event transients in fast electronic circuits,” *IEEE NSREC Short Course*, 2001, pp. V-1–V-105.
- [3] P. E. Dodd, F. W. Sexton, G. L. Hash, M. R. Shaneyfelt, B. L. Draper, A. J. Farino, and R. S. Flores, “Impact of technology trends on SEU in CMOS SRAMs,” *IEEE Trans. Nucl. Sci.*, vol. 43, no. 6, pp. 2797–2804, Dec. 1996.
- [4] A. H. Johnston, “Radiation effects in advanced microelectronics technologies,” *IEEE Trans. Nucl. Sci.*, vol. 45, no. 3, pp. 1339–1354, June 1998.
- [5] D. M. Fleetwood, “Radiation Effects in a Post-Moore World,” *IEEE Trans. Nucl. Sci.*, Jan. 2021.
- [6] G. Baccarani, M. R. Wordeman and R. H. Dennard, “Generalized Scaling Theory and Its Application to a $\frac{1}{4}$ Micrometer MOSFET Design,” *IEEE Trans. Elect. Dev.*, vol. ED-31, no. 4, pp. 452–462, Apr. 1984.

- [7] R. H. Dennard, F. H. Gaenslen, H-N. Yu, V. L. Rideout, E. Bassous and A. R. LeBlanc, "Design of Ion-Implanted MOSFETs with Very Small Physical Dimension," *IEEE J. Solid State Circuits*, vol. 9, no. 5, pp. 256–268, Oct. 1974.
- [8] C. Hu, "Future CMOS Scaling and Reliability," *Proc. of the IEEE*, vol. 81, no. 5, pp. 682–689, May 1993.
- [9] E. L. Petersen, P. Shapiro, J. H. Adams, Jr., and E. A. Burke, "Calculation of Cosmic-Ray Induced Soft Upset and Scaling in VLSI Devices," *IEEE Trans. Nucl. Sci.*, vol. 29, no. 6, pp. 2055–2063, Dec. 1982.
- [10] D. M. Fleetwood, "Evolution of Total Ionizing Dose Effects in MOS Devices With Moore's Law Scaling," *IEEE Trans. Nucl. Sci.*, vol. 65, no. 8, pp. 1465-1481, Aug. 2018.
- [11] S. Jagannathan, T. D. Loveless, E. X. Zhang, D. M. Fleetwood, R. D. Schrimpf, T. D. Haeffner, J. S. Kauppila, N. Mahatme, B. L. Bhuva, M. L. Alles, W. T. Holman, A. F. Witulski, L. W. Massengill, "Sensitivity of High-Frequency RF Circuits to Total Ionizing Dose Degradation," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 6, pp. 4498-4504, Dec. 2013.
- [12] T. D. Haeffner, T. D. Loveless, E. X. Zhang, A. L. Sternberg, S. Jagannathan, R. D. Schrimpf, J. S. Kauppila, M. L. Alles, D. M. Fleetwood, L. W. Massengill, N. F. Haddad, "Irradiation and Temperature Effects for a 32 nm RF Silicon-on-Insulator CMOS Process," *IEEE Trans. Nucl. Sci.*, vol. 61, no. 6, pp. 3037-3042, Dec. 2014.
- [13] T. D. Loveless, S. Jagannathan, E. X. Zhang, D. M. Fleetwood, J. S. Kauppila, T. D. Haeffner, and L. W. Massengill, "Combined Effects of Total Ionizing Dose and Temperature on a K-Band Quadrature LC-Tank VCO in a 32 nm CMOS SOI Technology," *IEEE Trans. Nucl. Sci.*, vol. 64, no. 1, pp. 204-211, Jan. 2017.
- [14] H. J. Barnaby, "Total-Ionizing-Dose Effects in Modern CMOS Technologies," *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, pp. 3103-3121, Dec. 2006.
- [15] J. R. Schwank, "Basic mechanisms of radiation effects in the natural space environment," *IEEE NSREC Short Course*, 1994, pp. II-1-II-109.
- [16] T. R. Oldham, "Analysis of damage in MOS devices in several radiation environments," *IEEE Trans. Nucl. Sci.*, vol. 31, pp. 1236–1241, 1984

- [17] J. R. Srour, “Basic mechanisms of radiation effects on electronic materials, devices, and integrated circuits,” *IEEE NSREC Short Course*, 1983, pp. I-1–I-96.
- [18] F. B. McLean and T. R. Oldham, “Basic mechanisms of radiation effects in electronic materials and devices,” *Harry Diamond Lab. Tech. Rep.*, vol. HDL-TR, p. 2129, 1987.
- [19] P. V. Dressendorfer, “Basic mechanisms for the new millennium,” *IEEE NSREC Short Course*, 1998.
- [20] R. L. Pease, R. D. Schrimpf and D. M. Fleetwood, “ELDRS in bipolar linear circuits: A review,” *2008 European Conference on Radiation and Its Effects on Components and Systems*, 2008, pp. 18-32.
- [21] S. L. Kosier, R. D. Schrimpf, R. N. Nowlin, D. M. Fleetwood, M. DeLaus, R. L. Pease, W. E. Combs, A. Wei, and F. Chai, “Charge separation for bipolar transistors,” *IEEE Trans. Nucl. Sci.*, vol. 40, no. 6, pp. 1276-1285, Dec. 1993.
- [22] F. Inanlou, N. E. Lourenco, Z. E. Fleetwood, I. Song, D. C. Howard, A. Cardoso, S. Zeinolabedinzadeh, E. Zhang, C. X. Zhang, P. Paki-Amouzou, and J. D. Cressler, “Impact of Total Ionizing Dose on a 4th Generation, 90 nm SiGe HBT Gaussian Pulse Generator,” *IEEE Trans. Nucl. Sci.*, vol. 61, no. 6, pp. 3050-3054, Dec. 2014.
- [23] M. F. Bernard, L. Dusseau, J. Boch, J-R. Vaillé, F. Saigné, R. D. Schrimpf, E. Lorfèvre, and J. P. David, “Analysis of Bias Effects on the Total-Dose Response of a Bipolar Voltage Comparator,” *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, pp. 3232-3236, Dec. 2006.
- [24] B. Blalock, “Radiation Effects on Analog Integrated Circuits and Extreme Environment Design,” *IEEE NSREC Short Course*, 2007, III-1–III-101.
- [25] S. Jagannathan, T. D. Loveless, E. X. Zhang, D. M. Fleetwood, R. D. Schrimpf, T. D. Haeffner, J. S. Kauppila, N. Mahatme, B. L. Bhuva, M. L. Alles, W. T. Holman, A. F. Witulski, and L. W. Massengill, “Sensitivity of High-Frequency RF Circuits to Total Ionizing Dose Degradation,” *IEEE Trans. Nucl. Sci.*, vol. 60, no. 6, pp. 4498-4504, Dec. 2013.
- [26] T. D. Haeffner, T. D. Loveless, E. X. Zhang, A. L. Sternberg, S. Jagannathan, R. D. Schrimpf, J. S. Kauppila, M. L. Alles, D. M. Fleetwood, L. W. Massengill, and N. F. Haddad, “T. D. Haeffner *et al.*, “Irradiation and Temperature Effects for a 32 nm RF

- Silicon-on-Insulator CMOS Process," *IEEE Trans. Nucl. Sci.*, vol. 61, no. 6, pp. 3037-3042, Dec. 2014.
- [27] T. D. Loveless, S. Jagannathan, E. X. Zhang, D. M. Fleetwood, J. S. Kauppila, T. D. Haeffner, and L. W. Massengill, "Combined Effects of Total Ionizing Dose and Temperature on a K-Band Quadrature LC-Tank VCO in a 32 nm CMOS SOI Technology," *IEEE Trans. Nucl. Sci*, vol. 64, no. 1, pp. 204-211, Jan. 2017.
- [28] R. Baumann, "Single-event effects in advanced CMOS," *IEEE NSREC Short Course*, 2005, pp. II-1-II-59.
- [29] L. W. Massengill, "SEU modeling and prediction techniques," *IEEE NSREC Short Course*, 1993, pp. III-1-III-93.
- [30] T. Daniel Loveless, Lloyd W. Massengill, W. Timothy Holman, Bharat L. Bhuva, Dale McMorrow, and J. Warner, "A Generalized Linear Model for Single Event Transient Propagation in Phase-Locked Loops," *IEEE Trans. Nucl. Sci.*, vol. 57, no. 5, pp. 2933-2947, Oct. 2010.
- [31] J. S. Kauppila, "Single-Event Modeling for Rad-Hard-by-Design Flows," *IEEE NSREC Short Course*, 2016, pp. IV-1-IV-91.
- [32] S. DasGupta, A. F. Witulski, B. L. Bhuva, M. L. Alles, R. A. Reed, , O. A. Amusan, J. R. Ahlbin, R. D. Schrimpf and L. W. Massengill, "Effect of Well and Substrate Potential Modulation on Single Event Pulse Shape in Deep Submicron CMOS," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, pp. 2407-2412, Dec. 2007.
- [33] A. D. Tipton, J. A. Pellish, R. A. Reed, R. D. Schrimpf, R. A. Weller, M. H. Mendenhall, B. Sierawski, A. K. Sutton, R. M. Diestelhorst, G. Espinel, J. D. Cressler, P. W. Marshall, and G. Vizkelethy, "Multiple-Bit Upset in 130 nm CMOS Technology," *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, pp. 3259-3264, Dec. 2006.
- [34] R. Koga, S. D. Pinkerton, S. C. Moss, D. C. Mayer, S. LaLumondiere, S. J. Hansel, K. B. Crawford, and W. R. Crain, "Observation of Single-Event Upsets in Analog Microelectronics," *IEEE Trans. Nucl. Sci.*, vol. 40, no. 6, pp. 1838-1844, Dec. 1993.
- [35] N. M. Atkinson, "System-Level Radiation Hardening of Low-Voltage Analog/Mixed-Signal Circuits," *PhD Dissertation*, Vanderbilt University, 2013.
- [36] Y. Boughassoul, S. Buchner, D. McMorrow, V. Pouget, L. W. Massengill, P. Fouillat, W. T. Holman, C. Poivey, J. W. Howard, M. Savage, and M. C. Maher,

- “Investigation of millisecond-long analog single-event transients in the LM6144 op amp,” *IEEE Trans. Nucl. Sci.*, vol. 51, no. 6, pp. 3529–3536, Dec. 2004.
- [37] S. Buchner and D. McMorrow, “Single-Event Transients in Linear Integrated Circuits,” *IEEE NSREC Short Course*, 2005, pp. IV-1–IV-77.
- [38] M. J. Gadlage, R. D. Schrimpf, B. Narasimham, J. A. Pellish, K. M. Warren, R. A. Reed, R. A. Weller, B. L. Bhuva, L. W. Massengill, and X. Zhu, “Assessing Alpha Particle-Induced Single Event Transient Vulnerability in a 90-nm CMOS Technology,” *IEEE Electron Device Lett.*, vol. 29, no. 6, pp. 638–640, June 2008.
- [39] Y. Boulghassoul, L. W. Massengill, A. L. Sternberg, R. L. Pease, S. Buchner, J. W. Howard, D. McMorrow, M. W. Savage, and C. Poivey, “Circuit Modeling of the LM124 Operational Amplifier for Analog Single-Event Transient Analysis,” *IEEE Trans. Nucl. Sci.*, vol. 49, no. 6, pp. 3090–3096, Dec. 2002.
- [40] T. D. Loveless, L. W. Massengill, B. L. Bhuva, W. T. Holman, A. F. Witulski and Y. Boulghassoul, “A Hardened-by-Design Technique for RF Digital Phase-Locked Loops,” *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, pp. 3432–3438, Dec. 2006.
- [41] T. D. Loveless, L. W. Massengill, B. L. Bhuva, W. T. Holman, R. A. Reed, D. McMorrow, J. S. Melinger, and P. Jenkins, “A Single-Event-Hardened Phase-Locked Loop Fabricated in 130 nm CMOS,” *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, pp. 2012–2020, Dec. 2007.
- [42] A. Ildefonso, G. N. Tzintzarov, N. E. Lourenco , Z. E. Fleetwood, A. Khachatrian, S. P. Buchner, D. McMorrow, J. H. Warner, M. Kaynak, and J. D. Cressler, “Tradeoffs Between RF Performance and SET Robustness in Low-Noise Amplifiers in a Complementary SiGe BiCMOS Platform,” *IEEE Trans. Nucl. Sci*, vol. 67, no. 7, pp. 1521–1529, July 2020.
- [43] D. McMorrow, W. T. Lotshaw, J. S. Melinger, S. Buchner, and R. L. Pease, “Sub-bandgap laser-induced single event effects: Carrier generation via two-photon absorption,” *IEEE Trans. Nucl. Sci.*, vol. 49, no. 6, pp. 3002–3008, Dec. 2002.
- [44] D. McMorrow, W. T. Lotshaw, J. S. Melinger, S. Buchner, Y. Boulghassoul, L. W. Massengill, and R. L. Pease, “Three-Dimensional Mapping of Single-Event Effects Using Two Photon Absorption,” *IEEE Trans. Nucl. Sci.*, vol. 50, no. 6, pp. 2199–2207, Dec. 2003.

- [45] Joel M. Hales, Ani Khachatrian, Jeffrey Warner, Stephen Buchner, Adrian Ildefonso, George N. Tzintzarov, Delgermaa Nergui, Daniele M. Monahan, Stephen D. LaLumondiere, John D. Cressler, and Dale McMorrow, “Using Bessel beams and two-photon absorption to predict radiation effects in microelectronics,” *Opt. Express*, vol. 27, no. 26, pp. 37652-37666, 2019.
- [46] D. McMorrow, “Laser-Based Testing for SEE,” *IEEE NSREC Short Course*, 2019, pp. IVA-1–IVA-63.
- [47] V. Pouget, “Facilities and Methods for Radiation Testing Part II - Laser,” *IEEE NSREC Short Course*, 2014, pp. IV-II-1–IV-II-43.
- [48] J. S. Kauppila, L. W. Massengill, W. T. Holman, A. V. Kauppila, and S. Sanathanamurthy, “Single Event Simulation Methodology for Analog/Mixed Signal Design Hardening,” *IEEE Trans. Nucl. Sci.*, vol. 51, no. 6, pp. 3603-3608, Dec. 2004.
- [49] S. E. Armstrong, T. D. Loveless, J. R. Hicks, W. T. Holman, D. McMorrow, and L. W. Massengill, “Phase-Dependent Single-Event Sensitivity Analysis of High-Speed A/MS Circuits Extracted from Asynchronous Measurements,” *IEEE Trans. Nucl. Sci.*, vol. 58, no. 3, pp. 1066-1071, June 2011.
- [50] F. Bezerra, “Facilities and Methods for Radiation Testing Part I,” *IEEE NSREC Short Course*, 2014, pp. IV-I-1–IV-I-47.
- [51] C. Hafer, “Ground-Based Testing and Evaluation of Soft Errors,” *IEEE NSREC Short Course*, 2008, pp. II-1–II-66.
- [52] A. H. Johnston, “The influence of VLSI technology evolution on radiation-induced latchup in space systems”, *IEEE Trans. Nucl. Sci.*, vol. 43, no. 2, pp. 505–521, Apr. 1996.
- [53] G. Bruguier and J.-M. Palau, “Single particle-induced latchup,” *IEEE Trans. Nucl. Sci.*, vol. 43, no. 2, pp. 522–532, Apr. 1996.
- [54] N. Dodds, “Single Event Latchup: Hardening Strategies, Triggering Mechanisms, and Testing Considerations”, *PhD Dissertation*, Vanderbilt University, 2012.
- [55] M. Nicolaidis, “A Low-Cost Single-Event Latchup Mitigation Scheme,” *12th IEEE International On-Line Testing Symposium (IOLTS'06)*, pp. 1-5, 2006.
- [56] J. R. Srour and K. Y. Chiu, “MOS Hardening Approaches for Low-Temperature Applications,” *IEEE Trans. Nucl. Sci.*, vol. 24, no. 6, pp. 2140 – 2146, Dec. 1977.

- [57] J. M. McGarrity, "Considerations for Hardening MOS Devices and Circuits for Low Radiation Doses," *IEEE Trans. Nucl. Sci.*, vol. 27, no. 6, pp. 1739-1744, Dec. 1980.
- [58] H. Hatano, "Radiation hardened high performance CMOS VLSI circuit designs," *IEEE Proceedings on Circuits, Devices, and Systems*, vol. 139, no. 3, pp. 287-294, Jun. 1992.
- [59] H. Hatano and K. Doi, "Radiation-Tolerant High-Performance CMOS VLSI Circuit Design," *IEEE Trans. Nucl. Sci.*, vol. 32, no. 6, pp. 4031-4035, Dec. 1985.
- [60] M. R. Shaneyfelt, P. E. Dodd, B. L. Draper, and R. S. Flores, "Challenges in hardening technologies using shallow-trench isolation," *IEEE Trans. Nucl. Sci.*, vol. 45, no. 6, pp. 2584-2592, Dec. 1998.
- [61] H. L. Hughes and J. M. Benedetto, "Radiation Effects and Hardening of MOS Technology: Devices and Circuits," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 43, pp. 500-521, June 2003.
- [62] J. D. Cressler, "Silicon-Germanium as an Enabling Technology for Extreme Environment Electronics," *IEEE Trans. Device Mater. Rel.*, vol. 10, no. 4, pp. 437-448, Dec. 2010.
- [63] J. D. Cressler, "Silicon-Germanium as an Enabling Technology for Extreme Environment Electronics," *FermiLab*, Batavia, IL, June 2009.
- [64] D. R. Williams and N. W. Van Vronno, "Two Radiation-Hardened Analog Multiplexers," *IEEE Trans. Nucl. Sci.*, vol. 30, no. 6, pp. 4273-4276, Dec. 1983.
- [65] W. J. Snoeys, T. A. P. Gutierrez, and G. Anelli, "A new NMOS layout structure for radiation tolerance," *IEEE Trans. Nucl. Sci.*, vol. 49, no. 4, pp. 822-826, Aug. 2002.
- [66] R. N. Nowlin, J. Bailey, R. Turfler, and D. R. Alexander, "A total-dose hardening-by-design approach for high-speed mixed-signal CMOS integrated circuits," *Int. J. High Speed Electronics*, vol. 14, no. 2, pp. 367-378, Jun. 2004.
- [67] R. Lacoé, "CMOS Scaling: Design Principles and Hardening-by-Design Methodology," *IEEE NSREC Short Course*, 2003, pp. II-1-II-142.
- [68] R. C. Lacoé, J. V. Osborn, D. C. Mayer, S. Brown, and J. Gambles, "Total-dose tolerance of the commercial Taiwan Semiconductor Manufacturing Company (TSMC) 0.35- μ m CMOS process," *IEEE European Conference on Radiation and Its Effects on Components and Systems*, pp. 464-468, Sept. 2001.

- [69] E. Vilella and A. Diéguez, “Design of a Bandgap Reference Circuit with Trimming for Operation at Multiple Voltages and Tolerant to Radiation in 90nm CMOS Technology,” *IEEE Computer Society Annual Symposium on VLSI*, pp. 269-272, July 2010.
- [70] M. McLain, H. J. Barnaby, K. E. Holbert, R. D. Schrimpf, H. Shah, A. Amort, M. Baze, and J. Wert, “Enhanced TID Susceptibility in Sub-100 nm Bulk CMOS I/O Transistors and Circuits,” *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, Dec. 2007.
- [71] N. Haddad, Ernesto Chan, Scott Doyle, Andrew Kelly, Reed Lawrence, David Lawson, Dinu Patel and Jason Ross, “The path and challenges to 90nm radiation hardened technology,” *IEEE European Conference on Radiation and Its Effects on Components and Systems*, pp. 269-273, 2008.
- [72] A.-J. Annema, “Low-power bandgap references featuring DT莫斯,” *IEEE Journal of Solid-State Circuits*, vol. 34, no. 7, pp. 949-955, Jul. 1999.
- [73] V. Ferlet-Cavrois, P. Paillet, O. Musseau, J. L. Leray, O. Faynot, C. Raynaud, and J. L. Pelloie, “Total dose behavior of partially depleted SOI dynamic threshold voltage MOS (DTMOS) for very low supply voltage applications (0.6-1 V),” *IEEE Trans. Nucl. Sci.*, vol. 47, no. 3, pp. 613-619, Jun. 2000.
- [74] F. Assaderaghi, D. Sinitsky, S. A. Parke, J. Bokor, P. K. Ko, and Chenming Hu, “Dynamic threshold-voltage MOSFET (DTMOS) for ultra-low voltage VLSI,” *IEEE Trans. on Electron Devices*, vol. 44, no. 3, pp. 414-422, Mar. 1997.
- [75] V. Gromov, A. J. Annema, R. Kluit, J. L. Visschers, P. Timmer, “A Radiation Hard Bandgap Reference Circuit in a Standard 0.13 μm CMOS Technology,” *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, pp. 2727-2733, Dec. 2007.
- [76] S. D. LaLumondiere, E. C. Dillingham, A. C. Scofield, J. P. Bonsall, P. Karuza, D. L. Brewe, R. D. Schrimpf, A. L. Sternberg, N. P. Wells, D. M. Cardoza, W. T. Lotshaw, and S. C. Moss, “Application of a Focused, Pulsed X-ray Beam for Total Ionizing Dose Testing of Bipolar Linear Integrated Circuits,” *IEEE Trans. Nucl. Sci.*, vol. 65, no. 1, pp. 478-485, Jan. 2018.
- [77] R. M. Chavez, B. G. Rax, L. Z. Scheick, A. H. Johnston, “Total ionizing dose effects in bipolar and BiCMOS devices,” *IEEE Radiation Effects Data Workshop*, pp. 144-148, 2005.

- [78] R. L. Pease, “Total Ionizing Dose Effects in Bipolar Devices and Circuits,” *IEEE Trans. Nucl. Sci.*, vol. 50, no. 3, pp. 539-551, June 2003.
- [79] A. Privat, H. J. Barnaby, P. C. Adell, B. S. Tolleson, Y. Wang, X. Han, P. Davis, B. R. Rax, and T. E. Buchheit, “Multiscale Modeling of Total Ionizing Dose Effects in Commercial-off-the-Shelf Parts in Bipolar Technologies,” *IEEE Trans. Nucl. Sci.*, vol. 66, no. 1, pp. 190-198, Jan. 2019
- [80] C. C. Enz and G. C. Temes, “Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling, and chopper stabilization,” *Proc. of the IEEE*, vol. 84, no. 11, pp. 1584-1614, Nov. 1996.
- [81] E. A. Goldberg, “Stabilized Direct Current Amplifier,” Patent, Serial No. 90,072, Filed April 28, 1949, Patented July 27, 1954.
- [82] C. C. Enz, E. A. Vittoz, and F. Krummenacher, “A CMOS chopper amplifier,” *IEEE Journal of Solid-State Circuits*, vol. 22, no. 3, pp. 335-342, June 1987.
- [83] A-G. Vasilica, G. Pristava, C. Pasoi, and G. Brezeanu, “Offset cancellation in bandgap references with CMOS operational amplifiers,” *Proc. of CAS 2011 (International Semiconductor Conference)*, pp. 421-424, 2011.
- [84] K. J. Shetler, N. M. Atkinson, W. T. Holman, J. S. Kauppila, T. D. Loveless, A. F. Witulski, B. L. Bhuva, E. X. Zhang, and L. W. Massengill, “Radiation Hardening of Voltage References Using Chopper Stabilization,” *IEEE Trans. Nucl. Sci.*, vol. 62, no. 6, pp. 3064-3071, Dec. 2015.
- [85] “Radiation Hardened Gain Digitizer,” *NASA Technology Transfer Program*, Available: <https://technology.nasa.gov/patent/GSC-TOPS-157>.
- [86] E. O. Mikkola, V. Swaminathan, B. Sivakumar, and H. J. Barnaby, “Ultra-Low-Power Radiation Hard ADC for Particle Detector Readout Applications,” *2013 JINST*, vol. 8, C04007, pp. 1-10, Apr. 2013.
- [87] K. Chestnut, “System-Level Hardening – What Could Go Wrong, and How to Make it Right,” *IEEE NSREC Short Course*, 2021.
- [88] S. Buchner and D. McMorrow, “Single-Event Transients in Bipolar Linear Integrated Circuits,” *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, pp. 3079-3102, Dec. 2006.
- [89] O. A. Amusan, L. W. Massengill, M. P. Baze, B. L. Bhuva, A. F. Witulski, J. D. Black, A. Balasubramanian, M. C. Casey, D. A. Black, J. R. Ahlbin, R. A. Reed, and

- M. W. McCurdy, "Mitigation Techniques for Single-Event-Induced Charge Sharing in a 90-nm Bulk CMOS Process," *IEEE Trans. Device Mater. Rel.*, vol. 9, no. 2, pp. 468-472, June 2009.
- [90] J. Popp, "Developing Radiation Hardened Complex System on Chip ASICs in Commercial Ultra Deep Submicron CMOS Processes," *IEEE NSREC Short Course*, 2010, pp. II-1-II-62.
- [91] Q. Zhou and K. Mohanram, "Transistor Sizing for Radiation Hardening," *Proc. of 42nd IEEE IRPS*, pp. 310-315, Apr. 2004.
- [92] O. A. Amusan, A. F. Witulski, L. W. Massengill, B. L. Bhuva, P. R. Fleming, M. L. Alles, A. L. Sternberg, J. D. Black, and R. D. Schrimpf, "Charge Collection and Charge Sharing in a 130 nm CMOS Technology," *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, pp. 3253-3258, Dec. 2006.
- [93] O. A. Amusan, M. C. Casey, B. L. Bhuva, D. McMorrow, M. J. Gadlage, J. S. Melinger, and L. W. Massengill, "Laser Verification of Charge Sharing in a 90 nm Bulk CMOS Process," *IEEE Trans. Nucl. Sci.*, vol. 56, no. 6, pp. 3065-3070, Dec. 2009.
- [94] J. A. Pellish, R. A. Reed, R. D. Schrimpf, M. L. Alles, M. Varadharajaperumal, G. Niu, A. K. Sutton, R. M., Diestelhorst, G. Espinel, R. Krishivasan, J. P. Comeau, J. D. Cressler, G. Vizkelethy, P. W. Marshall, R. A. Weller, M. H. Mendenhall, and E. J. Montes, "Substrate Engineering Concepts to Mitigate Charge Collection in Deep Trench Isolation Technologies," *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, pp. 3298-3305, Dec. 2006.
- [95] J. R. Schwank, V. Ferlet-Cavrois, M. R. Shaneyfelt, P. Paillet, and P. E. Dodd, "Radiation Effects in SOI Technologies," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 3, pp. 522-538, June 2003.
- [96] T. Poiroux, O. Faynot, C. Tabone, H. Tigelaar, H. Mogul, N. Bresson, and S. Cristoloveanu, "Emerging Floating-Body Effects in Advanced Partially-Depleted SOI Devices," *IEEE International SOI Conf.*, pp. 99-100, 2002.
- [97] L. W. Massengill and P. W. Tuinenga, "Single-Event Transient Pulse Propagation in Digital CMOS," *IEEE Trans. Nucl. Sci.*, vol. 55, no. 6, pp. 2861-2871, Dec. 2008.

- [98] V. Ferlet-Cavrois, V. Pouget, D. McMorrow, J. R. Schwank, N. Fel, F. Essely, R. S. Flores, P. Paillet, M. Gaillardin, D. Kobayashi, J. S. Melinger, O. Duhamel, P. E. Dodd, and M. R. Shaneyfelt, "Investigation of the Propagation Induced Pulse Broadening (PIPB) Effect on Single Event Transients in SOI and Bulk Inverter Chains," *IEEE Trans. Nucl. Sci.*, vol. 55, no. 6, pp. 2842-2853, Dec. 2008.
- [99] M. J. Gadlage, P. Gouker, B. L. Bhuva, B. Narasimham, and R. D. Schrimpf, "Heavy-Ion-Induced Digital Single Event Transients in a 180 nm Fully Depleted SOI Process," *IEEE Trans. Nucl. Sci.*, vol. 56, no. 6, pp. 3483-3488, Dec. 2009.
- [100] T. D. Loveless, J. S. Kauppila, S. Jagannathan, D. R. Ball, J. D. Rowe, N. J. Gaspard, N. M. Atkinson, R. W. Blaine, T. R. Reece, J. R. Ahlbin, T. D. Haeffner, M. L. Alles, W. T. Holman, B. L. Bhuva, and L. W. Massengill, "On-Chip Measurement of Single-Event Transients in a 45 nm Silicon-on-Insulator Technology," *IEEE Trans. Nucl. Sci.*, vol. 59, no. 6, pp. 2748-2755, Dec. 2012.
- [101] J. A. Maharrey, R. C. Quinn, T. D. Loveless, J. S. Kauppila, S. Jagannathan, N. M. Atkinson, N. J. Gaspard, E. X. Zhang, M. L. Alles, B. L. Bhuva, W. T. Holman, and L. W. Massengill, "Effect of Device Variants in 32 nm and 45 nm SOI on SET Pulse Distributions," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 6, pp. 4399-4404, Dec. 2013.
- [102] T. D. Loveless, J. S. Kauppila, J. A. Maharrey, R. C. Quinn, S. Jagannathan, M. L. Alles, B. L. Bhuva, W. T. Holman, and L. W. Massengill, "Single-Event Transients in 45 nm and 32 nm Partially Depleted SOI Technologies," *Proc. 2014 GOMACTech Conf.*, 2014.
- [103] J. A. Maharrey, R. C. Quinn, T. D. Loveless, J. S. Kauppila, S. Jagannathan, N. M. Atkinson, N. J. Gaspard, E. X. Zhang, M. L. Alles, B. L. Bhuva, W. T. Holman, and L. W. Massengill, "Effect of Device Variants in 32 nm and 45 nm SOI on SET Pulse Distributions," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 6, pp. 4399-4404, Dec. 2013.
- [104] R. C. Harrington, J. A. Maharrey, J. S. Kauppila, P. Nsengiyumva, D. R. Ball, T. D. Haeffner, E. X. Zhang, B. L. Bhuva, and L. W. Massengill, "Effect of Transistor Variants on Single-Event Transients at the 14-/16-nm Bulk FinFET Technology Generation," *IEEE Trans. Nucl. Sci.*, vol. 65, no. 8, pp. 1807-1813, Aug. 2018.
- [105] J. D. Black, A. L. Sternberg, M. L. Alles, A. F. Witulski, B. L. Bhuva, L. W. Massengill, J. M. Benedetto, M. P. Baze, J. L. Wert, and M. G. Hubert, "HBD Layout

- Isolation Techniques for Multiple Node Charge Collection Mitigation," *IEEE Trans. Nucl. Sci.*, vol. 52, no. 6, pp. 2536-2541, Dec. 2005.
- [106] B. D. Olson, O. A. Amusan, S. DasGupta, L. W. Massengill, A. F. Witulski, B. L. Bhuva, M. L. Alles, K. M. Warren, and D. R. Ball, "Analysis of Parasitic PNP Bipolar Transistor Mitigation Using Well Contacts in 130 nm and 90 nm CMOS Technology," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 4, pp. 894-897, Aug. 2007.
- [107] B. Narasimham, R. L. Shuler, J. D. Black, B. L. Bhuva, R. D. Schrimpf, A. F. Witulski, W. T. Holman, and L. W. Massengill, "Quantifying the Reduction in Collected Charge and Soft Errors in the Presence of Guard Rings," *IEEE Trans. Device Mater. Rel.*, vol. 8, no. 1, pp. 203-209, Mar. 2008.
- [108] B. Narasimham, J. W. Gambles, R. L. Schuler, B. L. Bhuva, and L. W. Massengill, "Quantifying the Effect of Guard Rings and Guard Drains in Mitigating Charge Collection and Charge Spread," *IEEE Trans. Nucl. Sci.*, vol. 55, no. 6, pp. 3456-3460, Dec. 2008.
- [109] A. K. Sutton, M. Bellini, J. D. Cressler, J. A. Pellish, R. A. Reed, P. W. Marshall, G. Niu, G. Vizkelethy, M. Turowski, and A. Raman, "An Evaluation of Transistor-Layout RHBD Techniques for SEE Mitigation in SiGe HBTs," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, pp. 2044-2052, Dec. 2007.
- [110] R. R. Troutman, Latchup in CMOS Technology: The Problem and Its Cure. Norwell, MA: Kluwer, 1986.
- [111] A. Hastings, The Art of Analog Layout, 2nd ed. New York: Prentice-Hall, 2005, ch. 4, 7.
- [112] M. Varadharajaoerumal, G. Niu, X. Wei, T. Zhang, J. D. Cressler, R. A. Reed, and P. W. Marshall, "3-D Simulation of SEU Hardening of SiGe HBTs Using Shared Dummy Collector," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, pp. 2330-2337, Dec. 2007.
- [113] O. A. Amusan, L. W. Massengill, B. L. Bhuva, S. DasGupta, A. F. Witulski, and J. R. Ahlbin, "Design Techniques to Reduce SET Pulse Widths in Deep-Submicron Combinational Logic," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, pp. 2060-2064, Dec. 2007.
- [114] B. Narasimham, B. L. Bhuva, R. D. Schrimpf, L. W. Massengill, M. J. Gadlage, O. A. Amusan, W. T. Holman, A. F. Witulski, W. H. Robinson, J. D. Black, J. M.

- Benedetto, and P. H. Eaton, "Characterization of Digital Single Event Transient Pulse-Widths in 130-nm and 90-nm CMOS Technologies," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, pp. 2506-2511, Dec. 2007.
- [115] M. J. Gadlage, J. R. Ahlbin, B. Narasimham, B. L. Bhuva, L. W. Massengill, R. A. Reed, R. D. Schrimpf, and G. Vizkelethy, "Scaling Trends in SET Pulse Widths in Sub-100 nm Bulk CMOS Processes," *IEEE Trans. Nucl. Sci.*, vol. 57, no. 1, pp. 3336-3341, Dec. 2010.
- [116] M. L. Alles, R. D. Schrimpf, R. A. Reed, L. W. Massengill, "Radiation Hardness of FDSOI and FinFET Technologies," *Proc. 2011 IEEE Int. SOI Conference*, Tempe, AZ, Oct. 2011.
- [117] P. Roche and G. Gasiot, "SEE on Advanced CMOS BULK, FinFET, and UTTB SOI Technologies," *IEEE NSREC Short Course*, 2014, pp. III-1-III-48.
- [118] D. R. Ball, M. L. Alles, R. D. Schrimpf, and S. Cristoloveanu, "Comparing Single Event Upset sensitivity of bulk vs. SOI based FinFET SRAM cells using TCAD simulations," *Proc. 2010 IEEE Int. SOI Conference*, San Diego, CA, Oct. 2010.
- [119] T. D. Loveless, M. L. Alles, D. R. Ball, K. M. Warren, and L. W. Massengill, "Parametric Variability Affecting 45 nm SOI SRAM Single Event Upset Cross-Sections," *IEEE Trans. Nucl. Sci.*, vol. 57, no. 6, pp. 3228-3233, Dec. 2010.
- [120] T. Calin, M. Nicolaidis, and R. Velazco, "Upset hardened memory design for submicron CMOS technology," *IEEE Trans. Nucl. Sci.*, vol. 43, no. 6, pp. 2874-2878, Dec. 1996.
- [121] M. P. Baze, M. P. Baze, B. Hughlock, J. Wert, J. Tostenrude, L. Massengill, O. Amusan, R. Lacoe, K. Lilja, and M. Johnson, "Angular dependence of single-event sensitivity in hardened flip/flop designs," *IEEE Trans. Nucl. Sci.*, vol. 55, no. 6, pp. 3295-3301, Dec. 2008.
- [122] K. Lee, K. Lilja, M. Bounasser, P. Relangi, I. R. Linscott, U. Inan, and S. Mitra, "LEAP: Layout design through error-aware transistor positioning for soft-error resilient sequential cell design," *Proc. IEEE Intl. Rel. Phys. Symp.*, 2010, pp. 203-412.
- [123] K. Warren, A. Stenberg, J. Black, R. Weller, R. Reed, M. Mendenhall, R. Schrimpf, and L. Massengill, "Heavy ion testing and single-event upset rate prediction

- considerations for a DICE flip-flop," *IEEE Trans. Nucl. Sci.*, vol. 56, no. 6, pp. 3130–3137, Dec. 2009.
- [124] K. Lilja, M. Bounasser, S.-J. Wen, R. Wong, J. Holst, N. Gaspard, S. Jagannathan, D. Loveless, and B. Bhuva, "Single-Event Performance and Layout Optimization of Flip-Flops in a 28-nm Bulk Technology," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 4, pp. 2782-2788, Aug. 2013.
- [125] B. Mossawir, I. R. Linscott, U. S. Inan, J. L. Roeder, J. V. Osborn, S. C. Witczak, E. E. King, and S. D. LaLumondiere, "A TID and SEE Radiation-Hardened, Wideband, Low-Noise Amplifier," *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, pp. 3439-3448, Dec. 2006.
- [126] A. T. Kelly, P. R. Fleming, W. T. Holman, A. F. Witulski, B. L. Bhuva, and L. W. Massengill, "Differential Analog Layout for Improved ASET Tolerance," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, pp. 2053-2059, Dec. 2007.
- [127] S. E. Armstrong, B. D. Olson, W. T. Holman, J. Warner, D. McMorrow, and L. W. Massengill, "Demonstration of a Differential Layout Solution for Improved ASET Tolerance in CMOS AMS Circuits," *IEEE Trans. Nucl. Sci.*, vol. 57, no. 6, pp. 3615-3619, Dec. 2010.
- [128] J. R. Ahlbin, L. W. Massengill, B. L. Bhuva, B. Narasimham, M. J. Gadlage, and P. H. Eaton, "Single-Event Transient Pulse Quenching in Advanced CMOS Logic Circuits," *IEEE Trans. Nucl. Sci.*, vol. 56, no. 6, pp. 3050-3056, Dec. 2009.
- [129] N. Seifert , V. Ambrose , B. Gill , Q. Shi , R. Allmon , C. Recchia , S. Mukherjee , N. Nassif , J. Krause , J. Pickholtz and A. Balasubramanian “On the radiation-induced soft error performance of hardened sequential elements in advanced bulk CMOS technologies”, *Proc. 2010 IEEE Int. Reliability Physics Symp.*, pp.188 -197, May 2010.
- [130] W. T. Holman, J. S. Kauppila, T. D. Loveless, L. W. Massengill, B. L. Bhuva, and A. F. Witulski, "Low-Penalty Radiation-Hardened-by-Design Concepts for High-Performance Analog, Mixed-Signal, and RF Circuits," *Proc. 2013 GOMACTech Conf.*, 2013.
- [131] R. W. Blaine, S. E. Armstrong, J. S. Kauppila, N. M. Atkinson, B. D. Olson, W. T. Holman, and L. W. Massengill, "RHBD Bias Circuits Utilizing Sensitive Node

- Active Charge Cancellation," *IEEE Trans. Nucl. Sci.*, vol. 58, no. 6, pp. 3060-3066, Dec. 2011.
- [132] R. W. Blaine, N. M. Atkinson, J. S. Kauppila, T. D. Loveless, S. E. Armstrong, W. T. Holman, and L. W. Massengill, "Single-Event-Hardened CMOS Operational Amplifier Design," *IEEE Trans. Nucl. Sci.*, vol. 59, no. 4, pp. 803-810, Aug. 2012.
- [133] N. W. van Vronno and B. R. Doyle, "Design considerations and verification testing of an SEE-hardened quad comparator," *IEEE Trans. Nucl. Sci.*, vol. 48, no. 6, pp. 1859-1864, Aug. 2002.
- [134] B. D. Olson, W. T. Holman, L. W. Massengill and B. L. Bhuva, "Evaluation of Radiation-Hardened Design Techniques Using Frequency Domain Analysis," *IEEE Trans. Nucl. Sci.*, vol. 55, no. 6, pp. 2957-2961, Dec. 2008.
- [135] S. Kim, A. Tsuchiya, and H. Onodera, "Dual-PLL based on Temporal Redundancy for Radiation Hardening," *Proc. of the 10th International Workshop on Radiation Effects in Semiconductor Devices for Space Applications*, pp. 115-118, 2013.
- [136] T. D. Loveless, L. W. Massengill, W. T. Holman and B. L. Bhuva, "Modeling and Mitigating SETs in Voltage-Controlled Oscillators," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, pp. 2561-2567, Dec. 2007.
- [137] T. D. Loveless, L. W. Massengill, B. L. Bhuva, W. T. Holman, M. C. Casey, R. A. Reed, S. A. Nation, D. McMorrow, and J. S. Melinger, "A Probabilistic Analysis Technique Applied to a Radiation-Hardened-by-Design Voltage-Controlled Oscillator for Mixed-Signal Phase-Locked Loops," *IEEE Trans. Nucl. Sci.*, vol. 55, no. 6, pp. 3447-3455, Dec. 2008.
- [138] L. Chen, X. Wen, Y. You, D. Huang, C. Li and J. Chen, "A radiation-tolerant ring oscillator phase-locked loop in 0.13μm CMOS," *2012 IEEE 55th International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2012, pp. 13-16.
- [139] H. Yuan, J. Chen, B. Liang, and Y. Guo, "Fault-tolerant multi-node coupling triple mode redundancy voltage controlled oscillator for reducing soft error in clock and data recovery," *IET Electronics Letters*, vol. 55, no. 5, pp. 250-252, Mar. 2019.
- [140] S. M. Jung and J. M. Roveda, "A radiation-hardened-by-design phase-locked loop using feedback voltage controlled oscillator," *Sixteenth International Symposium on Quality Electronic Design*, pp. 103-106, 2015.

- [141] R. Shuler, “SEU/SET Tolerant Phase-Locked Loops,” *Radiation Effects in Semiconductors, National Aeronautics and Space Administration, Houston, TX. Lyndon B. Johnson Space Center*, 2010.
- [142] D. Loveless and W. T. Holman, “Single-event mitigation techniques for analog and mixed-signal circuits,” *Ionizing Radiation Effects in Electronics: From Memories to Imagers (1st ed.)*, Bagatin, M., & Gerardin, S. (Eds.), 2016.
- [143] R. Kumar, V. Karkala, R. Garg, T. Jindal, and S. P. Khatri, “A Radiation Tolerant Phase Locked Loop Design for Digital Electronics,” *Proc. of IEEE ICCD*, pp. 505-510, Oct. 2009.
- [144] P. R Fleming, B. D. Olson, W. T. Holman, B. L. Bhuva, and L. W. Massengill, “Design Technique for Mitigation of Soft Errors in Differential Switched-Capacitor Circuits,” *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 55, no. 9, pp. 838-842, Sept. 2008.
- [145] B. D. Olson, W. T. Holman, L. W. Massengill, B. L. Bhuva, P. R. Fleming, “Single-Event Effect Mitigation in Switched-Capacitor Comparator Designs,” *IEEE Trans. Nucl. Sci.*, vol. 55, no. 6, pp. 3440-3446, Dec. 2008.
- [146] N. M. Atkinson, W. T. Holman, J. S. Kauppila, T. D. Loveless, N. C. Hooten, A. F. Witulski, B. L. Bhuva, L. W. Massengill, E. X. Zhang, and J. H. Warner, “The Quad-Path Hardening Technique for Switched-Capacitor Circuits,” *IEEE Trans. Nucl. Sci.*, vol. 60, no. 6, pp. 4356-4361, Dec. 2013.
- [147] W. T. Holman, B. L. Bhuva, J. S. Kauppila, A. F. Witulski, L. W. Massengill and M. L. Alles, “Advanced node-splitting techniques for radiation-hardened analog/mixed-signal circuits,” *2016 IEEE Aerospace Conference*, 2016, pp. 1-8.
- [148] W. P. Parker, “Single-Event Hardened Analog / Mixed-Signal Circuit Layouts Utilizing Node Splitting with Directional Temporal Filtering,” *M.S. Thesis*, Vanderbilt University, May 2018.
- [149] B. D. Olson, “Single-Event Effect Mitigation in Pipelined Analog-to-Digital Converters,” *PhD Dissertation*, Vanderbilt University, 2010.
- [150] E. Mikkola, B. Vermeire, H. J. Barnaby, H. G. Parks, and K. Borhani, “SET Tolerant CMOS Comparator,” *IEEE Trans. Nucl. Sci.*, vol. 51, no. 6, pp. 3609-3614, Dec. 2004.

- [151] L. Perbet, O. Bernal, and H. Tap, “Radiation Hardened by Design Pipeline Analog-to-Digital Converter Blocks in CMOS HV 0.18 μ m Technology,” *6th International Workshop on Analogue and Mixed-Signal Integrated Circuits for Space Applications (AMICSA)*, 2016.
- [152] J. L. Andrews, J. E. Schroeder, B. L. Gingerich, W. A. Kolasinski, R. Koga, and S. E. Diehl, “Single Event Error Immune CMOS RAM,” *IEEE Trans. Nucl. Sci.*, vol. 29, no. 6, pp. 2040-2043, Dec. 1982.
- [153] S. E. Diehl, A. Ochoa, P. V. Dressendorfer, R. Koga, and W. A. Kolasinski, “Error Analysis and Prevention of Cosmic Ion-Induced Soft Errors in Static CMOS RAMs,” *IEEE Trans. Nucl. Sci.*, vol. 29, no. 6, pp. 2032-2039, Dec. 1982.
- [154] A. L. Sternberg, L. W. Massengill, M. Hale, and B. Blalock, “Single-Event Sensitivity and Hardening of a Pipelined Analog-to-Digital Converter,” *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, pp. 3532-3538, Dec. 2006.
- [155] Y. Boulghassoul, P. C. Adell, J. D. Rowe, L. W. Massengill, R. D. Schrimpf, and A. L. Sternberg, “System-level design hardening based on worst case ASET simulations,” *IEEE Trans. Nucl. Sci.*, vol. 51, no. 5, pp. 2787-2793, Oct. 2004.
- [156] S. E. Armstrong, B. D. Olson, J. Popp, J. Braatz, T. D. Loveless, W. T. Holman, D. McMorrow, and L. W. Massengill, “Single-Event Transient Error Characterization of a Radiation-Hardened by Design 90 nm SerDes Transmitter Driver,” *IEEE Trans. Nucl. Sci.*, vol. 56, no. 6, pp. 3463-3468, Dec. 2009.
- [157] T. Uemura, R. Tanabe, Y. Tosaka, and S. Satoh, “Using Low Pass Filters in Mitigation Techniques against Single-Event Transients in 45nm technology LSIs,” *14th IEEE Int. On-line Testing Symposium*, pp. 117-122, July 2008.
- [158] A. L. Sternberg, L. W. Massengill, R. D. Schrimpf, Y. Boulghassoul, H. J. Barnaby, S. Buchner, R. L. Pease, and J. W. Howard, “Effect of Amplifier Parameters on Single-Event Transients in an Inverting Operational Amplifier,” *IEEE Trans. Nucl. Sci.*, vol. 49, no. 3, pp. 1496-1501, June 2002.
- [159] H. Chung, W. Chen, B. Bakkaloglu, H. J. Barnaby, B. Vermeire, and S. Kiaei, “Analysis of Single Event Effects on Monolithic PLL Frequency Synthesizers,” *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, pp. 3539-3543, Dec. 2006.

- [160] T. D. Loveless, L. W. Massengill, W. T. Holman, B. L. Bhuva, D. McMorrow, and J. H. Warner, “A Generalized Linear Model for Single Event Transient Propagation in Phase-Locked Loops,” *IEEE Trans. Nucl. Sci.*, vol. 57, no. 5, pp. 2933-2947, Oct. 2010.
- [161] M. J. Gadlage, P. H. Eaton, J. M. Benedetto, M. Carts, V. Zhu, and T. L. Turflinger, “Digital Device Error Rate Trends in Advanced CMOS Technologies,” *IEEE TNS*, vol. 53, no. 6, Dec. 2006.
- [162] Y. Boulghassoul, *et al.*, “Effects of Technology Scaling on the SET Sensitivity of RF CMOS Voltage-Controlled Oscillators,” *IEEE Trans. Nucl. Sci.*, vol. 52, no. 6, pp. 3466-3471, Dec. 2005.
- [163] E. Hegazi, H. Sjoland and A. A. Abidi, “A filtering technique to lower LC oscillator phase noise,” *IEEE Journal of Solid-State Circuits*, vol. 36, no. 12, pp. 1921-1930, Dec. 2001.
- [164] B. Soltanian and P. R. Kinget, “Tail Current-Shaping to Improve Phase Noise in LC Voltage-Controlled Oscillators,” *IEEE Journal of Solid-State Circuits*, vol. 41, no. 8, pp. 1792-1802, Aug. 2006.
- [165] W. Chen, V. Pouget, G. K. Gentry, H. J. Barnaby, B. Vermeire, B. Bakkaloglu, S. Kiaei, K. E. Holbert, and P. Fouillat, “Radiation Hardened by Design RF Circuits Implemented in 0.13 um CMOS Technology,” *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, pp. 3449-3454, Dec. 2006.
- [166] H. Lapuyade, V. Pouget, J.-B. Begueret, P. Hellmuth, T. Taris, O. Mazouffre, P. Fouillat, Y. Deval, “A Radiation-Hardened Injection Locked Oscillator Devoted to Radio-Frequency Applications,” *IEEE Trans. Nucl. Sci.*, vol. 53, no. 4, pp. 2040-2046, Aug. 2006.
- [167] H. Lapuyade, O. Mazouffre, B. Goumballa, M. Pignol, F. Malou, C. Neveu, V. Pouget, Y. Deval, J.-B. Begueret, “A Heavy-Ion Tolerant Clock and Data Recovery Circuit for Satellite Embedded High-Speed Data Links,” *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, pp. 2080-2085, Dec. 2007.
- [168] I. Esqueda, *Presented at JPL Workshop*, 2019.

- [169] L. Palkuti, M. Alles, and H. Hughes, “The Role of Radiation Effects in SOI Technology Development,” *2014 SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)*, pp. 1-2, 2014.
- [170] H. Hughes, P. McMarr, M. Alles, E. Zhang, C. Arutt, B. Doris, D. Liu, R. Southwick, and P. Oldiges, “Total Ionizing Dose Radiation Effects on 14 nm FinFET and SOI UTBB Technologies,” *2015 IEEE Radiation Effects Data Workshop (REDW)*, pp. 1-6, 2015.
- [171] J. Riffaud, M. Gaillardin, C. Marcandella, N. Richard, O. Duhamel, M. Martinez, M. Raine, P. Paillet, T. Lagutere, F. Andrieu, S. Barraud , M. Vinet, and O. Faynot, “TID Response of Nanowire Field-Effect Transistors: Impact of the Back-Gate Bias,” *IEEE Trans. Nucl. Sci.*, vol. 67, no. 10, pp. 2172-2178, Oct. 2020.
- [172] L. W. Massengill, B. L. Bhuva, W. T. Holman, M. L. Alles, and T. D. Loveless, “Technology Scaling and Soft Error Reliability,” *2012 IEEE International Reliability Physics Symposium (IRPS)*, pp. 3C.1.1-3C.1.7, 2012.
- [173] M. M. Shulaker, G. Hills, R. S. Park, R. T. Howe, K. Saraswat, H.-S. P. Wong, and S. Mitra, ”Three-dimensional integration of nanotechnologies for computing and data storage on a single chip,” *Nature*, vol. 547, pp. 74–78, 2017.
- [174] M. L. Breeding, R. A. Reed, K. M. Warren, and M. L. Alles, “Radiation Effects in 3D Integrated Systems: A Monte Carlo Analysis of Metallic Layers,” *DTRA Report*, 2019.
- [175] M. L. Breeding, R. A. Reed, K. M. Warren and M. L. Alles, “Exploration of the Impact of Physical Integration Schemes on Soft Errors in 3D ICs Using Monte Carlo Simulation,” *2019 IEEE International Reliability Physics Symposium (IRPS)*, pp. 1-7, 2019.
- [176] P. M. Gouker, B. Tyrrrell, R. D’Onfrio, P. Wyatt, T> Soares, W> Hu, C. Chen, J. R. Schwank, M. R. Shaneyfelt, E. W. Blackmore, K. Delikat, M. Nelson, P. McMarr, H. Hughes, J. R. Ahlbin, S. Weeden-Wright, and R. D. Schrimpf, “Radiation Effects in 3D Integrated SOI SRAM Circuits,” *IEEE Trans. Nucl. Sci.*, vol. 58, no. 6, pp. 2845-2854, Dec. 2011.
- [177] L. Sterpone, L. Bozzoli, C. De Sio, B. Du and S. Azimi, “A new Method for the Analysis of Radiation-induced Effects in 3D VLSI Face-to-Back LUTs,” *Proc. 16th*

- International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD)*, pp. 205-208, 2019
- [178] F. Abouzeid, C. L. de Boissac, V. Malherbe, J.-M. Daveau, A. Asquini, V. Bertin, S. De-Paoli, G. Gasiot, C. Timineri, J.-L. Autran, and P. Roche, “Radiation Hardened Cortex R -R4F System-on-Chip Prototype with Total Ionizing Dose Dynamic Compensation in 28nm FD-SOI,” *IEEE Trans. Nucl. Sci.*, vol. PP, 2021.
 - [179] F. Abouzeid, G. Gasiot, D. Soussan, C. L. de Boissac, V. Malherbe, V. Bertin, G. Lallement, J. Autran, and P. Roche, “On-chip total ionizing dose digital monitor in fully depleted SOI technologies,” *IEEE Trans. Nucl. Sci.*, vol. 67, no. 7, pp. 1326–1331, July 2020.
 - [180] A. F. Witulski, M. B. Smith, N. Mahadevan, A. L. Sternberg, C. Barnes, D. Sheldon, R. D. Schrimpf, G. Karsai, and M. W. McCurdy, “Bayesian Modeling of COTS Power MOSFET Ionizing Dose Impact on Circuit Response,” *Proc. 17th European Conference on Radiation and Its Effects on Components and Systems (RADECS)*, 2017, pp. 1-5, 2017.
 - [181] A. F. Witulski, J. Kauppila, G. Karsai, A. Sternberg, R. D. Schrimpf, R. A. Reed, P. Adell, H. Schone, A. Daniel, A. Privat, and H. Barnaby, “Simulation of Transistor-Level Radiation Effects on System-Level Performance Parameters,” *Simulation of Transistor-Level Radiation Effects on System-Level Performance Parameters*, *IEEE Trans. Nucl. Sci.*, vol. 66, no. 7, pp. 1634-1641, July 2019
 - [182] “Intel Powers First Satellite with AI on Board,” Oct. 2020, Available: <https://www.intel.com/content/www/us/en/newsroom/news/first-satellite-ai.html#gs.23ml7k>
 - [183] R. Velazco, A. Assoum, N. E. Radi, R. Ecoffet and X. Botey, “SEU fault tolerance in artificial neural networks,” *IEEE Trans. Nucl. Sci.*, vol. 42, no. 6, pp. 1856-1862, Dec. 1995.
 - [184] A. Assoum, M. E. Radi, R. Velazco, F. Elie and R. Ecoffet, “Robustness against S.E.U. of an artificial neural network space application,” *Proc. 3rd Conference on Radiation and its Effects on Components and Systems*, 1995, pp. 443-448.
 - [185] S. Buchner, M. Olmes, Ph. Cheynet, R. Velazco, D. McMorrow, J. Melinger, R. Ecoffet, and J. D. Muller, “Pulsed laser validation of recovery mechanisms of critical

- SEE's in an artificial neural network system," *Proc. 4th European Conference on Radiation and its Effects on Components and Systems (Cat. No.97TH8294)*, 1997, pp. 353-359.
- [186] Z. Ye, R. Liu, H. Barnaby and S. Yu, "Evaluation of Single Event Effects in SRAM and RRAM Based Neuromorphic Computing System for Inference," *Proc. IEEE International Reliability Physics Symposium (IRPS)*, pp. 1-4, 2019.
 - [187] Z. Ye, R. Liu, J. L. Taggart, H. J. Barnaby and S. Yu, "Evaluation of Radiation Effects in RRAM-Based Neuromorphic Computing System for Inference," *IEEE Trans. Nucl. Sci.*, vol. 66, no. 1, pp. 97-103, Jan. 2019.
 - [188] R. M. Brewer *et al.*, "The Impact of Proton-Induced Single Events on Image Classification in a Neuromorphic Computing Architecture," *IEEE Trans. Nucl. Sci.*, vol. 67, no. 1, pp. 108-115, Jan. 2020.
 - [189] W. Li *et al.*, "Soft Error Mitigation for Deep Convolution Neural Network on FPGA Accelerators," *Proc. 2nd IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS)*, 2020, pp. 1-5.
 - [190] H. . -B. Wang, Y. . -S. Wang, J. . -H. Xiao, S. . -L. Wang and T. . -J. Liang, "Impact of Single-Event Upsets on Convolutional Neural Networks in Xilinx Zynq FPGAs," *IEEE Trans. Nucl. Sci.*, vol. 68, no. 4, pp. 394-401, April 2021.
 - [191] B. Patel, M. Joplin, R. C. Boggs, D. R. Reising, M. W. McCurdy, L. W. Massengill, and T. D. Loveless, "Ionizing Radiation Effects Spectroscopy for Analysis of Total-Ionizing Dose Degradation in RF Circuits," *IEEE Trans. Nucl. Sci.*, vol. 66, no. 1, pp. 61-68, Jan. 2019.
 - [192] T. D. Loveless, B. Patel, D. R. Reising, R. Roca, M. Allen, L. W. Massengill, and D. McMorrow, "Ionizing Radiation Effects Spectroscopy for Analysis of Single Event Transients," *IEEE Trans. Nucl. Sci.*, vo. 67, no. 1, pp. 99-107, Jan. 2020.
 - [193] T. D. Loveless, D. R. Reising, J. C. Cancelleri, L. W. Massengill, and D. McMorrow, "Analysis of Single Event Transients (SET) using Machine Learning (ML) and Ionizing Radiation Effects Spectroscopy (IRES)," *IEEE Trans. Nucl. Sci.*, vol. PP, 2021.

Part III

Hardening Techniques for

Image Sensors

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1 Introduction

1.1 Scope of the course

This course aims at summarizing the main techniques used to improve by design – or by minor process modification – the radiation hardness of solid-state image sensors based on semiconductor materials. For the reasons detailed in the next section, the focal point of this document is the CMOS Image Sensor (CIS) technology. However, the presented basic mechanisms, mitigation techniques, and discussions can be transposed or applied to many other solid-state image sensor technologies. Since one of the most important parameters discussed here is the radiation induced leakage current in reverse biased PN-junctions, the conclusions presented in this course can as well be useful to improve the tolerance to radiation of any leakage sensitive CMOS Integrated Circuit (IC).

This course is aimed at non-expert in imaging technologies but with a background in radiation effects [1]–[10] and Radiation-Hardening-by-Design (RHBD) techniques [11]–[15] for CMOS devices and ICs in general.

1.2 Overview of Solid-State Image Sensors

Solid-state image sensors are electronic devices that convert optical images into an electronic signal (Figure 1). This analog electronic representation of an optical scene is generally digitized to obtain a digital image divided into elementary spatial samples called pixels (combination of “picture” and “element”). In the image sensor circuit, the spatial sampling is performed by elementary electronic cells, generally called pixels as well. Physical pixels are often identical and repeated in an array of the desired size (called resolution or format and defined as a number of pixels). These imaging devices play in cameras and optical instruments a similar role as the retina in human eye.

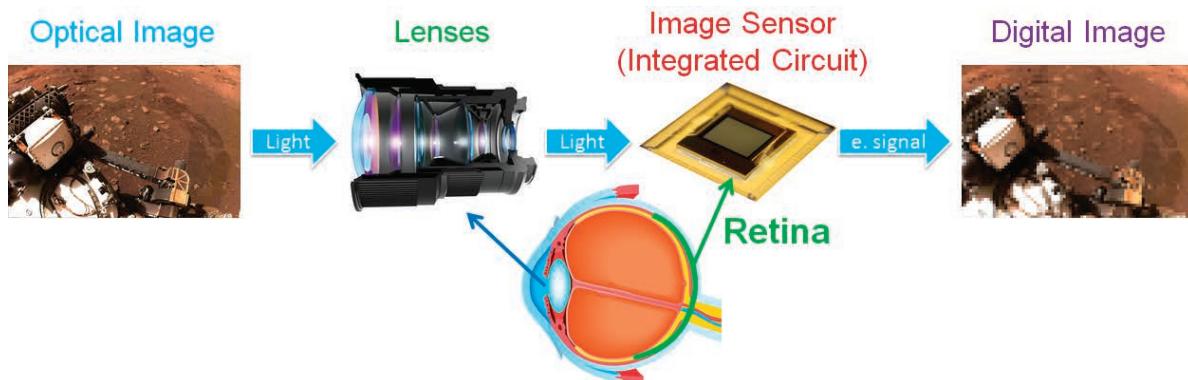


Figure 1 : Solid-state image sensor illustration. Perseverance Rover picture credits: NASA/JPL-Caltech.

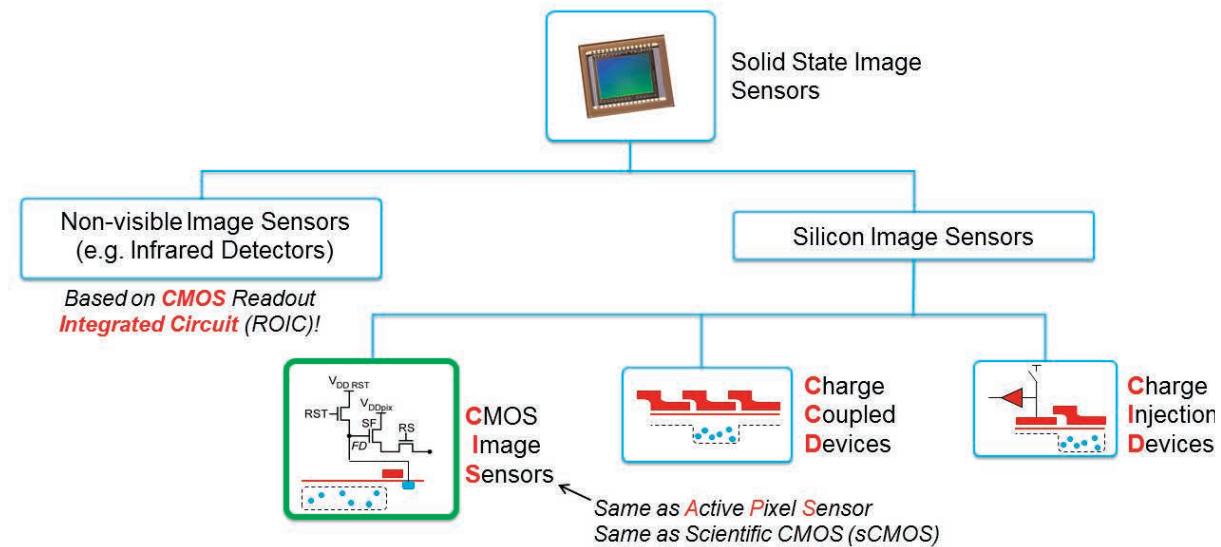


Figure 2 : A classification of the main image sensors technologies.

A wide variety of solid-state image sensors and pixel array technologies exist. Especially, depending on the electromagnetic radiation spectrum or the particle to detect, various materials, architectures and concepts can be used to absorb, convert and collect the image information. Giving a comprehensive list goes beyond the scope of this course and only the main imager technologies are presented in Figure 2.

The quantum efficiency (ratio of the number of collected carriers to the number of incoming photons) of silicon photodetectors is high in the visible spectrum (roughly photon wavelengths between 400 nm – 800 nm). This makes silicon the semiconductor of choice for visible imaging and optical applications. Three main silicon detectors technologies have been developed: Charge Coupled Devices (CCD), Charge Injection Devices (CID), and CMOS Image Sensors.

1.2.1 Charge Coupled Devices

A Charge Coupled Device consists of an array of MOS capacitors that can be placed into deep depletion by the application of the required voltage on their gate. By doing so, potential wells are created under each gate and the well depth can be adjusted by varying the gate voltage. In such device, photogenerated carriers are collected by the created potential wells when the CCD array is exposed to light. By periodically changing the MOS capacitor gate voltages, the photo-collected charge can be transferred to adjacent pixels. In state-of-the-art CCDs, this charge transfer process can be considered as nearly lossless and noiseless, allowing to move the signal charge over the array without any measurable degradation. More than one MOS capacitor per pixel is required to allow this pixel-to-pixel transfer (at least three). In a basic CCD, to readout the photogenerated charge collected by one CCD pixel, the charge has to be moved by numerous pixel-to-pixel transfers (as illustrated in Figure 3) to the output stage where the charge can be converted to a voltage signal and sent outside the sensor. More detailed and accurate descriptions of the CCD technology can be found in [16], [17]. For this course, the most relevant information regarding the CCD technology is the following:

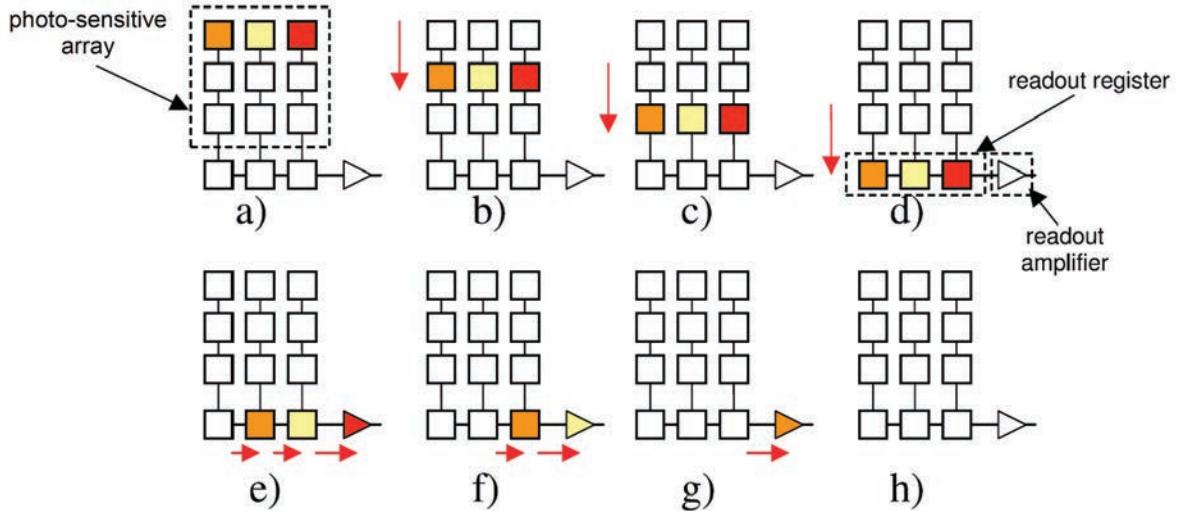


Figure 3 : 3x3 CCD pixel array basic read-out principle. a-d) Each row is transferred vertically to the readout register. e-h) Each pixel value stored in the readout register is read-out sequentially through the amplifier. The charge to voltage conversion is performed at the entrance of the output amplifier.

- CCD pixels are readout through numerous successive charge transfers (up to several thousands of successive transfers). These devices are thus very sensitive to charge transfer degradation.
- Except the output amplifier, no active electronics can be integrated in classical CCD (no complementary N and P MOS transistors), nor in the pixels, neither on the chip outside the pixel array.
- Thicker oxides and higher voltages than CMOS technologies are generally used in CCDs.

1.2.2 Charge Injection Devices

As CCD, CIDs [18], [19] are based on MOS capacitors to collect, store and sense the photo-generated carriers. CID operating principle also relies on charge transfer but only a single one is required to readout the signal. Contrary to CCDs, the charge-to-voltage conversion is performed inside each pixel and the resulting signal can directly be accessed without having to readout the entire array. CIDs can be manufactured using NMOS, PMOS or CMOS processes. Active electronics can then be integrated on-chip and even in pixel. One of the major advantages of CIDs compared to CCDs is their higher radiation hardness at the cost of lower optoelectronics performances and higher noise. The capability to integrate active electronics on-chip is also a benefit compared to CCDs.

1.2.3 CMOS Image Sensors

CMOS Image Sensors [20], [21] can be described as any solid-state image sensor manufactured with a CMOS process (which is the case of some CIDs). Most CISs can be considered as Active Pixel Sensors (APS) since in-pixel active electronics (at least a basic source follower amplifier) is used in the wide majority of CISs. The term APS is sometimes preferred for detectors and pixel arrays manufactured with a standard CMOS process whereas CIS can be

reserved to imagers manufactured using optimized CIS processes with special features to enhance the imaging performances. CIS are sometimes simply called CMOS sensors or scientific CMOS (sCMOS) in commercial applications. In the particle detection community, CMOS detectors are often referred to as Monolithic Active Pixel Sensors by opposition to hybrid detectors with a CMOS Readout Integrated Circuit (ROIC). Contrary to CCD and CID, there is no limit to what can be integrated into a CIS pixel and various types of photosite can be used (photodiode, pinned photodiode, photogate...). However, most of modern CISs are based on reverse biased PN-junctions, as discussed in section 1.3.2.

1.2.4 CMOS vs CCD vs CID

Table 1 gives a comparison of the reported capabilities of the three main silicon image sensor technologies just mentioned. Whereas the CCD technology has been the technology of choice for high-end applications for decades, the CMOS technology is now as good as CCDs at nearly everything and can do so much more thanks to the regular cutting-edge innovations offered by state-of-the-art CIS processes [22]. There is a single case where CCD can win over CMOS: when massive use of noiseless and lossless charge transfer is required. Specific imaging modes like Time Delay Integration (TDI) [23]–[25] illustrate this point. However, CIS technology can still compete either by emulating charge transfer in the digital domain (but with added noise compared to CCD), or more efficiently by using CCD on CMOS technology [26] features offered by some CIS foundries such as Capacitive Trench-Based Charge Transfer Devices [27].

In terms of radiation hardness, all the three technologies exhibit radiation induced dark current increase when exposed to ionizing and non-ionizing radiation. Most CCDs typically suffer from flatband voltage shifts of 100 mV/krad [10], [28] that lead to complete failure at TID level ranging from 10 to 100 krad (see [29] for instance). By using thinner gate oxides, CCD tolerance to TID can be pushed to 500 krad [28] and possibly beyond, but most likely not much further. Radiation induced charge transfer efficiency degradation is also an important issue for CCDs, especially because both TID and displacement damage can degrade this parameter. By getting rid of the numerous successive charge transfers required to readout the signal in CCDs, CIDs are more tolerant to flatband voltage shifts and to radiation induced charge transfer degradation. By sensing and compensating voltage shifts, CIDs can still provide useful images at TID as high as a few Mrad [18], [19]. This higher radiation tolerance (compared to CCDs) has made CID a popular technology for radiation tolerant cameras for years.

Depending on the technology node and the integrated peripheral functions, unhardened Commercial-Off-The-Shelf (COTS) CIS failure TID is expected to be higher than 100 krad and core CIS functions can generally withstand several Mrad before complete failure. This makes some unhardened COTS CISs nearly as radiation tolerant as hardened CIDs. By using RHBD techniques, radiation hardness as high as 1 Grad has been demonstrated on CMOS sensors[30], [31]. In addition to this demonstrated higher tolerance to radiation, the CIS technology offers numerous possibilities to go beyond by using minor manufacturing process modifications or by implementing additional mitigation techniques at the layout or circuit level. CIS are then the technology of choice when radiation hardness is a constraint and most of the newest radiation tolerant camera products are based on CMOS sensors.

	CCD	CID	CMOS
Sensitivity / Quantum Efficiency	Highest	Lower than state-of-the-art CCD and CMOS	Can be as good as CCDs with the same treatment.[32] Photon Counting <u>without avalanche multiplication</u> achievable.[33]
Read Noise	Low	High	Can be lower than CCDs. Sub 0.3 e- read noise achieved.[34]
Dark Current	Ultra-low	Higher than state-of-the-art CCD and CMOS	Can be lower than CCDs. Less than 1 e-/s at 60°C often reported in small pixel pitch CIS.
Electronic Function Integration	None	Generally limited but in theory could benefit of any modern CMOS feature	All the possibilities offered by state-of-the-art CMOS technologies can be used
Binning	Extremely high noiseless binning levels can be naturally achieved	No binning	Charge, analog and digital binning possible. Might not be as good as CCD yet for high binning levels.
Blooming	Blooming is a key issue in CCDs and antiblooming structures degrade the performance	Less critical than in CCDs	Native anti blooming feature through the in-pixel reset transistor. Additional features available to reduce further blooming effects. A CIS with full height DTI is totally immune to blooming
Specific operation that requires charge transfer over many rows / columns	CCD most suited	Not possible	Possible in the voltage / digital domain but with added noise.[25] Recent CCD on CMOS technologies such as the use of Capacitive Deep Trench isolations[27] makes it possible to compete with CCD in this last bastion.
Cost	Generally expensive	-	As expensive as CCDs (or even more) for custom sensors with higher performances. Can be extremely cheap for mass market applications (e.g. smartphone cameras).
Radiation Hardness	Typically 10 krad – 100 krad on classical CCDs [10] Above 500 krad by using thin gate oxide	5 Mrad [18]	Typically, between 100 krad and a few Mrad for COTS. 1 Grad demonstrated on radiation hardened CIS. [30], [31]
Room for RHBD	Limited	Limited	Process level, layout level and circuit design level radiation hardening possible

Table 1 : CCD, CID and CMOS comparison based on reported technology capabilities.

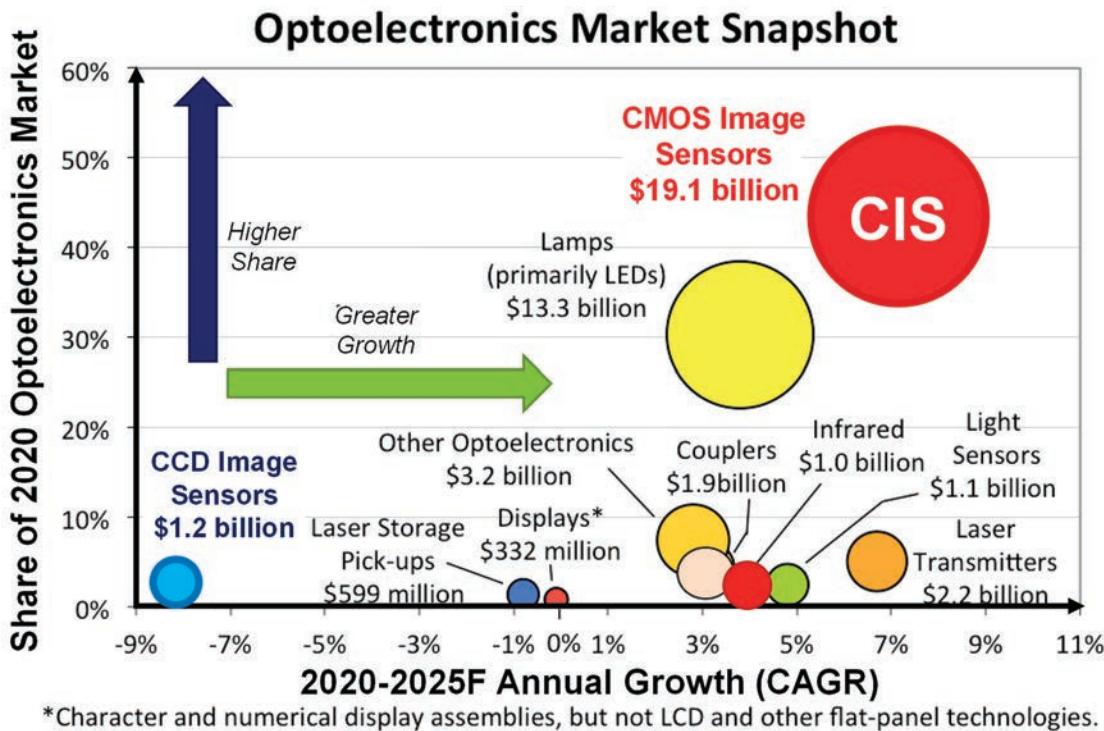


Figure 4 : 2021 optoelectronic market snapshot. Source IC Insights 2021 O-S-D Report. Courtesy of Rob Lineback from IC Insights.

Overall, this table clearly shows that, based on the technology capability criterion, CISs are the best choice in almost every situation. If instead of comparing what each technology can do, we perform the same comparison but based on the performance of Commercial Off-The-Shelf (COTS) sensors, the CIS technology would have a less obvious dominating position, since some of the benefits listed in this table can only be obtained on custom sensors or has only been recently demonstrated in the lab but not in a mature product. This difference between the technology point of view and the market point of view can be justified by the fact that, in some niche applications, the market is not significant enough to justify the development of a new CMOS based product when an existing CCD or CID provides satisfactory results. That is the main reason why CCDs and CIDs are still used in some niche applications and some camera products in 2021, but the CIS technology appears clearly as the technology of choice for any new sensor development, whatever the application and whatever the requirement level.

This conclusion can be illustrated by the 2021 state of the optoelectronics market shown in Figure 4 (adapted with permission from [35]). CISs occupy nearly 50% of the whole optoelectronics market with an 8% annual growth whereas the CCD technology only represents less than 5% of the same market with an 8% annual reduction. Even compared to the entire semiconductor category, CISs remain a key semiconductor product representing 5% of the whole market. IC Insights even concluded in 2020 that “CMOS image sensors were the fastest growing semiconductor product category in the last decade”[36].

1.2.5 Non-VISIBLE Image Sensors

For non-visible imaging, other semiconductor materials are often used to efficiently absorb the radiation, such as III-V (InSb, GaAs...) and II-VI (e.g. HgCdTe) compound semiconductors. Compared to CMOS sensors, the literature about radiation effects and radiation hardening is less developed on infrared detectors. On the other hand, those detectors are generally based on reverse biased PN-junctions, such as in most CMOS sensors, and to make a pixel array and turn these photodetectors into an imaging device, a CMOS IC is generally required and hybridized to the infrared radiation sensitive layer. These similarities with CISs allow transposing in part the recommendations presented here to IR detectors and other non-visible image sensors with comparable similarities.

1.2.6 Selected Image Sensor Technology for this Short-Course

After all, CMOS Image Sensors appear as the main solid-state image sensor technology in 2021 (and it seems here to stay) with probably the highest achievable performances and the highest intrinsic radiation hardness. Besides those key advantages, there is an important activity in CMOS sensor custom design in laboratories and companies all over the world. CMOS processes also offer numerous possibilities to mitigate radiation induced performance degradation. Finally, radiation induced degradations and associated counter measures are often similar in alternative image sensor technologies. For all these reasons, this course focuses its discussions on CMOS sensors.

1.3 The CMOS Image Sensor Technology

This section aims at providing a minimum background to discuss radiation effects in CISs and radiation hardening.

1.3.1 Architecture Overview

Descriptions of CMOS Active Pixel Image Sensors can be found in [21], [37]–[41]. As any APS, CIS are constituted by [21] a pixel array, addressing circuits to access the pixels (the address decoders) and an analog signal processing circuit (often called readout circuit). This basic architecture common to nearly every APS IC is presented in Figure 5. In addition to these necessary building blocks, modern CIS products often integrate on-chip one or more of the following functions: one Analog-to-Digital Converter (ADC) per column (see for example [42]–[44] and references therein for ADC architectures used in CISs), a sequencer, a digital image processing unit, high speed I/O interfaces, configuration registers, a Serial Programming Interface (SPI), a Phase Locked Loop (PLL), memories, processors, and so on.

For peripheral analog or digital functions, radiation effects and RHBD techniques are the same as for any CMOS IC. The reader can refer to the two previous parts of this short course: Balaji Narasimham short course [15] for dealing with Single Event Effects (SEE) in peripheral circuits and Daniel Loveless short course [14] on mitigating SEE and Total Ionizing Dose (TID) effects in analog and mixed-signal CMOS circuits.

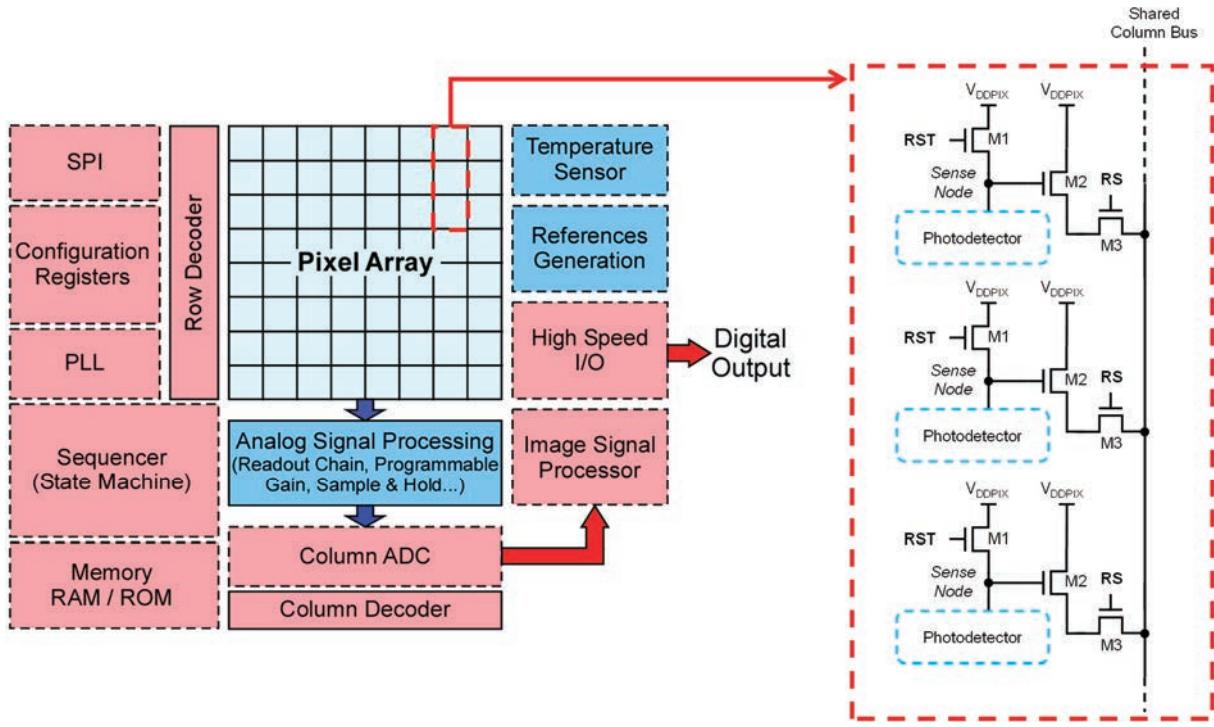


Figure 5 : Typical CMOS Image Sensor Integrated Circuit architecture (the dashed blocks are optional and depends on the product/the application) with the details of three selected pixels (outlined with a red dashed line).

This document focuses on radiation effects and hardening techniques that are specific to image sensors:

- TID effects in pixel arrays (including photodetector and in-pixel transistors)
- SEE in pixel arrays and, more generally, the impact of the CIS substrate on the full circuit tolerance to Single Event Transient (SET) and Single Event Latchup (SEL)
- Displacement Damage (DD) effects in pixel arrays

Figure 6 gives the details of a basic CIS pixel architecture constituted of three transistors:

- One to reset the photodetector (M1). Also called the reset (RST) transistor.
- One to isolate the sense node from the rest of the circuit (M2), also called Source Follower (SF) transistor.
- One to select the pixel (M3) also called Row Switch or Row Select (RS) transistor.

In most of modern CIS products (and as well in most of solid-state image sensors), the photodetector consists in a reverse biased PN-junction used to collect the free carriers generated by the absorption of light. As discussed hereafter, an additional transistor can be necessary to access this photodetector.

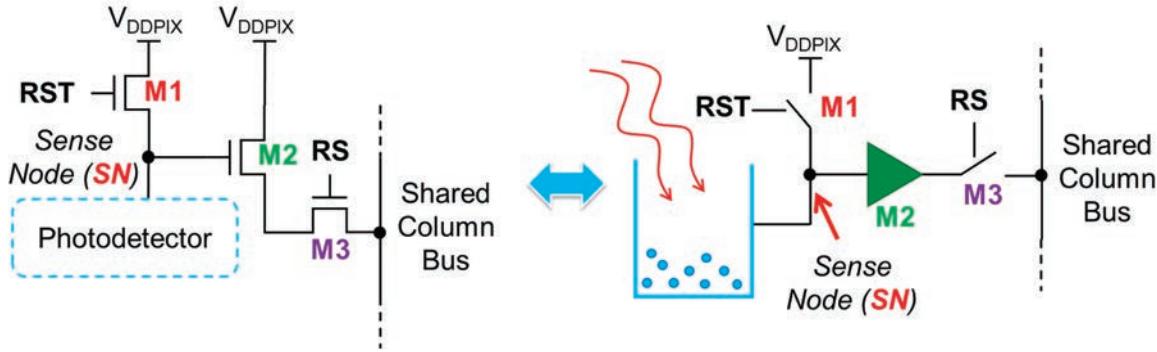


Figure 6 : Equivalent functional model of a basic CIS pixel presenting the details of in-pixel transistor functions.

1.3.2 Main CIS Photodetector Technologies

Several photosensitive semiconductor devices (e.g. photogates [21], [45]) can be used to make a CMOS sensors[21], but only the two main technologies used in 2021 are covered in these notes:

- The conventional photodiode used in so-called 3T-pixel architectures (most basic APS pixel [21] with 3 transistors per pixel). This historical photodetector is mainly used in niche applications that do not require the use of more advanced devices (or when more advanced devices cannot be used).
- The pinned photodiode (PPD) [46]–[49] with in-pixel charge transfer used in 4T-pixel architectures (with 4 transistors per pixel). This photodetector structure is used in almost all CCDs and CISs due to its low noise, high quantum efficiency and low dark current” [49].

The cross-sectional views of these two photodiodes are shown in Figure 7. The conventional CIS photodiode used in 3T-pixels is typically a deep N-CIS implant (similar to N-well implants but optimized for photodetection) on a P-epitaxial layer and surrounded by a P-well. Depending on the design, the Shallow Trench Isolation (STI) can cover the whole N-CIS implant or be recessed from the N-CIS region. In any case, the depletion region in conventional photodiodes reaches an oxide interface all over its perimeter. In other type of APS (such as MAPS), this conventional photodiode can be made using the N-MOSFET Source/Drain N+ implant or the P-MOSFET N-well implant. Some APS even use triple or quadruple well technologies to realize deeper photodiodes[50][51][52]. It is also possible to reverse the doping types and to use P on N substrate photodiodes.

Contrary to the conventional CIS photodiode, the PPD is a buried N-PPD implant surrounded by a P-well (or trench isolation passivation P doping) and protected from the first Inter Layer Dielectric (ILD) interface by a P+ pinning implant on top of it. This pinning layer is also used to ensure the full depletion of the PPD N region after a complete charge transfer. If the Transfer Gate (TG) is completely turned OFF (i.e. biased in accumulation regime, generally with the use of negative gate voltage), the PPD depletion region is not supposed to reach any oxide interface

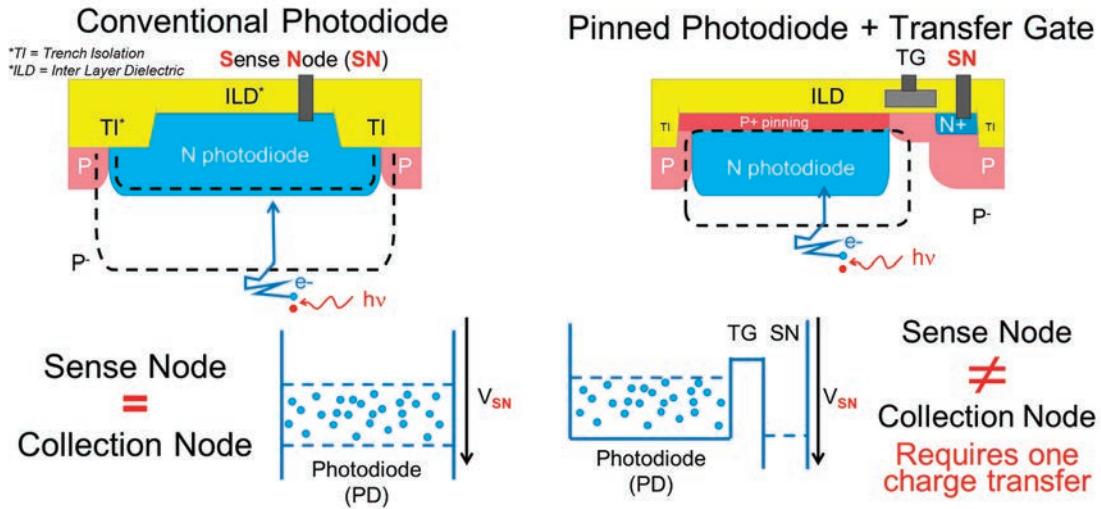


Figure 7 : Cross section illustration of the two main CIS photodiodes: the conventional photodiode (left) and the pinned photodiode with in pixel charge transfer (right).

because it is protected from the STI by the P-well doping, from the ILD by the pinning layer and from the TG channel by the TG accumulation layer.

It should be emphasized that in classical 3T-pixel the photodiode cathode is the same node as the Sense Node (SN). Therefore, the pixel Charge to Voltage conversion Factor (CVF) is given by the photodiode capacitance and the sensor gain will depend on the photodiode size (the larger the photodiode, the lower the gain). In a 4T-PPD pixel, since the photodiode and the SN are two distinct nodes, the photodiode size does not impact the CVF and the pixel gain can be adjusted without changing the photodiode size.

1.3.3 Operating Principles

Figure 8 presents the simplified operations of the 3T conventional photodiode pixel and the 4T pinned photodiode pixel. In a 3T pixel, three main phases can be described:

- Reset: the photodiode is first pre-charged to V_{DD} by enabling the RST MOSFET.
- Integration: the RTS MOSFET is disconnected and the Sense Node (SN) is left floating to integrate the photosignal on the photodiode capacitance. In this mode, the free carriers generated by photoelectric effects are collected by the PN junction depletion region electric field, leading to a photocurrent. This photocurrent discharges the floating reverse biased photodiode capacitance.
- Measure: in this last phase, the Row Select switch is enabled to readout the sense node voltage at the end of the integration time. If compared to the reference level measured after reset (see Figure 9 for a more detailed timing diagram), this measured value gives the number of photo-collected carriers.

In a 4T-PPD pixel, the photodiode collection well is not directly connected to the SN. Hence, an additional step is necessary to transfer the useful photodiode charge from the PPD to the SN (the transfer phase in Figure 8).

Figure 9 presents more detailed timing diagrams showing how this pattern is repeated to readout a full array and when the reference signal is sampled. The first figure (Figure 9.a) shows an overview of an electronic rolling shutter (ERS) timing diagram. In this classical readout mode, each row is sampled individually in sequence on the two capacitances of the column Sample and Hold (S/H) stage to perform the double sampling operation. Once the signal and reference values of each pixel in a row have been sampled on the S/H stages, the column multiplexer sends the analog or digital (if a column ADC is used) pixel values to the sensor output. The column multiplexer is driven by the column decoder whereas the row S/H phase is enabled by the row decoder. The detail of a classical 3T-pixel S/H phase is shown in Figure 9.b. The RST signal reset the photodiode by turning on the RST MOSFET whereas the SHS command samples the signal value and SHR samples the reference value. During a 3T-pixel S/H phase, the sampled reference value does not correspond to the same frame as the sampled signal value. This kind of differential sampling is called Delta Reset Sampling (DRS). It allows to cancel the offset Fixed Pattern Noise (FPN) and makes it possible to reduce the low frequency noise but it does not cancel the reset noise [53]

In 4T-PPD-pixels, the collecting node (i.e. the PPD) and the readout node (i.e. the SN or FD) are separated. It leads to a different readout scheme. During integration, the PPD and TG are isolated by turning the TG OFF (i.e. biased to V_{LOTG} as shown in (Figure 9.c)) and the photo generated electrons are collected in the PPD potential well. Right before the end of the integration phase (Figure 9.c), the FD node is reset to its reference level by turning ON the RST MOSFET, then the FD reference voltage level is sampled on the column SH stage (i.e. SHR is turned on). Next, the TG is also activated (i.e. biased to V_{HITG}) to transfer the charge from the PPD to the FD and finally, the signal value (reference value + the voltage drop induced by the transferred charge) is sampled by pulsing the SHS command signal. An optional dump phase in which RTS and TG are both enabled can be used to further reset the photodiode and reduce image lag (if any).

It is important to notice that, contrary to the classical 3T-pixel readout timing diagram, the sampled reference and signal values belong to the same frame, as shown in Figure 9.c. This double sampling operation is then called Correlated Double Sampling (CDS) and allows to cancel both the offset FPN and the reset noise (and also to reduce the low frequency noise) [53].

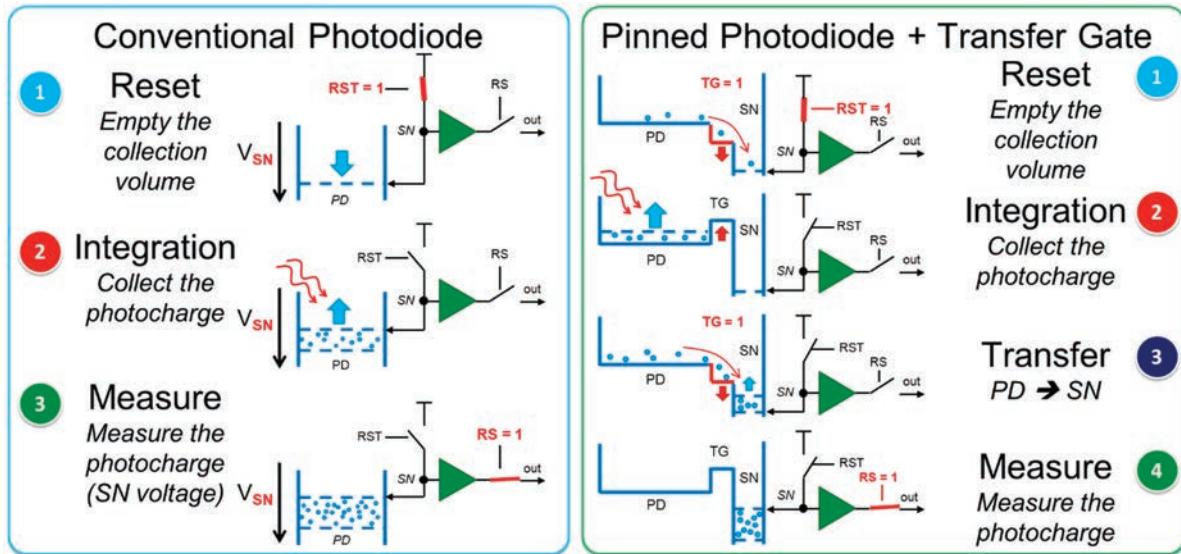


Figure 8 : Simplified pixel operation: 3T pixel with conventional photodiode case (left) and 4T-PPD pixel case (right).

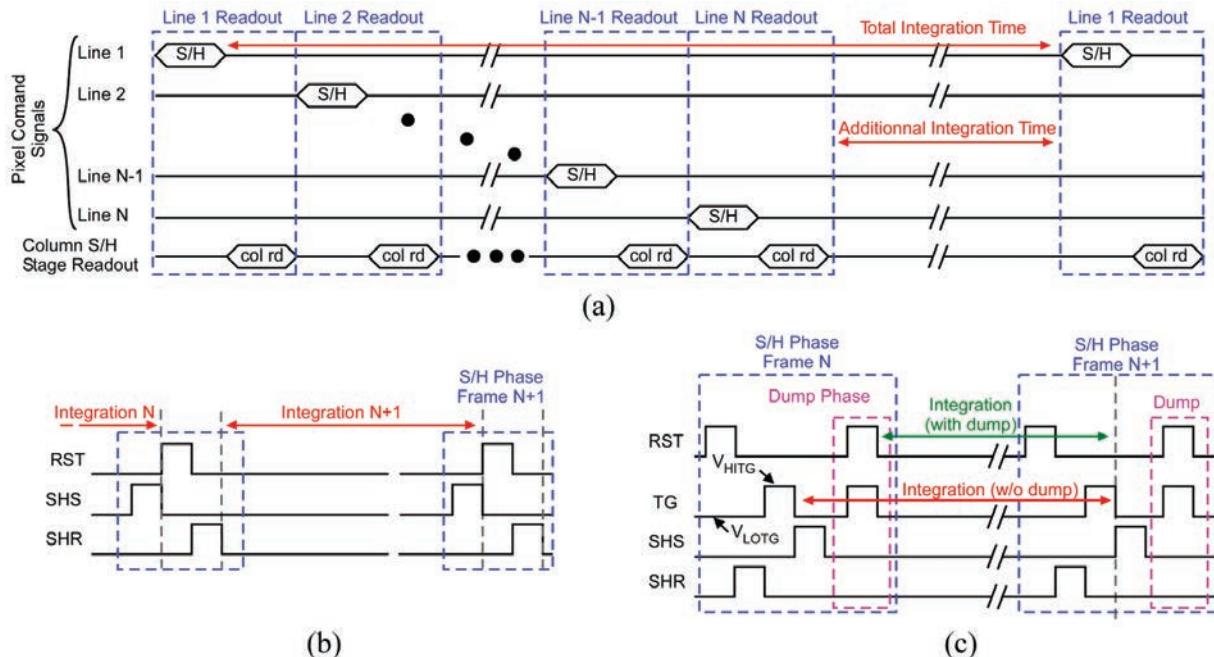


Figure 9 : Detailed CIS typical timing diagrams: (a) Basic Electronic Rolling Shutter timing diagram overview. (b) 3T Pixel command signal timing diagram. (c) 4T PPD pixel command signal timing diagram.

1.3.4 Dark Current and Random Telegraph Signals in CIS

As developed in chapters 2 and 3 of these notes, the dark current increase is the main radiation induced degradation that needs to be mitigated in image sensors. This section aims at clarifying the nature of dark current, its physical origin and its impact on CIS image quality. Since it is closely related to dark current, Dark Current-Random Telegraph Signal (DC-RTS) is also introduced in this section. More information about the other typical solid-state imager performance parameters can be found in the following references [16], [17], [21], [37]–[41], [54].

1.3.4.1 Dark Current Definition, Origin and Modelling

At the beginning of the integration time (right after the reset phase), the CIS photodiode is reverse biased to empty the collecting well of previously integrated charge carriers. This reverse bias increases the depletion volume and places the collecting well under non-equilibrium condition (i.e. $p \cdot n < n_i^2$ in the depletion region, as shown in Figure 10). The Shockley-Read-Hall (SRH) recombination/generation process [55][56], originating from defect/trap energy states in the bandgap, induces a parasitic reverse current that fills the well by discharging the potential to return to equilibrium (i.e. 0V photodiode bias and $p \cdot n = n_i^2$). The net SRH recombination rate U for **one single given defect** – with an energy level E_t in the bandgap and electron and hole capture cross sections σ_n and σ_p , respectively – is given by:

$$U = \frac{\sigma_n \sigma_p v_{th} (pn - n_i^2)}{\sigma_n \left[n - n_i \exp\left(\frac{E_t - E_i}{kT}\right) \right] + \sigma_p \left[p - n_i \exp\left(\frac{E_i - E_t}{kT}\right) \right]} \quad (1)$$

In this equation, the intrinsic carrier concentration n_i is defined as $n_i = \sqrt{N_c N_v} \exp\left(-\frac{E_g}{2kT}\right)$.

Since $p \cdot n < n_i^2$, the net recombination/generation rate U is negative and the dominating SRH mechanism is the electron-hole pair generation through defect states in the band-gap. In CMOS sensors, this SRH generation induced parasitic current is called the dark current. Under illumination, it adds up to the photocurrent to discharge the photodiode capacitance and corrupt the measured signal, as illustrated in Figure 11.

The dark current can take several forms depending on its origin inside the pixel:

- **Interface state generation dark current (source 1 in Figure 12):** if the photodiode depletion region is in contact with a Si-oxide interface, the high density of mid-gap interface states (N_{it}) leads to an intense generation contribution [57] that generally hides the other dark current sources. Starting with (1), if we consider that the main leakage current contribution is provided by mid-gap interface states (i.e. $E_t \approx E_i$), that $\sigma_n = \sigma_p = \sigma$ and that the concentrations of electrons n and holes p are zero in at the depleted interface, this dark current contribution can be expressed as:

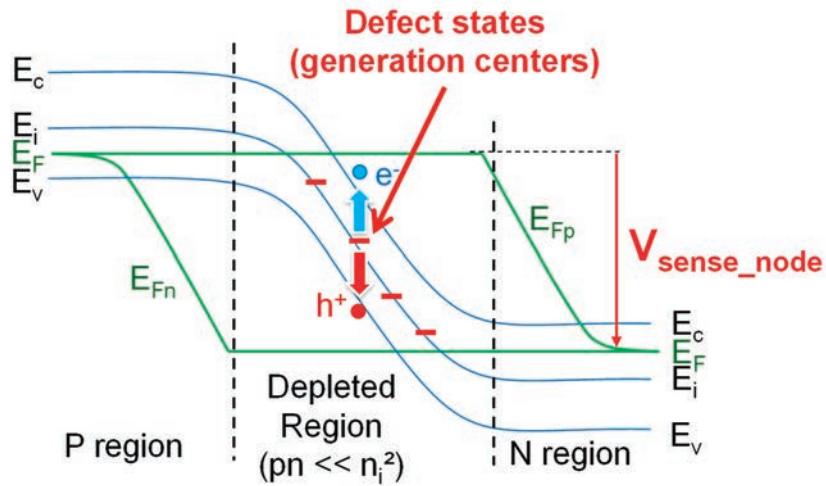


Figure 10 : Energy band diagram of a reverse biased PN-junction illustrating the SRH generation of electron/hole pairs through defect centers.

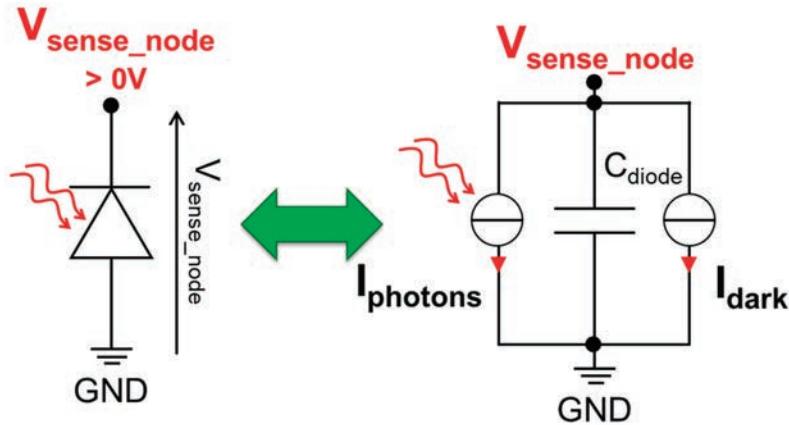


Figure 11 : Equivalent electrical schematic of a reverse biased photodetector showing the photodiode capacitance (C_{diode}), the photocurrent ($I_{photons}$) and the dark current (I_{dark}) contribution.

$$I_{itgen} = \frac{1}{2} q \sigma v_{th} \sqrt{N_c N_v} \exp\left(-\frac{E_g}{2kT}\right) A_{itdep} N_{it} \quad (2)$$

with q the elementary charge, v_{th} the thermal velocity, N_c and N_v the effective densities of states in the conduction and valence bands respectively, A_{itdep} the area of depleted Si/oxide interface, N_{it} the interface state density, k the Boltzmann constant, E_g the bandgap energy and T the temperature. It should be emphasized that the **apparent**

activation energy¹ of this leakage current in an Arrhenius plot would be around $E_a = 0.63\text{-}0.65 \text{ eV}$ in silicon. It corresponds to the mid-gap energy (0.56 eV) slightly increased by the temperature dependence of the preexponential terms.

- **Bulk generation dark current (source 2 in Figure 12):** a bulk defect with energy E_t in the bandgap will generate the following dark current if it is located in the depletion region of the photodiode (under non-equilibrium) [57], [59]:

$$I_{\text{bkgen}} = \frac{q\sigma v_{th}\sqrt{N_c N_v} \exp\left(-\frac{E_g}{2kT}\right) V_{\text{dep}} N_t}{2\cosh(|E_i - E_t|/kT)} \quad (3)$$

with V_{dep} the depleted volume and N_t the defect concentration. This equation is derived from (1) with the same assumptions as in the previous case, except that the trap energy state is not necessarily mid-gap. Further simplifications can be obtained if some assumptions are made on the trap energy level:

$$\text{if } E_i = E_t \text{ (mid-gap state): } I_{\text{bkgen}} = \frac{q\sigma v_{th}\sqrt{N_c N_v}}{2} V_{\text{dep}} N_t \exp\left(-\frac{E_g}{2kT}\right) \quad (4)$$

$$\text{if } |E_i - E_t| \gg kT : I_{\text{bkgen}} = q\sigma v_{th}\sqrt{N_c N_v} V_{\text{dep}} N_t \exp\left(-\frac{\frac{E_g}{2} + |E_i - E_t|}{kT}\right) \quad (5)$$

This last equation shows that the **apparent activation energy of a non-mid-gap trap will be $0.63 + |E_i - E_t|$** – hence higher than the expected value for a mid-gap defect – and that the trap energy E_t can be estimated from an Arrhenius plot as it is done in [59]–[65].

- **Interface state diffusion dark current (source 3 in Figure 12):** if the generation currents originating from the depletion region (I_{itgen} and I_{bkgen}) are low enough (as in state-of-the-art PPDs), the dark current contribution coming from the generation of undepleted interfaces can be visible. Minority carriers generated at the interface (outside the depletion region) diffuse toward the photodiode depletion region, leading to a generation induced diffusion current often simply referred to as diffusion current [57], [66]. Under certain simplifying assumptions (realistic for CIS), this interface state diffusion dark current contribution can be expressed as [67][68]:

$$I_{\text{itdiff}} = q\sigma v_{th} N_c N_v \exp\left(-\frac{E_g}{kT}\right) \frac{A_{\text{it}} N_{\text{it}}}{N_{A,D} \left(1 + \frac{x_{SiO_2} \sigma v_{th}}{D_{n,p}} N_{\text{it}}\right)} \quad (6)$$

¹ If the dark current evolution with temperature is fitted using the Arrhenius law $A=K \exp(-E_a/kT)$ [58], the value of E_a is the activation energy of the dark current.

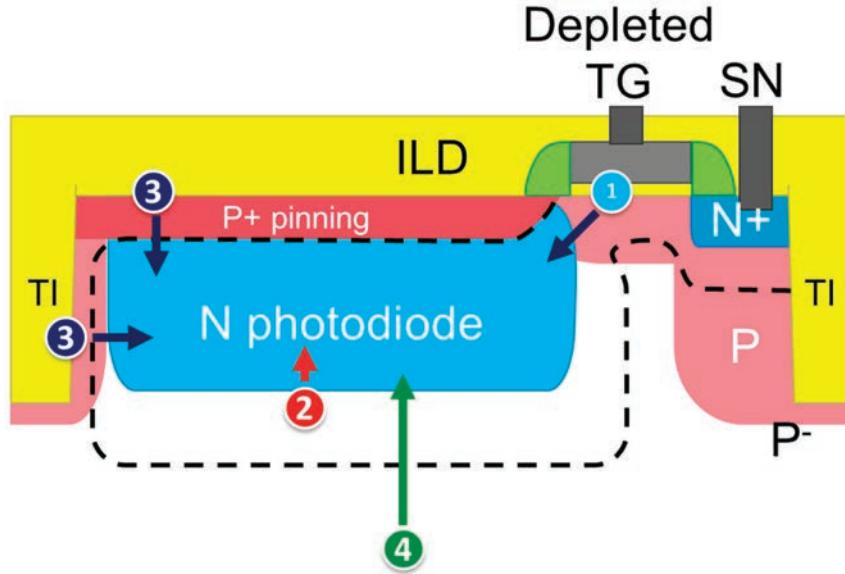


Figure 12 : Dark current sources illustration in a CIS Pinned Photodiode Pixel with a depleted transfer gate during integration (i.e. TG OFF voltage higher than the flat-band voltage). The boundary of the depletion region is represented as a dashed line.

with x_{SiO_2} the distance between the depletion region edge and the undepleted interface, $D_{n,p}$ the diffusion constant, A_{it} the area of the considered Si/oxide interface outside the depletion region and $N_{A,D}$ the P or N doping concentration at the interface. This expression can be simplified if $\frac{x_{SiO_2}\sigma v_{th}}{D_{n,p}}N_{it} \ll 1$, which is realistic except in heavily irradiated devices, where $\frac{x_{SiO_2}\sigma v_{th}}{D_{n,p}}N_{it} > 1$ leading to a saturation of this current contribution[67][68]:

$$I_{itdiff} \approx q\sigma v_{th} N_c N_v \exp\left(-\frac{E_g}{kT}\right) \frac{A_{it} N_{it}}{N_{A,D}} \quad (7)$$

This contribution decreases when the distance between the photodiode depletion region and the Si/oxide interface increases (as shown by equation (6) in [68]). Therefore, only the nearest Si/oxide interfaces generally bring a significant contribution (ILD or trench oxide interfaces right above or beside the PPD). This interface state diffusion dark current exhibits an **apparent activation energy slightly higher than the full bandgap, i.e. slightly above 1.12 eV**, here again because of the temperature dependence of the preexponential factor that shifts the measured energy above E_g in an Arrhenius plot.

- **Bulk diffusion dark current (source 4 in Figure 12):** the dark current coming from the generation of minority carriers in the quasi-neutral region that diffuse toward the depletion region can be visible if all the other sources are weak enough. As the previous source, this current is also called a “diffusion current” despite the fact it also comes from

a SRH generation process [57] and it is given by [16], [66] (for the electron contribution in a P region):

$$I_{\text{bkdiff}} \approx \frac{qD_n n_i^2}{L_n N_A} \quad (8)$$

The electron diffusion coefficient D_n can be replaced by $\mu_n \frac{kT}{q}$ with μ_n the electron mobility and the diffusion length L_n can be rewritten as:

$$L_n = \sqrt{D_n \tau_n} \quad (9)$$

If we consider that the main generation mechanism is the SRH process, that the p concentration is close to de P doping concentration N_A (because $E_{Fp} = E_F$ in the P region) and that the $p \times n$ product is still far lower than n_i^2 in the region of interest (because E_{Fn} is much lower than E_F here as shown in Figure 10), the generation lifetime τ_n [69] of electrons in the P region near the depletion region of a reversed biased PN junction can be rewritten as:

$$\tau_n = -\frac{n_i}{N_t U} = +\frac{1}{N_t} \frac{N_A}{\sigma v_{th} n_i} \quad (10)$$

Combining (8), (9), and (10) yields:

$$I_{\text{bkdiff}} \approx \frac{q \sqrt{D_n} n_i^2}{\sqrt{\tau_n} N_A} \quad (11)$$

$$I_{\text{bkdiff}} \approx \frac{q \sqrt{\sigma v_{th} D_n} n_i^{5/2}}{N_A^{3/2}} \sqrt{N_t} \quad (12)$$

Which leads to the following equation after developing n_i :

$$I_{\text{bkdiff}} \approx \frac{q \sqrt{\sigma v_{th} D_n} (N_c N_v)^{5/4}}{N_A^{3/2}} \times \exp\left(-\frac{5 E_g}{4 kT}\right) \times \sqrt{N_t} \quad (13)$$

This expression highlights that the bulk diffusion dark current increases as the square root of the defect density and that **its apparent activation energy is slightly above E_g** , as the interface diffusion dark current.

Each of these contributions can dominate the dark current observed at a sensor output. In unirradiated 3T conventional photodiodes, eq. (2) dominates and the apparent activation energy of the dark current will be close to $E_g/2$, as discussed above.

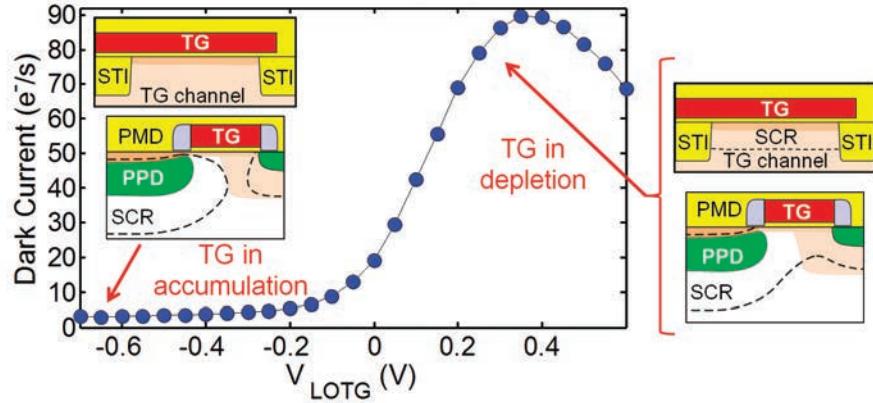


Figure 13 : Dark current evolution with TG OFF bias (i.e. V_{LOTG}) in a PPD CIS. When the TG channel is accumulated (for negative V_{LOTG}) the PPD depletion region does not reach any oxide interface and the dark current is minimum. If the TG channel is depleted, the PPD depletion region is in contact with the oxides in the PPD-TG transition region and the dark current is maximum. SCR= Space Charge Region.

In a state-of-the-art PPD, the depletion region is not supposed to reach any Si/oxide interface when the TG is placed into accumulation (with a negative V_{LOTG} bias, typically lower than -0.5V) as shown in Figure 13. In this case I_{itdiff} and/or I_{bkdiff} contributions (eq. (7) and (13)) dominate and the apparent activation energy is close to E_g . If V_{LOTG} is increased, the PPD depletion region reaches the Si/oxide interface near the TG sidewall spacer. The interface state generation current coming from this depleted interface (eq. (2)) becomes the dominant current contribution (and it is much higher than the diffusion dark current, as illustrated in Figure 13).

Other physical processes at the origin of dark current exist, and they can be visible in reverse biased PN-junctions under certain conditions or in particular devices or materials:

- Electric Field Enhancement (EFE) [70]–[76] mechanisms (illustrated in Figure 14) such as Poole-Frenkel and Trap Assisted Tunneling (TAT) can enhance the generation rate of SRH defects if the local electric field magnitude at the defect site is higher than 10^5 V/cm. EFE can be modelled by adding an enhancement factor in the previous generation current expressions (2),(4) and (5) as follows:

$$I_{EFE} = I_{gen} \times \Gamma \quad (14)$$

with Γ the enhancement factor that can be modelled by:

$$\Gamma = \exp\left(\sqrt{\frac{q^3}{\pi \varepsilon_s}} \frac{1}{\alpha k T} \sqrt{E}\right) \quad (15)$$

when Poole-Frenkel or Schottky barrier lowering occurs (at low field) or by:

$$\Gamma = 1 + 2\sqrt{3\pi} \frac{E}{E_r} \exp\left(\frac{E}{E_r}\right)^2 \quad (16)$$

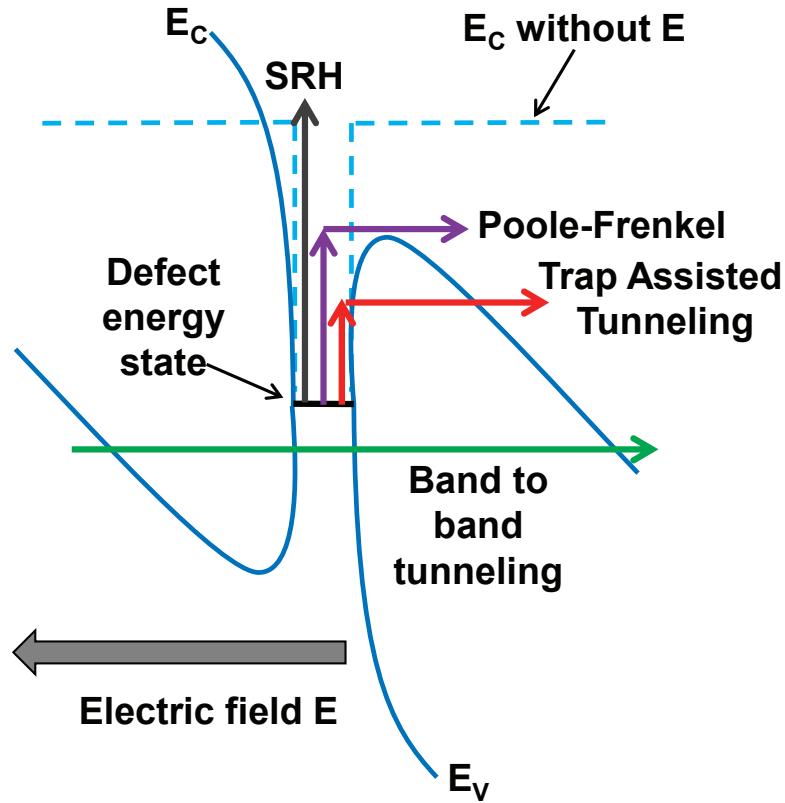


Figure 14 : Illustration of the main electron emission electric field enhancement mechanisms. The local electric field strength lowers the energy barrier that limits the generation rate.

for higher electric field strength, when TAT dominates. E is the electric field magnitude at the vicinity of the generation center and the other constants are defined in the [70]–[74].

Overall, for the discussion presented in this course, if one considers that most of the dependence on E is given by the exponential term, one can simply approximate the effect of electric field on the generation rate as:

$$I_{EFE} = I_{gen} \times K \times \exp(E^\gamma) \quad (17)$$

with $\gamma = \frac{1}{2}$ or 2 and K a constant that changes depending on the dominating mechanism. This last equation summarizes that the electric field enhances exponentially the generation rate of defect site in the depleted region. It should be emphasized that this enhancement factor lowers the apparent activation energy of generation dark current (because it reduces the effective energy barrier to overcome to generate an electron-hole pair as shown in Figure 14) and that the higher is the electric field strength, the lower is the activation energy [71]. In presence of EFE, a clear correlation between the highest dark current values and the lowest activation energy is

observed (see [75], [76] for instance), leading generally to measured activation energies well below the mid-gap value. Such mechanisms are very infrequent in state-of-the-art CIS photodiodes, where the manufacturing process and the operating conditions are optimized to mitigate these unwanted sources (by keeping low the electric field strength in the photodiode depletion region). EFE can however be significant in custom layouts (like radiation hardened designs), in other nodes than the photodiode (e.g. the sense node [77]), after irradiation or when high voltages are used, such as in single photon avalanche diodes (SPADs) and in Silicon Photomultipliers (SiPMs).

- At even higher electric field strength (near 7×10^5 V/cm estimated in [73]), or at low temperature when the other thermally activated contributions are frozen, band-to-band tunneling can become prominent and hide the generation center contribution.
- In avalanche diodes, the avalanche gain will also boost further the collected dark charge per unit time, leading to a measured dark count rate much higher than the starting SRH generation rate.
- Metallic contamination [63], [78] can be an important source in a defective manufacturing process, and the corresponding physical electron/hole generation process corresponds to the bulk generation contribution.
- Auger generation (also called impact ionization) [69] can also be an important source in reverse biased photodetectors, e.g. in HgCdTe photodetector [79], [80], but this contribution is hardly visible in CMOS sensors [81].

1.3.4.2 Dark Current Impact on Image Sensor Performances

To really appreciate the impact of dark current on image sensor performances, we must first introduce the Dynamic Range (DR) concept, which is one of the most important imager figures of merit. The DR can be seen as the working range of a camera and it can be defined as the ratio between the maximum and minimum measurable light intensities (in a single frame). The noise floor can be considered as the minimum detectable signal. The maximum measurable signal amplitude (i.e. the maximum useful signal swing) is given by the difference between the saturation charge (i.e. the Full Well Capacity or FWC) and the signal level in absence of illumination (i.e. the dark level). With these definitions (illustrated in Figure 15), the DR can be expressed as:

$$DR_{dB} = 20 \log \left(\frac{\text{FWC} - \text{dark level}}{\text{noise floor}} \right) \quad (18)$$

The dark level is given by the product of the dark current I_{dark} and the integration time t_{int} . The noise floor can be defined as:

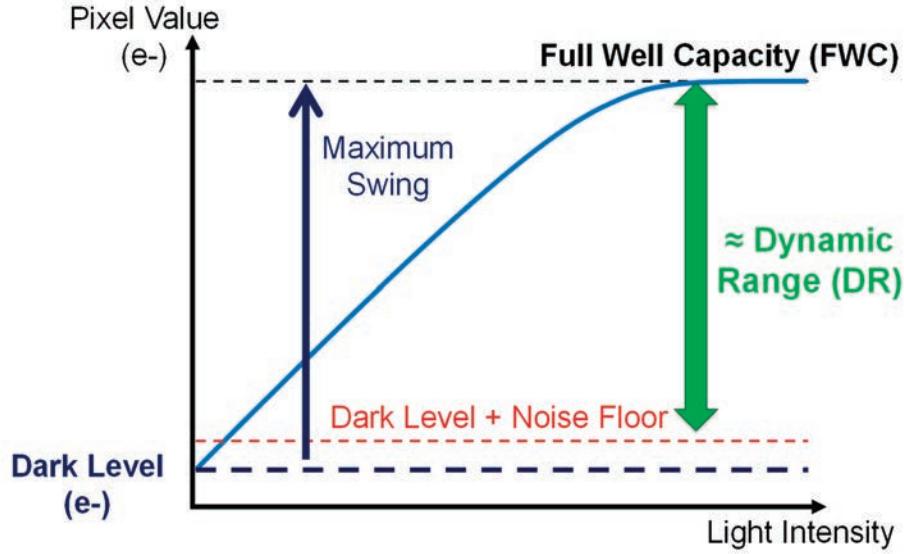


Figure 15 : Illustration of the Dynamic Range concept. The presented graph represents the pixel value as a function of light intensity. The main parameters used to define de dynamic range are illustrated in this figure.

$$\sigma_{\text{floor}} = \sqrt{\sigma_{\text{readout}}^2 + \sigma_{\text{dark}}^2} \quad (19)$$

with σ_{readout} the noise brought by the readout electronics and σ_{dark} the dark current shot noise. By definition, the standard deviation of a shot noise is equal to the square root of its mean:

$$\sigma_{\text{dark}} = \sqrt{\text{dark level}} = \sqrt{I_{\text{dark}} \times t_{\text{int}}} \quad (20)$$

In the end we get the following first order estimation of the DR of an image sensor:

$$DR = 20 \log \left(\frac{\text{FWC} - \text{dark level}}{\sqrt{\sigma_{\text{readout}}^2 + \sigma_{\text{dark}}^2}} \right) \quad (21)$$

$$DR = 20 \log \left(\frac{\text{FWC} - I_{\text{dark}} \times t_{\text{int}}}{\sqrt{\sigma_{\text{readout}}^2 + I_{\text{dark}} \times t_{\text{int}}}} \right) \quad (22)$$

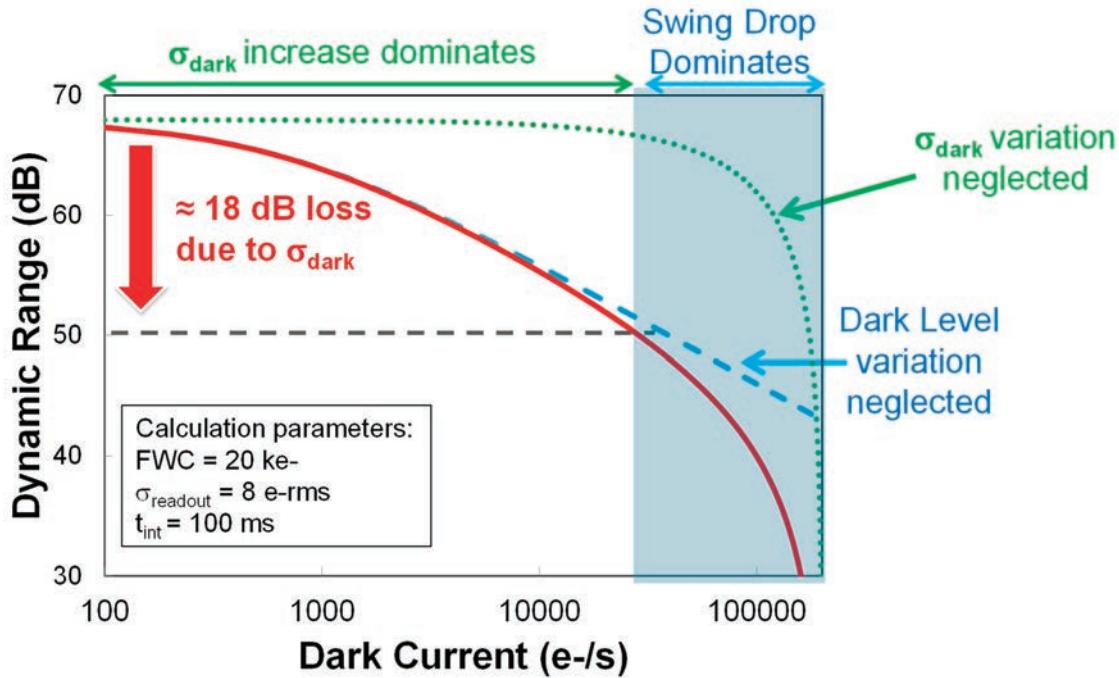


Figure 16 : Calculated evolution of the dynamic range as a function of the average dark current. The solid red curve represents the evolution of the full DR calculation from (22). The dashed blue plot is (22) with the variation of average dark level neglected in the numerator (i.e. with a fixed I_{dark} at the numerator). The dotted green plot represents (22) but with a constant dark current shot noise (i.e. fixed I_{dark} in the denominator). It can be seen that the main cause of DR loss is the dark current shot noise augmentation and not the average dark current level increase.

This equation is plotted in Figure 16 for three conditions:

- with the influence of both the loss of voltage swing due to the dark level increase and the increase of minimum detectable signal due to the dark current shot noise increase (full calculation case),
- with only the influence of the dark current increase induced voltage swing drop (case where the denominator is kept constant and thus the influence of the dark current shot noise is neglected) and
- with only the influence of the dark current shot noise (case where the numerator is kept constant).

This shows that the main impact of the dark current increase on the sensor performance is a large drop of dynamic range mainly caused by the increase of dark current shot noise. The rise of the average dark current level only plays a role when most of the DR degradation has already occurred, for very high dark current levels.

It can be concluded from this analysis that a high dark current severely degrades the sensor performance by reducing significantly the dynamic range. It also shows that subtracting an average dark current level to compensate the average dark current increase will not help keeping a high dynamic range and that the dark current generation mechanism must be turned off to cancel its associated shot noise and to recover the initial performance. This conclusion is

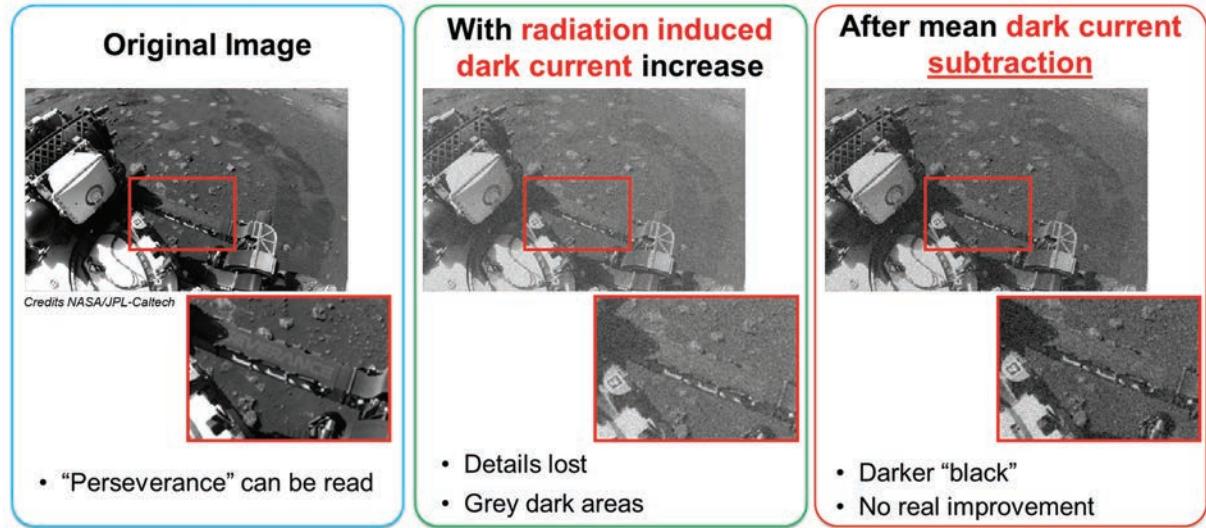


Figure 17 : Simulated effect of dark current shot noise on dynamic range.

illustrated by simulated radiation induced image degradations in Figure 17. We see in this figure that once the details are lost because of the dark current shot noise, removing a dark current offset (to compensate the average dark current level increase) does not allow recovering the lost information.

1.3.4.3 Random Telegraph Signal Noises: DC-RTS and SF-RTS

A Random Telegraph Signal (RTS) is a random process that switches alternatively between two or more discrete levels [82][83], as illustrated in Figure 18. This phenomenon has been observed in many electronic devices [83] and can have several different physical origins. Several names are used to describe it: RTS, Random Telegraph Noise (RTN), burst noise, popcorn noise, Variable Junction Leakage (VJL)[84] and some application specific names such as blinking pixels in CIS or Variable Retention Time (VRT) in DRAMs[85][86][87]. In CMOS images sensors, RTSs lead to bright pixels that seem to be turned on and off randomly (Figure 18). Such pixels are generally called blinking pixels. Because of the constant progress in the reduction of dark current and noises, this parasitic behavior is becoming the limiting factor for a growing number of high-end applications. Two kinds of RTS have been observed in CIS (as depicted in Figure 19).

DC-RTS was first reported[88][89][90] and analyzed[91]–[96] in irradiated CCDs and this phenomenon has been attributed to bulk meta-stable SRH generation centers, located in a depleted region (with $p \cdot n < n_i^2$, such as in a reverse biased PN junction), which are able to instantaneously switch between two generation rates. Figure 20 illustrates this concept. Since then, this bulk DC-RTS has been observed in CMOS APSs[97][98][99], in MAPSs[100], in CISs [101], in SPADs [102]–[105], in HgCdTe detectors [106], [107], in InGaAs detectors [107] and in InSb detectors [108]. DC-RTS generation centers can also be located at the depleted Si-oxide interface[109], [110], [107], [111]–[113] and in other CIS nodes than the photodiodes, such as the floating diffusion sense node [114]–[116].

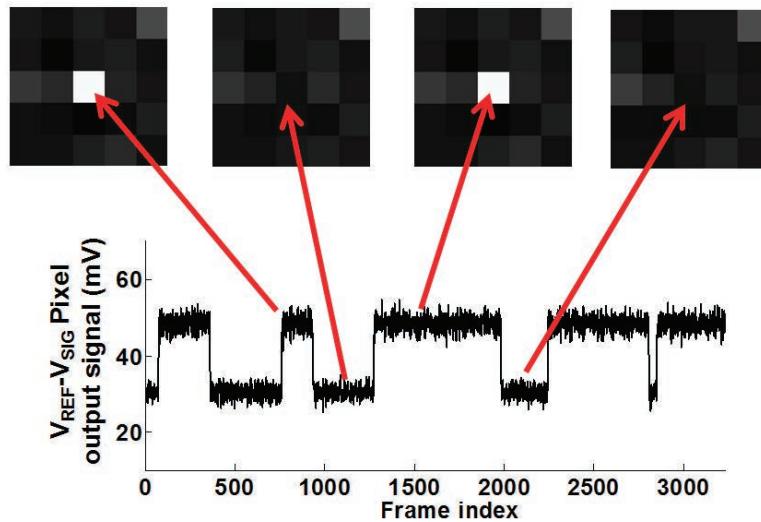


Figure 18 : Typical 2-level Dark Current RTS trace and its effect on dark frames.

Blinking pixels due to Random Telegraph Signals (RTS)

- In Transistors: channel conductance variation (**SF-RTS**)
- In Photodiodes: Dark Current variation (**DC-RTS**)

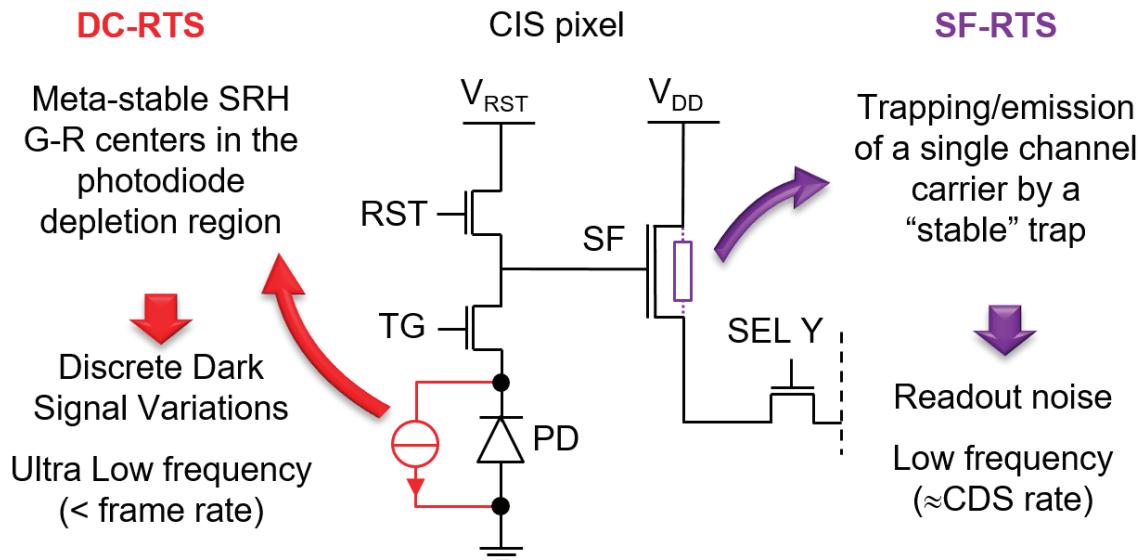


Figure 19 : Summary of the two main RTS phenomena in CIS: Dark Current RTS (DC-RTS) and Source Follower RTS (SF-RTS).

Meta-stable SRH Generation center

(Generation = emission of both electrons & holes)

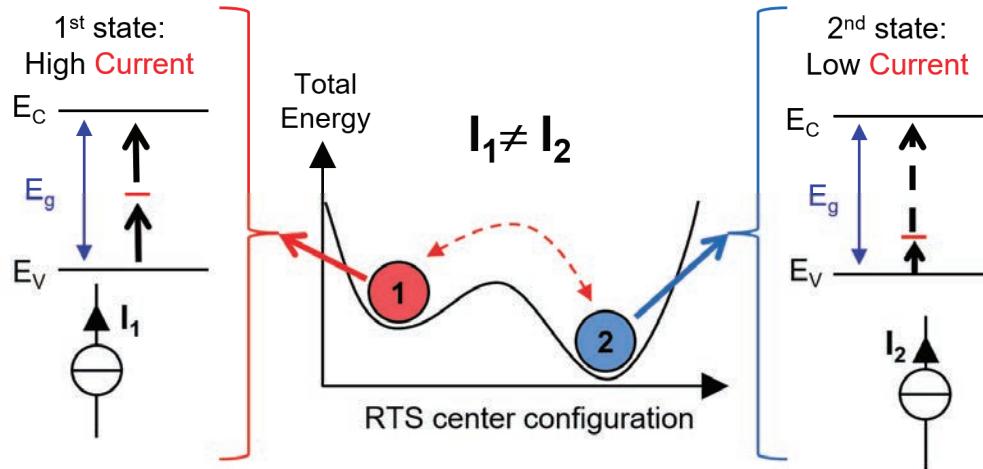


Figure 20 : Illustration of a meta-stable SRH generation center. The generation rate discrete fluctuation is illustrated here by a change of apparent trap energy level but a change of emission cross section (or a combination of both) could also justify this phenomenon.

This kind of RTS has the following characteristics:

- the amplitudes of the dark signal discrete fluctuations are proportional to the integration time (as shown in Figure 21) and they can be much higher than what would be expected from a single point defect
- the DC-RTS fluctuations are instantaneous (no transient regime between two states)
- a DC-RTS temporal trace can exhibit more than two discrete current levels and these multilevel RTS can be caused by the superimposition of several independent bi-level RTS centers or by a single multilevel RTS center with more than two different generation rates (see [117] for example)
- the RTS behavior can directly be observed at the sensor output on the dark signal evolution with time of a single RTS pixel
- the inter-transition times are exponentially distributed and the time constants of DC-RTS do not seem restricted to a particular range (time constants ranging from milliseconds to hours have been reported)
- the maximum transition amplitudes are also exponentially distributed [101][110]
- the time constants and the amplitudes are thermally activated (typically with an activation energy of about 0.58-0.6 eV for the amplitude in modern CIS)
- several theories (summarized in Figure 22 from [118]) have been proposed to explain this phenomenon in image sensors and in DRAMs, but the mechanism that best corresponds to the observed behavior seems to be the structural fluctuation of complex defects [118], [119]. Contrary to SF-RTS, it seems very unlikely that trapping and emission processes are involved in the metastability of DC-RTS, as discussed in [118]

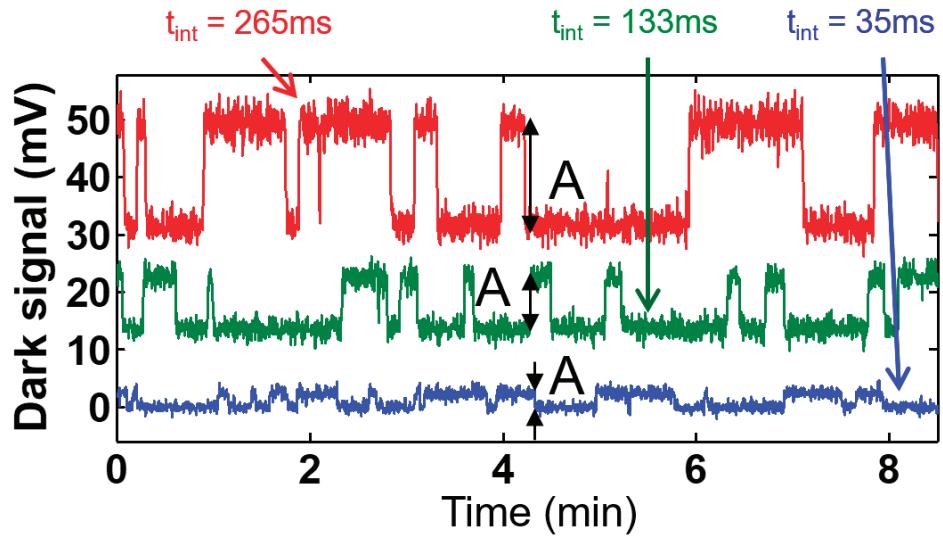


Figure 21 : RTS pixel output dark signal versus time (frames) of a single pixel for three different integration durations (t_{int}).

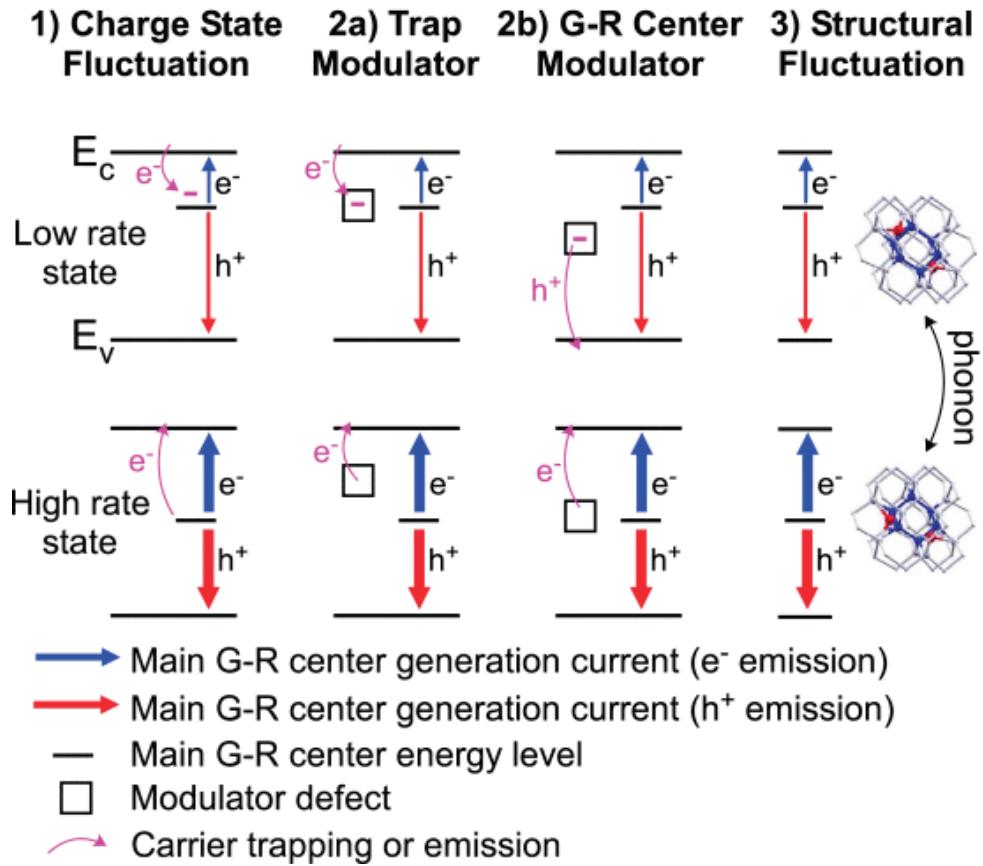


Figure 22 : Illustration of the possible explanations for the random switching behavior of DC-RTS in CIS and VRT in DRAM.

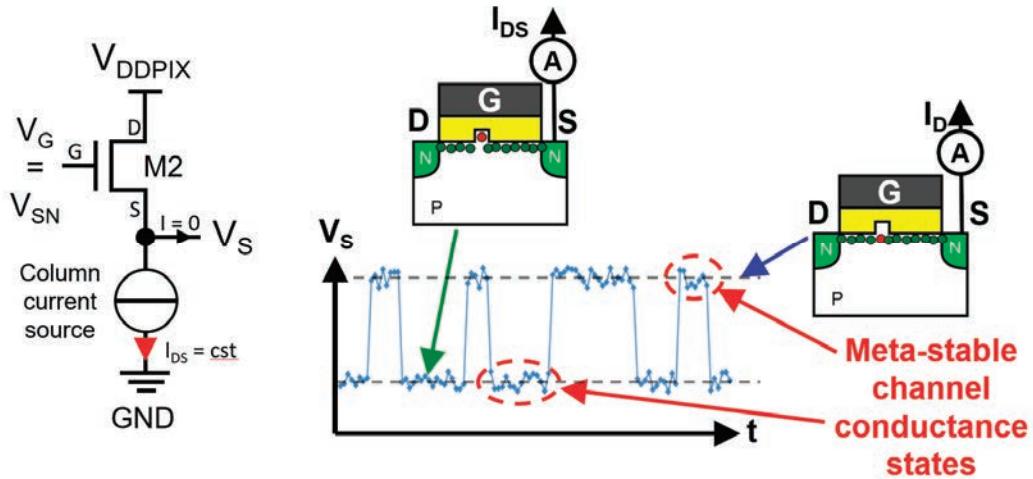


Figure 23 : Illustration of the SF RTS physical mechanism (assuming fixed V_G , V_D and I_{DS} as in a typical source follower operation, at the end of the sampling phase).

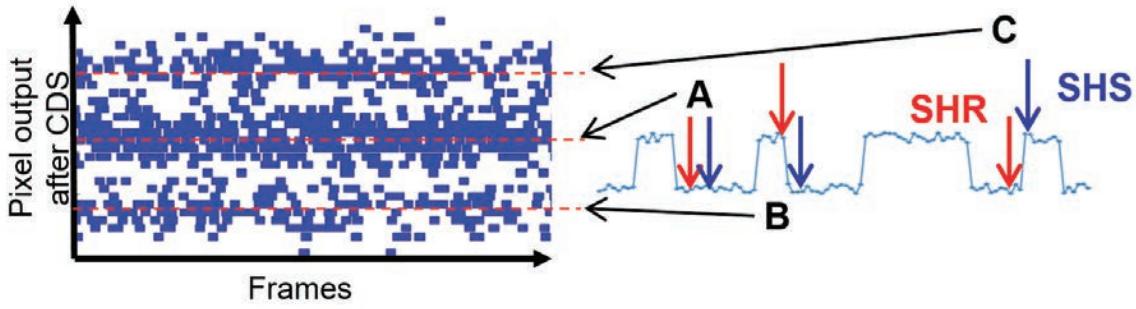


Figure 24 : Effect of SF-RTS on the sensor output signal: a discrete dark voltage variation is seen only if the source follower RTS state has changed between the two samples (SHS and SHR). Contrary to DC-RTS, SF-RTS meta-stable states are not visible at the sensor output and the SF-RTS amplitude is not proportional to integration time.

- the wide majority of DC-RTS pixels observed in unirradiated CIS appears to come from meta-stable generation centers located at Si-oxide interfaces (i.e. not from bulk DC-RTS centers)[109], [111]

SF-RTS in CIS is due to the well-known MOSFET gate oxide trapping RTS [120][121], also often called RTN. It is due to the random trapping and emission of inversion channel carriers ([83][122] and references therein). When an electron is trapped by a channel interface state (at the gate oxide or STI oxide interface[122]), the channel conductance is reduced, leading to a low source potential state (as shown in Figure 23). When the electron is released, the channel conductivity is increased back to its initial value and the MOSFET source voltage is then in a high potential state.

Both phenomena are different physical mechanisms: SF-RTS is a discrete change of channel resistance whereas DC-RTS is a discrete fluctuation of the dark current. They also have different

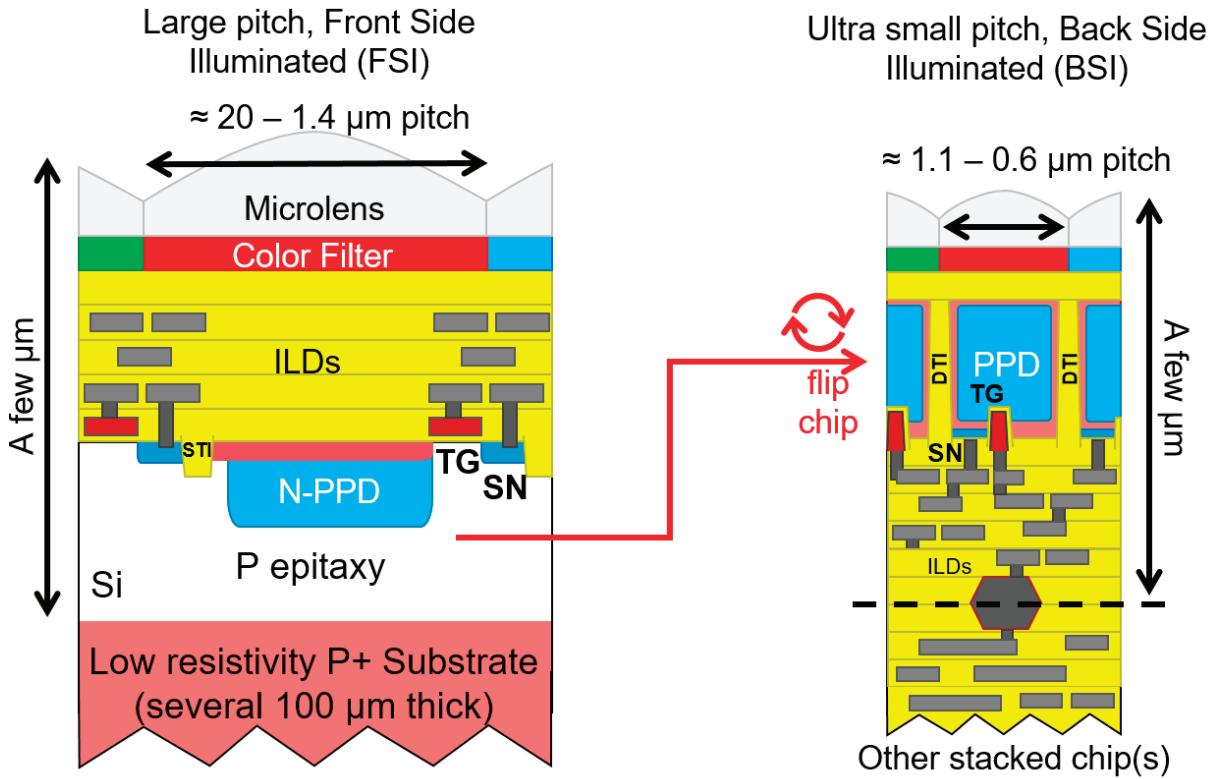


Figure 25 : Cross sectional views of the CIS technology and its evolution in the last decade. Left-hand side: illustration of the classical Front-Side-Illuminated (FSI) Pinned Photodiode CIS technology representative of ≈ 2010 consumer sensors and still used in 2021 for custom sensor developments. Right-hand side: illustration of 2021 ultra-small pixel pitch ($< 1 \mu\text{m}$), back side illuminated, 3D stacked sensors for consumer applications.

signatures at the CIS output and can thus be easily discriminated. For example, SF-RTS leads to an increase of the sensor temporal noise but the RTS behavior is hardly visible at the output and no stable RTS state can be seen in this case (Figure 24), contrary to DC-RTS (Figure 21).

1.3.5 Modern CIS Technology: An Overview

1.3.5.1 State-of-the-Art of Consumer Grade Image Sensors

Most of CIS ICs are produced with dedicated CIS processes optimized for visible light detection. The left sketch in Figure 25 presents a simplified cross sectional view of the typical CIS technologies used for consumer grade application before 2010 [123]–[126]. The base of a CIS process is similar to a standard Deep Sub-Micron (DSM) CMOS technology[127]: outside the pixel array, the MOSFETs are most often the same as the ones used in the mixed-mode version of the process (i.e. non CIS) with the use of classical Source/Drain implants, N and P wells, Shallow Trench Isolation (STI), polysilicon gates and the typical dielectric stack (constituted by the Inter-Layer Dielectrics (ILD)) on top of the semiconductor devices to ensure the isolation between the interconnect layers. Compared to mainstream CMOS ICs, CISs have however several unique features to improve the light collection:

- a reduced number of interconnection metal levels
- dedicated dielectrics such as Anti-Reflection (AR) Coatings
- filters for color imaging
- microlenses and light guides[128][129]
- ...

Several improvements are also made at the device level to optimize the photo-generated charge collection while reducing the dark signal and the noise:

- dedicated photodiode and in-pixel isolation doping profiles (P-wells, trench sidewall passivation...) with optimized electric field distribution
- dedicated pixel devices (optimized in-pixel MOSFETs with specific threshold voltages, dedicated MOSFET devices for in-pixel charge transfer...)
- a lightly doped epitaxial layer with a thickness optimized for the targeted wavelength range
- dedicated in-pixel trench isolations to minimize crosstalk [130], such as Deep Trench Isolation (DTI)
- ...

In addition to these special features, CISs can be Front-Side Illuminated (FSI) or Back-Side Illuminated (BSI). BSI technologies make it possible to collect more light (leading to higher External Quantum Efficiency (EQE)[53]) for a given fill factor. However, they require the thinning of the sensitive layer down to a few micrometers and the use of backside passivation techniques to reduce signal charge recombination and dark current generation at the back interface[126], [131]–[133]. It is also more difficult to shield the sense node from light in BSI sensors, which may be a constraint for global shutter applications.

This description is still valid for most of custom CMOS image sensor developments in 2021, including custom scientific sensors or custom imagers for space applications, but not for smartphone imagers that participate to the race for pixel pitch reduction. The sustained quest for smaller pixel pitches is explained by the steady increase in sensor resolution (for the lowest possible cost) requested by the market. The timeline of this race (updated May 10, 2021[134]) is presented hereafter :

- 1.1 μm in 2010 (Omnivision BSI-2, presented at MWC in Barcelona)
- 1.0 μm in 2015 (Samsung S5K3P3, samples started in 2014)
- 0.9 μm in 2017 (Samsung Slim 2X7)
- 0.8 μm in 2018 (Sony IMX586)
- 0.7 μm in 2019 (Samsung Slim GH1)
- 0.64 μm in 2021 (Samsung presentation at ISSCC [135])
- 0.61 μm in 2021 (Omnivision OV60A)

When the pixel size is reduced, the noise intensity stays the same or even increases while less light enters the sensitive volume and less photogenerated charges reach the collection region. Operating voltage is also often reduced, enhancing the relative importance of noise sources. To keep an acceptable Signal-to-Noise Ratio (SNR) in pixel pitches below 1 μm many cutting edges innovations have been developed and integrated in state-of-the-art CIS processes [22], such as [136]–[138]:

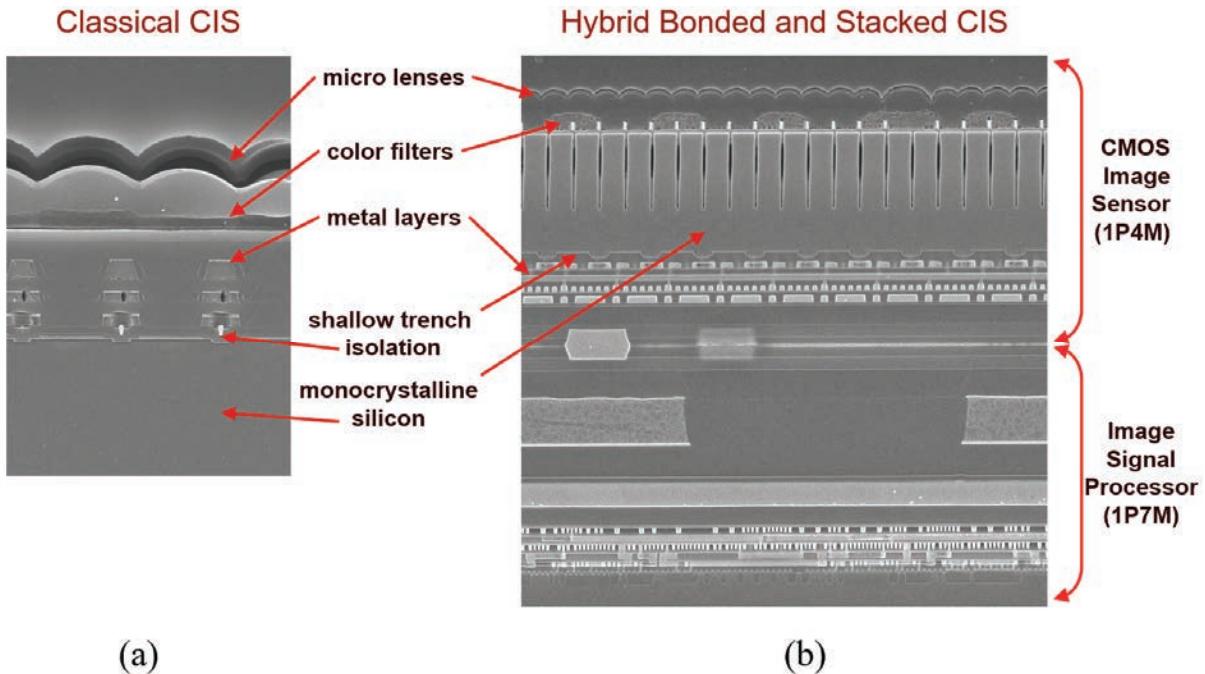


Figure 26 : Real cross sections of two different generations of CIS products. (a) A classical CIS technology used around 2010 for consumer grade products and still used today for custom sensors. (b) A modern hybrid bonded stacked CIS with B-DTI. Courtesy of Albert Theuwissen, Harvest Imaging. Electron microscopy cross sections are from Techinsights. Courtesy of Ray Fontaine.

- Vertical PPD [139]
- Vertical TG (poly-filled trench isolation) [140]
- Backside or Frontside Deep Trench Isolation (F-DTI or B-DTI) [136]
- Capacitive DTI (filled with poly) [27], [141]
- 3D-Stacked, hybrid bonded, onto one (or two!) other ICs (DRAM, Image Signal Processor...) [22], [138], [138]
- Through Silicon Vias (TSV) [123], [125]
- Light guide / Light pipes [123], [125]
- And more...

This evolution is illustrated by the representation in Figure 25 and a more accurate view is given by the real cross sections in Figure 26 (modified from [22], [142] with permission). Most of the recent advances are restricted to mass market applications and they are often difficult to access (or simply not relevant) for research, scientific and other niche applications where the market may not be large enough to justify the cost of state-of-the-art features. The wide majority of CMOS processes dedicated to image sensors that are accessible for low or medium volume custom sensor developments in 2021 are then based on classical CIS processes (left-hand side of Figure 25 and Figure 26) on which some of the listed features can sometimes be added if required. Besides the market point of view, custom sensor developments generally require pixel pitches larger than 1-2 μm (typically 4-10 μm) to maximize light collection. For such “large-

Table 2: Example of technology nodes used in stacked CMOS sensors. Courtesy of Ray Fontaine.

Chip Vendor	Year	Stacked CIS Foundry/Gen.	Stacked ISP Foundry/Gen.
Sony	2013	Sony 90 nm	Sony 65 nm
Sony	2014	Sony 90 nm	TSMC 40 nm
Sony	2016	Sony 90 nm	TSMC 28 nm
OmniVision	2015	XMC 65 nm	XMC 65 nm
OmniVision	2016	TSMC 65 nm	TSMC 65 nm
Samsung	2015	Samsung 65 nm	Samsung 65 nm
Samsung	2016	Samsung 65 nm	Samsung 28 nm HKMG
<i>Sony</i>	<i>ISSCC 2017</i>	<i>90 nm CIS*</i>	<i>30 nm DRAM*</i>
			<i>40 nm ISP*</i>

pitch” sensors, most of the latest innovations are not relevant, not feasible at this scale or simply too expensive compared to the gain they bring in this context.

For all these reasons, this short course mainly focuses on CIS processes that are the most relevant for discussing radiation hardening: the “classical” CIS processes.

1.3.5.2 Technology Nodes and In-Pixel MOSFET Feature Size

The evolution of consumer grade CIS technologies used in smartphones is compared to the International Roadmap for Devices and Systems (IRDS)[143] in Figure 27 (from [22]). The IRDS plot here represents the smallest CMOS technology node available in the industry, which is generally used for DRAM manufacturing. The node used in mass market CMOS sensors appears to follow the IRDS curve but with a 10 year delay [22]. This apparent delay is due to the fact that CIS and DRAM do not have the same requirements and that the smallest possible MOSFET optimized for logic circuits is not the most important technology brick to enable the manufacturing of high performance, ultra-small pitch pixel. For this reason, bigger transistors are generally more suited to sense and readout a photosignal when associated to the latest innovations mentioned in the last section. CIS processes should not simply be seen as “older CMOS processes” compared to DRAM, but more as CMOS processes optimized for another goal than storing digital information on a minimum area. As highlighted in [22], it is also interesting to notice that the minimum pixel pitch appears linked to the CIS technology node by a factor of 20.

Technology node has a complex meaning for CMOS sensors. First, the CMOS process used to manufacture the detection layer often mix features coming from different technology nodes, making it difficult to summarize the process by a single feature size. For instance, the manufacturing processes used for Back-End-Of-Line (BEOL) structures (like metal interconnects) generally correspond to more advanced CMOS nodes than the CMOS technology used for the pixel transistors.

Pixel Size Evolution

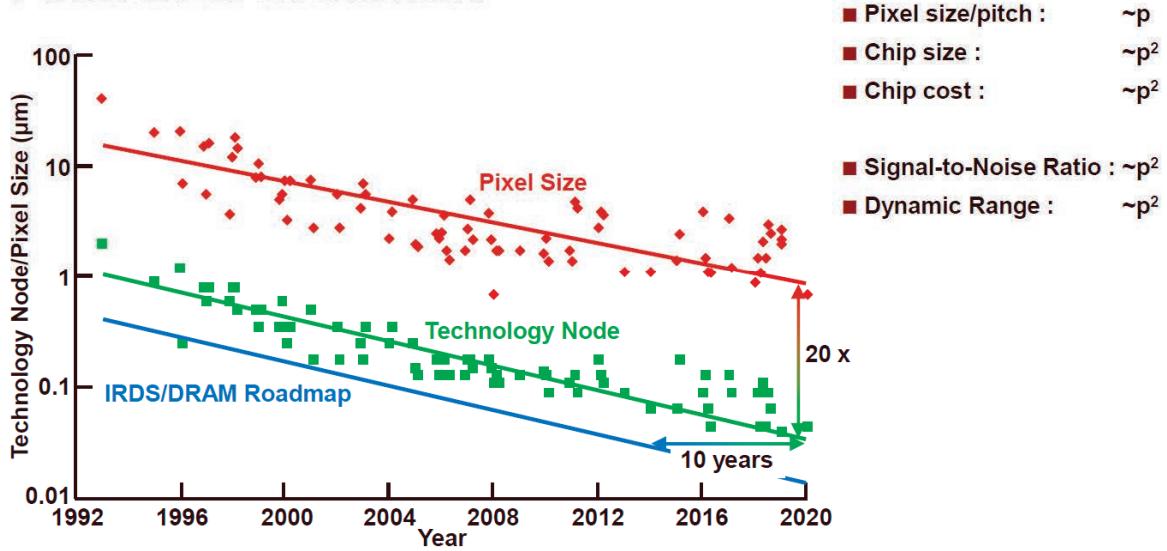


Figure 27 : Evolution of consumer grade CIS pixel size and technology node compared to the IRDS/DRAM roadmap. Courtesy of Albert Theuwissen from Harvest Imaging. The data used for this chart come from IEDM, ISSCC and IISW conferences.

Second, with the advent of stacked sensors, several technology nodes can be used in a single CIS chip as illustrated in Table 2 from [137]. In some cases, the pixel itself can be distributed over two different chips, blurring further the meaning of technology node, even when only the pixel is considered.

For the sake of clarity, the CIS technology node is defined here as the CMOS process generation considered to draw the in-pixel transistors (i.e. that gives the pixel transistor design rules) and not the process generation representative of BEOL manufacturing.

“High” operating voltages (i.e. 2 - 3.3V) are required for high imaging performance, especially to ensure a high dynamic range, to enable lossless charge transfer from the photodiode to the sense node as well as to allow the extraction of the photosignal with a minimum number of transistors. To stand these voltage levels, the core transistors offered by the CMOS process are generally not integrated inside the pixel and optimized double gate oxide (GO2) MOSFETs are used instead. Figure 28 presents the typical GO2 MOSFET used in most of CIS with pixel pitch larger than 1 - 2 μm . The ILD stack description given here is based on [144]. From one CIS process generation to another, in-pixel GO2 MOSFETs do not evolve much and this sketch can be considered as representative of CIS technology “nodes” between 180 nm and 90 nm (and possibly 65 nm as well). The typical feature size of in-pixel GO2 MOSFET is generally a few hundreds of nanometers (length and width of 0.3-0.7 μm are typical for 180 nm CIS) to stand the operating voltage, to reduce noises such as SF-RTS and to ensure optimum charge transfer by allowing channel doping optimization. Furthermore, since in BSI sensors the light is coming from the back of the chip, in-pixel MOSFETs are not shielding the pixel from light anymore, which relaxes the pressure on the size of in-pixel MOSFETs. For this reason, the planar GO2

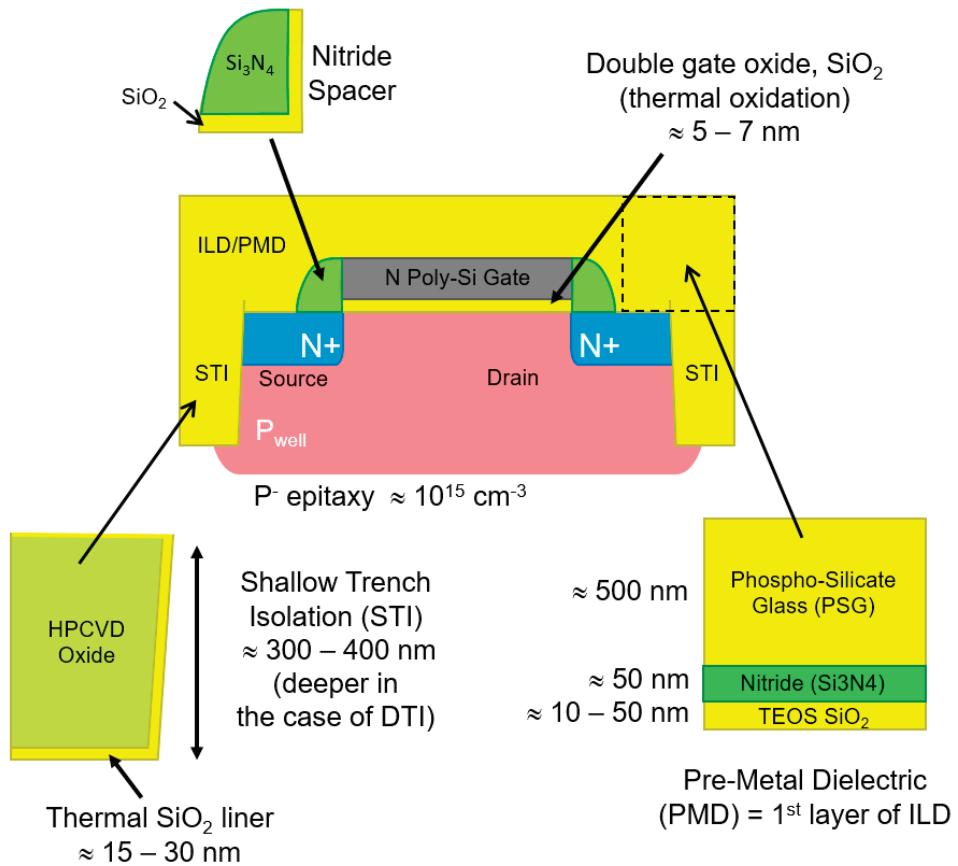


Figure 28 : Illustration of typical in-pixel MOSFETs used in 180 nm – 90 nm CIS technologies with the main surrounding dielectrics.

MOSFET description shown in Figure 28 remains relevant for a wide range of sensor developments that do not require ultra-scaled in-pixel MOSFETs.

In 2021, the majority of Pinned Photodiode CIS processes open to laboratories and small volume applications are still 180 nm CIS processes. If the market is large enough or if the application strictly requires a more advanced node, 130, 110 and 90 nm (and maybe 65 nm) can sometimes be used for custom sensors, but as discussed above, the in-pixel devices (GO2 MOSFETs) do not change much.

The description of the MOSFET technology used in ultra-small pixel pitch CIS is more complex since exotic devices can be used (such as vertical TG) and those particular processes have only a limited interest to discuss RHBD in 2021, given the limited access to such technology for custom sensor development.

Therefore, for the rest of this document, the reader can consider that the GO2 MOSFETs manufactured with typical 180 nm – 90 nm CMOS processes (illustrated in Figure 28) are the basis of the discussion developed in these notes.

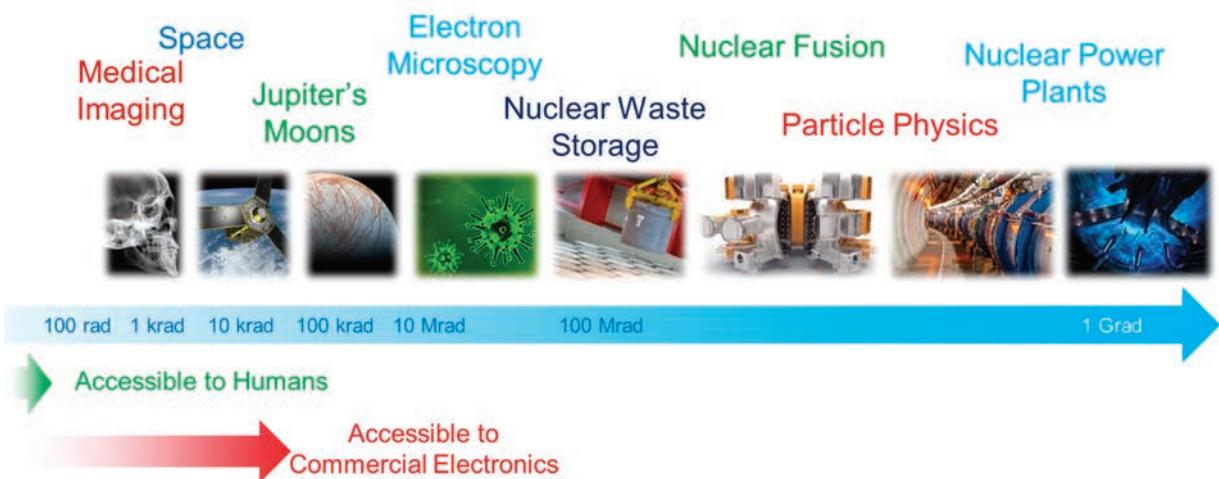


Figure 29 : Illustration of the main applications that require the use of image sensors in harsh radiation environments.

1.4 Use of Image Sensors in Radiation Environments

Cameras and optical instruments based on solid-state image sensors are used in a wide variety of applications to replace or complement human vision. Several of them require to expose imagers to harsh radiation environments, as shown in Figure 29.

In the Total Ionizing Dose (TID) range from 1 to 100 krad we find most of space (e.g. optical instruments for Earth or Space observation) and medical (X-ray imaging, and especially dynamic X-ray imaging [145]) applications. Whereas 100 krad can be considered as an upper limit rarely reached for instruments on-board satellites orbiting Earth, radiation doses well above 1 Mrad are mentioned for the exploration of Jupiter's moons. TID as high as 100 Mrad and above can be reached in the following applications:

- Transmission Electron Microscopy [146]
- Inspection and monitoring of nuclear facilities including power plants, nuclear waste storage and nuclear fusion reactors [31]
- Dismantling operations of nuclear power plants [147], remote handling in nuclear environment and mobile rescue robots
- Particle physics facility monitoring and instrumentation (e.g. CERN LHC high luminosity upgrade which will expose electronics to TID as high as 1 Grad [148])

Commercial unhardened cameras can only cover a small part of this TID range with failure reported well below 100 krad [149], [150]. Therefore, it appears clearly that the intrinsic tolerance of image sensors to particle radiation has to be improved to see where humans cannot. The rest of this manuscript will cover the various techniques that can be used to increase the radiation hardness of CMOS image sensors by modifying their design or manufacturing process.

2 Total Ionizing Dose Effects and Hardening Techniques

For the discussion developed in this section, the reader has to keep in mind that the absorption of ionizing radiation by MOS devices and integrated circuits generally leads to the buildup of positive trapped charge in oxides and to the creation of interface traps at the Si/SiO₂ interface. More detailed background information about TID effects on MOS devices and ICs can be found in [1]–[6]. The details of the Radiation-Hardening-by-Design (RHBD) techniques used to mitigate these effects in CMOS circuits are discussed in [11]–[15].

To provide some orders of magnitude, the ionizing radiation dose unit used in this manuscript is the rad (expressed in SiO₂) knowing that the SI unit is the Gray with 1 Gy = 1 J/kg = 100 rad.

2.1 Conventional Photodiode RHBD Techniques

2.1.1 Overview of TID Effects on Conventional Photodiodes

Figure 30 depicts a cross section of a conventional photodiode pixel where the most active radiation induced defects are represented. As mentioned previously, TID leads to the trapping of a net positive charge in the CMOS dielectric layers and to the creation of interface traps. Those defects are created all along the Si/SiO₂ interface but only a few of them play a role in the radiation induced degradation. For the case of the conventional photodiode, the most problematic defects are located along the perimeter of the PN junction, at the vicinity of the depleted interface as illustrated by + and x signs in Figure 30.

Figure 31 presents a magnification of the area of interest (highlighted by the red rectangle in Figure 30) for three different dose ranges. Before irradiation and at low TID, the main dark current contribution is a generation dark current coming from the interface traps on the perimeter of the diode [151]–[155]. As shown by (2), dark current increases linearly with the interface trap density N_{it} augmentation induced by the radiation dose. At higher TID levels, typically above 100 krad in modern CIS processes [155], the TID induced positive trapped charge starts to have an influence on the photodiode performance by extending the depletion region area at the Si/SiO₂ interface A_{itdep} in (2). This leads to a faster increase of dark current with the absorbed dose. At even higher absorbed dose (typically above 1 Mrad) the positive trapped charge in the oxide leads to the creation of an inversion channel under the isolation oxides that surround the photodiodes, leading to intense leakage current and short-circuits between adjacent photodiodes. As discussed in section 1.3.4.2, the increase of dark current degrades the dynamic range of the sensor and has to be mitigated to enable the use of image sensors in radiation environments. The following sections present the main techniques used to improve the radiation hardness of conventional photodiodes.

More detailed presentation of TID effects in conventional photodiode CIS can be found in [156] and references therein.

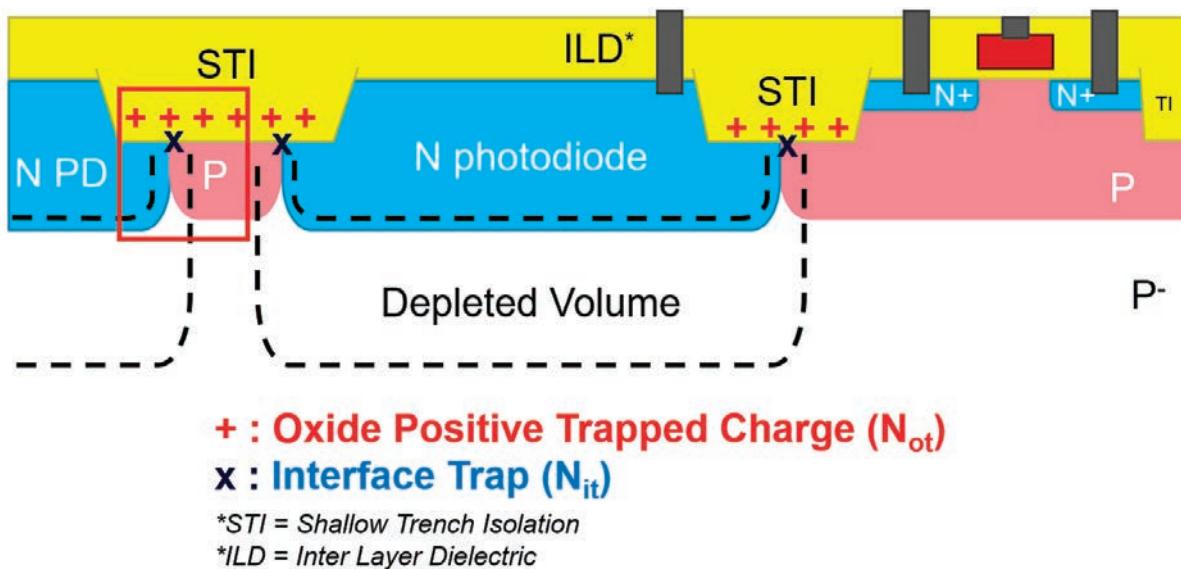


Figure 30 : Cross section of a conventional photodiode CIS pixel showing the location of the most disturbing radiation induced defects. The red rectangle indicates the region of interest for the next figure.

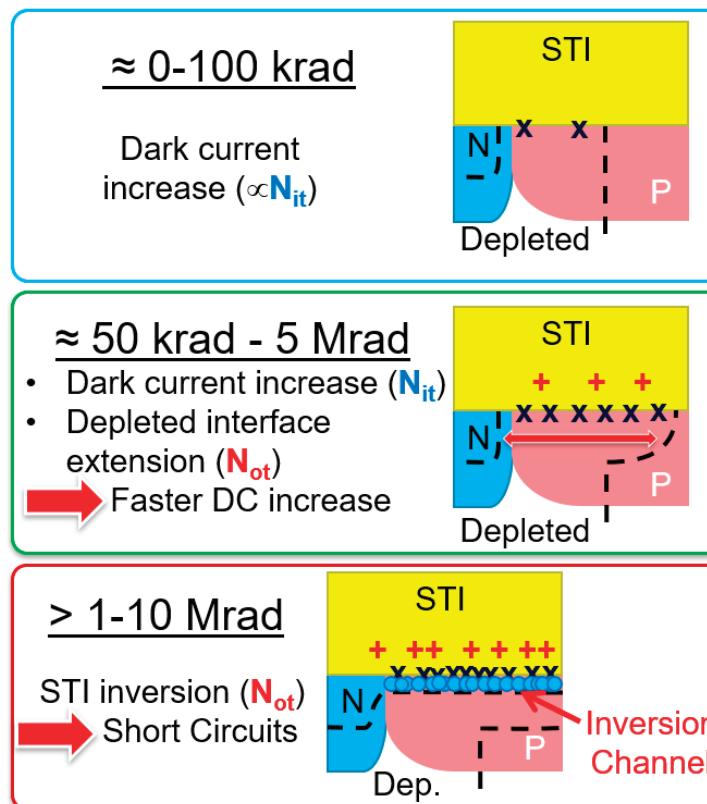


Figure 31 : Illustration of radiation induced degradations on the edge of the conventional photodiode in for three different dose ranges. The region of interest is the one highlighted by a red rectangle in the previous figure.

2.1.2 Dark Current Subtraction/Compensation

A first technique that can be considered to improve the radiation hardness of a sensor is the subtraction of the radiation induced dark current (or the dark signal). The parasitic dark electrons cannot be discriminated from the useful photoelectrons in real time in a pixel of a given frame. The only correction that can be done is the subtraction of an estimated or averaged constant dark current (or dark signal) value. This is classically done as one of the very first step of the image processing operation.

The most basic approach consists in shifting the zero value in an image to ensure that the darkest area of the image have a digital value close to the zero code. This operation can be done when the image is displayed, without requiring any calibration measurement. As discussed in section 1.3.4.2, removing a dark current offset does not mitigate most of the radiation induced dynamic range degradation. Moreover, using a single offset to compensate the dark signal level of a whole frame does not attenuate the dark signal non-uniformity (DSNU) associated to the increase of dark current.

In high-end applications, including scientific imaging and space instrumentation, a per pixel dark signal offset subtraction is performed by image processing. This calibration operation requires the acquisition of an average dark frame taken in comparable conditions (e.g., same temperature) as the useful image but in absence of illumination. From this average dark frame, the mean dark signal can be estimated per pixel and the zero value of each and every pixel can be accurately corrected. This technique allows to cancel the DSNU for pixels that are not saturated by dark current. However, it does not reduce the dark current shot noise and does not solve the dynamic range problem. It is also ineffective against DC-RTS.

Those techniques can be implemented on the sensor chip. An average dark signal level can be estimated by using masked pixels at the periphery of the pixel array (e.g. as in [157]) and this dark reference can then either be subtracted on-chip or off-chip. This optical black feature is classically used in commercial sensors, especially to remove the average dark level variation with the temperature. One interesting benefit of performing the subtraction on-chip is that, if the subtraction is performed before the signal saturates the readout chain, it can avoid the drop of available voltage swing in dark current saturated pixels by cancelling the “dark level” term in (21). This subtraction can even be performed in current, directly inside the pixel (as in current skimming architectures [158]). However, not only this technique is ineffective at mitigating the dynamic range degradation but it adds a shot noise contribution that increases the total noise as discussed in [31].

Overall dark current calibration or subtraction techniques can be a good complement to RHBD but they do not mitigate the main radiation induced sensor performance degradation: the dynamic range reduction. Moreover, these techniques cannot be used if the sensor is not functional anymore (e.g. if the photodiodes are shorted because of the radiation induced trapped charge).

The only way to prevent the degradation of imaging performance in harsh radiation environments is to extinguish the physical source of radiation induced dark current by modifying the design or the manufacturing process of CMOS photodiodes, as discussed in the following sections.

2.1.3 Perimeter reduction

The most straightforward way of reducing the TID induced dark current is to reduce A_{itdep} in (2) by reducing the photodiode perimeter. This solution is not considered further here, since this variable is often determined as a trade-off between other parameters like CVF and quantum efficiency, when tailoring the sensor for a given application. Worse, in the particular case of the classical 3T photodiode, decreasing the perimeter implies decreasing the overall size of the photodiode and so, its capacitance, thus reducing the FWC (and increasing the gain, so the relative importance of dark current when converted in voltage). In the end, the achieved dark current reduction may not be beneficial if compared to the reduced saturation charge. When designing a conventional CIS photodiode, it is important to keep in mind that the perimeter has a direct impact on the magnitude of the radiation induced dark current but radiation hardening possibilities are very limited in the case of the standard diode.

2.1.4 Operating/Reset Voltage Reduction

Lowering the photodiode reverse bias voltage is efficient at reducing radiation induced dark current. Indeed, it reduces the depletion region extension (at the interface and in the bulk) and so it decreases the number of radiation induced defects that can contribute to the generation of dark charges. The electric field is also weakened when using lower voltages, hence reducing dark current sources amplified by EFE. Besides, using lower voltages makes it possible to replace the classical double gate oxide generally used in CMOS sensor pixels by single layer gate oxide (GO1) transistors (as in [159]). It can improve further the radiation hardness since thinner gate oxides trap less radiation induced charge and exhibit less interface trap buildup than GO2 transistors.

It can be concluded that lowering the operating voltage of the photodiode is always beneficial to limit radiation induced dark current. However, this voltage reduction degrades other CIS performance parameters as the FWC and the dynamic range and it may simply not be possible to operate the pixel properly if the operating voltage is too low. Switching from GO2 to GO1 for in-pixel gate oxides can also have unwanted side effects, such as the modification of the source/drain and P-well (and so MOSFET channel) doping profiles, that can also degrade the analog performance.

Therefore, a trade-off has to be found between the hardness improvement brought by lowering the operating voltage and the sensor performance degradations that come with it.

2.1.5 Operating Temperature

As discussed in section 3.2.4 for displacement damage, lowering the operating temperature reduces significantly the radiation induced dark current but it does not mitigate the TID induced failures occurring at high dose levels like charge transfer degradation or trapped charge induced short circuits. A periodical increase of the temperature to accelerate the annealing process can clear TID induced defects [160] but care should be taken when choosing the elevated temperature to avoid degrading the long term reliability of the sensor (and the camera).

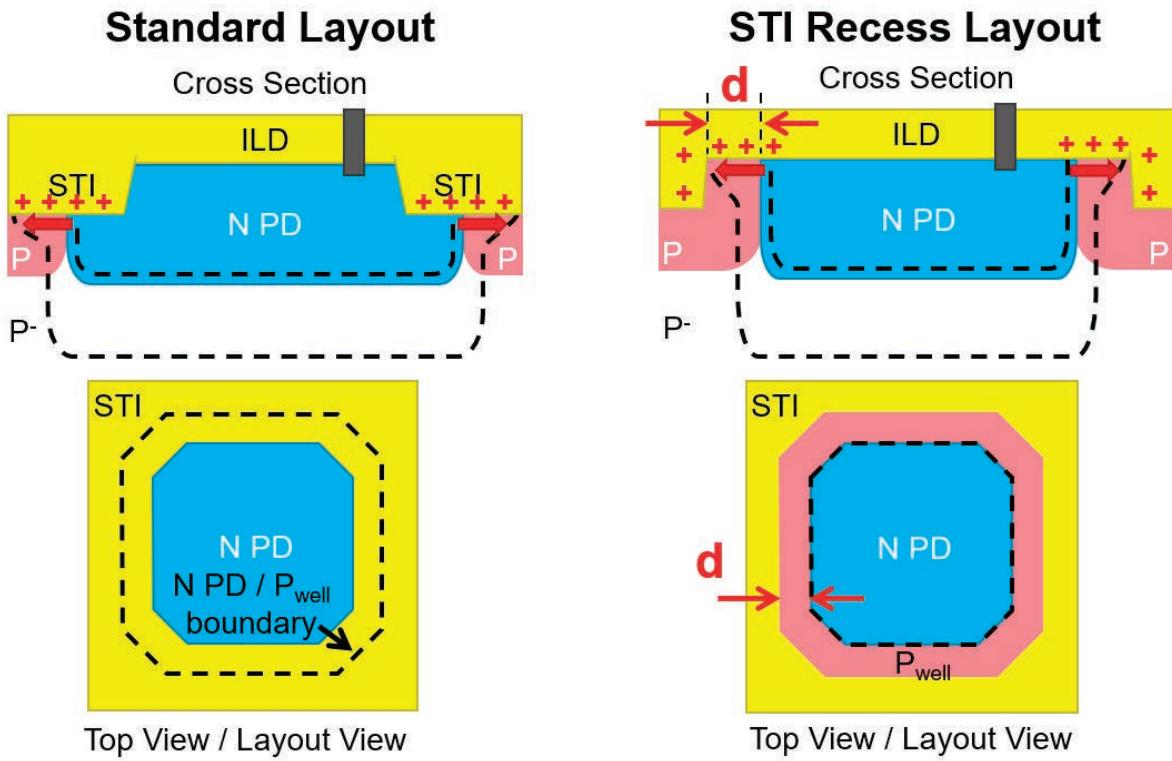


Figure 32 : Cross section and layout top view of the STI recess layout (right) compared to the standard conventional photodiode layout (left).

2.1.6 STI Recess

The first layout modification that can be considered is presented in Figure 32. It consists in moving the dielectric responsible from the degradation away from the photodiode perimeter. In this radiation hardened layout called here STI recess, the active region is larger than the N region of the photodiode. The distance d between the as-drawn N photodiode layer and the STI edge is simple to optimize since it just has to be large enough to ensure that the STI does not touch the depletion region anymore. The cross-sections in Figure 32 shows that it does not really solve the issue, since another dielectric (the first ILD layer) takes the place of the STI and exactly the same radiation induced defects are expected. Nevertheless, some improvements have been observed in the literature [152], [155], [161], mainly a delay of the appearance of degradation. It can be explained by a higher P-well doping concentration at the surface and a different dynamic of radiation induced defect creation in this isolation oxide with a different dielectric stack than the STI (as illustrated in Figure 28). At high TID, full depletion of the ILD interface occurs as in the standard diode leading to a very high dark current (and to short circuits between diodes when the inversion dose is reached). It is often observed that recessing the isolation oxides increases the dark current level before irradiation (a factor of 2 increase is typical), most likely due to the non-optimized ILD interface (TEOS oxide versus the thermal SiO₂ liner of the STI) and also to the higher doping concentration at the surface already mentioned above.

P+ Guardring Layout

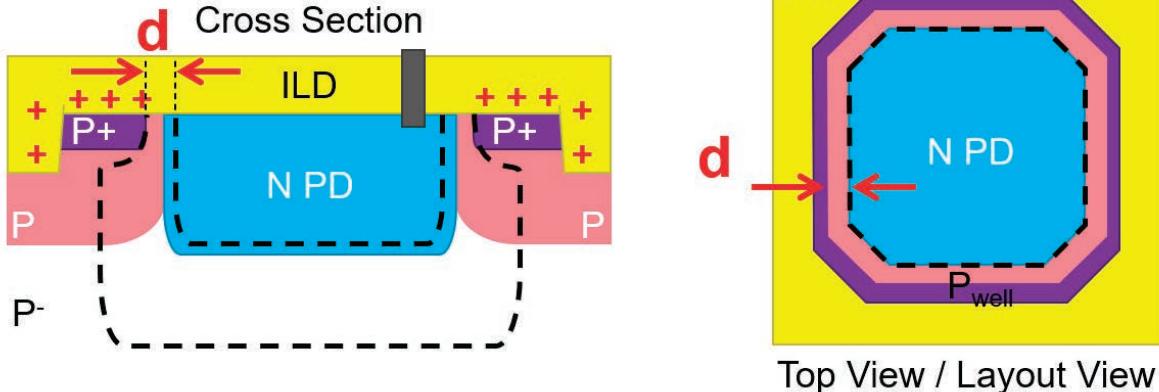


Figure 33 : Cross section and layout top view of the P+ guarding photodiode design.

All in all, this layout is a simple technique that can bring some radiation hardness improvement (not guaranteed) in a 3T pixel at low TID but that does not really enable the use of CIS in extreme radiation environments. For this low TID range, an unhardened 4T-PPD might be a better choice if available.

2.1.7 P+ surround layout

The previous layout can be improved by adding a P+ implant to control the depletion width extension at the interface, as shown in [154], [161], [162]. Figure 33 presents this design and highlight the main parameter to optimize: the distance d between the as-drawn P+ and N photodiode layers. Contrary to the previous case, optimizing d can be complicated and may require trial and error. If d is too small, the doping concentration of the formed P+/N+ junction will probably be much too high leading to intense electric field enhancement (see section 1.3.4.1) that will boost the radiation induced degradation. If d is too long, the surface depletion width will be unnecessarily wide, summing the contribution of a large number of interface states and leading as well to a high dark current before and after irradiation. Technology Computer-Aided Design (TCAD) can help finding the optimum distance, but such simulation is extremely difficult to calibrate properly to determine this distance accurately.

The main advantage of this solution is the fact that it gives a good control over the surface depletion area (A_{itdep} in (2)) and reduces significantly the influence of the positive trapped charge on the radiation induced dark current increase. It also prevents the surrounding field oxide depletion that appears at high TID. Depending on the P+ doping concentration, this depletion could still appear at ultra-high TID ($> 10\text{-}50 \text{ Mrad}$), which makes it a potentially risky choice for the most demanding applications.

It is worth noting that a P+ ring improves the radiation hardness of a conventional CIS photodiode only if it is placed next to the N photodiode region without any field oxide between both [162]. Classical P+ guardrings [12] (separated by a field oxide) are generally not required in CIS pixel if the photodiode itself is properly hardened [161], [163].

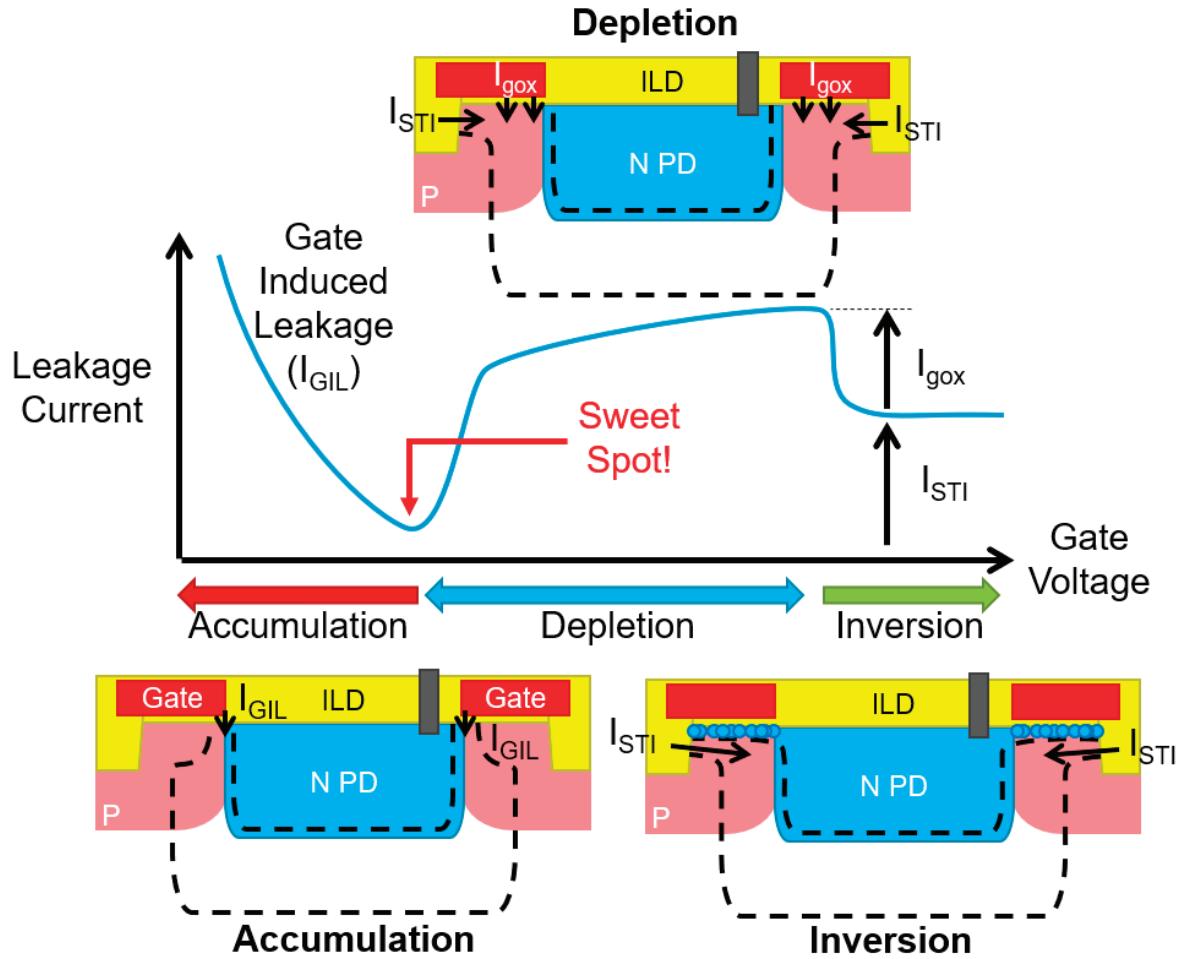


Figure 34 : Cross sections of a generic gated photodiode design for different gate bias voltages.

2.1.8 Gated Photodiode Designs

A more efficient surface potential control can be achieved by surrounding the photodiode N implant by a polysilicon gate, as proposed in [151]–[154], [161], [162], [164], [165]. Figure 34 shows that the resulting structure corresponds to the classical gated diode case [166]. Depending on the voltage applied on the gate, its channel can be placed into accumulation, depletion or inversion. In the depletion regime, the interface leakage current is the sum of the depleted gate oxide interface traps contribution and the depleted field oxide interface traps contribution, leading to a high dark current before irradiation and a fast increase with TID. In the inversion regime (for high gate voltages), the gate oxide contribution is cancelled but not the STI one. When the gate channel is placed under accumulation, both the gate oxide and the STI contribution are cancelled since the depletion region under the gate collapses. However, putting the gate into accumulation creates electric hot spots that leads to very high leakage current level. This phenomenon, well-known in MOSFET drains, is called Gate Induced Drain Leakage (GIDL)[167]. The curve presented in Figure 34 shows that an optimum gate bias can be found at

Self Aligned Gated PD

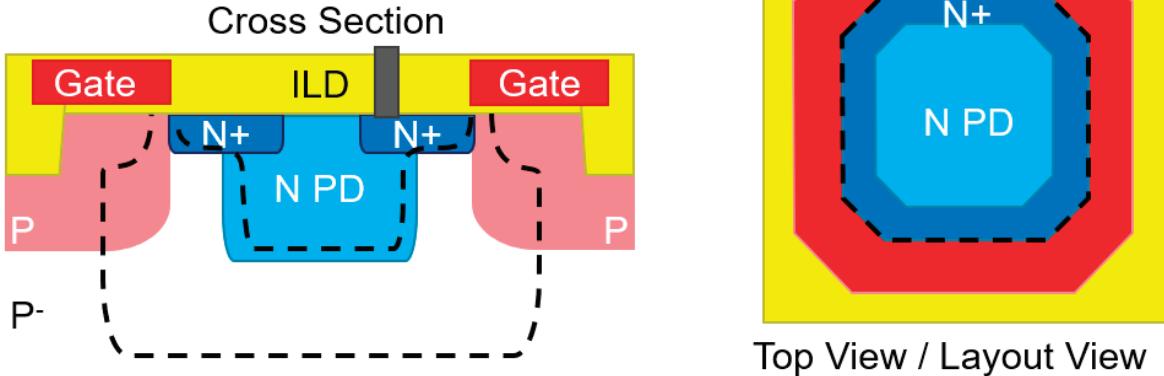


Figure 35 : Cross section and layout view of the self-aligned gated photodiode design.

the threshold of the accumulation regime, before the electric field becomes too high but after having reduced significantly the contributions from the depleted gate oxide and STI.

A key benefit of the gated photodiode design is the very good control over the depleted region width. Contrary to the P+ surround design, this control can be adjusted as a function of the absorbed radiation dose to compensate any possible drift of the optimum bias. Furthermore, since this surrounding gate is based on a very thin oxide (typically < 7 nm, see Figure 28 for example) compared to the trench isolation oxides and the ILD, the radiation induced positive trapped charge has very little effect even at TID levels above 50 Mrad.

Several implementations are possible for this gated photodiode design. The simplest to optimize is the self-aligned gated version [30] (also called ELD [161]) depicted in Figure 35. To align the surrounding gate on the photodiode N region, the main N-well photodiode implant is surrounded by a shallow N+ source/drain implant which is implanted after the polysilicon gate deposition in CMOS processes. Doing so allows to benefit both from the doping profile of the photodiode implant optimized for photodetection and the self-alignment features of N+ implants. This layout is a very efficient and simple way to ensure a radiation hardness of 100 Mrad and beyond. Its main drawback is the electric field strength in the region where the gate overlaps the N+ region when the accumulation regime is reached [30], [154], [161], limiting the minimum dark current value that can be obtained before and after irradiation. It is worth noticing that, from the radiation induced leakage current point of view, the self-aligned gated photodiode design is similar to the case of the enclosed terminal of an Enclosed Layout Transistor (ELT). Therefore, if a leakage sensitive node of a CMOS IC is protected from radiation induced degradation by an enclosed gate layout, its radiation hardness can be enhanced by adjusting the transistor OFF voltage value, as in a self-aligned gated photodiode.

It is possible to lower the minimum dark current at optimum gate bias by removing the N+ implant and by managing manually the alignment between the N region and the gate. This new degree of freedom for the designer enables the fine tuning of the surface depletion width and the associated electric field strength without the need to modify the manufacturing process. The gate can either be drawn away from the as-drawn N region [161] or on top of the photodiode [30] (i.e.

The Gate Overlap Design

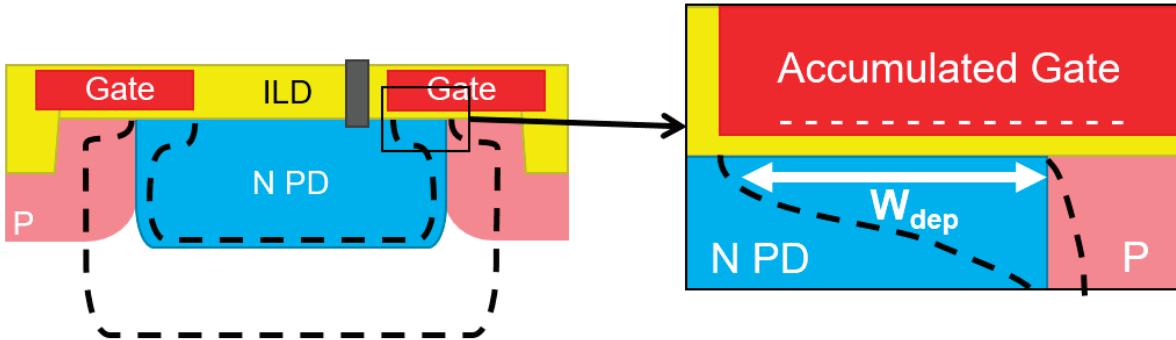


Figure 36 : Cross section of the gate overlap design.

with an overlap). Both approaches are efficient at reducing EFE and at lowering the minimum achievable dark current but contrary to the self-aligned version, the optimum distance has to be determined by trial and error.

The case of the gate-overlap design is presented in Figure 36. In most conventional diode CIS processes, drawing a gate on top of the photodiode region leads to the creation of an N doping region below the gate either because the photodiode is implanted before the gate deposition or because the deep CIS implant passes through the gate (leading to a shallower N implant below the gate [31]).

When the accumulation regime is approached in this structure, the depletion width W_{dep} at the interface is directly given by the overlap distance between the gate and the N photodiode region. Increasing the overlap distance extends W_{dep} and so the total depleted interface (A_{itdep} in (2)) and the resulting radiation induced dark current. On the other hand, reducing too much the overlap distance increases the electric field strength at this bias voltage, enhancing the dark current. It should be emphasized that finding the optimal overlap distance allows reducing the radiation induced dark current by eliminating EFE at the optimum gate voltage but that using more negative gate voltages will create a field induced junction by inverting the N region, leading to a sharp increase in dark current. Hence, both the right distance and the right voltage have to be experimentally determined in this design. Doing so allows to reduce significantly the pixel dark current (between a factor 2 and 6 depending on the TID) as shown in Figure 37 (data from [30]).

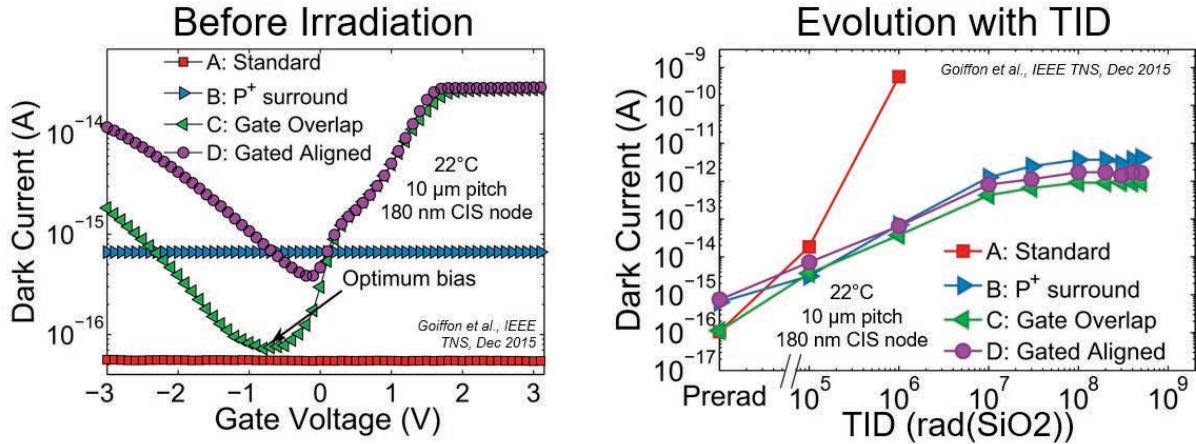


Figure 37 : Dark current comparison between the standard, the P+ surround, the gate overlap and the self-aligned gated photodiode designs before irradiation (left) and as a function of TID (right).

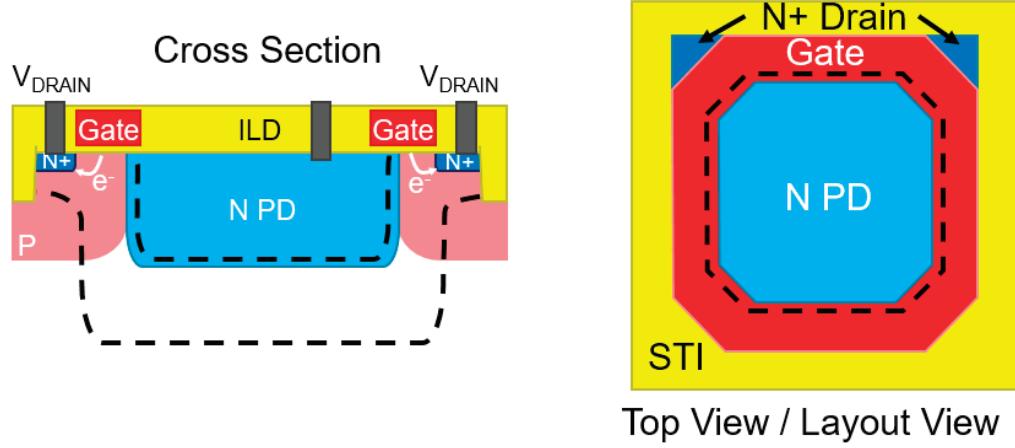


Figure 38 : Cross section and layout view of the gate overlap design.

An additional refinement of the gate overlap design can be made by adding an N+ dark charge drain biased at V_{DD} at the exterior of the circular gate [31], [168]. If the transistor made by the addition of this drain is kept in a deep subthreshold regime (i.e. if the gate to photodiode voltage never approaches the strong inversion threshold) a part of the dark charge generated in the depletion region is collected by the drain instead of the photodiode. This is different from the dark current subtraction techniques discussed in sec. 2.1.2, since the drained dark carriers are never collected by the photodiode. Hence, the dark current integrated by the photodiode is really extinguished and so is the associated shot noise [31], contrary to a dark current subtraction technique (e.g. current skimming discussed in sec. 2.1.2) that increases the shot noise. It is worth emphasizing that, if this dark charge drain is well integrated inside a P-well, it will not influence significantly the quantum efficiency of the photodiode (same influence as the other in-pixel MOSFET sources and drains).

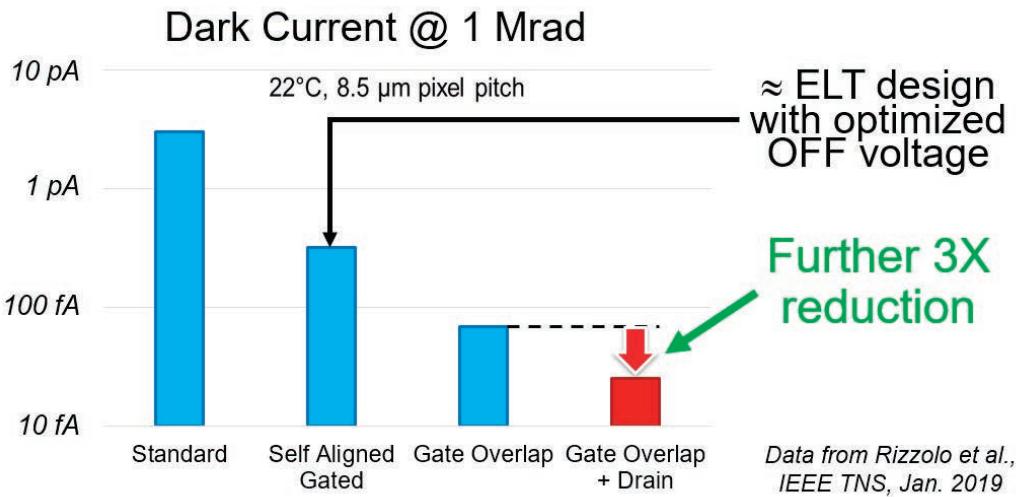


Figure 39 : Dark current comparison illustrating the benefit of adding a drain to the gate overlap design.

Small drains (as represented in Figure 38) are preferable since they are as effective at draining the gate oxide dark charges as large drains whereas the latter may lower the saturation voltage of the photodiode. Figure 39 (data from [168]) presents the benefit resulting from the addition of a dark charge drain compared to the other gated photodiode designs.

2.1.9 Process Modifications

If the manufacturing process can be slightly modified, additional possibilities appear to improve the radiation hardness of 3T-conventional photodiodes. A first option is to fully cover the N photodiode region by a custom surface P implant so isolate the photodiode from the top oxide interface as depicted in Figure 40 (top left photodiode). This photodiode will still suffer from the radiation induced dark current increase as the standard diode because the surface P+ implant must be opened somewhere to contact the N photodiode region. It leads to a depleted Si/SiO₂ interface around the N+ contact but this depleted area is much smaller than in the unhardened photodiode case. In other words, A_{itdep} in (2) is significantly reduced in this design without having to reduce the photodiode size. It is generally not possible to design efficiently such photodiode by using classical P+ source/drain implant because of the resulting high electric field at the surface P+/N+ junction. That is the reason why an additional custom surface P+ implant is required. If the P+ surface layer is sufficiently doped and if the underneath N region is shallow enough, the resulting photodiode can be almost fully depleted after reset. Such CMOS photodiode structure illustrated in Figure 40 is called a partially pinned photodiode [169]–[171]. Otherwise, the N region stays undepleted and this radiation hardened design is then referred to as a surface protected photodiode [172]. The partially pinned photodiode can be offered as a standard option on some CIS processes, but it is considered as a “process modification” in these notes, since it is rarely accessible. The radiation hardness of both photodiodes strongly depends on the P doping concentration and few data can be found in the literature. Bogaerts *et al.* demonstrated a remarkably high radiation hardness with a surface protected photodiode in [172] whereas the tolerance to ionizing radiation of the partially pinned photodiode tested in [168] was only slightly higher than the unhardened standard photodiode. In any case, as for the P+

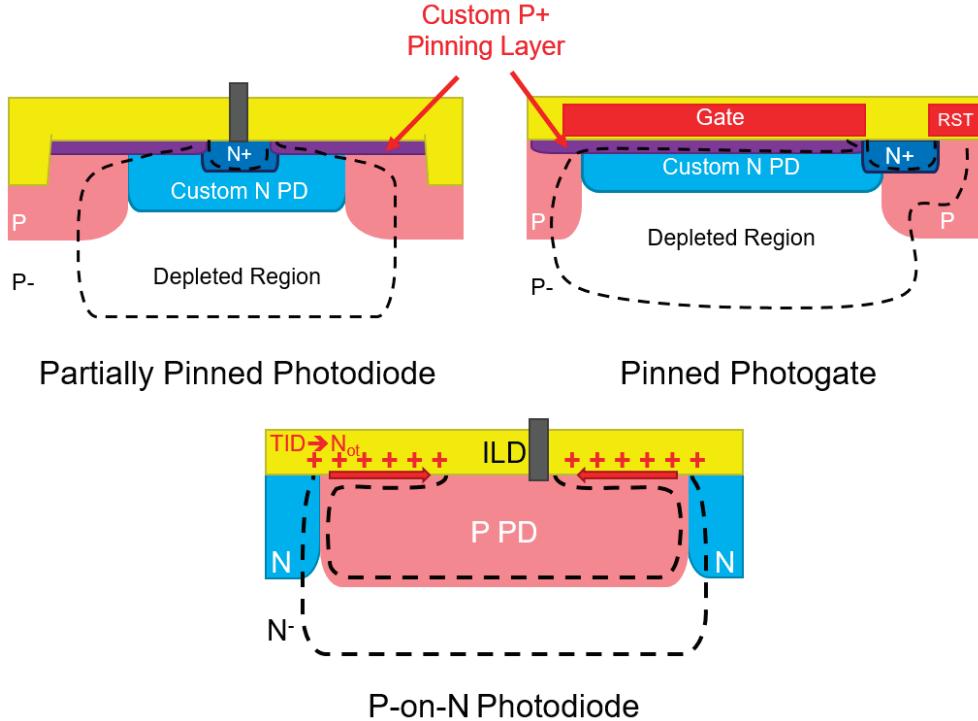


Figure 40 : Example of radiation hardened CIS photodiode that require a manufacturing process modification.

surround layout, since the radiation hardness is provided by a P+ doping, the radiation hardness at ultra-high TID is less ensured than with a surrounding gate.

The pinned photogate [173] displayed in Figure 40 (top right cross section) is basically the same concept as the partially pinned photodiode, except that a gate fully covers the surface custom P implant. This extra protection ensures that the surface P implant remains accumulated even at ultra-high TID. Several process modifications are required to obtain this structure, including the extra optimized P implant. The radiation hardness reported in [173] demonstrates that it is a promising structure (for back-side illuminated sensor since most of the photodiode area is covered by the polysilicon gate). Nonetheless the benefits of these process modifications compared to a RHBD gated photodiode manufactured using a non-modified CIS process is difficult to assess, since no direct comparison has been reported yet and very few data are available on the pinned photogate.

Another possibility is to invert the doping type by making a P-well on N epitaxy photodiode as shown at the bottom of Figure 40. Such structure could be designed in a classical CMOS process using a standard P-well but it will still require a N epitaxy (which might not be standard). Moreover, to ensure a high collection efficiency and a low dark current, an optimized P photodiode implant has to be developed. No real radiation hardness improvement is expected compared to the various N on P photodiodes discussed before since the surface PN junction will suffer from the same TID induced dark current degradation mechanisms. Still, this solution prevents the appearance of short circuits between photodiodes at high TID (as most of the

Table 3: Comparison of the main radiation hardened conventional photodiodes.

Photodiode Design	Standard CIS Process	Prerad	10 krad – 1 Mrad	1 Mrad – 10 Mrad	10 Mrad – 100 Mrad	100 Mrad – 1 Grad	Comments
Standard	✓	😊😊	😢	💀	💀	💀	
P+ Surround	✓	😊⚠ EFE	😊⚠ EFE	😊⚠ EFE	⚠😊 EFE/Depletion?	⚠😊 Depletion?	Difficult to optimize
Self Aligned Gated	✓	😊⚠ EFE	😊⚠ EFE	😊⚠ EFE	😊⚠ EFE	😊⚠ EFE	Easy Design DC > other Gated PD
Gate Overlap	✓	😊	😊	😊	😊😊	😊😊	Difficult to optimize
Pinned Photogate	✗	😊	😊	😊	😊😊	😊😊 TBC?	Difficult to optimize More data/comparison needed

RHBD photodiode presented in the previous sections), since the N region that separates the photodiodes cannot be inverted by the positive trapped charge.

2.1.10 Comparison Table

To summarize this part, Table 3 compares the most relevant radiation hardened conventional photodiodes discussed previously.

The unhardened conventional photodiode is quickly degraded in the 10 krad – 1 Mrad range (as shown in Figure 37) and becomes unusable beyond.

The P+ surround is an efficient technique to extend the lifetime of a 3T CMOS pixel in an ionizing radiation environment but it can suffer from an intense electric field induced leakage current if its drawing is not well optimized. Besides, the effectiveness of the P+ doping may be strongly reduced at ultra-high TID (beyond 10 Mrad), if the positive trapped charge is sufficient to deplete this layer.

The self-aligned gated photodiode design ensures the maximum radiation hardness and its design is straightforward with no key distance to optimize. It is the recommended design for guaranteed performance with limited time and resources to optimize the pixel design. The main reason why other designs are explored is the rather elevated dark current level exhibited by this photodiode before and after irradiation because of strong electric field related issues.

The gate-overlap design makes it possible to tackle the electric field issue of the self-aligned gated version. The lowest dark current levels reported in the literature for a RHBD photodiode are generally achieved with this layout. Its main drawback compared to the self-aligned gated diode lies in the various degrees of freedom that have to be optimized when drawing such pixel.

Finally, the pinned photogate design appears on paper as a promising radiation hardened photodiode structure but at the cost of significant manufacturing process modifications and doping profile optimization. Furthermore, the lack of comparative data in the literature about this recently proposed photodiode makes it difficult to assess if the efforts required to tune the process are worth spending.

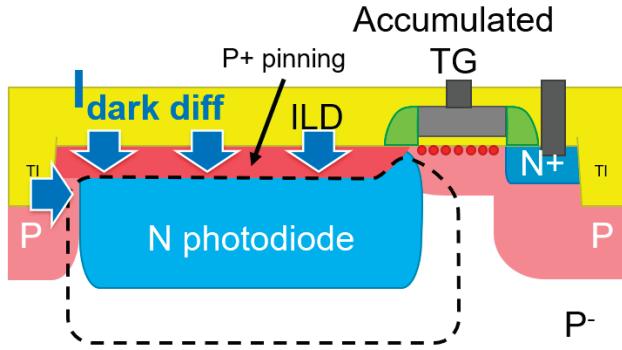


Figure 41 : Cross section of a CIS pinned photodiode and its transfer gate placed under accumulation highlighting the main dark current contribution at low TID.

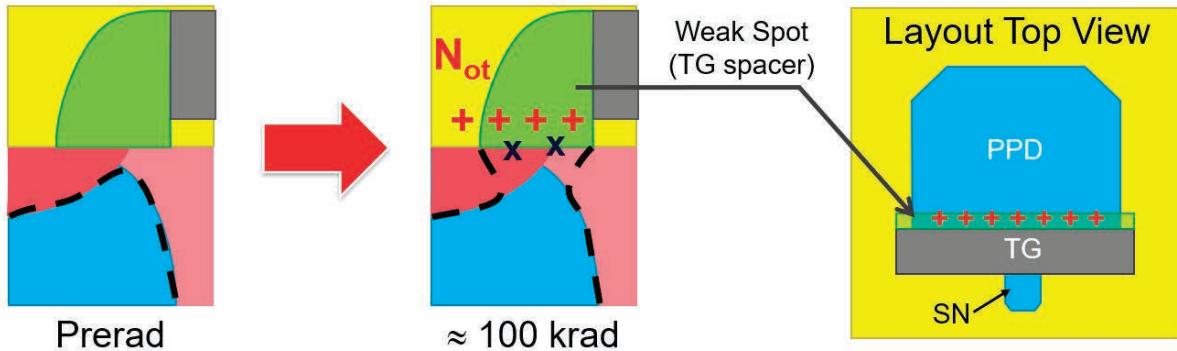


Figure 42 : Magnification of the photodiode-TG overlap region highlighting the TID induced degradation expected near 100 krad and beyond in a PPD pixel.

2.2 TID Effects on Pinned Photodiodes and RHBD

2.2.1 Overview of TID Effects on Pinned Photodiodes

Figure 41 presents the cross section of a CIS pinned photodiode in the particular case where the transfer gate is accumulated during the integration phase. A zero or negative voltage is generally used in a CMOS sensor to ensure that this regime is reached and that the surface generation dark current coming from the gate (source 1 in Figure 12) is eliminated. In these conditions, and in the absence of particularly active defects in the depleted volume of the diode (i.e. midgap defects), the dark current of as-fabricated PPD CIS is generally dominated by oxide interface diffusion dark current contributions (source 3 in Figure 12).

When exposed to ionizing radiation, as far as the TID induced positive trapped charge influence stays negligible (typically up to 50-100 krad), the main degradation is a strengthening of the diffusion dark current due to the interface trap buildup at the generating interfaces [67][68] (top ILD/PMD and possibly the STI/DTI as well).

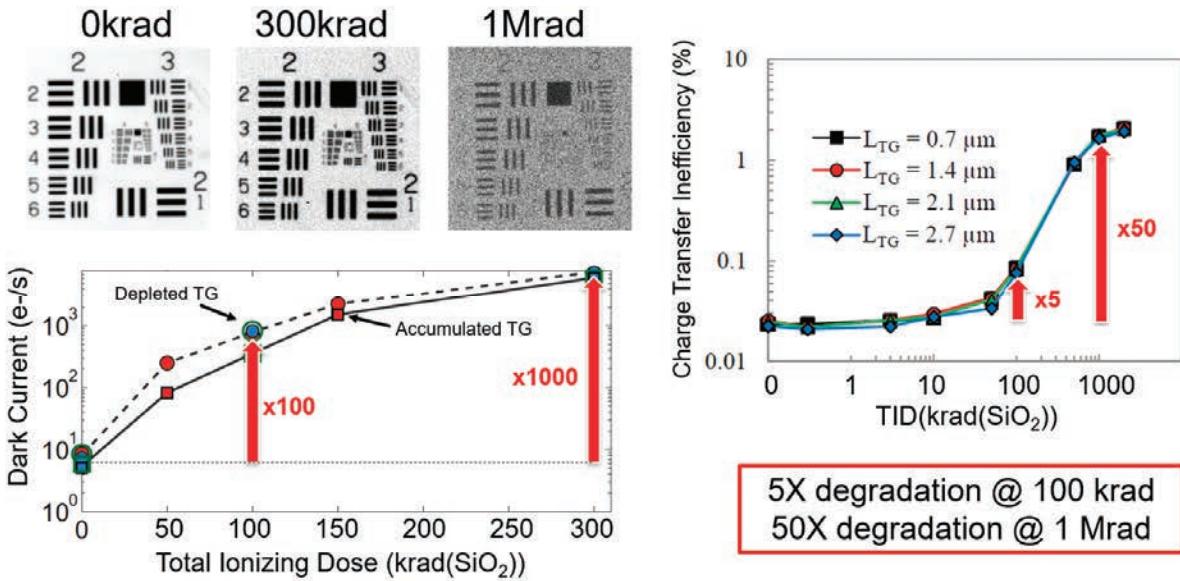


Figure 43 : Illustration of the typical degradation reported on PPD CIS pixel when exposed to ionizing radiation.

When the TID levels exceeds several tens of krad, the positive trapped charge above the PPD-TG overlap region becomes sufficient to deplete the interface below the TG spacer as depicted in Figure 42. This has two consequences [112], [174], [175]:

- An interface state generation current contribution (described by equation 2) arises from this newly depleted interface.
- The positive charge trapped in the spacer creates a potential pocket that can retain useful signal electrons during transfer, leading to severe charge transfer degradation.

An example of the typical orders of magnitude of these radiation induced degradation is given in Figure 43 (data from [112]and [175]). For higher TID, typically 1 Mrad and above, the positive trapped charge can deplete the ILD interface enhancing further the dark current and charge transfer degradation and preventing the proper operation of the photodetector.

This brief overview of the main effects is sufficient to discuss the radiation hardening possibilities. More detailed presentation of TID effects in PPD CIS can be found in [156] and references therein.

2.2.2 Mitigating TID induced dark current and CTE degradation

2.2.2.1 Good practices

Not much can be done at the design level on a standard PPD CIS process to really mitigate the presented degradation mechanisms. The following good practices can help lowering the magnitude of the radiation induced dark current:

- The transfer gate shall be placed into accumulation to avoid the TG gate oxide generation dark current contribution. However, doing so may lead to blooming issues in CIS where the pixels are not fully isolated using DTIs. Especially, dark current

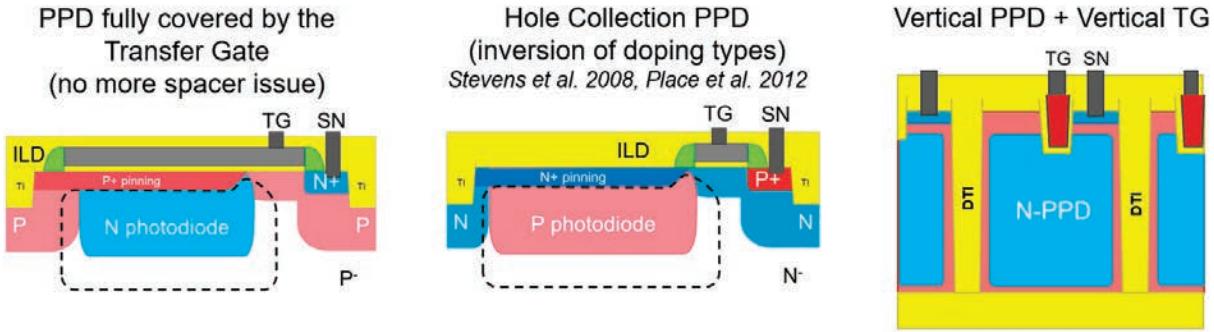


Figure 44 : Possible improvement of the radiation hardness of PPD CIS based on process modifications.

blooming [176] could become an issue. In this case, a trade-off has to be found between anti-blooming performance and dark current.

- If the trench isolations appear to bring a noticeable diffusion dark current contribution, the distance between the trenches and the lateral P-well/N-photodiode junction shall be increased [177]. The minimum distance allowed by the design rule in large pitch pixels are often sufficiently large to cancel the STI contribution (if the STI P passivation or the P-well is sufficiently doped). This may not be the case in small or ultra-small pitch pixels using STI or DTI where this distance is reduced to its minimum to leave enough room for the photodiode. This explains why the STI contribution was not seen in [67] whereas trench isolation appeared to be the main source of radiation dark current in [68].
- Reducing the photodiode area can weaken the radiation induced dark current if the main contribution is the diffusion dark current from the ILD interface (low TID case with accumulated TG and trench isolations far enough to bring a negligible contribution).
- Wide transfer gates shall be avoided since they maximize the spacer interface generation dark current contribution.
- It is recommended not to add any secondary transfer gate, as antiblooming and global-reset transfer gate, since it would bring its own spacer generation dark current contribution.

Following these recommendations can improve the behavior of a PPD CIS at low TID (below 100 krad) but it will not mitigate the charge transfer efficiency degradation followed by a complete loss of functionality observed at higher TID (≈ 1 Mrad). Because of that, PPD CIS manufactured using unmodified CIS processes are not suitable, in 2021, for high and ultra-high TID applications.

2.2.2.2 Radiation hardening solutions based on process modification

The picture is more optimistic if PPD CIS process modifications are envisaged. Some possibilities are presented in Figure 44. Placing an electrode that covers entirely the PPD (as proposed in [156], [174], [178]) could potentially completely mitigate the spacer and ILD related radiation effects and make it possible to use PPD CIS for ultra-high TID applications. The solution proposed on the left of Figure 44 would require a simple process sequence modification, without any additional implant. By covering the PPD entirely, the spacer region would not

influence the transfer region anymore and the depletion of the top oxide interface would not occur thanks to the thin gate oxide and the negative gate bias applied. Unfortunately, this structure has only been validated by TCAD simulation [174] and an experimental confirmation is required to reach final conclusions.

Contrary to the conventional photodiode case, inverting the doping type of a pinned photodiode pixel improves significantly its radiation hardness [179]. Such hole-collection PPD [179], [180] is represented in Figure 44 (middle drawing). The sensitive region is now P and it is surrounded by N doped layers. Hence it does not suffer anymore from the depletion of the surrounding interfaces, which mitigates the spacer induced dark current. It also prevents the creation of a potential pocket below the spacer that degrades the charge transfer efficiency. However, TID still induces an important positive trapped charge in the spacer that will most likely deteriorate the charge transfer at high TID by creating a potential barrier. This effect has not been studied in the literature and cannot be confirmed, but it is a potential limitation. It should be emphasized that some CIS foundries propose the hole-collection PPD in their offer, but if it is not available, developing this technology from scratch is an important effort.

The illustration on the right of Figure 44 is not really a process modification since COTS image sensors use such vertical PPD with a vertical TG in their sub-1 μm -pitch pixels as discussed in section 1.3.5.1. It is however interesting to consider this case from the point of view of radiation hardening. At first glance, such topology should mitigate the TG spacer related issues (but could bring new degradation mechanisms), allowing its use in ultra-high TID applications. On the other hand, this sketch shows that the photodiode is surrounded by thick oxides in all the directions and given the pixel dimensions, these oxide interfaces are very close to the sensitive volume. It is then likely that the radiation hardness of such state-of-the-art pixel may not be significantly higher than a more classical PPD.

If the vertical PPD concept is mixed with the inversion of the doping types, improved radiation hardness is also expected. This is demonstrated up to 100 krad in [181], but no data have been reported at higher TID, making it difficult to conclude about the possibility to use this technology for ultra-high TID applications. The Fully Depleted Trench-Pinned Photo Gate pixel proposed in [45] could also bring extra intrinsic radiation hardness thanks to the inverted CDTI on the side of the P-doped region. Still, the effect of TID on the vertical TG with a gate oxide probably thicker than 10 nm has to be clarified (as for the pixel depicted on the right of Figure 44).

2.2.3 Radiation Hardening of the Sense Node

In addition to the main TID effects on the PPD and the TG mentioned in section 2.2.1, the sense node is also susceptible to the absorption of ionizing radiation [77], [115]. The case of the SN is similar to the case of the conventional photodiode and of any floating reverse biased PN junction in a CMOS ICs. Hence, the SN degradation mechanisms are the same as the one presented in section 2.1.1. The main issue is the radiation induced leakage current increase mainly coming from an intensification of the interface trap generation dark current (equation (2) again). The two main sources are the peripheral STI (as for the conventional photodiode, except that here the contribution comes from the STI sidewalls, not the STI bottom) and the spacer/gate oxide interface on the TG side. This latter cause of leakage can be enhanced by the TG OFF voltage because of the well-known GIDL-TAT effect discussed in section 1.3.4.1.

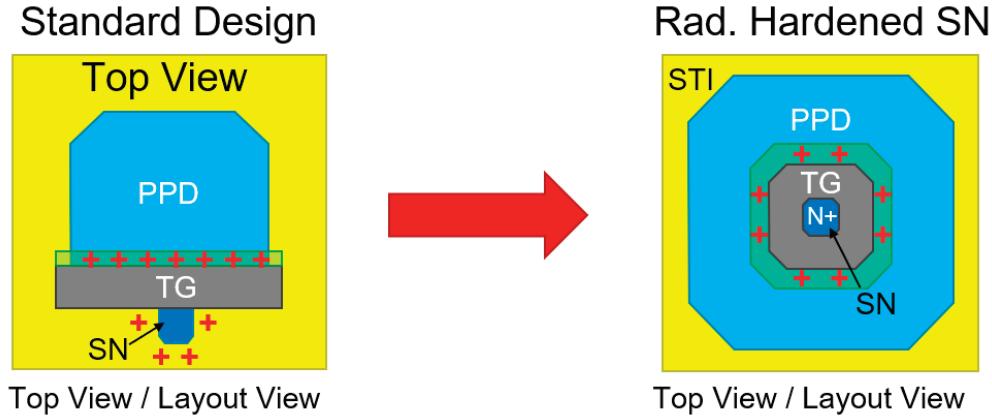


Figure 45 : Recommended TG layout to mitigate TID induced SN leakages.

In most applications (using a rolling shutter operating mode, see section 1.3.3 for details) this leakage may not be an issue because the SN is integrating this parasitic current only for a short amount of time: the time between the SHR and SHS samples visible in Figure 9. This duration is typically of the order of magnitude of $1 \mu\text{s}$, which is generally too short to see a real impact of the SN leakage current. However, in applications where the signal charge is stored for a longer time on this floating node, as in global shutter sensors or burst imagers, this leakage become the limiting factor.

Figure 45 presents a PPD pixel layout that mitigates most of this TID effect. It consists in enclosing the SN by the TG [182], thus cancelling the STI contribution. Since the TG spacer/oxide contribution remains, the TG OFF voltage has to be carefully chosen to avoid EFE. This technique is very effective at hardening the SN but does not improve the PPD-TG radiation hardness [174]. So, its use is mainly recommended when the SN leakage is limiting the application.

2.3 TID Effects on in-pixel MOSFETs

2.3.1 RHBD of In-Pixel MOSFETs

Below 100 krad in modern CIS technologies, radiation induced degradation of in-pixel MOSFETs is rarely an issue. The pixel linearity, FWC, saturation behavior or image lag performance can possibly be degraded if the pixel operation relies on the use of the in-pixel RST transistor in its subthreshold regime [163], since subthreshold leakage is the main TID effect expected in this range. This is for example the case when the soft-reset [183] technique is used. In this case, hardening solely the RST transistor is sufficient and P+ guardrings are not required.

For TID beyond 1-10 Mrad, all the in-pixel transistors need to be radiation hardened using the well-known techniques [11]–[15] since threshold voltage shifts (mainly caused by the Radiation Induced Narrow Channel Effect [184], or RINCE) and source to drain leakages become significant. If enclosed layouts are used and if the most sensitive nodes are enclosed (SN and the nodes connected to the shared column bus), P+ guardrings are still not necessary (i.e. in-pixel inter device leakage does not seem to have any influence if ELT are used in the pixel).

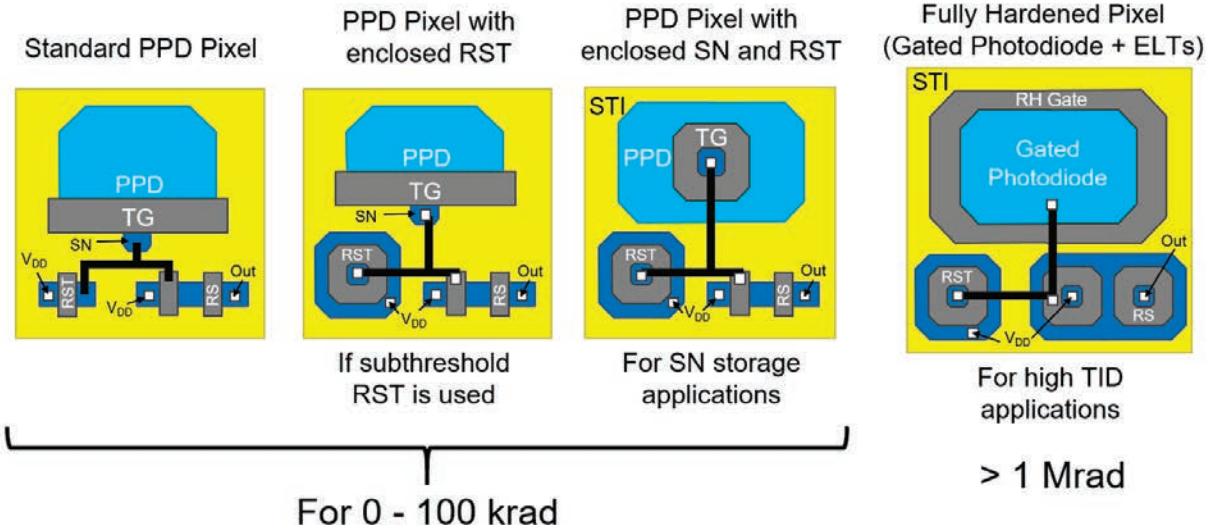


Figure 46 : Illustration of the possible radiation hardened CIS pixel layouts (pixel top view) as a function of the TID range and the application/the operating mode. These sketches are not optimized layout with optimized opto-electrical performances (such as fill factor, FWC, transfer efficiency, etc.) and many possibilities exist to draw the PPD/TG and to assemble the pixel building blocks.

2.3.2 RHBD Pixel Layout Illustrations

A summary of the previous recommendations is presented in Figure 46. At low TID, possibly up to 100 krad, unhardened PPD CIS pixels might provide the best performances in most applications, with an ultra-low dark current, high gain, high sensitivity and low noise. If in this TID range the MOSFET RST subthreshold leakage can be an issue, better performance can be obtained by using an enclosed layout for it. If SN junction leakage cannot be tolerated in the application, both the SN and the RST source shall be enclosed. Finally, if the targeted TID level for the application exceeds a few Mrad, PPD based design might suffer severe TID induced degradation and a radiation hardened by design pixel layout based on a conventional photodiode is probably the best choice. Here, a gated photodiode with in-pixel ELT is represented as an example. PPD-based pixel designs are not envisaged in this 2021 summary for ultra-high TID since none has been proven yet tolerant enough to be usable at such high TID.

In between 100 krad and a few Mrad, the optimum pixel design will depend on the technology sensitivity to TID and on the application requirements and either PPD or conventional photodiodes could be selected.

3 Mitigating Displacement Damage in CMOS Image Sensors

3.1 Displacement Damage in CIS: a Brief Overview

This section gives a brief overview of the most relevant displacement damage effects in CMOS imagers for a radiation hardening discussion: the linear augmentation of the average dark current with non-ionizing radiation dose and the increase in dark current non-uniformity, also referred to as the creation of hot or bright pixels. DDD induced DC-RTS is also presented in the third subsection. More detailed discussions about displacement damage effects in CIS can be found in [156] and references therein. Charge trapping by DDD induced bulk defect is generally not an issue in CISs but it can degrade the charge transfer efficiency of CCDs [10], [16]. It can also be the limiting factor in particle detectors[9] with thick collection volumes (several tens or even a few hundreds of micrometers) because the signal charge density is extremely high along the track of the particle (maximizing the carrier trapping probability) and because the signal charge has to be collected very quickly (\approx nanosecond range). In classical CISs, the collection volumes are very thin (a few micrometers), the local injection level due to light absorption is much lower than the local density of charge created by ionizing particles and the typical charge collection timescale is at least in the microsecond range (except for high-speed imaging or time of flight sensors). These particularities minimize the carrier trapping probability by DDD induced defects and their effects on CIS imaging performances. Therefore, this specific effect is not discussed further in these notes.

3.1.1 Displacement Damage Dose

When energetic particle radiation penetrates a material, it may transfer its energy directly to the nuclei of its constituting atoms. If the transferred energy is sufficient, atoms of the materials may be displaced from their original site by this non-ionizing interaction. In a perfect crystal, this radiation induced atomic displacement leaves a vacancy and the ejected nucleus ends up being an interstitial as illustrated in Figure 47. These crystalline imperfections can recombine (and so disappear) or lead to permanent defects by agglomerating or by combining with other defects or impurities (like dopants). In a semiconductor, displacement damage mainly consists in the creation of SRH recombination/generation centers, thus adding extra dark current sources in reverse biased PN junctions.

Similarly to TID, the amount of energy deposited by unit mass through non-ionizing interactions can be defined as a displacement damage dose (DDD). In the applications of interest for these notes, the DDD is mainly deposited by hadrons (i.e. protons, neutrons and ions) and electrons even if high energy photons can transfer part of their energy through non-ionizing interactions as well.

Typical units used in the literature are J/kg, eV/g or 1 MeV equivalent neutron fluence. The latter gives the fluence of 1 MeV neutrons that would lead to the same DDD transferred to the material by the particle. For instance, the DDD absorbed by a micrometer thick slab of silicon exposed to a beam of 50 MeV protons at a total fluence of 10^{11} cm^{-2} corresponds to about $6 \times 10^{-14} \text{ J/kg}$, 400 TeV/g and to a 1 MeV neutron equivalent fluence of $2 \times 10^{11} \text{ cm}^{-2}$ (i.e. it would require approximately $2 \times 10^{11} \text{ cm}^{-2}$ 1 MeV neutrons to reach the same displacement damage dose). It is interesting to notice that at this 50 MeV proton fluence, the absorbed TID would be about 16 krad(Si), i.e. 160 J/kg, many orders of magnitude higher than the DDD.

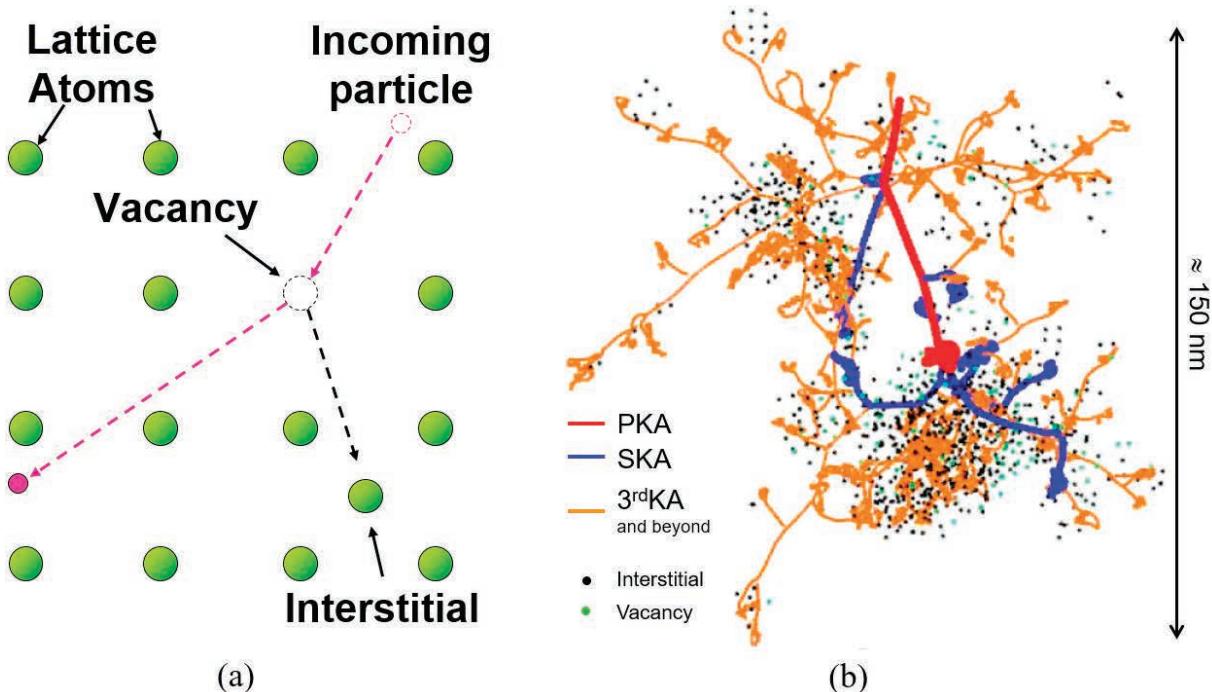


Figure 47 : Displacement damage illustrations. (a) Sketch of a displacement damage in an ideal semiconductor crystal. The incoming particle displaces one nucleus from its original lattice site leaving a vacancy and creating an interstitial. (b) Molecular dynamics simulation of displacement damage in silicon. PKA = Primary Knock-on Atom, SKA = Secondary Knock-on Atom. PKA energy = 10 keV. Simulation timescale ≈ 1 ps. Courtesy of Antoine Jay.

For space applications, the 1 MeV equivalent neutron fluence considered to evaluate the DDD absorbed by detectors is generally below 10^{12} cm^{-2} (below a few PeV/g) whereas for nuclear applications or particle physics some instruments and detector can be exposed to particle fluences as high as 10^{16} cm^{-2} for the most extreme cases [9].

Detailed background information on displacement damage theory and effects on semiconductor devices can be found in [7]–[10].

3.1.2 Displacement Damage Induced Dark Current and Hot Pixels

The permanent defects created by displacement damage are often very effective SRH generation centers. When one of them ends up in a reverse biased photodetector depletion volume, it gives rise to a very large dark current that can lead to pixels already saturated in dark conditions (as illustrated in Figure 48).

The average dark current generated in silicon by displacement damage is well described by Srou and Lo Universal Damage Factor (UDF) for the particles of interest in these notes (i.e. protons and neutrons of a few MeV to a few hundreds of MeV):

$$\bar{I}_{\text{DDD}} = K_{\text{dark}} \times \text{DDD} \times V_{\text{dep}} \quad (23)$$

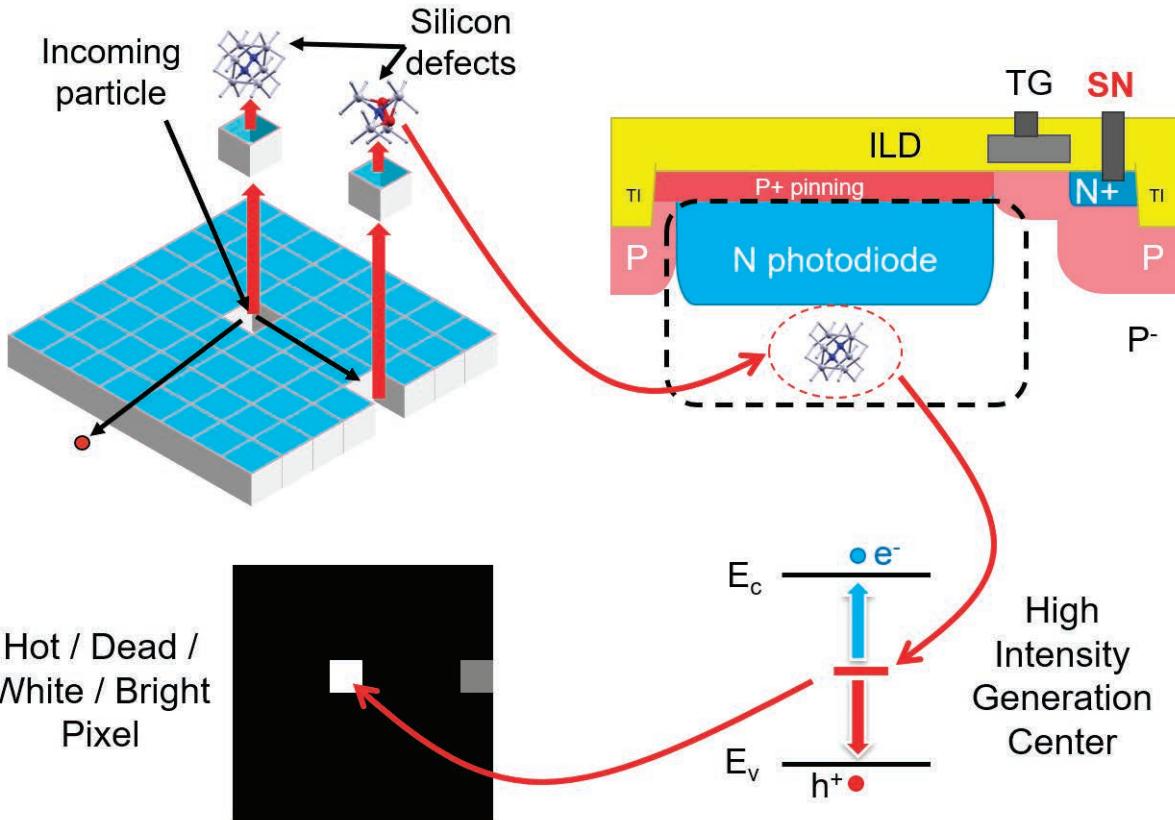


Figure 48 : Illustration of the creation of hot pixels caused by non-ionizing interaction (i.e. displacement damage).

with $K_{\text{dark}} = 1.9 \times 10^5 \text{ carrier.s}^{-1} \cdot (\text{MeV/g})^{-1} \cdot \text{cm}^{-3}$ at 300K after 1 week annealing [185], which gives $K_{\text{dark}} \approx 0.1 \text{ e-.s}^{-1} \cdot (\text{TeV/g})^{-1} \cdot \mu\text{m}^{-3}$ at 22°C after six weeks of annealing [186]. A similar current-related damage factor is also used in the particle detection community [9].

Both damage factor modelling approaches show that the dark current increase averaged on the whole pixel array is proportional to the displacement damage dose and the depleted volume and that it does not depend on the technology (in absence of strong electric field).

The distribution of displacement damage dark current over a pixel array for a given DDD can also be forecasted using the following exponential empirical model giving the probability density function of the dark current generated in a depleted microvolume by a non-ionizing interaction [77], [186], [187]:

$$f_{v\text{dark}}(x) = \frac{1}{\nu_{\text{dark}}} \exp\left(-\frac{x}{\nu_{\text{dark}}}\right) \quad (24)$$

with ν_{dark} the mean generation current increase per non-ionizing interaction estimated to be about between 4100 carrier.s⁻¹ at 22°C after six weeks of room temperature annealing. To obtain the probability density function of generated dark current per microvolume, one has to take into account the probability to get k displacement damage events generating dark current in a pixel. This probability is given by the Poisson distribution:

$$P(k; \mu) = \frac{\mu^k e^{-\mu}}{k!} \quad (25)$$

Where the μ factor is given by:

$$\mu = \frac{K_{\text{dark}}}{V_{\text{dark}}} \times \text{DDD} \times V_{\text{dep}} \quad (26)$$

In the end, the total distribution of displacement damage induced dark current increase in a pixel array is described by the following probability density function:

$$f_{\Delta I_{\text{dark}} \text{DDD}}(x) = P(0; \mu) \cdot \delta(x) + P(1; \mu) \cdot f_{\text{vdark}}(x) + P(2; \mu) \cdot f_{\text{vdark}}(x) * f_{\text{vdark}}(x) + \dots \quad (27)$$

For discussing radiation hardening we can focus on the second term of this distribution and neglect the pixels that are not damaged (i.e. the first term) and the pixels that encountered more than one non-ionizing interaction in their depleted volume (third term and beyond). Besides, if μ is considered to be much less than 1 (case of low DDD or small depleted volume) the second term becomes:

$$f'(x) = \frac{K_{\text{dark}}}{(V_{\text{dark}})^2} \times \exp\left(-\frac{x}{V_{\text{dark}}}\right) \times \text{DDD} \times V_{\text{dep}} \quad (28)$$

This simplified equation shows that at low DDD (or when the depleted volume is small enough) the dark current increase of damaged pixels is exponentially distributed and the relative number of these damaged pixels is given by the product $\text{DDD} \times V_{\text{dep}}$. In other words, at low particle fluence, displacement damage interactions are expected to create an exponential distribution tail in the experimental dark current distribution as illustrated in Figure 49 (data from [188]). This tail is shifted upward when the DDD increases or when the depletion volume is enlarged (as depicted in Figure 50). As for the average dark current increase, this DDD induced dark current distribution seems to be universal and to only depend on the radiation dose and the depletion volume (at least for neutrons and protons between a few MeV to a few hundreds of MeV). Technological or process parameters like doping does not seem to play any role. One likely explanation is the fact that for these particles in this energy range, the dominant dark current generation centers are defect clusters which are weakly influenced by doping concentrations and other manufacturing conditions.

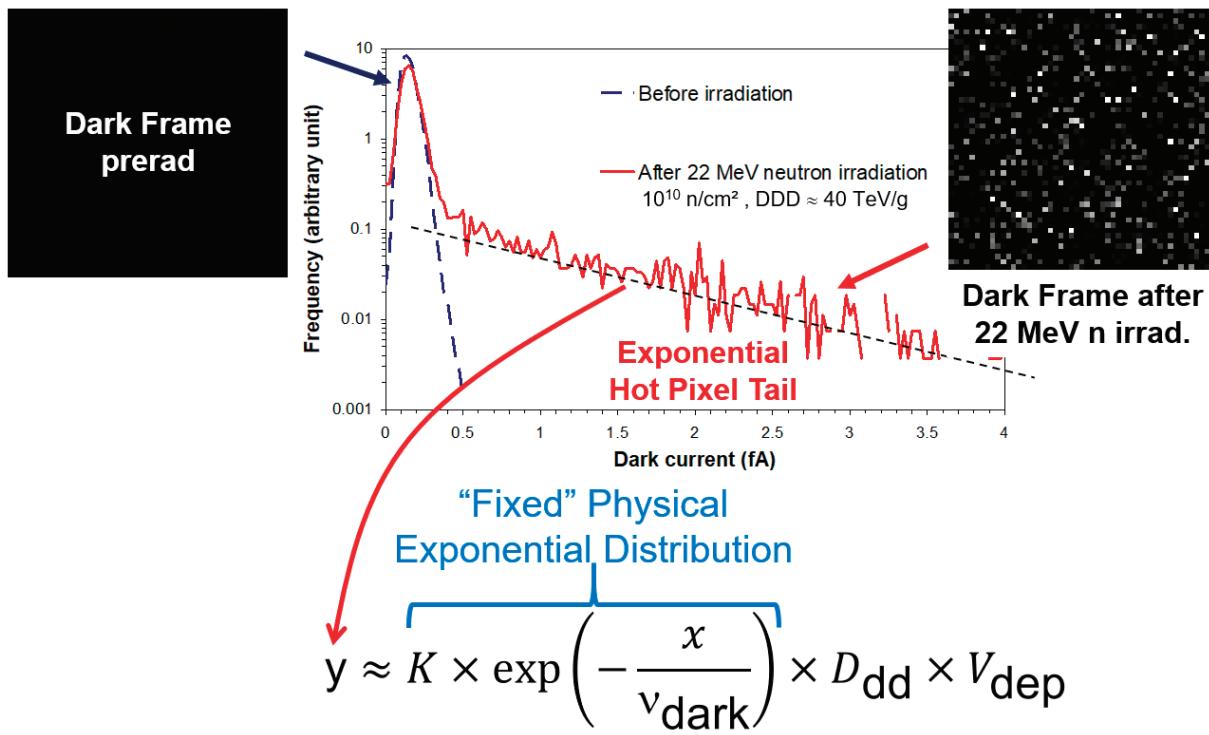


Figure 49 : Displacement damage induced dark current distribution in a conventional photodiode 3T CIS exposed to 22 MeV neutrons at a fluence of 10^{10} n/cm².

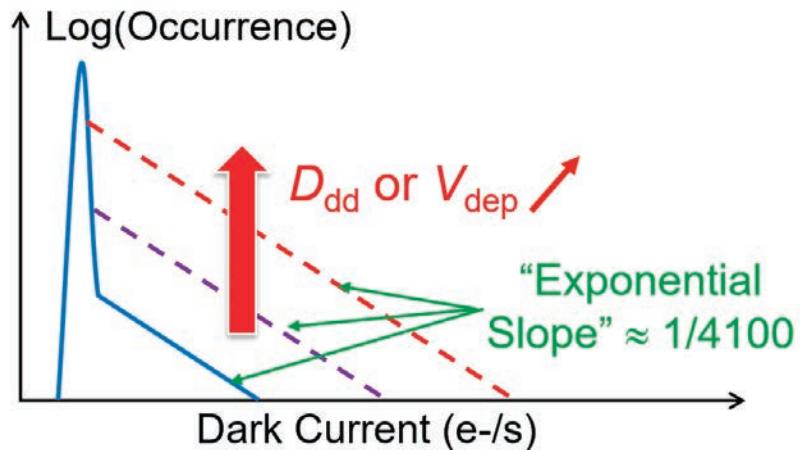


Figure 50 : Illustration of the impact of displacement damage and the depletion volume on the dark current distribution.

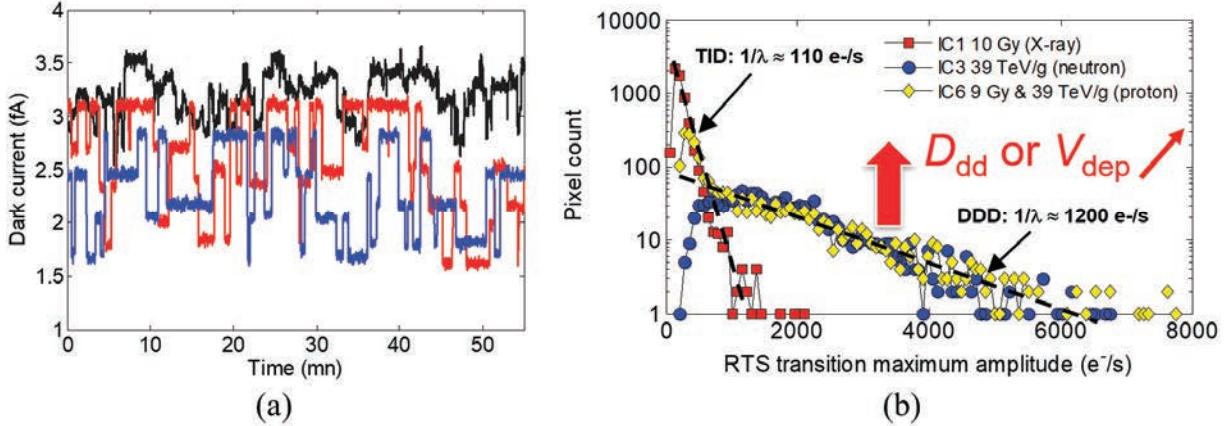


Figure 51 : Radiation induced DC-RTS illustrations. (a) Typical DC-RTS traces measured in proton or neutron irradiated silicon pixel arrays. **(b)** Experimental RTS MTA distributions for CIS exposed to X-rays, protons and neutrons highlighting the differences between TID and DDD induced DC-RTS.

3.1.3 Displacement Damage Induced RTS

As introduced in section 1.3.4.3, the dark current is not always stationary and it can exhibit a random telegraph signal behavior. Ionizing and non-ionizing interactions can both lead to the creation of DC-RTS centers in pixel sensitive volumes but displacement damage is more effective at generating high amplitude and multilevel RTS behaviors (as illustrated in Figure 51, data from [110]).

To count DC-RTS pixels and quantify their impact on sensor performances, one possibility is to extract their maximum transition amplitudes (MTA) and to plot their distribution. It is regularly observed that the RTS MTA follows here again an exponential probability density function:

$$f_{\text{DC-RTS}}(x) = \frac{1}{A_{\text{RTS}}} \exp\left(-\frac{x}{A_{\text{RTS}}}\right) \quad (29)$$

with $A_{\text{RTS}} \approx 1100-1200 \text{ e}^{-}/\text{s}$ at 22-23°C after a few weeks annealing for displacement damage induced DC-RTS and $A_{\text{RTS}} \approx 110-120 \text{ e}^{-}/\text{s}$ for TID induced DC-RTS [77], [101], [107], [110], [117], [189], [190]. Contrary to dark current for which the measured value corresponds to the sum of the contributions of all the radiation induced defects generated in the sensitive volume, only one DC-RTS center per pixel contributes to the measured MTA. Indeed, if there are more than one DC-RTS center in a pixel sensitive volume, the extracted MTA will not correspond to the sum of the contributions but only to the MTA of the most active RTS defect. Hence, the superimposition of DC-RTS sources does not have to be considered to forecast the experimental MTA distribution and the final distribution can be directly approximated by multiplying equ. (29) by the expected proportion of DC-RTS in a pixel array:

$$f'_{\text{DC-RTS_DDD}}(x) = \frac{\text{DDD} \times V_{\text{dep}} \times K_{\text{RTS}}}{A_{\text{RTS}}} \exp\left(-\frac{x}{A_{\text{RTS}}}\right) \quad (30)$$

where K_{RTS} is a damage factor that gives the number of generated DC-RTS centers per unit of depleted volume and of DDD. The DC-RTS displacement damage factor seems to be a constant as well in silicon image sensors with a classically reported value $K_{\text{RTS}} \approx 30\text{-}35 \text{ centers.cm}^{-3}.\text{(MeV/g)}^{-1}$ [101], [107], [110], [189], [190] in very different CMOS and CCD sensor technologies. This last equation shows that, as for DDD induced dark current increase distributions, the sole parameters that play a role in the creation of DC-RTS pixel are the DDD and the depleted volume.

3.2 Hardening Against Displacement Damage

3.2.1 Electric Field Strength Reduction

The previous conclusions that the occurrence and intensity of DDD induced dark current and DC-RTS in silicon pixel arrays only depends on the radiation dose and the depleted volume holds only if electric field hot spots are not present in the sensitive volume of the pixel. As discussed in section 1.3.4.1, high electric field regions are not expected in state-of-the-art CMOS sensors. However, a non-optimized design or manufacturing process can lead to electric field hot spots that can enhance the radiation induced dark current generation and so, the amplitude of radiation induced DC-RTS [191]. Such intense electric field is also generally found in classical source/drain PN junctions in CMOS integrated circuits and especially in the sense node (or floating diffusion) of CIS [77]. The exact same situation occurs in SPADs [104] where the DC-RTS amplitude is amplified when the overvoltage is increased because of the EFE mechanisms discussed in 1.3.4.1.

As a consequence, if the pixel dark current appears to suffer from EFE, the first step to improve the radiation hardness against displacement damage effects is to reduce the occurrence of high electric field regions by optimizing the design or by lowering the operating voltage.

3.2.2 FWC and Gain Optimization

The relative impact of dark current can be reduced simply by lowering the sensor gain or by increasing the FWC. Both parameters are generally directly linked since in most designs the output saturation signal is given by the product of the total gain (including the CVF) and the FWC. For the sake of clarity, it is considered here that the gain or the FWC can be tuned without modifying the photodiode depletion volume. This is for example the case when the gain of the readout chain is modified or when the sense node in a 4T PPD pixel is enlarged or reduced. The next section discuss separately the impact of a modification of the photodiode depletion volume.

Figure 52 illustrates how lowering the gain (or increasing the FWC) can significantly reduce the impact of displacement damage induced dark current (and DC-RTS as well) by decreasing the number of saturated pixels and also by lowering the resulting dark signal of every pixel. The main drawback of this technique is the fact that by reducing the gain, the system sensitivity is reduced as well, which may not be acceptable at the system level. In most of the cases, the

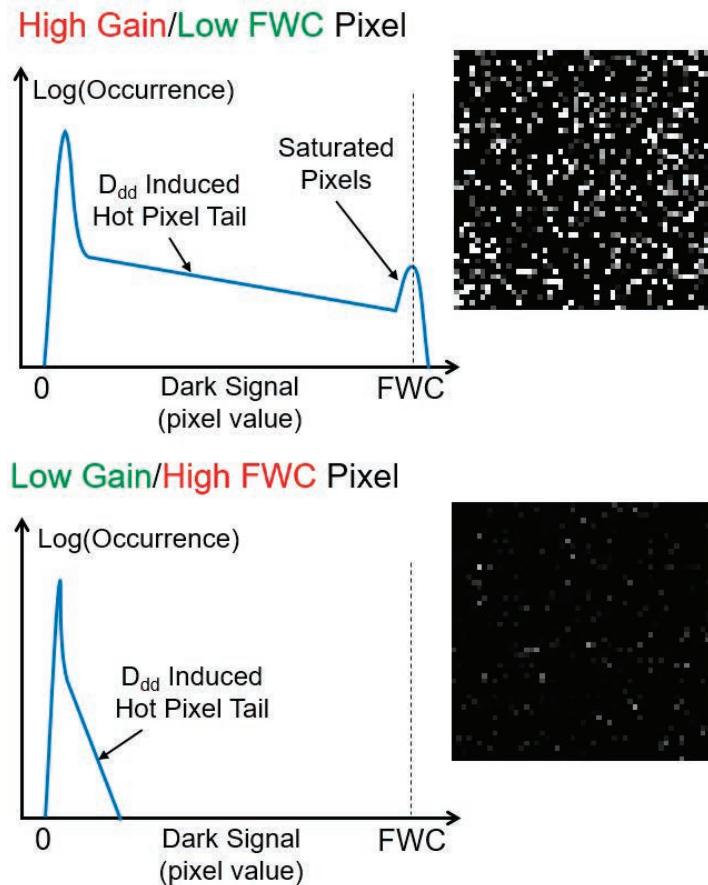


Figure 52 : Illustration of the influence of the gain or FWC on the relative importance of the displacement damage induced hot pixel tail. It is considered here that the modification of gain or FWC is obtained without modifying the depletion volume.

application imposes the FWC/gain specification of the sensor, removing any freedom to modulate DDD effects.

It can be useful to realize the impact of the FWC/gain couple on the sensitivity to displacement damage, since it can improve the radiation hardness of an imaging system if the tolerance to displacement damage is the primary concern. However, in most situations, it may not be applicable. It is also interesting to notice that the same approach can be used to improve the tolerance to TID induced dark current increase without having to use radiation hardened layouts. It will not prevent the failure of unhardened photodiodes and pixels at high TID thought.

3.2.3 PPD Layout Hardening Technique

A few photodiode layout optimizations can be envisaged to improve the radiation hardness versus displacement damage without impacting much the sensor sensitivity. For PPD-TG pixels, the area of the photodiode can be modified without changing the CVF, and so without gain variation. It is then possible to reduce the depletion volume by reducing the as-drawn PPD area as shown in Figure 53. According to equations (28) and (30), it will lead to a reduction of displacement damage effects proportional to the area reduction (by reducing the probability to get a radiation induced bulk defect in the depleted volume). This technique is effective but since

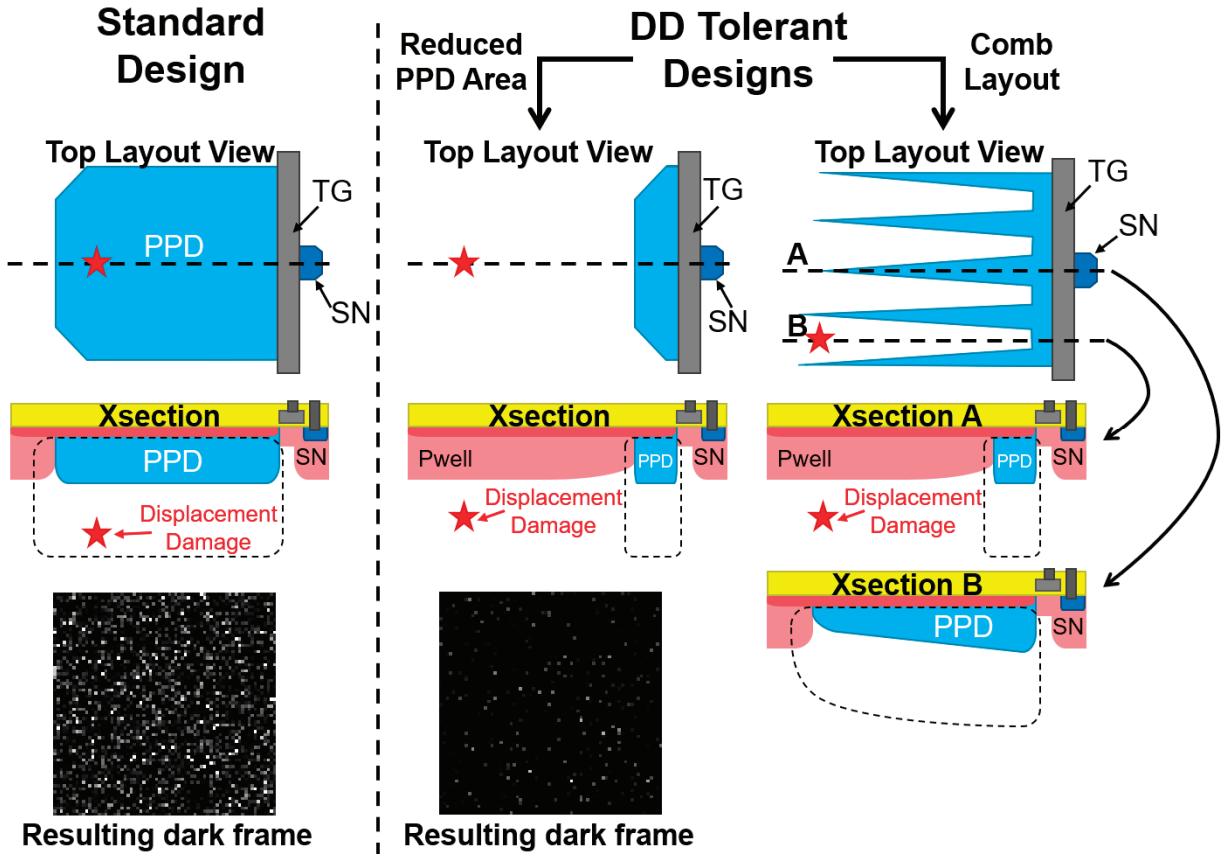


Figure 53 : Radiation hardening by design techniques applicable to PPD pixels to mitigate displacement damage effects with limited impact on the sensor's performance.

the PPD does not cover the full available pixel area anymore, a degradation of the charge collection efficiency (and so of the external quantum efficiency) is expected. It is possible to push further the concept by covering the pixel area with an original PPD design, such as a comb design [192] presented in Figure 53 or other variants with a circular TG and star-shaped layouts [193]. By doing so, a higher radiation hardness can be obtained without a significant impact on the sensor performance (like the quantum efficiency). A similar optimization can be performed by modifying the PPD doping concentration [193], [194]. Indeed, by optimizing the PPD doping profile one can significantly reduce displacement damage effects by reducing the depletion volume without degrading the other sensor parameters.

The same logic could be applied to the conventional photodiode, but since the pixel gain (i.e. the CVF) and the photodiode size are intimately related, there is no real room for radiation hardness improvement. For instance, reducing the area of a conventional photodiode improves its tolerance to DDD by reducing the depletion volume but at the same time it increases the pixel CVF, leading to more relative impact of the radiation induced dark current (and with a loss of quantum efficiency). Putting in parallel dots or islands of photodiode Nwells can mitigate the quantum efficiency drop induced by the photodiode area reduction but with still an impact on the gain and FWC.

Using a CIS process that offers the partially pinned photodiode (presented in Figure 40) can help optimizing a 3T-conventionnal photodiode pixel to improve its tolerance to displacement damage since the pixel CVF is mainly given by the surface N+ contact and not by the area of the collecting Nwell photodiode. In this case, by optimizing the deep N photodiode implant to reduce the depletion thickness on one hand and by optimizing the shape of this implant to cover the pixel area with the minimum necessary depletion volume on the other hand (e.g. again with a star-like shape), an improved radiation hardness can possibly be achieved with limited impact on the 3T CIS performance.

It should be mentioned that redundancy is also sometimes mentioned as a solution to harden a pixel array against displacement damage [195]. For instance, it can consist in implementing two photodiodes inside the same pixel instead of one and disabling electrically the photodiode damaged by a non-ionizing interaction when it is detected. In general, these techniques degrade the pixel performance (by increasing the noise, reducing the fill factor and the quantum efficiency...) whereas selecting a standard higher resolution sensor and discarding the signal of damaged pixels during the image processing step can be as efficient without any performance degradation and without the need of a pixel customization.

3.2.4 Operating Temperature

A technique commonly used in space and nuclear physics instrument to mitigate displacement damage effects is cooling. Indeed, as discussed in section 1.3.4.1, generation dark current exhibits an activation energy around 0.63 eV. Therefore, every 8-degree temperature reduction divides by 2 the radiation induced dark current. This is an effective technique without major drawbacks (beyond the difficulties linked to the implementation of the temperature control and the associated dissipated power) and it is frequent to see detectors cooled down to -10/-30°C to enable their use in radiation environments. Lowering the operating temperature decreases the TID induced dark current as well but it changes the room temperature annealing dynamic with possible unwanted effects.

Periodically increasing the temperature when the sensor becomes too damaged can be used to anneal TID induced defects [160] and displacement damage as well. Such operation is also common practice for space instruments. Care must be taken that these elevated temperature steps do not degrade the circuit reliability.

4 Single Event Effects: The Particularity of Image Sensors

4.1.1 Relevant SEE in Pixel Arrays

As any CMOS mixed signal integrated circuit, CMOS sensors are sensitive to all kinds of Single Event Effects (SEE) [196] and this sensitivity strongly depends on the design and the technology of the tested sensor. Typical SEEs observed in CISs are illustrated in Figure 54. However, the peripheral circuits of most of the CISs tested in the literature do not exhibit high SEE sensitivity (for example, no effect has been observed in [197]) even in extreme conditions such as Inertial Confinement Fusion (ICF) radiation environment [198]. Single Event Latchups [199], [200] (SEL) have been observed in CIS digital circuits [201], [202] whereas simple analog readout circuits are generally immune to SEL (because they usually do not have N and P-MOSFETs close to each other[203]). Single Event Upsets (SEU) have been observed in CIS [202], [204] but only in peripheral circuits (such as on-chip sequencers) that embed digital

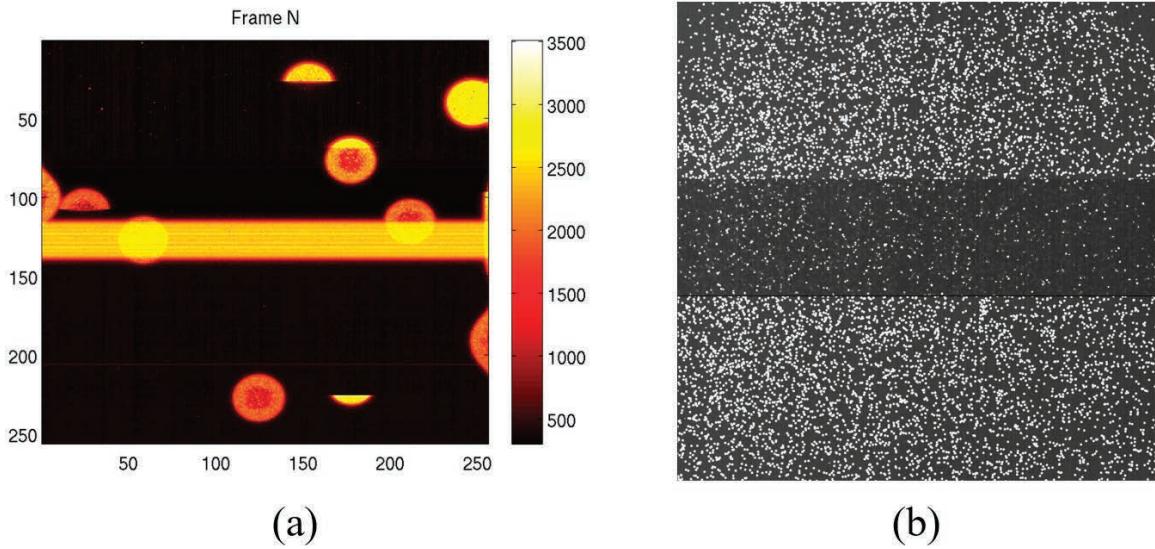


Figure 54 : Typical SEEs observed on CMOS sensor pixel arrays. (a) SET (bright spots) and SEL (horizontal bright band) induced by effect of 305 MeV Kr ions in a 256x256-7 μ M-pitch-PPD-CIS. Courtesy of Valerian Lalucaa. **(b)** SET (bright spots) and SEU induced image corruption (dark horizontal band) induced by Kr ions in a 1024x1024-18 μ m-pitch-3T-radiation-hardened-CIS. Courtesy of Matthieu Beaumel from Sodern.

memories, latches or flip-flops. Some Single Event Functional Interrupts (SEFI) [201], [205] and some Single Event Transients (SET) [203] have also been reported. Most of these SEE occurring in peripheral circuits can be mitigated by using the classical Radiation-Hardening-By-Design (RHBD) techniques [11]–[15], [196], [199], [200], [206].

As most of radiation effects in CIS, the most frequent SEEs occur in the pixel array as highlighted by Figure 54. Incoming particles generate electron-hole pairs in the sensitive silicon volume through direct (for charged particles) or indirect ionization (for neutrons and also charged particles). These high densities of parasitic carriers are collected like photo-generated signal carriers and they lead to the transient saturation of the collecting pixels. Such pixel SETs do not last more than a frame. They can saturate large clusters of pixels [203], [207], [208] or generate secondary recoil ion tracks [198], [209] and several modelling approaches have been proposed in the literature to predict their effect on image quality, their occurrence or shape of their track [204], [210]–[212]. The same single particle induced parasitic charge collection mechanisms are also actively studied and modelled in the particle detector community, but in this case, the collected charge is seen as the signal, not as a parasitic SET (see [213] for example).

Other kinds of SEE are not likely in simple 3T or 4T pixels but can be an issue in smart sensors with in-pixel integrated functions.

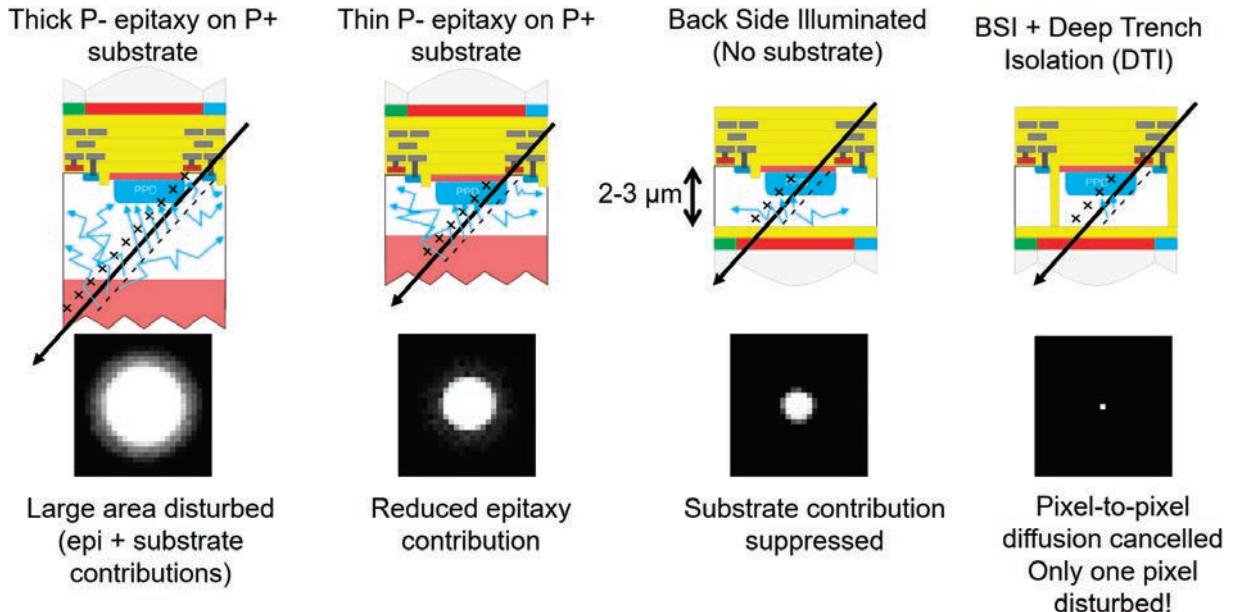


Figure 55 : Technological choices that minimize the impact of pixel SETs in pixel arrays without degrading the optoelectrical performance.

4.1.2 Mitigating Pixel Single Event Transient

To mitigate pixel SETs one has to diminish the collected charge. It can be done by design by reducing the charge collection area (i.e. the photodiode area) but it has a direct impact on the useful signal charge collection efficiency. The addition of in-pixel charge drains (e.g. N+/P_{sub} collecting diode) can decrease the SET induced charge collected by the main photodiode but they also drain the useful photocharge. In some cases, anti-blooming structures can help reducing the size of the particle track (in PPD pixels[201] but not in 3T conventional photodiode pixels [203]) without degrading the optoelectrical performance. Nevertheless, in general, not much can be done by design to mitigate SETs without a direct impact on the external quantum efficiency.

Figure 55 shows process modifications or technology choices that can efficiently reduce SETs in pixel arrays without any cost in terms of performances. The first move is to reduce the epitaxial layer thickness if the targeted application does not require a thick sensitive layer. That is for example the case for visible color imaging that only requires 2-4 μm of epitaxial thickness to ensure a good absorption in the range of interest ($\approx 400\text{-}650 \text{ nm}$) with limited diffusion cross-talk. To observe a real impact of the epitaxial layer, the substrate doping has to be much higher than the epitaxy to ensure that most of the electron/hole pairs generated in the substrate recombine before reaching the sensitive volume, as illustrated in Figure 56.

When switching to BSI sensors, the substrate is removed and the flow of carriers that escape recombination in the substrate is suppressed. This may lead to a further reduction of the collected ion induced charge, still without disturbing the main purpose of the sensor: collecting the electrons generated by visible light. The last case considered in Figure 55 corresponds to the usual configuration of consumer grade ultra-small pitch CIS in which DTI are used to fully

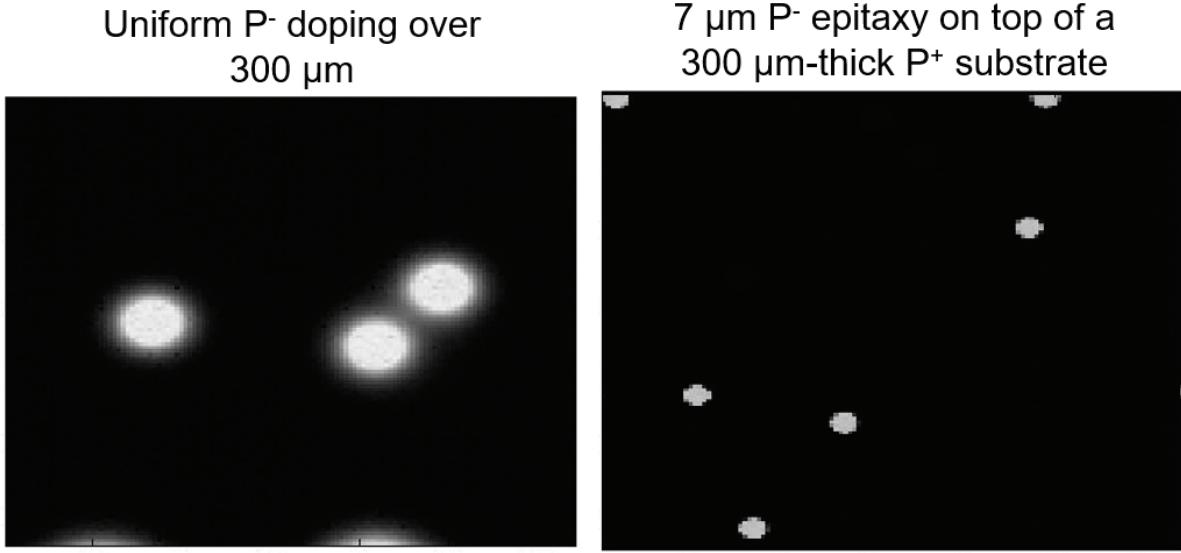


Figure 56 : SETs measured on the same CIS design with two different substrate doping concentrations: similar doping than the epitaxial layer on the left and much higher P doping concentration on the right.
Courtesy of Valerian Lalucaa.

isolate pixels and cancel cross-talks [130]. In this case, the SET spot size for a normal incidence ion is reduced to a single saturated pixel.

These technology choices used to weaken the impact on SETs are also efficient against the so-called gamma-ray induced snow typically observed in nuclear applications. Hence, the image quality in high dose rate gamma radiation environment can be significantly improved by choosing the right substrate.

In some particular applications, system level hardening techniques can be used to get rid of the unwanted parasitic charge generation by the radiation [214], [215].

4.1.3 Reducing Singlet Event Latchup Sensitivity

SELs do not occur in pixel arrays (except if CMOS functions are integrated inside the pixel) but the technological choices offered by CIS manufacturing process can have a direct impact on the SEL sensitivity of the rest of the circuit. A summary is given in Figure 57. The classical FSI CIS configuration, i.e. a thin lightly doped P⁻ epitaxy ($\approx 10^{15} \text{ cm}^{-3}$) on top of a highly doped P⁺ substrate ($\approx 10^{19} \text{ cm}^{-3}$) is already beneficial to mitigate SELs and it is generally referred to as a SEL hardening-by-process technique for CMOS ICs [200]. The heavily doped substrate lowers the parasitic resistance terms of the parasitic bipolar junction transistors at the origin of SEL and it reduces the collected parasitic charge, as discussed for SETs (and as shown in Figure 56). Hence, FSI sensors with thin epitaxial layer already exhibit a very weak SEL sensitivity. As for SETs, thinning the epitaxial layer improves the radiation hardness to SEL by reducing further the collected charge and by increasing the SEL holding voltage [216].

The impact of BSI substrate on the SEL sensitivity of the peripheral on-chip electronics is less clear. On one hand the collected charge is reduced compared to the FSI case, as discussed for SELs. On the other hand, the epitaxial layer resistance is very high and the heavily doped P⁺

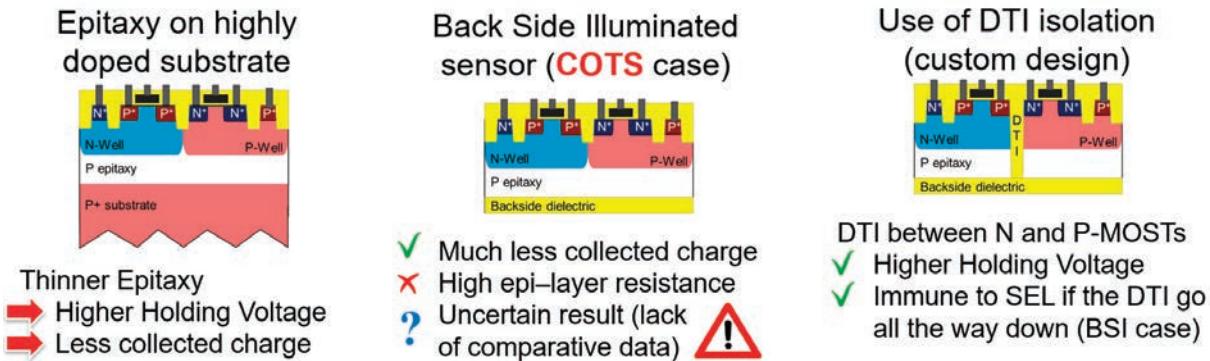


Figure 57 : Impact of CIS technology choices on the SEL sensitivity.

substrate is not there anymore to lower the parasitic resistances. The resulting SEL sensitivity is also highly dependent on how the backside interface is treated and doped. The number of substrate contacts (and their spacing) also plays a key role.

There is therefore no guarantee that a BSI sensor will exhibit a higher hardness to SEL than its FSI counterpart. The main consequence of that is the uncertain SEL radiation hardness of consumer grade BSI CIS.

Finally, SEL probability could be importantly reduced by the use of DTI outside the pixel to isolate N and P-MOSFETs from each-others. If full height DTIs are used for this purpose, complete SEL immunity could be reached. It is worth noting that this technique is not likely to be used in commercial grade sensors (outside the pixel array) and that it is only relevant for custom radiation hardened designs based on BSI CIS processes with available full height DTIs.

5 Conclusion: Hardening vs Application Requirements

5.1 Comments on the Meaning of Radiation Hardness

The radiation hardness of an image sensor depends on its purpose and it can then be difficult to compare to other devices. A striking example is the case of a conventional Nwell photodiode on a P substrate manufactured using a classical CMOS process that is meant to be used in an image sensor on one hand and in a particle detector on the other hand. Let's consider that both silicon pixel arrays have to be exposed to a high displacement damage dose. According to the discussion developed in these notes, to reach the highest hardness against displacement, the pixel sensitive depletion volume shall be minimum. On the contrary, in a typical silicon particle detector, the depletion region of the exact same Nwell photodiode has to be extended as much as possible into the substrate to provide the maximum radiation hardness.

This can be explained by the fact that the two types of detectors serve a different purpose. In an image sensor, the steady dark current directly compete with the useful photosignal and dark current as low as 1 fA can degrade the imaging performance. In this case, the depletion volume has to be minimum to reduce the displacement damage induced dark current increase.

In particle detectors, the useful signal is usually AC coupled and the main function of a pixel is to detect the pulse induced by an ionizing particle and to measure the collected charge in a nanosecond timescale. It has to be compared to the typical millisecond-to-second-timescale during which the photosignal is integrated in image sensors. Therefore, the DC dark current background is not that important in particle detectors and it becomes a real issue when it leads to high power consumption and thermal runaway on the whole detector [217]. The primary displacement damage effect for such detector is the charge trapping by bulk defects that leads to useful charge loss. To mitigate this effect on detectors the typical solution is to fully deplete the sensitive layer (that can be thicker than 100 μm). By doing so, the useful charge is quickly collected thanks to the induced electric field and the trapping probability by radiation induced defects is minimized.

This illustration shows how the purpose of a photodiode, a pixel or a detector, can completely change the RHBD approach to follow to improve its tolerance to radiation.

Figure 58 presents another situation where the radiation hardening approach comparison can be blurred. It describes the case where a pixel with a high prerad leakage is compared to a low leakage pixel. Since the latter is much more sensitive than the first, it will be degraded by low radiation dose whereas no degradation will be seen on the leaky pixel design. Does it make the leaky pixel a radiation hard pixel? Does adding a band-to-band leakage source in a pixel make it radiation hard? There is probably no unique answer to this question even if choosing the low leakage pixel seems to be the best choice for the added sensitivity it brings at low TID compared to the leaky one. It is interesting to notice avalanche photodiodes have a behavior comparable to the leaky pixel case. The prerad dark count rate is dominated by the field enhanced and multiplied dark current generation from bulk defects in the high field region of the device and interface state generation is generally not visible. For this reason, TID induced DCR increase is not observed below 1 Mrad [218], which generally makes these avalanche-based sensors radiation hard in this TID range.

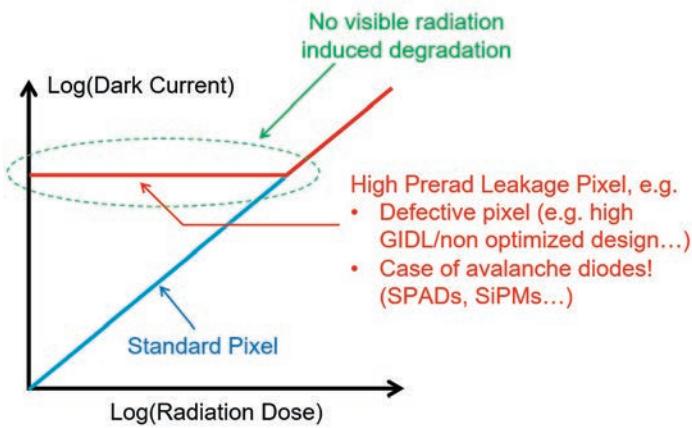


Figure 58 : Comparison of the radiation hardness of a leaky pixel and a standard low leakage pixel.

To avoid any ambiguity to discuss and compare radiation hardness in the next section, an image sensor design or technology is considered radiation tolerant or hard (at a given dose) here if:

- It performs better than the standard design when exposed to radiation.
- It can properly perform the function required by the application when exposed to radiation.

Moreover, since dark current is a very variable parameter, improvement in terms of radiation induced dark current increase shall be significant (at least a 2x improvement) and especially higher than device-to-device and lot-to-lot variability.

5.2 Summary Comparison Table

Table 4 lists, for each application case mentioned in section 1.4, the expected performance of different CMOS sensors technologies or designs. TID and SEE are the main radiation effects considered for this comparison since all these technologies can be considered equal before displacement damage, even if the pixel size and design can modulate the magnitude of this radiation effect as discussed in section 3.

Table 4: Summary Table Showing the Expected Radiation Hardness of Selected CMOS Image Sensors Technologies for Different Applications in Radiation Environments

CIS technology	Prerad	10-100 krad	100 krad – 1 Mrad	1 Mrad – 10 Mrad	10 Mrad – 100 Mrad	100 Mrad – 1 Grad	Comments
Applications		<ul style="list-style-type: none"> Medical Space 	<ul style="list-style-type: none"> Jupiter's Moon Electron Microscopy 	<ul style="list-style-type: none"> Nuclear Particle Physics 		<ul style="list-style-type: none"> Nuclear Particle Ph 	
Commercial off the shelf (COTS) (PPD)							<ul style="list-style-type: none"> No hardness guarantee State-of-the-art features Integrated complex and sensitive functions Low cost
Custom PPD Sensor							<ul style="list-style-type: none"> RH limited by photodiode Custom design might be required by the application Better control on RH No useless weak features
RHBD Sensor (Conv. PD)							<ul style="list-style-type: none"> Maximum hardness Limited performances
RHBD PPD Sensor							Dream sensor to come?

The first row of the table is dedicated to Commercial-Off-The-Shelf CMOS sensors, almost all based on PPD-TG pixel architectures. They offer probably the best performances before irradiation except in some niche applications, where custom sensors can be tailored to match specific requirements. Depending on the integrated functions, COTS imagers can fail at TID as low as a few hundreds of krad but some can still work properly in the Mrad range. They all suffer from the typical radiation induced degradations one can expect on a standard PPD pixel (see section 2.2.1 for more details) with a significant dark current increase and charge transfer efficiency degradation in the 50 krad – 1 Mrad range. However, they can still outperform radiation hardened sensors based on conventional photodiodes and so, remain an interesting choice. The main issue with the use of COTS CIS in radiation environment is probably the tolerance to SEE. The high density of complex integrated functions in consumer grade sensors makes them highly sensitive to various single event effects. It is often possible to tolerate the non-destructive SEEs that can be recovered by power cycling the camera or the instrument, but SEL detection and protection systems may be required [202]. This trade-off between performance and radiation hardness, at least at low TID, makes COTS CIS an interesting choice for a growing number of space applications. For instance, the Mars 2020 Perseverance Rover embed nearly 20 COTS CMOS imagers.

An alternative to benefit from the high performances of the PPD photodetector with a controlled radiation hardness is a custom PPD based CIS design. By carefully choosing the on-chip functions, or even by applying some RHBD rules, failures below 1 Mrad can be avoided and the SEE tolerance can be ensured. For most space applications, this is the technology selected.

Unfortunately, because of the intrinsic limitations of the PPD (the radiation induced depletion of the TG spacer and the top dielectric that ruins the charge transfer efficiency), this technology cannot be used in high TID applications such as nuclear facility monitoring or particle physics instrumentation. Depending on the mission design (and the associated TID level), unhardened PPD CIS may not be the best choice for the exploration of Jupiter's moons as well.

For such high and ultra-high TID applications, custom radiation hardened conventional photodiode-based CMOS sensors are the technology to select in 2021. They ensure the maximum radiation hardness (demonstrated up to 1 Grad [30], [31]) but at the cost of a higher prerad dark current, a lower sensitivity and a higher noise than PPD based CISs.

The last row of the table considers the ultimate CMOS sensor technology for radiation environments: a radiation hardened PPD sensor with comparable performances as the classical PPD but with a high tolerance to TID levels well above 1 Mrad. While such a high radiation hardness has not been demonstrated yet on a PPD-TG structure, several promising solutions that push this frontier are emerging, as discussed in section 2.2.2.2.

6 Acknowledgements:

The author is grateful to Marta Bagatin for her invitation to contribute to this short course and for her time and effort in reviewing these notes. The author would also like to thank the IEEE NSREC 2021 committee and the Radiation Effects Steering Group for supporting this invitation and for their guidance and support. The author thanks Matthieu Beaumel from SODERN for his hard work in reviewing this manuscript. The authors would also like to thank the ISAE-SUPAERO image sensor research group, post docs, students and interns for their direct contributions to this research work and for their everyday stimulating discussions. The coauthors and funders of the studies that form the basis of this document are warmly thanked for their contributions and support. Albert Theuwissen from Harvest Imaging, Dan McGrath from GOODIX, Jean-Pierre Carrere from ST Microelectronics, Bruno Bosset from Thales and Ray Fontaine from Techinsights are also thanked for stimulating discussions and for providing some of the material used in these notes.

7 References

- [1] T. P. Ma and P. V. Dressendorfer, *Ionizing Radiation Effects in MOS Devices and Circuits*. New York: Wiley-Interscience, 1989.
- [2] T. R. Oldham and F. B. McLean, “Total ionizing dose effects in MOS oxides and devices,” *IEEE Trans Nucl Sci*, vol. 50, pp. 483–499, Jun. 2003.
- [3] J. R. Schwank *et al.*, “Radiation Effects in MOS Oxides,” *IEEE Trans. Nucl. Sci.*, vol. 55, no. 4, pp. 1833–1853, Aug. 2008, doi: 10.1109/TNS.2008.2001040.
- [4] P. E. Dodd, M. R. Shaneyfelt, J. R. Schwank, and J. A. Felix, “Current and Future Challenges in Radiation Effects on CMOS Electronics,” *IEEE Trans. Nucl. Sci.*, vol. 57, no. 4, pp. 1747–1763, Aug. 2010, doi: 10.1109/TNS.2010.2042613.
- [5] D. M. Fleetwood, “Total Ionizing Dose Effects in MOS and Low-Dose-Rate-Sensitive Linear-Bipolar Devices,” *IEEE Trans. Nucl. Sci.*, vol. 60, no. 3, pp. 1706–1730, Jun. 2013, doi: 10.1109/TNS.2013.2259260.
- [6] H. J. Barnaby, “Total-Ionizing-Dose Effects in Modern CMOS Technologies,” *IEEE Trans Nucl Sci*, vol. 53, no. 6, pp. 3103–3121, Dec. 2006.
- [7] G. C. Messenger, “A summary review of displacement damage from high energy radiation in silicon semiconductors and semiconductor devices,” *IEEE Trans. Nucl. Sci.*, vol. 39, no. 3, pp. 468–473, Jun. 1992, doi: 10.1109/23.277547.
- [8] J. R. Srour and J. W. Palko, “Displacement Damage Effects in Irradiated Semiconductor Devices,” *IEEE Trans. Nucl. Sci.*, vol. 60, no. 3, pp. 1740–1766, Jun. 2013, doi: 10.1109/TNS.2013.2261316.
- [9] M. Moll, “Displacement damage in silicon detectors for high energy physics,” *IEEE Trans. Nucl. Sci.*, vol. 65, no. 8, pp. 1561–1582, 2018.
- [10] J. C. Pickel, A. H. Kalma, G. R. Hopkinson, and C. J. Marshall, “Radiation effects on photonic imagers-a historical perspective,” *IEEE Trans. Nucl. Sci.*, vol. 50, no. 3, pp. 671–688, Jun. 2003, doi: 10.1109/TNS.2003.813126.
- [11] R. C. Lacoë, “Improving Integrated Circuit Performance Through the Application of Hardness-by-Design Methodology,” *IEEE Trans. Nucl. Sci.*, vol. 55, no. 4, pp. 1903–1925, Aug. 2008, doi: 10.1109/TNS.2008.2000480.
- [12] H. L. Hughes and J. M. Benedetto, “Radiation effects and hardening of MOS technology: devices and circuits,” *IEEE Trans Nucl Sci*, vol. 50, pp. 500–501, Jun. 2003.
- [13] F. Faccio, “Design Hardening Methodologies for ASICs,” in *Radiation Effects on Embedded Systems*, Springer Netherlands, 2007, pp. 143–160. Accessed: Sep. 30, 2014. [Online]. Available: http://link.springer.com/chapter/10.1007/978-1-4020-5646-8_7
- [14] D. Loveless, “Hardening techniques for analog and mixed-signal circuits,” in *2021 IEEE NSREC Short Course*, 2021.
- [15] B. Narasimham, “Hardening techniques for digital circuits,” in *2021 IEEE NSREC Short Course*, 2021.

- [16] J. R. Janesick, *Scientific charge-coupled devices*. Bellingham: SPIE, 2001.
- [17] A. J. P. Theuwissen, *Solid-State Imaging with Charge-Coupled Devices*. Kluwer Academic, 1995.
- [18] S. Bhaskaran, T. Chapman, M. Pilon, and S. VanGorden, “Performance based CID imaging: past, present, and future,” in *Infrared Systems and Photoelectronic Technology III*, 2008, vol. 7055, p. 70550R.
- [19] T. C. Scientific Thermo Fisher, “Charge-Injection Devices Overcome Radiation Effects,” *Photonics*, Dec. 2012. https://www.photonics.com/Articles/Charge-Injection_Devices_Overcome_Radiation/a52489 (accessed May 04, 2021).
- [20] E. R. Fossum, “Active Pixel Sensors: Are CCD’s Dinosaurs?,” *Proc SPIE*, vol. 1900, pp. 1–14, 1993.
- [21] E. R. Fossum, “CMOS image sensors: electronic camera-on-a-chip,” *IEEE Trans Electron Devices*, vol. 44, no. 10, pp. 1689–1698, Oct. 1997.
- [22] A. Theuwissen, “There’s More to the Picture Than Meets the Eye, and in the future it will only become more so,” in *2021 IEEE International Solid- State Circuits Conference (ISSCC)*, Feb. 2021, vol. 64, pp. 30–35. doi: 10.1109/ISSCC42613.2021.9366058.
- [23] H.-S. Wong, Y. L. Yao, and E. S. Schlig, “TDI charge-coupled devices: Design and applications,” *IBM J. Res. Dev.*, vol. 36, no. 1, pp. 83–106, Jan. 1992, doi: 10.1147/rd.361.0083.
- [24] J. F. Johnson, “Modeling imager deterministic and statistical modulation transfer functions,” *Appl. Opt.*, vol. 32, no. 32, pp. 6503–6513, Nov. 1993, doi: 10.1364/AO.32.006503.
- [25] G. Lepage, J. Bogaerts, and G. Meynants, “Time-Delay-Integration Architectures in CMOS Image Sensors,” *IEEE Trans. Electron Devices*, vol. 56, no. 11, pp. 2524–2533, Nov. 2009, doi: 10.1109/TED.2009.2030648.
- [26] F. Mayer *et al.*, “First measurements of true charge transfer TDI (Time Delay Integration) using a standard CMOS technology,” in *International Conference on Space Optics — ICSO 2012*, Nov. 2017, vol. 10564, p. 105640N. doi: 10.1117/12.2309230.
- [27] P. Touron, F. Roy, P. Magnan, O. Marcelot, S. Demiguel, and C. Virmontois, “Capacitive Trench-Based Charge Transfer Device,” *IEEE Electron Device Lett.*, vol. 41, no. 9, pp. 1388–1391, 2020.
- [28] D. Burt *et al.*, “Improving radiation tolerance in e2v CCD sensors,” in *Astronomical and Space Optical Systems*, Aug. 2009, vol. 7439, p. 743902. doi: 10.1117/12.825273.
- [29] K. D. Stefanov *et al.*, “Electron and neutron radiation damage effects on a two-phase CCD,” *IEEE Trans Nucl Sci*, vol. 47, pp. 1280–1291, 2000.
- [30] V. Goiffon *et al.*, “Multi-MGy Radiation Hard CMOS Image Sensor: Design, Characterization and X/Gamma Rays Total Ionizing Dose Tests,” *IEEE Trans. Nucl. Sci.*, vol. 62, no. 6, pp. 2956–2964, Dec. 2015, doi: 10.1109/TNS.2015.2490479.

- [31] V. Goiffon *et al.*, “Total Ionizing Dose Effects on a Radiation-Hardened CMOS Image Sensor Demonstrator for ITER Remote Handling,” *IEEE Trans. Nucl. Sci.*, vol. 65, no. 1, pp. 101–110, Jan. 2018, doi: 10.1109/TNS.2017.2765481.
- [32] P. Jerram, D. Burt, N. Guyatt, V. Hibon, J. Vaillant, and Y. Henrion, “Back-thinned CMOS sensor optimization,” in *Optical Components and Materials VII*, Feb. 2010, vol. 7598, p. 759813. doi: 10.1117/12.852389.
- [33] J. Ma and E. R. Fossum, “Quanta Image Sensor Jot With Sub 0.3e- r.m.s. Read Noise and Photon Counting Capability,” *IEEE Electron Device Lett.*, vol. 36, no. 9, pp. 926–928, Sep. 2015, doi: 10.1109/LED.2015.2456067.
- [34] M.-W. Seo, S. Kawahito, K. Kagawa, and K. Yasutomi, “A 0.27e-rms Read Noise 220- μ V/e-Conversion Gain Reset-Gate-Less CMOS Image Sensor With 0.11- μ m CIS Process,” *IEEE Electron Device Lett.*, vol. 36, no. 12, pp. 1344–1347, Dec. 2015, doi: 10.1109/LED.2015.2496359.
- [35] “2021 O-S-D Report—A Market Analysis and Forecast for the Optoelectronics, Sensors/Actuators, and Discretes.,” IC Insights, 2021.
- [36] “2020 O-S-D Report—A Market Analysis and Forecast for the Optoelectronics, Sensors/Actuators, and Discretes.,” IC Insights, 2020.
- [37] E. R. Fossum, “Camera-on-a-chip: technology transfer from saturn to your cell phone,” *Technol. Innov.*, vol. 15, no. 3, pp. 197–209, Dec. 2013, doi: 10.3727/194982413X13790020921744.
- [38] D. Durini and D. Arutinov, “Operational principles of silicon image sensors,” in *High Performance Silicon Imaging*, Elsevier, 2014, pp. 25–77. Accessed: Jul. 30, 2014. [Online]. Available: <http://www.woodheadpublishingonline.com/content/m37v3226w547mw6u/?p=ece7c9d7eb134b57945266ab297e5f8b&pi=2>
- [39] A. J. P. Theuwissen, “CMOS image sensors: State-of-the-art,” *Solid-State Electron*, vol. 52, no. 9, pp. 1401–1406, Sep. 2008.
- [40] O. Yadid-Pecht and R. Etienne-Cummings, *CMOS Imagers: From Phototransduction to Image Processing*. Springer Science & Business Media, 2004.
- [41] J. Ohta, *Smart CMOS Image Sensors and Applications*. CRC Press, 2007. Accessed: Jul. 30, 2014. [Online]. Available: <http://www.crcpress.com/product/isbn/9780849336812>
- [42] R. J. Gove, “Complementary metal-oxide-semiconductor (CMOS) image sensors for mobile devices,” in *High Performance Silicon Imaging*, Elsevier, 2014, pp. 191–234. Accessed: Jul. 30, 2014. [Online]. Available: <http://www.woodheadpublishingonline.com/content/hr938kw851878223/?p=54c1285aef854e19a57b7f6bce55d17d&pi=0>
- [43] B. Choubey, W. Mughal, and L. Gouveia, “5 - Circuits for high performance complementary metal-oxide-semiconductor (CMOS) image sensors,” in *High Performance Silicon Imaging*, D. Durini, Ed. Woodhead Publishing, 2014, pp. 124–164. Accessed: Sep. 30, 2014. [Online]. Available: <http://www.sciencedirect.com/science/article/pii/B9780857095985500051>

- [44] J. A. Leñero-Bardallo, J. Fernández-Berni, and Á. Rodríguez-Vázquez, “Review of ADCs for imaging,” 2014, vol. 9022, pp. 90220I–90220I–6. doi: 10.1117/12.2041682.
- [45] F. Roy *et al.*, “Fully Depleted, Trench-Pinned Photo Gate for CMOS Image Sensor Applications,” *Sensors*, vol. 20, no. 3, Art. no. 3, Jan. 2020, doi: 10.3390/s20030727.
- [46] N. Teranishi, A. Kohno, Y. Ishihara, E. Oda, and K. Arai, “An interline CCD image sensor with reduced image lag,” *Electron Devices IEEE Trans. On*, vol. 31, no. 12, pp. 1829–1833, Dec. 1984.
- [47] B. C. Burkey *et al.*, “The pinned photodiode for an interline-transfer CCD image sensor,” in *IEDM Tech. Dig.*, 1984, pp. 28–31.
- [48] P. Lee, R. Gee, M. Guidash, T. Lee, and E. R. Fossum, “An active pixel sensor fabricated using CMOS/CCD process technology,” in *Proc. IEEE Workshop on CCDs and Advanced Image Sensors*, 1995, pp. 115–119.
- [49] E. R. Fossum and D. B. Hondongwa, “A Review of the Pinned Photodiode for CCD and CMOS Image Sensors,” *IEEE J Electron Devices Soc.*, 2014, doi: 10.1109/JEDS.2014.2306412.
- [50] G. Casse, “Recent developments on silicon detectors,” *Nucl. Instrum. Methods Phys. Res. Sect. Accel. Spectrometers Detect. Assoc. Equip.*, vol. 732, pp. 16–20, Dec. 2013, doi: 10.1016/j.nima.2013.05.191.
- [51] J. A. Ballin *et al.*, “Monolithic Active Pixel Sensors (MAPS) in a Quadruple Well Technology for Nearly 100% Fill Factor and Full CMOS Pixels,” *Sensors*, vol. 8, no. 9, pp. 5336–5351, Sep. 2008, doi: 10.3390/s8095336.
- [52] S. Zucca, L. Ratti, G. Traversi, F. Morsani, A. Gabrielli, and F. Giorgi, “A quadruple well CMOS MAPS prototype for the Layer0 of the SuperB SVT,” *Nucl. Instrum. Methods Phys. Res. Sect. Accel. Spectrometers Detect. Assoc. Equip.*, vol. 718, pp. 380–382, Aug. 2013, doi: 10.1016/j.nima.2012.12.106.
- [53] A. El Gamal and H. Eltoukhy, “CMOS image sensors,” *IEEE Circuits Devices Mag.*, vol. 21, no. 3, pp. 6–20, May 2005.
- [54] G. R. Hopkinson, T. M. Goodman, and S. R. Prince, *A Guide to the use and calibration of detector array equipment*. SPIE, 2004.
- [55] W. Shockley and W. T. Read, “Statistics of the recombination of holes and electrons,” *Phys Rev*, vol. 87, pp. 835–842, 1952.
- [56] R. N. Hall, “Electron-Hole Recombination in Germanium,” *Phys Rev B*, vol. 87, Jul. 1952.
- [57] A. S. Grove, *Physics and Technology of Semiconductor Devices*. Wiley International, 1967.
- [58] S. W. Benson, *The Foundations of Chemical Kinetics*. McGraw-Hill Education, 1960.
- [59] J.-M. Belloir *et al.*, “Dark current spectroscopy on alpha irradiated pinned photodiode CMOS image sensors,” *IEEE Trans. Nucl. Sci.*, vol. 63, no. 4, pp. 2183–2192, 2016.

- [60] R. D. McGrath, J. Doty, G. Lupino, G. Ricker, and J. Vallerga, “Counting of deep-level traps using a charge-coupled device,” *IEEE Trans. Electron Devices*, vol. 34, no. 12, pp. 2555–2557, 1987.
- [61] W. C. Mccolgin, J. P. Lavine, and C. V. Stancampiano, “Dark current spectroscopy of metals in silicon,” *MRS Online Proc. Libr. OPL*, vol. 442, 1996.
- [62] C. Tivarus and W. C. McColgin, “Dark current spectroscopy of irradiated CCD image sensors,” *IEEE Trans. Nucl. Sci.*, vol. 55, no. 3, pp. 1719–1724, 2008.
- [63] F. Domengie, J. L. Regolini, and D. Bauza, “Study of Metal Contamination in CMOS Image Sensors by Dark-Current and Deep-Level Transient Spectroscopies,” *J. Electron. Mater.*, vol. 39, no. 6, pp. 625–629, Jun. 2010, doi: 10.1007/s11664-010-1212-6.
- [64] E. A. Webster, R. L. Nicol, L. Grant, and D. Renshaw, “Per-pixel dark current spectroscopy measurement and analysis in CMOS image sensors,” *IEEE Trans. Electron Devices*, vol. 57, no. 9, pp. 2176–2182, 2010.
- [65] J.-M. Belloir *et al.*, “Dark Current Spectroscopy in neutron, proton and ion irradiated CMOS Image Sensors: from Point Defects to Clusters,” *IEEE Trans. Nucl. Sci.*, vol. 64, no. 1, pp. 27–37, 2016.
- [66] M. M. Blouke, “Diffusion dark current in CCDs and CMOS image sensors,” in *Sensors, Cameras, and Systems for Industrial/Scientific Applications IX*, Feb. 2008, vol. 6816, p. 68160I. doi: 10.1117/12.787729.
- [67] S. Place, J.-P. Carrere, S. Allegret, P. Magnan, V. Goiffon, and F. Roy, “Radiation Effects on CMOS Image Sensors With Sub-2um Pinned Photodiodes,” *IEEE Trans Nucl Sci*, vol. 59, no. 4, pp. 909–917, Aug. 2012, doi: 10.1109/TNS.2012.2193671.
- [68] V. Goiffon *et al.*, “Identification of Radiation Induced Dark Current Sources in Pinned Photodiode CMOS Image Sensors,” *IEEE Trans Nucl Sci*, vol. 59, no. 4, pp. 918–926, Aug. 2012, doi: 10.1109/TNS.2012.2190422.
- [69] D. K. Schroder, “The concept of generation and recombination lifetimes in semiconductors,” *IEEE Trans. Electron Devices*, vol. 29, no. 8, pp. 1336–1338, 1982.
- [70] G. Vincent, A. Chantre, and D. Bois, “Electric field effect on the thermal emission of traps in semiconductor junctions,” *J Appl Phys*, vol. 50, no. 8, pp. 5484–5487, Aug. 1979.
- [71] M. J. J. Theunissen, “Analysis of the soft reverse characteristics of n⁺p drain diodes,” *Solid-State Electron*, vol. 28, no. 5, pp. 417–425, May 1985.
- [72] G. A. M. Hurkx, H. C. De Graaff, W. J. Kloosterman, and M. P. G. Knuvers, “A new analytical diode model including tunneling and avalanche breakdown,” *IEEE Trans Electron Devices*, vol. 39, no. 9, pp. 2090–2098, Sep. 1992.
- [73] G. A. M. Hurkx, D. B. M. Klaassen, and M. P. G. Knuvers, “A new recombination model for device simulation including tunneling,” *IEEE Trans. Electron Devices*, vol. 39, no. 2, pp. 331–338, 1992.
- [74] A. Poyai, E. Simoen, and C. Claeys, “Impact of a high electric field on the extraction of the generation lifetime from the reverse generation current component of shallow n⁺/p-well diodes,” *IEEE Trans. Electron Devices*, vol. 48, no. 10, pp. 2445–2446, 2001.

- [75] J. R. Srour and R. A. Hartmann, “Enhanced displacement damage effectiveness in irradiated silicon devices,” *IEEE Trans Nucl Sci*, vol. 36, no. 6, pp. 1825–1830, Dec. 1989.
- [76] J. Bogaerts, B. Dierickx, and R. Mertens, “Enhanced Dark Current Generation in Proton-Irradiated CMOS Active Pixel Sensors,” *IEEE Trans Nucl Sci*, vol. 49, no. 3, pp. 1513–1521, Jun. 2002.
- [77] A. Le Roch *et al.*, “Radiation-Induced Leakage Current and Electric Field Enhancement in CMOS Image Sensor Sense Node Floating Diffusions,” *IEEE Trans. Nucl. Sci.*, vol. 66, no. 3, pp. 616–624, Mar. 2019, doi: 10.1109/TNS.2019.2892645.
- [78] G. Meynarts, W. Diels, J. Bogaerts, and W. Ogiers, “Emission Microscopy analysis of hot cluster defects of imagers processed,” presented at the International Image Sensor Workshop (IISW), 2013. Accessed: Oct. 13, 2014. [Online]. Available: http://www.imagesensors.org/Past%20Workshops/2013%20Workshop/2013%20Papers/04-4_059-meynarts2_paper.pdf
- [79] S. Hanna *et al.*, “MCT-Based LWIR and VLWIR 2D Focal Plane Detector Arrays for Low Dark Current Applications at AIM,” *J. Electron. Mater.*, vol. 45, no. 9, pp. 4542–4551, Sep. 2016, doi: 10.1007/s11664-016-4523-4.
- [80] C. Cervera *et al.*, “Low-dark current p-on-n MCT detector in long and very long-wavelength infrared,” in *Infrared Technology and Applications XLI*, Jun. 2015, vol. 9451, p. 945129. doi: 10.1117/12.2179216.
- [81] D. McGrath, S. Tobin, V. Goiffon, P. Magnan, and A. Le Roch, “Dark Current Limiting Mechanisms in CMOS Image Sensors,” *Electron. Imaging*, vol. 2018, no. 11, pp. 354-1-354-8, Jan. 2018, doi: 10.2352/ISSN.2470-1173.2018.11.IMSE-354.
- [82] A. Papoulis and S. U. Pillai, *Probability, random variables, and stochastic processes*, 4th ed. McGrawHill, 2002.
- [83] M. J. Kirton and M. J. Uren, “Noise in solid-state microstructures: A new perspective on individual defects, interface states and low-frequency (1/f) noise,” *Adv Phys*, vol. 38, no. 4, pp. 367–468, 1989.
- [84] Y. Mori, K. Takeda, and R. Yamada, “Random telegraph noise of junction leakage current in submicron devices,” *J. Appl. Phys.*, vol. 107, no. 1, p. 014509, Jan. 2010, doi: 10.1063/1.3268479.
- [85] D. S. Yaney, C. Y. Lu, R. A. Kohler, M. J. Kelly, and J. T. Nelson, “A meta-stable leakage phenomenon in DRAM charge storage - Variable hold time,” in *IEDM Tech. Dig.*, Dec. 1987, pp. 336–339. doi: 10.1109/IEDM.1987.191425.
- [86] P. J. Restle, J. W. Park, and B. F. Lloyd, “DRAM variable retention time,” in *IEDM Tech. Dig.*, Dec. 1992, pp. 807–810. doi: 10.1109/IEDM.1992.307481.
- [87] Y. Mori, K. Ohya, K. Okonogi, and R. -i. Yamada, “The origin of variable retention time in DRAM,” in *IEDM Tech. Dig.*, 2005, pp. 1034–1037. doi: 10.1109/IEDM.2005.1609541.
- [88] J. R. Srour, R. A. Hartmann, and K. S. Kitazaki, “Permanent damage produced by single proton interactions in silicon devices,” *Nucl. Sci. IEEE Trans. On*, vol. 33, no. 6, pp. 1597–1604, 1986.

- [89] P. W. Marshall, C. J. Dale, E. A. Burke, G. P. Summers, and G. E. Bender, “Displacement damage extremes in silicon depletion regions,” *Nucl. Sci. IEEE Trans. On*, vol. 36, no. 6, pp. 1831–1839, Dec. 1989.
- [90] G. R. Hopkinson, “Cobalt60 and proton radiation effects on large format, 2-D, CCD arrays for an Earth imaging application,” *IEEE Trans Nucl Sci*, vol. 39, no. 6, pp. 2018–2025, Dec. 1992.
- [91] I. H. Hopkins and G. R. Hopkinson, “Random Telegraph Signals from Proton-Irradiated CCDs,” *IEEE Trans Nucl Sci*, vol. 40, no. 6, pp. 1567–1574, Dec. 1993.
- [92] I. H. Hopkins and G. R. Hopkinson, “Further Measurements of Random Telegraph Signals in Proton-Irradiated CCDs,” *IEEE Trans Nucl Sci*, vol. 42, no. 6, pp. 2074–2081, 1995.
- [93] A. M. Chugg, R. Jones, M. J. Moutrie, J. R. Armstrong, D. B. S. King, and N. Moreau, “Single particle dark current spikes induced in CCDs by high energy neutrons,” *Nucl. Sci. IEEE Trans. On*, vol. 50, no. 6, pp. 2011–2017, 2003.
- [94] D. R. Smith, A. D. Holland, and I. B. Hutchinson, “Random telegraph signals in charge coupled devices,” *Nucl Instr Meth A*, vol. 530, no. 3, pp. 521–535, Sep. 2004.
- [95] T. Nuns, G. Quadri, J.-P. David, O. Gilard, and N. Boudou, “Measurements of Random Telegraph Signal in CCDs Irradiated With Protons and Neutrons,” *Nucl. Sci. IEEE Trans. On*, vol. 53, no. 4, pp. 1764–1771, Aug. 2006.
- [96] T. Nuns, G. Quadri, J.-P. David, and O. Gilard, “Annealing of Proton-Induced Random Telegraph Signal in CCDs,” *Nucl. Sci. IEEE Trans. On*, vol. 54, no. 4, pp. 1120–1128, 2007.
- [97] G. R. Hopkinson, “Radiation effects in a CMOS active pixel sensor,” *IEEE Trans Nucl Sci*, vol. 47, no. 6, pp. 2480–2484, Dec. 2000.
- [98] G. R. Hopkinson, V. Goiffon, and A. Mohammadzadeh, “Random telegraph signals in proton irradiated CCDs and APS,” *IEEE Trans Nucl Sci*, vol. 55, no. 4, Aug. 2008.
- [99] J.Bogaerts, B.Dierickx, and R.Mertens, “Random Telegraph Signals in a Radiation-Hardened CMOS Active Pixel Sensors,” *IEEE Trans Nucl Sci*, vol. 49, pp. 249–257, 2002.
- [100] M. Deveaux *et al.*, “Random telegraph signal in monolithic active pixel sensors,” in *Nuclear Science Symposium Conference Record*, 2008, pp. 3098–3105. Accessed: Sep. 29, 2014. [Online]. Available: http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=4775010
- [101] V. Goiffon, G. R. Hopkinson, P. Magnan, F. Bernard, G. Rolland, and O. Saint-Pe, “Multilevel RTS in Proton Irradiated CMOS Image Sensors Manufactured in a Deep Submicron Technology,” *IEEE Trans Nucl Sci*, vol. 56, no. 4, pp. 2132–2141, Aug. 2009.
- [102] M. A. Karami, C. Niclass, and E. Charbon, “Random telegraph signal in single-photon avalanche diodes,” 2009.
- [103] M. A. Karami, L. Carrara, C. Niclass, M. Fishburn, and E. Charbon, “RTS noise characterization in single-photon avalanche diodes,” *IEEE Electron Device Lett.*, vol. 31, no. 7, pp. 692–694, 2010.

- [104] F. Di Capua *et al.*, “Random telegraph signal in proton irradiated single-photon avalanche diodes,” *IEEE Trans. Nucl. Sci.*, vol. 65, no. 8, pp. 1654–1660, 2018.
- [105] D. Fiore, M. Campajola, C. Nappi, E. Sarnelli, and F. Di Capua, “Random Telegraph Signal Investigation in Different CMOS SPAD Layouts,” in *2018 IEEE Nuclear Science Symposium and Medical Imaging Conference Proceedings (NSS/MIC)*, 2018, pp. 1–4.
- [106] A. Brunner *et al.*, “Improvement of RTS noise in HgCdTe MWIR detectors,” *J. Electron. Mater.*, vol. 43, no. 8, pp. 3060–3064, 2014.
- [107] C. Virmontois *et al.*, “Dark Current Random Telegraph Signals in Solid-State Image Sensors,” *IEEE Trans Nucl Sci*, vol. 60, no. 6, Dec. 2013.
- [108] C. Durnez, V. Goiffon, C. Virmontois, P. Magnan, and L. Rubaldo, “Comparison of Dark Current Random Telegraph Signals in Silicon and InSb-Based Photodetector Pixel Arrays,” *IEEE Trans. Electron Devices*, vol. 67, no. 11, pp. 4940–4946, 2020.
- [109] V. Goiffon, P. Magnan, P. Martin-Gonthier, C. Virmontois, and M. Gaillardin, “Evidence of a Novel Source of Random Telegraph Signal in CMOS Image Sensors,” *IEEE Electron Device Lett.*, vol. 32, no. 6, pp. 773–775, Jun. 2011.
- [110] C. Virmontois *et al.*, “Total Ionizing Dose Versus Displacement Damage Dose Induced Dark Current Random Telegraph Signals in CMOS Image Sensors,” *IEEE Trans. Nucl. Sci.*, vol. 58, no. 6, pp. 3085–3094, Dec. 2011, doi: 10.1109/TNS.2011.2171005.
- [111] V. Goiffon, C. Virmontois, and P. Magnan, “Investigation of Dark Current Random Telegraph Signal in Pinned PhotoDiode CMOS Image Sensors,” in *IEDM Tech. Dig.*, Dec. 2011, p. 8.4.1-8.4.4.
- [112] V. Goiffon *et al.*, “Radiation Effects in Pinned Photodiode CMOS Image Sensors: Pixel Performance Degradation Due to Total Ionizing Dose,” *IEEE Trans Nucl Sci*, vol. 59, no. 6, pp. 2878–2887, Dec. 2012, doi: 10.1109/TNS.2012.2222927.
- [113] E. Martin, T. Nuns, C. Virmontois, J.-P. David, and O. Gilard, “Proton and -Rays Irradiation-Induced Dark Current Random Telegraph Signal in a 0.18- CMOS Image Sensor,” *IEEE Trans. Nucl. Sci.*, vol. 60, no. 4, pp. 2503–2510, Aug. 2013, doi: 10.1109/TNS.2013.2251662.
- [114] C. Y.-P. Chao *et al.*, “Random telegraph noises in CMOS image sensors caused by variable gate-induced sense node leakage due to X-ray irradiation,” *IEEE J. Electron Devices Soc.*, vol. 7, pp. 227–238, 2019.
- [115] C. Y.-P. Chao *et al.*, “Random Telegraph Noises from the Source Follower, the Photodiode Dark Current, and the Gate-Induced Sense Node Leakage in CMOS Image Sensors,” *Sensors*, vol. 19, no. 24, p. 5447, 2019.
- [116] C. Y.-P. Chao *et al.*, “Identifying the sources of random telegraph noises in pixels of CMOS image sensor,” in *Proceedings of the 2019 International Image Sensor Workshop (IISW), Snowbird, UT, USA*, 2019, pp. 24–27.
- [117] C. Durnez, V. Goiffon, C. Virmontois, J.-M. Belloir, P. Magnan, and L. Rubaldo, “In-depth analysis on radiation induced multi-level dark current random telegraph signal in silicon solid state image sensors,” *IEEE Trans. Nucl. Sci.*, vol. 64, no. 1, pp. 19–26, 2016.

- [118] V. Goiffon *et al.*, “Radiation-Induced Variable Retention Time in Dynamic Random Access Memories,” *IEEE Trans. Nucl. Sci.*, vol. 67, no. 1, pp. 234–244, Jan. 2020, doi: 10.1109/TNS.2019.2956293.
- [119] A. Jay *et al.*, “Simulation of Single Particle Displacement Damage in Silicon—Part II: Generation and Long-Time Relaxation of Damage Structure,” *IEEE Trans. Nucl. Sci.*, vol. 64, no. 1, pp. 141–148, Jan. 2017, doi: 10.1109/TNS.2016.2628089.
- [120] C. Leyris, F. Martinez, M. Valenza, A. Hoffmann, J.C. Vildeuil, and F. Roy, “Impact of Random Telegraph Signal in CMOS Image Sensors for Low-Light Levels,” in *Proc. ESSCIRC*, 2006, pp. 376–379.
- [121] X. Wang, P. R. Rao, A. Mierop, and A. J. P. Theuwissen, “Random Telegraph Signal in CMOS Image Sensor Pixels,” in *IEDM Tech. Dig.*, 2006, pp. 1–4.
- [122] R.-V. Wang, Y.-H. Lee, Y.-L. R. Lu, W. McMahon, S. Hu, and A. Ghetti, “Shallow Trench Isolation Edge Effect on Random Telegraph Signal Noise and Implications for Flash Memory,” *IEEE Trans. Electron Devices*, vol. 56, no. 9, pp. 2107–2113, Sep. 2009, doi: 10.1109/TED.2009.2026116.
- [123] R. Fontaine, “Trends in Consumer CMOS Image Sensor Manufacturing,” 2009.
- [124] R. Fontaine, “A Review of the 1.4 um Pixel Generation,” 2011.
- [125] R. Fontaine, “The Evolution of Pixel Structures for Consumer-Grade Image Sensors,” *IEEE Trans. Semicond. Manuf.*, vol. 26, no. 1, pp. 11–16, Feb. 2013, doi: 10.1109/TSM.2012.2237187.
- [126] A. Lahav, A. Fenigstein, and A. Strum, “Backside illuminated (BSI) complementary metal-oxide-semiconductor (CMOS) image sensors,” in *High Performance Silicon Imaging*, Elsevier, 2014, pp. 98–123. Accessed: Jul. 30, 2014. [Online]. Available: <http://www.woodheadpublishingonline.com/content/v7q338g01gp14210/?p=a3d097e7cae d452c98eebe27d9bf92df&pi=0>
- [127] S. Wolf, *Silicon Processing for the VLSI Era, Volume 4: Deep-submicron process technology*, vol. 4. California: Lattice Press, 2002.
- [128] J. Gambino *et al.*, “CMOS Imager with Copper Wiring and Lightpipe,” in *IEDM Tech. Dig.*, Dec. 2006, pp. 1–4. doi: 10.1109/IEDM.2006.346977.
- [129] G. Agranov *et al.*, “Pixel continues to shrink, pixel development for novel CMOS image sensors,” in *Proceedings of the 2009 International Image Sensor Workshop*, 2009, pp. 58–61. Accessed: Sep. 22, 2014. [Online]. Available: http://www.imagesensors.org/Past%20Workshops/2009%20Workshop/2009%20Papers/01 6_paper_agranov_aptina_smallpix.pdf
- [130] B. J. Park *et al.*, “Deep Trench Isolation for Crosstalk Suppression in Active Pixel Sensors with 1.7 μm Pixel Pitch,” *Jpn. J. Appl. Phys.*, vol. 46, no. 4S, p. 2454, Apr. 2007, doi: 10.1143/JJAP.46.2454.
- [131] B. Pain, “Backside Illumination Technology For SOI-CMOS Image Sensors,” Jun. 2009.
- [132] S. Wuu, “BSI technology with bulk Si wafer,” Jun. 2009.

- [133] H. Rhodes, “Mass production of BSI image sensors: performance results,” Jun. 2009.
- [134] V. Koifman, “Omnivision to Announce 0.61um Pixel Sensor,” *Image Sensors World*, May 10, 2021. <http://image-sensors-world.blogspot.com/2021/05/omnivision-to-announce-061um-pixel.html> (accessed May 10, 2021).
- [135] J. Park *et al.*, “7.9 1/2.74-inch 32Mpixel-Prototype CMOS Image Sensor with 0.64 μ m Unit Pixels Separated by Full-Depth Deep-Trench Isolation,” in *2021 IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2021, vol. 64, pp. 122–124. doi: 10.1109/ISSCC42613.2021.9365751.
- [136] R. Fontaine, “The state-of-the-art of mainstream CMOS image sensors,” in *Proceedings of the International Image Sensors Workshop*, 2015, pp. 6–12.
- [137] R. Fontaine, “A Survey of Enabling Technologies in Successful Consumer Digital Imaging Products - Recherche Google,” presented at the IISW 2017, 2017.
- [138] R. Fontaine, “The State-of-the-Art of Smartphone Imagers - Recherche Google,” presented at the IISW, 2019.
- [139] J. Michelot *et al.*, “Back illuminated vertically pinned photodiode with in depth charge storage,” in *Proc. IISW*, 2011, p. R08.
- [140] J. Ahn *et al.*, “7.1 A 1/4-inch 8Mpixel CMOS image sensor with 3D backside-illuminated 1.12 μ m pixel with front-side deep-trench isolation and vertical transfer gate,” in *ISSCC Tech. Dig.*, Feb. 2014, pp. 124–125. doi: 10.1109/ISSCC.2014.6757365.
- [141] N. Ahmed *et al.*, “MOS capacitor deep trench isolation for CMOS image sensors,” in *2014 IEEE international electron devices meeting*, 2014, pp. 4–1.
- [142] A. Theuwissen, “There’s More to the Picture Than Meets the Eye (and in the future, it will become only much more),” presented at the ISSCC 2021, Feb. 2021. [Online]. Available: <https://youtu.be/TDYqIJFREQ4>
- [143] “International Roadmap for Devices and Systems (IRDS) 2020 Edition - IEEE IRDS,” 2020. Accessed: May 23, 2021. [Online]. Available: <https://irds.ieee.org/editions/2020>
- [144] Y. Sacchettini, J.-P. Carrère, R. Duru, J.-P. Oddou, V. Goiffon, and P. Magnan, “CMOS Image Sensors and Plasma Processes: How PMD Nitride Charging Acts on the Dark Current,” *Sensors*, vol. 19, no. 24, Art. no. 24, Jan. 2019, doi: 10.3390/s19245534.
- [145] A. Lomako and B. Delodder, “Dynamic X-ray Imaging: A Second Look, a New Diagnosis,” Sep. 24, 2014. <https://possibility.teledyneimaging.com/new-diagnosis-dynamic-x-ray-imaging/> (accessed May 23, 2021).
- [146] D. Contarato, P. Denes, D. Doering, J. Joseph, and B. Krieger, “High Speed, Radiation Hard CMOS Pixel Sensors for Transmission Electron Microscopy,” *Phys. Procedia*, vol. 37, pp. 1504–1510, 2012, doi: 10.1016/j.phpro.2012.04.103.
- [147] V. Goiffon *et al.*, “CAMRAD: Development of a multi-megagray radiation hard CMOS camera for dismantling operations,” presented at the Dismantling Challenges: Industrial Reality, Prospects and Feedback Experience (DEM 2018), Avignon, France, Oct. 2018.

- [148] F. Faccio *et al.*, “Influence of LDD Spacers and H+ Transport on the Total-Ionizing-Dose Response of 65-nm MOSFETs Irradiated to Ultrahigh Doses,” *IEEE Trans. Nucl. Sci.*, vol. 65, no. 1, pp. 164–174, Jan. 2018, doi: 10.1109/TNS.2017.2760629.
- [149] S. Burger, E. Bravin, and G. Trad, “Irradiation test of Commercial (BASLER) digital cameras @ CHARM,” presented at the CERN RADWG Meeting, Apr. 13, 2017.
- [150] E. Simova and P. Rochefort, *Ionizing Radiation Effects in Non-Radiation-Tolerant Commercial Video Cameras*. 2015. doi: 10.1109/REDW.2015.7336719.
- [151] B. R. Hancock and G. A. Soli, “Total dose testing of a CMOS charged particle spectrometer,” *IEEE Trans Nucl Sci*, vol. 44, no. 6, pp. 1957–1964, Dec. 1997.
- [152] B. R. Hancock *et al.*, “Multi-megarad (Si) radiation-tolerant integrated CMOS imager,” in *Proc. SPIE*, 2001, vol. 4306, pp. 147–155.
- [153] B. Pain *et al.*, “Hardening CMOS imagers: radhard-by-design or radhard-by-foundry,” in *Proc. SPIE*, San Diego, CA, USA, 2004, vol. 5167, pp. 101–110.
- [154] V. Goiffon, P. Magnan, O. Saint-Pé, Frederic Bernard, and G. Rolland, “Total Dose Evaluation of Deep Submicron CMOS Imaging Technology Through Elementary Device and Pixel Array Behavior Analysis,” *IEEE Trans Nucl Sci*, vol. 55, no. 6, pp. 3494–3501, Dec. 2008.
- [155] V. Goiffon, C. Virmontois, P. Magnan, S. Girard, and P. Paillet, “Analysis of Total Dose Induced Dark Current in CMOS Image Sensors from Interface State and Trapped Charge Density Measurements,” *IEEE Trans Nucl Sci*, vol. 57, no. 6, pp. 3087–3094, Dec. 2010.
- [156] Vincent Goiffon, “Radiation Effects on CMOS Active Pixel Image Sensors,” in *Ionizing Radiation Effects in Electronics*, CRC Press, 2015, pp. 295–332. [Online]. Available: <http://dx.doi.org/10.1201/b19223-12>
- [157] G. Meynants *et al.*, “A 47 MPixel 36.4 x 27.6 mm² 30 fps Global Shutter Image Sensor,” in *Proc. Int. Image Sensor Workshop*, 2017, pp. 410–413.
- [158] C. Friedman, A. Arbel, and R. Ginosar, “Current skimming-based CMOS readout architectures for Quantum Well Infrared Photodetectors,” 1999.
- [159] V. Goiffon *et al.*, “Radiation Hardening of Digital Color CMOS Camera-on-a-Chip Building Blocks for Multi-MGy Total Ionizing Dose Environments,” *IEEE Trans. Nucl. Sci.*, vol. 64, no. 1, pp. 45–53, Jan. 2017, doi: 10.1109/TNS.2016.2636566.
- [160] J. M. Armani, P. Barrochin, F. Joffre, R. Gaillard, F. Saigne, and J. L. Mainguy, “Enhancement of the total dose tolerance of a commercial CMOS active pixel sensor by use of thermal annealing,” in *Proc. RADECS*, Sep. 2011, pp. 340–344. doi: 10.1109/RADECS.2011.6131409.
- [161] V. Goiffon, P. Cervantes, C. Virmontois, F. Corbiere, P. Magnan, and M. Etribeau, “Generic Radiation Hardened Photodiode Layouts for Deep Submicron CMOS Image Sensor Processes,” *IEEE Trans Nucl Sci*, vol. 58, no. 6, pp. 3076–3084, Dec. 2011.
- [162] W. Dulinski, G. Deptuch, Yu. Gornushkin, P. Jalocha, J.-L. Riester, and M. Winter, “Radiation hardness study of an APS CMOS particle tracker,” in *IEEE Nucl. Sci. Symp. Conf. Rec.*, Nov. 2001, vol. 1, pp. 100–103.

- [163] V. Goiffon, M. Estribeau, and P. Magnan, “Overview of Ionizing Radiation Effects in Image Sensors Fabricated in a Deep-Submicrometer CMOS Imaging Technology,” *IEEE Trans Electron Devices*, vol. 56, no. 11, pp. 2594–2601, Nov. 2009.
- [164] M. A. Szelezniak *et al.*, “Small-Scale Readout System Prototype for the STAR PIXEL Detector,” *IEEE Trans Nucl Sci*, vol. 55, no. 6, pp. 3665–3672, Dec. 2008.
- [165] M. Battaglia *et al.*, “A rad-hard CMOS active pixel sensor for electron microscopy,” *Nucl Instr Meth A*, vol. 598, no. 2, pp. 642–649, Jan. 2009.
- [166] A. S. Grove and D. J. Fitzgerald, “Surface effects on p-n junctions: Characteristics of surface space-charge regions under non-equilibrium conditions,” *Solid-State Electron*, vol. 9, no. 8, pp. 783–806, Aug. 1966.
- [167] T. Y. Chan, J. Chen, P. K. Ko, and C. Hu, “The impact of gate-induced drain leakage current on MOSFET scaling,” in *IEDM Tech. Dig.*, 1987, vol. 33, pp. 718–721.
- [168] S. Rizzolo *et al.*, “Radiation hardness comparison of CMOS image sensor technologies at high total ionizing dose levels,” *IEEE Trans. Nucl. Sci.*, vol. 66, no. 1, pp. 111–119, 2018.
- [169] T.-H. Lee, R. M. Guidash, and P. P. Lee, “Partially pinned photodiode for solid state image sensors,” US6051447A, Apr. 18, 2000 Accessed: Jun. 01, 2021. [Online]. Available: <https://patents.google.com/patent/US6051447/en?oq=US+patent+9164968>
- [170] A. Lahav, R. Reshef, and A. Fenigstein, “Enhanced X-ray CMOS sensor panel for radio and fluoro application using a low noise charge amplifier wixel with a partially pinned PD,” in *Proc. Int. Image Sensor Workshop (IISW)*, 2011, pp. 1–4.
- [171] S. Rizzolo *et al.*, *Partially Pinned Photodiode Performances for Emerging Space and Nuclear Applications*, IISW2019_Proceeding, 2019.
- [172] J. Bogaerts, B. Dierickx, G. Meynants, and D. Uwaerts, “Total dose and displacement damage effects in a radiation-hardened CMOS APS,” *IEEE Trans Electron Devices*, vol. 50, no. 1, pp. 84–90, Jan. 2003.
- [173] T. Watanabe, T. Takeuchi, O. Ozawa, H. Komanome, T. Akahori, and K. Tsuchiya, “A Radiation-Hardened CMOS Image Sensor With Pixels Exhibiting a Negligibly Small Dark-Level Increase During Ionizing Radiation,” *IEEE Trans. Nucl. Sci.*, vol. 67, no. 8, pp. 1835–1845, 2020.
- [174] V. Goiffon, M. Estribeau, P. Cervantes, R. Molina, M. Gaillardin, and P. Magnan, “Influence of Transfer Gate Design and Bias on the Radiation Hardness of Pinned Photodiode CMOS Image Sensors,” *IEEE Trans Nucl Sci*, vol. 61, no. 6, Dec. 2014.
- [175] S. Rizzolo *et al.*, “Total-ionizing dose effects on charge transfer efficiency and image lag in pinned photodiode CMOS image sensors,” *IEEE Trans. Nucl. Sci.*, vol. 65, no. 1, pp. 84–91, 2017.
- [176] J.-M. Belloir *et al.*, “Dark current blooming in pinned photodiode CMOS image sensors,” *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 1161–1166, 2017.
- [177] P. R. Rao, X. Wang, and A. J. P. Theuwissen, “Degradation of CMOS image sensors in deep-submicron technology due to γ -irradiation,” *Solid-State Electron*, vol. 52, no. 9, pp. 1407–1413, Sep. 2008.

- [178] O. Marcelot, V. Goiffon, and P. Magnan, “Exploration of Pinned Photodiode Radiation Hardening Solutions Through TCAD Simulations,” *IEEE Trans. Electron Devices*, vol. 66, no. 8, pp. 3411–3416, 2019.
- [179] S. Place, J.-P. Carrere, P. Magnan, V. Goiffon, and F. Roy, “Rad Tolerant CMOS Image Sensor Based on Hole Collection 4T Pixel Pinned Photodiode,” *IEEE Trans Nucl Sci*, vol. 59, no. 6, Dec. 2012.
- [180] E. Stevens *et al.*, “Low-Crosstalk and Low-Dark-Current CMOS Image-Sensor Technology Using a Hole-Based Detector,” in *ISSCC Tech. Dig.*, Feb. 2008, pp. 60–595. doi: 10.1109/ISSCC.2008.4523056.
- [181] B. Mamdy, G.-N. Lu, and F. Roy, “P-type BSI image sensor with active deep trench interface passivation for radiation-hardened imaging systems,” *Procedia Eng.*, vol. 168, pp. 176–180, 2016.
- [182] M. Innocent, “A radiation tolerant 4T pixel for space applications,” in *Proc. Int. Image Sensor Workshop (IISW)*, 2009.
- [183] B. Pain, G. Yang, M. Ortiz, C. Wrigley, B. Hancock, and T. Cunningham, “Analysis and Enhancement of Low-Light-Level Performance Photodiode-Type CMOS Active Pixel Imagers Operated with Sub-Threshold Reset,” 1999.
- [184] F. Faccio and G. Cervelli, “Radiation-induced edge effects in deep submicron CMOS transistors,” *IEEE Trans Nucl Sci*, vol. 52, no. 6, pp. 2413–2420, Dec. 2005.
- [185] J. R. Srour and D. H. Lo, “Universal damage factor for radiation induced dark current in silicon devices.,” *IEEE Trans Nucl Sci*, vol. 47, no. 6, pp. 2451–2459, Dec. 2000.
- [186] J.-M. Belloir *et al.*, “Pixel pitch and particle energy influence on the dark current distribution of neutron irradiated CMOS image sensors,” *Opt. Express*, vol. 24, no. 4, pp. 4299–4315, 2016.
- [187] C. Virmontois *et al.*, “Similarities Between Proton and Neutron Induced Dark Current Distribution in CMOS Image Sensors,” *IEEE Trans. Nucl. Sci.*, vol. 59, no. 4, pp. 927–936, Aug. 2012, doi: 10.1109/TNS.2012.2203317.
- [188] C. Virmontois *et al.*, “Displacement Damage Effects Due to Neutron and Proton Irradiations on CMOS Image Sensors Manufactured in Deep Sub-Micron Technology,” *IEEE Trans Nucl Sci*, vol. 57, no. 6, Dec. 2010.
- [189] M. S. Robbins and L. Gomez Rojas, “An Assessment of the Bias Dependence of Displacement Damage Effects and Annealing in Silicon Charge Coupled Devices,” *IEEE Trans. Nucl. Sci.*, vol. 60, no. 6, pp. 4332–4340, Dec. 2013, doi: 10.1109/TNS.2013.2287255.
- [190] B. Liu *et al.*, “Study of dark current random telegraph signal in proton-irradiated backside illuminated CMOS image sensors,” *Results Phys.*, vol. 19, p. 103443, Dec. 2020, doi: 10.1016/j.rinp.2020.103443.
- [191] C. Duriez *et al.*, “Total ionizing dose radiation-induced dark current random telegraph signal in pinned photodiode CMOS image sensors,” *IEEE Trans. Nucl. Sci.*, vol. 65, no. 1, pp. 92–100, 2017.

- [192] X. Cao *et al.*, “Design and optimisation of large 4T pixel,” in *Proc. Int. Image Sensor Workshop (IISW)*, 2015, pp. 112–115.
- [193] J.-M. Belloir *et al.*, “Radiation effects in pinned photodiode CMOS image sensors: Variation of photodiode implant dose,” *IEEE Trans. Nucl. Sci.*, vol. 66, no. 7, pp. 1671–1681, 2019.
- [194] M. Innocent, “A Radiation Tolerant 4T pixel for Space Applications: Layout and Process Optimization,” in *Proc. Int. Image Sensor Workshop (IISW)*, 2013.
- [195] Bart Dierickx, “Radiation hard design in CMOS image sensors,” presented at the CPIX Workshop, Bonn, Sep. 2014. [Online]. Available: http://www.caeleste.com/caeleste_publications/2014cpix/20140916_cpix_presentation.pdf
- [196] M. Baze, “Single Event Effects in Digital and Linear ICs,” 2011.
- [197] P. Vu, B. Fowler, B. Rodricks, J. Balicki, S. Mims, and W. Li, “Evaluation of 10MeV Proton Irradiation on 5.5 Mpixel Scientific CMOS Image Sensor,” in *Proc. SPIE*, 2010, vol. 7826.
- [198] V. Goiffon *et al.*, “Vulnerability of CMOS image sensors in megajoule class laser harsh environment,” *Opt. Express*, vol. 20, no. 18, pp. 20028–20042, Aug. 2012, doi: 10.1364/OE.20.020028.
- [199] R. R. Troutman, “Latchup in CMOS technology: the problem and its cure,” 1986.
- [200] N. A. Dodds, “Single event latchup: hardening strategies, triggering mechanisms, and testing considerations,” PhD Thesis, 2012.
- [201] V. Lalucaa, V. Goiffon, P. Magnan, Cedric Virmontois, G. Rolland, and S. Petit, “Single Event Effects in 4T Pinned Photodiode Image Sensors,” *IEEE Trans Nucl Sci*, vol. 60, no. 6, Dec. 2013.
- [202] C. Virmontois *et al.*, “Radiation-Induced Dose and Single Event Effects on Digital CMOS Image Sensors,” *IEEE Trans Nucl Sci*, vol. 61, no. 6, Dec. 2014.
- [203] V. Lalucaa, V. Goiffon, P. Magnan, G. Rolland, and S. Petit, “Single-Event Effects in CMOS Image Sensors,” *IEEE Trans. Nucl. Sci.*, vol. 60, no. 4, pp. 2494–2502, Aug. 2013, doi: 10.1109/TNS.2013.2260355.
- [204] M. Beaumel, D. Hervé, D. Van Aken, P. Pourrouquet, and M. Poizat, “Proton, Electron, and Heavy Ion Single Event Effects on the HAS2 CMOS Image Sensor,” *IEEE Trans. Nucl. Sci.*, vol. 61, no. 4, pp. 1909–1917, Aug. 2014, doi: 10.1109/TNS.2014.2307759.
- [205] L. Gomez Rojas, M. Chang, G. Hopkinson, and L. Duvet, “Radiation effects in the LUPA4000 CMOS image sensor for space applications,” in *Proc. RADECS*, Sep. 2011, pp. 800–805. doi: 10.1109/RADECS.2011.6131324.
- [206] F. Kastensmidt, “SEE mitigation strategies for digital circuit design applicable to ASIC and FPGAs,” in Short Course of the Nuclear and Space Radiation Effects Conference (NSREC), 2007.

- [207] T. S. Lomheim *et al.*, “Imaging charge-coupled device (CCD) transient response to 17 and 50 MeV proton and heavy-ion irradiation,” *IEEE Trans. Nucl. Sci.*, vol. 37, no. 6, pp. 1876–1885, Dec. 1990, doi: 10.1109/23.101204.
- [208] C. J. Marshall *et al.*, “Heavy ion transient characterization of a hardened-by-design active pixel sensor array,” in *2002 IEEE Radiation Effects Data Workshop*, 2002, pp. 187–193. doi: 10.1109/REDW.2002.1045552.
- [209] J. Baggio, M. Martinez, C. D’hoose, and O. Musseau, “Analysis of transient effects induced by neutrons on a CCD image sensor,” 2002, vol. 4547, pp. 105–115. doi: 10.1117/12.454383.
- [210] J. C. Pickel *et al.*, “Radiation-induced charge collection in infrared detector arrays,” *IEEE Trans. Nucl. Sci.*, vol. 49, no. 6, pp. 2822–2829, Dec. 2002, doi: 10.1109/TNS.2002.805382.
- [211] M. Raine *et al.*, “Modeling Approach for the Prediction of Transient and Permanent Degradations of Image Sensors in Complex Radiation Environments,” *IEEE Trans. Nucl. Sci.*, vol. 60, no. 6, Dec. 2013.
- [212] G. Rolland, L. Pinheiro da Silva, C. Inguimbert, J.-P. David, R. Ecoffet, and M. Auvergne, “STARDUST: A Code for the Simulation of Particle Tracks on Arrays of Sensitive Volumes With Substrate Diffusion Currents,” *IEEE Trans. Nucl. Sci.*, vol. 55, no. 4, pp. 2070–2078, Aug. 2008, doi: 10.1109/TNS.2008.920427.
- [213] L. Ratti *et al.*, “Modeling Charge Loss in CMOS MAPS Exposed to Non-Ionizing Radiation,” *IEEE Trans. Nucl. Sci.*, vol. 60, no. 4, pp. 2574–2582, Aug. 2013, doi: 10.1109/TNS.2013.2248383.
- [214] G. J. Yates and B. T. Turko, “Circumvention of radiation-induced noise in CCD and CID imagers,” *IEEE Trans. Nucl. Sci.*, vol. 36, no. 6, pp. 2214–2222, Dec. 1989, doi: 10.1109/23.45427.
- [215] V. Goiffon *et al.*, “Mitigation technique for use of CMOS image sensors in megajoule class laser radiative environment,” *Electron. Lett.*, vol. 48, no. 21, p. 1338, 2012, doi: 10.1049/el.2012.2667.
- [216] A. H. Johnston, “The influence of VLSI technology evolution on radiation-induced latchup in space systems,” *IEEE Trans. Nucl. Sci.*, vol. 43, no. 2, pp. 505–521, 1996.
- [217] E. Butz, “Macroscopic effects of radiation on silicon detectors,” presented at the VIII International Course “Detectors and Electronics for High Energy Physics, Astrophysics, Space and Medical Applications, Legnaro, Apr. 2019.
- [218] L. Ratti *et al.*, “Dark count rate degradation in CMOS SPADs exposed to X-rays and neutrons,” *IEEE Trans. Nucl. Sci.*, vol. 66, no. 2, pp. 567–574, 2019.



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**System Mitigation
Strategies
What Could Go Wrong
and How to Make it
Right?**

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Thank You!

- To Raytheon for supporting my work on the short course.
- To Alex St. Claire for the accelerated review of the contents.
- For the years of collaboration and support from the Radiation Effects community and the IEEE; they have helped solve real system problems!
- To Marta Bagatin for her support on development of this material.
- To previous IEEE NSREC short course instructors; they have done a tremendous job educating the space community on radiation issues.



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 - Classifications/system types impacted
 - Orbits
 - Spacecraft environments
- Radiation Impact on Satellite Subsystems
 - Spacecraft charging
 - Ionizing radiation & displacement damage requirements
 - A special word about SEL and destructive effects
- How to Make it Right? Mitigation Strategies
 - Operational strategies
 - Digital systems with flexible platforms
 - Power systems
 - Conclusions



The exhaust plume from space shuttle Atlantis is seen as it launches from pad 39A on Friday, July 8, 2011, at NASA's Kennedy Space Center in Cape Canaveral, Fla. Original from NASA. Digitally enhanced by rawpixel.



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My introduction to anomalies started early in my career when I had an amplifier that acted as an oscillator. The first thing we learn regarding anomalies often occurs during school, and that is that “ideal” models are not reality. The real world reveals circuit sensitivities that you have to figure out as part of the design process. The limits of engineering includes this reality check and that will be what teaches us (if we are open to this). This talk starts with an understanding of the kinds of anomalies that have occurred in space. This will give a sense of why we have to think about radiation effects; there are real consequences if we do not. From a background of what could go wrong, we will delve into mission types, including orbits and environments, the radiation impacts observed based on those orbits, damaging effects, and mitigation strategy considerations for (more) robust systems.

What Could Go Wrong?

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- The Space Era started in 1957 From IEEE 2011 NSREC Short Course, R. Ecoffet, P288
 - Sputnik launched 4 October 1957 starting the Space Race
 - Van Allen Belts were discovered in 1958 using detectors built by Van Allen and his students (Geiger counter attached to a tape recorder)
 - The inner belt was discovered by the US's Explorer 1 satellite launched Jan 31, 1958
 - The outer belt was discovered later in 1958
 - The detector actually failed when the counter saturated and undercounted the expected number of galactic cosmic rays
 - Trajectory calculations were done by hand by this group of women. JPL used the term "computer" to refer to a person rather than a machine.



http://www.nasa.gov/mission_pages/explorer/computers.html

https://en.wikipedia.org/wiki/James_Van_Allen

Detector built by students at the State University of Iowa



Bill Pickering (JPL)
James Van Allen
Werner Von Braun

Knowledge of the space environment was due to space exploration and the environment caused an anomaly...



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When the US launched Explorer I on January 31, 1958, the intention of the mission was to measure Galactic Cosmic Rays which had previously been studied in ground and in high altitude balloon experiments. Initially the counters were registering rates a thousand times higher than expected. As the instrument moved higher in its trajectory, the count ceased. This was our first glimpse into the existence of trapped particle belts and this was experienced as an anomaly – an unexpected result.

As a side note: history files included a note that women calculated the mission trajectory by hand. I could not find their names. When I started in space engineering, 4% of the technical population were women. Today we are running about 20%.

Hughes Satellite Anomaly 1972

- In 1972, a Hughes satellite experienced an upset where the communication with the satellite was lost for 96 seconds and then recaptured.
 - Other anomalies were attributed to charge buildup due to the energetic plasmas
 - Characteristics of the anomaly (not reported) lead to an investigation of other possible anomaly causes
- Scientists Dr. Edward C. Smith, Al Holman, and Dr. Dan Binder proposed a different possible root cause and explained the anomaly as a single-event upset (SEU)
 - They published the first NSREC SEU paper, “SATELLITE ANOMALIES FROM GALACTIC COSMIC RAYS” in the IEEE TNS in 1975.
 - Cocktail trivia: They used a 30 keV scanning electron microscope to identify sensitive areas on the JK Flip Flop that could cause circuit reactions that matched the anomaly
 - First “SEU” paper was written in 1962 and was assessing scaling effects on microelectronics and upset at terrestrial altitudes

https://en.wikipedia.org/wiki/Single-event_upset
 SATELLITE ANOMALIES FROM GALACTIC COSMIC RAYS, TNS 1975, Binder, P. 2675

Basic Mechanisms and Modeling of Single-Event Upset in Digital
 Microelectronics TNS2003 Dodd & Massengill, P. 583



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One of the big performance parameters for satellites involves “availability”. The loss of a communication satellite for any period is considered extremely critical since no satellite customer wants an interruption of service. They don’t get paid!

When the engineers and scientists examined the anomaly, they could not make the symptoms match that of the consequence of charge buildup in the spacecraft so they sought other explanations.

The first Transactions on Nuclear Science paper in 1975 did not use the term single event upset. That description was not used in TNS publications until 1979. Interestingly, this paper was heavily discussed during the MELD meeting as to whether or not it should be included in the conference (per discussions with Dan Fleetwood). SEUs are now a very important part of radiation conferences and technical papers.

The “Particle Detector” in the First SEU Paper at NSREC

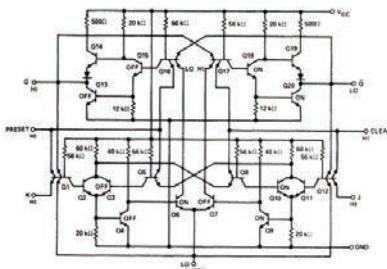


Figure 1. J-K Flip-Flop Circuit with Transistor States
SATELLITE ANOMALIES FROM GALACTIC COSMIC RAYS, IEEE TNS 1975, Binder, P.2675

- Detector in the satellite was a JK Flip-Flop. (SN74L109?)
- The JK Flip Flop is named after the inventor, Jack Kilby, from Texas Instruments, co-inventor of the integrated circuit
- Tried to find the part number and technology node— could not find this online, but did find the 54L00 referenced in the paper
- Data books at that time would actually show the circuit down to the transistor level.
 - IC layouts were drawn by hand
- Binder, Holman, and Smith's estimate of the critical charge was 0.8pC
- First use of the term “single event upset” at NSREC was in 1979

SINGLE EVENT UPSET OF DYNAMIC RAMS BY NEUTRONS AND PROTONS IEEE TNS 1979, Guenzer P5048



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The first single event upset paper (although it was not called that) outlined an investigation on a JK flip flop (named after Jack Kilby from Texas Instruments). At that time the data books included a very detailed transistor level diagram and not just a simple black box version of the function. Since the part structures were simple the parts could be examined and energy injected using a scanning electron microscope (SEM). This could be done because metallization did not cover the critical nodes.

The SEM energy was tuned to inject energy and identify critical nodes. Base emitter junctions of OFF transistors were critical to upset the device (and that is still true today). Note that the critical charge estimate was 0.8pC and some devices today have fCs of critical charge. That translates to higher upset rates for devices today.

What I really appreciate about this paper is the creative process and critical thinking required to understand the anomaly (quite inspiring). It is worth reading to understand how totally new this idea was at the time it was written and to give us historical context.

On Orbit Anomalies-What Could Go Wrong??

Table 13. Distribution (number of forms) of reported anomalies by diagnosis [75].

Diagnosis	Number of Forms
ESD - Internal Charging	74
ESD - Surface Charging	59
ESD - Uncategorized	28
Surface Charging	1
Total ESD & Charging	162
SEU - Cosmic Ray	15
SEU - Solar Particle Event	9
SEU - South Atlantic Anomaly	20
SEU - Uncategorized	41
Total SEU	85
Solar Array - Solar Proton Event	9
Total Radiation Dose	3
Materials Damage	3
South Atlantic Anomaly	1
Total Radiation Damage	16
Micrometeoroid/Debris Impact	10
Solar Proton Event - Uncategorized	9
Magnetic Field Variability	5
Plasma Effects	4
Atomic Oxygen Erosion	1
Atmospheric Drag	1
Sunlight	1
IR background	1
Ionospheric Scintillation	1
Energetic Electrons	1
Other	2
Total Miscellaneous	36

H. Garrett 2011 IEEE NSREC Short Course, P. 89



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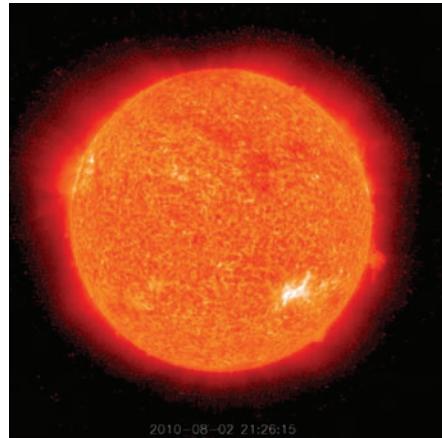


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On Orbit Anomalies-What Could Go Wrong??

- 47 satellites reported malfunctions between 23 October and 6 November 2003 during the “Halloween” solar storm.
- Solar activity significantly modulates the space environment and can significantly boost the local radiation environment

From: IEEE 2017 6th International Conference on Space Mission Challenges for Information Technology Conference Paper “Space Weather Conditions During the Galaxy 15 and Telstar 401 Satellites Anomalies”, Cid, Consuelo



[flare_stereo_a_20102132126_lrg.jpg \(2048x2048\) \(nasa.gov\)](#)



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Anomalies on 47 satellites occurred during the “Halloween” 2003 solar storm. Solar activity really boosts the local radiation environment and it is critical that systems assess the impacts of these greatly increased periods where high numbers of particles hit spacecraft.

Brief Review of Satellite Missions & Orbit



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Understanding the satellite orbit is key to understanding the radiation environment. We will go through the types of satellites for more complex systems and look at the impact of the orbits and local shielding on the spacecraft's internal radiation environment.

Mission Classifications



Risk Classification (NPR 7120.5 Projects)

- **Class A:** Lowest risk posture by design
 - Failure would have extreme consequences to public safety or high priority national science objectives.
 - In some cases, the extreme complexity and magnitude of development will result in a system launching with many low to medium risks based on problems and anomalies that could not be completely resolved under cost and schedule constraints.
 - Examples: HST and JWST
- **Class B:** Low risk posture
 - Represents a high priority National asset whose loss would constitute a high impact to public safety or national science objectives.
 - Examples: GOES-R, TDRS-K/L/M, MAVEN, JPSS, and OSIRIS-REX
- **Class C:** Moderate risk posture
 - Represents an instrument or spacecraft whose loss would result in a loss or delay of some key national science objectives.
 - Examples: LRO, MMS, TESS, and ICON
- **Class D:** Cost/schedule are equal or greater considerations compared to mission success risks
 - Technical risk is medium by design (may be dominated by yellow risks).
 - Many credible mission failure mechanisms may exist. A failure to meet Level 1 requirements prior to minimum lifetime would be treated as a mishap.
 - Examples: LADEE, IRIS, NICER, and OSOCOV

Risk Classification and Risk-based Safety and Mission Assurance. Leitner 2014 <https://ses.gsfc.nasa.gov/>

- Mission strategies depend on the mission type.
- Missions range from simple Cubesats that operate for 1-3 years and are intended for concept demonstration, to complex systems that must operate up to 20 years (or more) with high reliability.
- NASA defines missions based on risk posture.
- Communication and navigation satellites are considered Class A and are typically designed to handle space environments for 12-15 years.



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We often use mission classifications to determine the rigor required for reliability, availability, and radiation assessments. We use this for an intrinsic understanding of the risk posture for a mission.

For example, high reliability, high availability missions with high visibility and importance to the customer, entail a low risk posture, and these missions are deemed class A. A good example of class A missions include the James Webb Space Telescope and communications satellites.

Space System Applications Impacted by Radiation

The collage illustrates various space system applications:

- INTERPLANETARY:** Curiosity selfie NASA (Mars rover on the surface).
- IMAGING:** NASA logo and Earth image.
- EXPLORATION:** JPL NASA (Close-up of a rock on the Moon's surface).
- COMMUNICATIONS:** USAF AEHF public domain (Satellite in space).
- WEATHER:** Raytheon Intelligence & Space (ECOSTRESS Land Surface Temperature over Los Angeles map).
- NAVIGATION:** GPS NASA (GPS satellite in orbit).
- RADAR:** Wikipedia Space Based Radar (Illustration of a satellite with a large dish antenna).

Text descriptions for each application:

- IMAGING:** Image understanding, sensors, surveillance capability
- EXPLORATION:** Autonomous smart robots
- COMMUNICATIONS:** Smart switching, high bandwidth and capacity, space internet, global mobile communications
- WEATHER:** Time, place, accuracy of prediction
- NAVIGATION:** In-space location computation of space, air, marine and land objects
- RADAR:** Imaging and locations at night and all weather

Logos and sources:

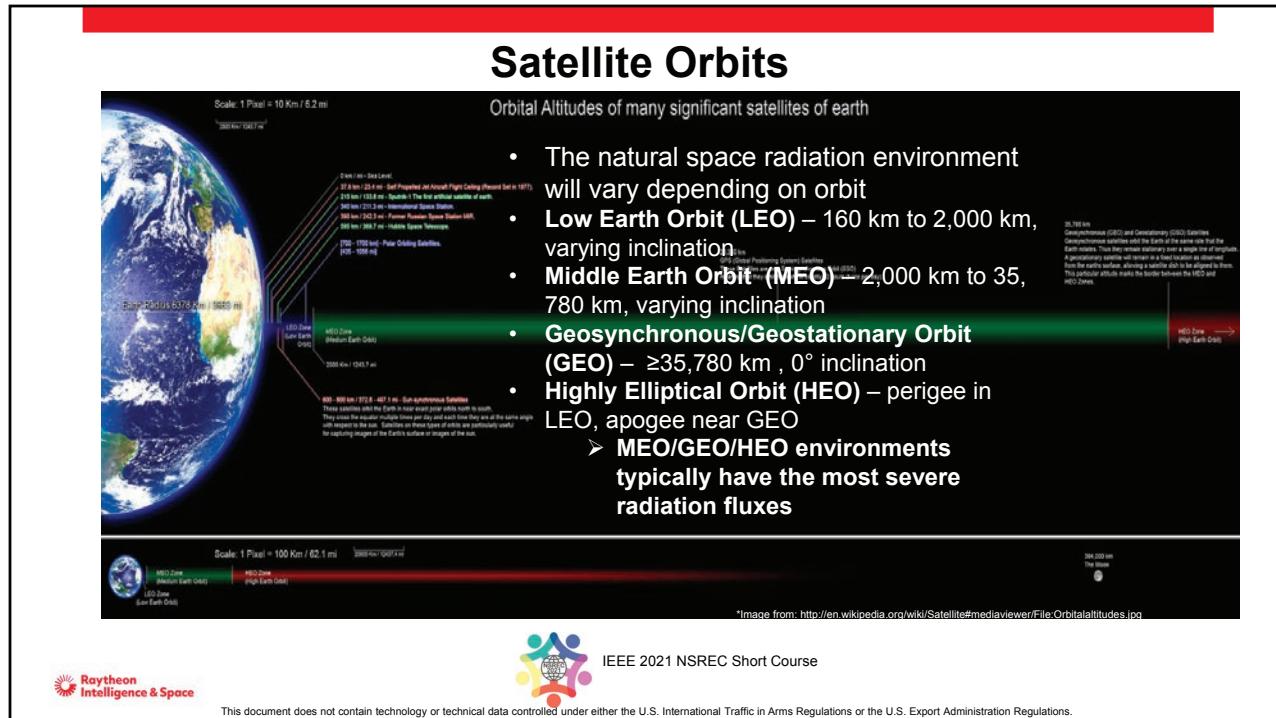
- Raytheon Intelligence & Space
- JPL NASA
- IEEE 2021 NSREC Short Course

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Every type of space system must deal with radiation impacts. These include systems used for imaging, weather, telecommunications, radar, solar system and interplanetary exploration, and navigation satellites.

One of the more well known space systems is the International Space Station, and that involves human flight, which makes requirements for safety even more critical.

These systems fly in different locations around the earth, or in our solar system, and because of their orbits, mission durations, and local shielding, the resulting internal radiation environment can be quite different. This will drive design parameters for the parts we use and what is needed for system mitigation.



This picture attempts to show to scale where different satellites orbit relative to the Earth's surface and its radius. The top section shows a close up of the LEO region in blue and this is where the ISS orbits. Many are familiar with the ISS as a reference for humans working in a space environment. This system operates at 51.6 degrees orbital inclination and $\sim 340\text{-}400$ km flight altitude which will determine the natural SEE environments. For ISS astronauts, measurements from the crew's personal dosimeters indicate a range from 12 to 28.8 milli-rads per day. This varies due to shielding levels and where the ISS is relative to radiation belts. The ISS benefits due to geomagnetic shielding since it primarily orbits below the inner radiation belt. This geomagnetic shielding also protects the crew from intense radiation bursts due to solar activity.

An astronaut could be killed by a two hour dose from solar activity while on the moon.

A system that flies at a 0 degree inclination = a path around the equator, and a 90 degree inclination would be a polar orbit.

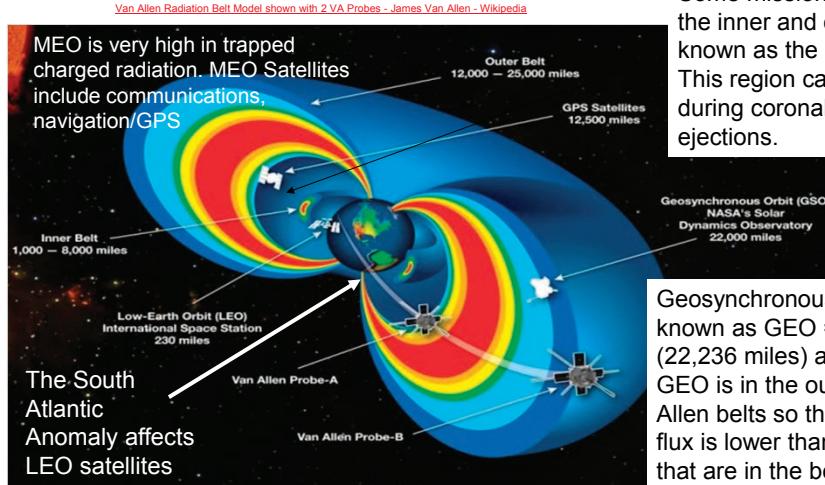
The angle of inclination and the altitude are important because these define trajectories through trapped radiation belts which I show in the next chart.

GEO orbits are out at about 36K km which puts it to the right of the green zone, and HEO orbits extend all the way into the red zone on the right hand side of the chart. The extent of the HEO orbits is shown in the bottom ribbon.

The bottom ribbon attempts to show the scaled picture out to the moon. LEO is very close to Earth!

Orbits & Belts

LEO satellites include sun-synchronous satellites (to capture images of Earth's surface or images of the Sun); International Space Station (340 km); Hubble Space Telescope (595km); VIIRS (828km, 98.75°) LEOs are somewhat protected under the belts so the environment is more benign.



Some missions fly in between the inner and outer belts known as the "slot region". This region can get pumped during coronal mass ejections.

Geosynchronous orbit is also known as GEO = 35,786 km (22,236 miles) above the earth. GEO is in the outer part of the Van Allen belts so the trapped particle flux is lower than for the MEO orbits that are in the belts. GEO Satellites include telecommunications and weather satellites.



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This shows the importance of understanding the location of the satellite relative to the trapped belts. The picture shows the location of the inner and outer belts and the location of common types of orbits relative to the belts. The ISS is shown tucked under the inner belt and benefits from the geomagnetic shielding.

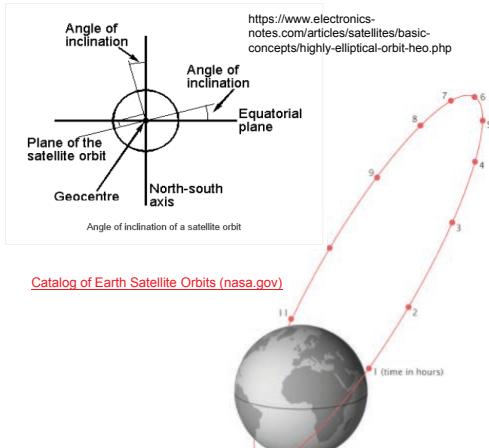
Other orbits bring satellites into the "charged particle Jacuzzi" in the belts and the doses can become quite high in comparison.

The region between the belts is often referred to as the slot region. This region can get pumped due to solar activity.

The geomagnetic field is weak at the South Atlantic (magnetic) Anomaly (SAA) so the belt region approaches the lowest level closest to Earth's surface. The ISS which flies in the range of 340-400 km is affected by the SAA, and is also affected in the high latitude regions.

The altitude is capped at 500 km since this would increase the astronaut's doses to unacceptable levels (50 mrem per day).

HEO



- HEOs are often used for systems for polar coverage since most of the orbit time is at apogee.
- Examples of HEO orbits include Molniya and Tundra orbits.
- The Molniya orbit combines high inclination (63.4°) with high eccentricity (0.722) to maximize viewing time over high latitudes.
 - Each orbit lasts 12 hours, the slow, high-altitude portion of the orbit repeats over the same location every day and night.
 - Russian communications satellites and the Sirius radio satellites currently use this type of orbit
- The eccentricity and the angle of inclination are important parameters for spacecraft environment determination since magnetic field lines come down at the magnetic poles and trapped particles follow the field lines.
- HEO satellite orbits include polar and equatorial orbits.



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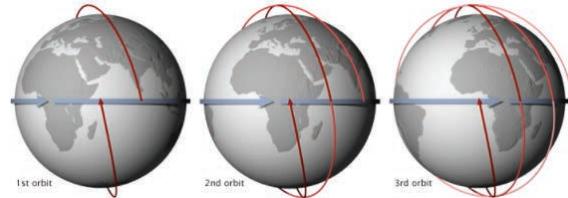


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The shape of HEO orbits include parameters that define its eccentricity and the angle of its orbital plane relative to the equator. An inclination of 0 degrees would be an equatorial orbit. An inclination of 90 degrees would be a polar orbit. An inclination of greater than 90 degrees would tip the ellipse to the left instead of the right.

The shape of the orbit and its period will define how long the satellite dwells in the trapped particle belts and that will translate to dose.

Sun Synchronous Orbit



[Catalog of Earth Satellite Orbits \(nasa.gov\)](https://nssdc.gsfc.nasa.gov/space-track/orbits/)

- A Sun-synchronous orbit crosses over the equator at approximately the same local time each day (and night).
- This orbit allows consistent scientific observations with the angle between the Sun and the Earth's surface remaining relatively constant.
- This shows 3 consecutive orbits of a sun-synchronous satellite with an equatorial crossing time of 1:30 pm.
- If a satellite is at a height of 100 kilometers, it must have an orbital inclination of 96 degrees to maintain a Sun-synchronous orbit.

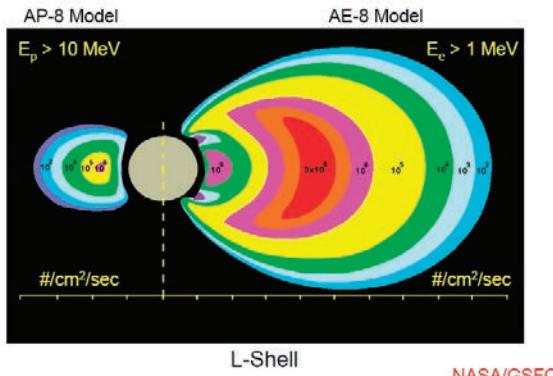


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Trapped Proton & Electron Intensities



- The intensity of the trapped electron flux is shown on the right side of the plot, plotted as a function of the L-shell
- The intensity of the trapped proton flux is shown on the left side of the plot, plotted as a function of the L-shell
- These belts wrap around the earth following the magnetic field lines pictured below in a toroidal shape
- This means the spacecraft's environment strongly depends on its orbit

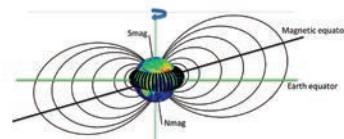


Figure 1: Dipole magnetic field tilted and off-center with respect to Earth
Bourdarie 2014 IEEE NSREC Short Course P.11



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We will first cover the trapped particle environments since these environments really impact radiation requirements. The picture shows a view of the belts relative to what is called the L-shell (magnetic coordinate). The L value is determined at the magnetic equator and the picture shows the shape of the magnetic field lines. The magnetic field strength is important since that determines the particle energy that can penetrate and get trapped by the belts. At higher altitudes, the magnetic field strength is not great enough to trap particles in a stable fashion. The Earth's atmosphere forms the lower level of the radiation belts due to atmospheric energy loss mechanisms. . (See Barth P. 31 1997 IEEE Short Course figure 4.2.2)

The picture on the left shows the trapped electrons on the right, and the trapped protons on the left. You can see how the belt is the closest to Earth at the southern end of Earth where the magnetic field lines bend in at the SAA. The intensity numbers are for proton energies greater than 10 MeV and for electron energies greater than 1 MeV. These are energies that affect typical spacecraft internal to typical shielding levels. The units are in particles/cm²/sec and this shows that the flux intensities change by orders of magnitude depending on where you are in the magnetic field. This illustrates why it is important to know where the space mission is flying.

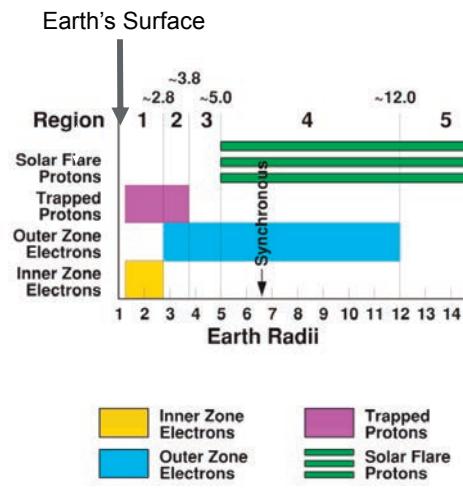
The belts are tilted relative to the rotational axis and follow magnetic field lines as shown in the smaller inset picture, so the belts wrap around in toroidal (donut) shapes around Earth.

This is a very dynamic environment and can rapidly change by orders of magnitude depending on solar activity and resulting belt pumping. This will show up in mission specifications as worst hour, worst day, and worst week requirements.

Radiation Zones – Why the Orbits Matter

Mission	Radiation rad/100 mils-Al	Duration (Years)
Europa	2-3 Mrad	> 9
Titan	30 krad	14
Venus	20 krad	2
Moon	10 krad	20
Mars	10 krad	>2
Earth (GEO-1 year)	30 krad	10
Earth (MEO-1 year)	2 krad - 2 Mrad	10
Earth (LEO-1 year)	1 krad	10
Deep Space	1-10 krad	10

Extracted from Adell and Boch IEEE 2014
NSREC Short Course P. 45



- This plot shows the locations of the trapped particles relative to the distance from the Earth's surface in terms of Earth radii.
- One Earth radius = 6380 km referenced to the Earth's center.
- Earth's surface is @ 1 Earth radius
- The table to the left shows mission ionizing doses
- These depend on the mission trajectory through the different radiation regimes, duration, shielding, and flare activity

Adell and Boch IEEE 2014 NSREC Short Course P. 42



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The table gives a relative total ionizing dose comparison for different missions behind a 100 mil Al shield (which is used as a common reference shield for different studies). This includes Earth missions, interplanetary missions, and deep space missions. These have different mission durations although many are on the order of 10 years.

For Earth missions, the heavier doses at GEO and MEO are due to orbits that encounter the trapped radiation belts, whereas LEO is relatively benign (depending on the LEO orbit). For the Earth doses, these are doses in 1 year so you need to multiply the annual dose by the number of mission years to get the total ionizing dose for the mission. The other mission doses are already given in terms of mission dose.

The chart on the right gives an idea of the locations of the radiation belts relative to the altitude above the earth's surface (at 1 Earth radii) where the satellite orbits. The numbers refer to the number of earth radii that define the belt regions, for example the inner zone electrons extend to 2.8 Earth radii and the outer zone electrons extend to 12 Earth radii. To give this perspective, the ISS is at about 0.053 Earth radii so it is just underneath the belts for the most part. The maximum dose rate for the ISS is typically at the SAA (where astronauts get most of their dose) although it can get higher doses in the auroral regions during solar activity due to the ISS orbit's inclination, and due to cosmic particles coming in at higher latitudes.

The GEO orbit is shown on the chart at about 6.6 Earth radii and this lies in the outer electron zone. GEO satellites can be significantly impacted by solar generated protons shown in the green striped region.

MEO satellites that fly in the belts suffer the highest doses of the Earth orbits due to encountering trapped protons and electrons. GPS lies at about 3.14 Earth radii which puts this satellite system in both electron and proton belts. As a result, this system has tougher, more stringent radiation requirements.

Proton Spectra Orbit Dependence

DODDS *et al.*: CONTRIBUTION OF LOW-ENERGY PROTONS TO THE TOTAL ON-ORBIT SEU RATE IEEE TNS 2015 P. 2441

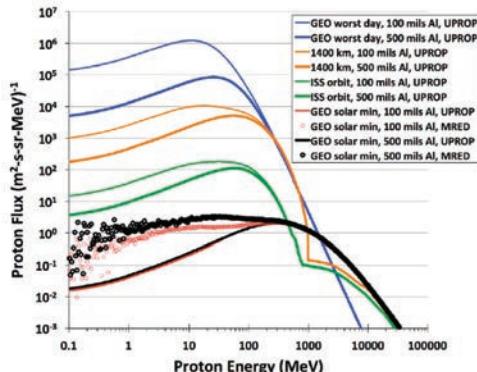


Fig. 1. Proton spectra simulated with (solid lines) CREME-96 UPROP and (circles) MRED for two shielding thicknesses in four space environments. UPROP agrees with MRED for the *GEO worst day*, *1400 km*, and *ISS* orbits (MRED results omitted for clarity), but disagrees with MRED results for *GEO solar min* at low proton energies.

- This shows the translation of the external proton environment through different shielding thicknesses.
- The proton flux differs by orders of magnitude depending on orbit.
- Flux gives the rate of particle impingement
- Notice that *GEO worst day* is due to solar activity and the proton flux is boosted more than 5 orders of magnitude
- Shielding can mitigate protons to some degree but cannot make up for the huge change in proton flux due to the solar activity
- The proton flux for the *ISS* is much more benign than for the *1400 km* orbit that cuts through the Van Allen belts.



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Solar protons can significantly impact the number of particles encountered by a satellite. These events are often defined by worst hour, worst day, and worst week for many missions, where the number of hours, days and weeks will be defined for radiation impact assessments.

The figure from N. Dodds et al from TNS 2015, shows the contribution of low energy protons and these can be significantly attenuated by shielding because they are lower energy. Typical shielding levels however do not overcome the sheer increase by OOM in the flux due to solar events and that means the designer must determine the impact of such an increase to the system's function.

This can have implications for the use of softer radiation technologies due to proton particle strikes causing device upsets. If strike rates are very high, the probability of having multiple strikes within critical timing windows can go up and defeat system hardening strategies such as triple modular redundancy (TMR). This may limit TMR block sizes and will be a part of the design trades for successful system designs.

Galactic Cosmic Rays (GCRs)

- Beyond the trapped radiation, the space engineer must deal with the presence of radiation from GCRs
 - In 1936, an Austrian physicist, Victor Hess, won the Nobel Prize for the discovery of galactic cosmic rays and even though they are still called rays, they are actually particles.
- The origin of GCRs is not totally understood but they are believed to have been created in supernova shock waves.
- Although always present, the GCRs are modulated by the solar cycle: the maximum GCR flux is at solar min and min GCR is at solar max.
- GCRs are believed to be fully ionized particles, with energies from 10s of MeV/nucleon to 100s of GeV/nucleon.
 - These particles are so energetic that shielding is not practical
- The total dose from GCRs is around 10 rads (Si) per year but they represent a hazard to hardware due to Single Event Effects (SEEs)

From Barth, J. 1997 IEEE NSREC Short Course



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We now move beyond the trapped belts and examine radiation impacts of galactic cosmic rays (GCRs). These highly ionized particles that originate outside our solar system, are incredibly energetic, and travel at relativistic speeds. As such, shielding is not a mitigation strategy.

While the number of particles from GCRs are much lower than that encountered in trapped particle belts (*compare 10 rads per year vs krads to Mrads per year*), their ability to penetrate and cause device upsets (SEEs) and concomitant system reactions requires an assessment of the impacts and the strategies for dealing with these strikes.

Even on Earth's surface we can detect the presence of these penetrating rays and our atmospheric shielding at sea level represents 0.9 m of lead. To put that in perspective, our atmosphere represents almost a factor of 1500 times greater shielding than the standard space shield of 100 mils or 2.54 mm of Al.

GCR Relative Abundance

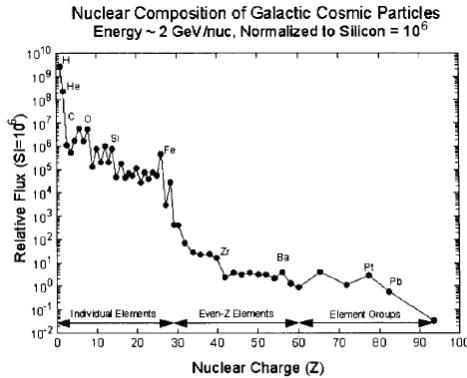


Figure 5.4.1.1: Relative abundances of galactic cosmic ray ions in interplanetary space. *after Medwalt*

From Barth, J. 1997 IEEE NSREC Short Course

- This compares the relative abundance of the different elements in GCRs and is normalized to Si = 10^6
- GCRs travel at relativistic speeds and represent all elements in the periodic table
- 83% of GCRs are protons (H+), 13% are alpha particles, 3% electrons, 1% are heavier nuclei
- The number of heavier elements drops off by orders of magnitude after iron and are relatively rare



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While GCRs are always present, they are modulated by solar activity. When solar activity is at a peak the number of GCRs is lower. When solar activity is in a quiet period, GCR intensities increase.

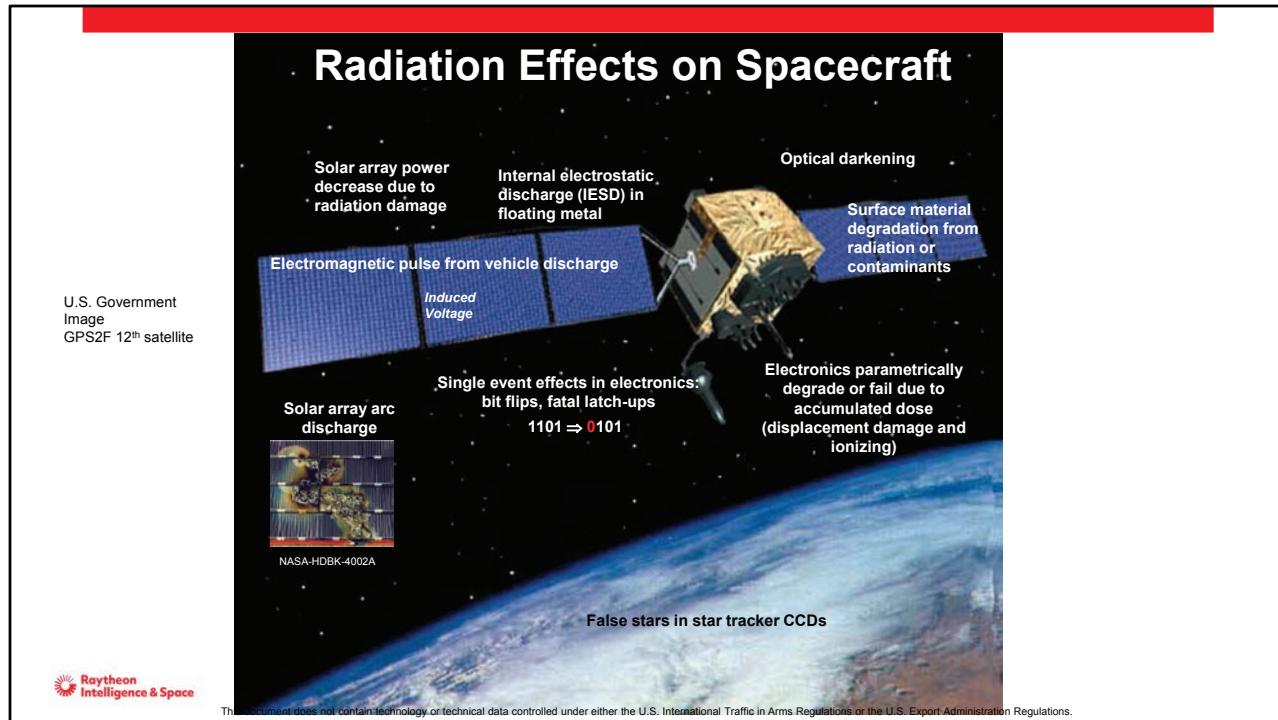
Note that the particle abundance is roughly proportional to the solar system material presence

Radiation Impact on Satellite Subsystems



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Radiation impacts spacecraft in several ways. There are four primary radiation types we deal with: 1) Charging, 2) Total Ionizing Dose (TID), 3) Displacement Damaging Effects (DD) and 4) Single Event Effects (SEE).

On the outer surfaces, materials can be degraded (displacement damage) and weakened from both radiation and contamination. Coatings can darken and can decrease the quality of images.

Solar array power can decrease if solar cells surfaces and coatings are damaged (TID, DD) or due to intense charging differences across a solar panel that result in arcing. Vehicle discharge can induce voltage pulses that can create system disturbances.

Internal electronics can suffer from floating metal charging due to high energy electron penetration of the Faraday cage of the spacecraft.

Internal electronics can suffer parametric degradation or fail due to TID and DD.

Heavy ion and proton particle strikes can cause device upset and destructive effects that can impact system operation and availability

How Does Radiation Affect Spacecraft?

- Radiation Reaction Types:
 - ***Charging***
 - Total Ionizing Dose
 - Displacement Damage
 - Single Event Effects



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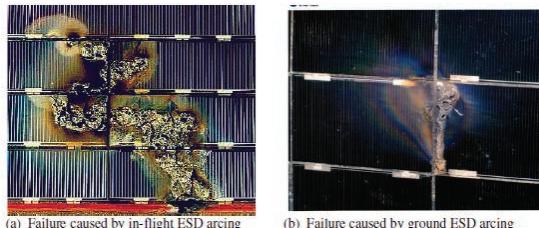


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Spacecraft Charging

- NASA's handbook NASA-HDBK-4002A is a very good reference for the following and is worth studying
- Spacecraft charging effects are attributed to almost 25% of the cost of anomalies and failures

NASA-HDBK-4002A



(a) Failure caused by in-flight ESD arcing (b) Failure caused by ground ESD arcing

Figure 10—Examples of Solar Array Failure

- Differences in the LEO vs GEO plasma environments lead to different types of arcing events but the arc initiation conditions are the same



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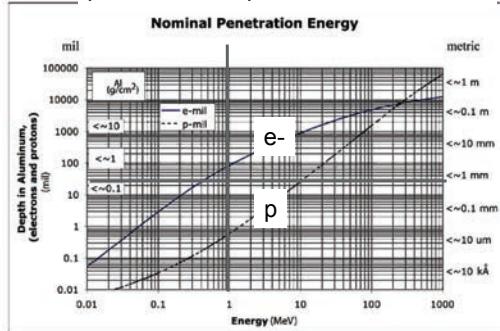


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Since charging has a significant economic impact to spacecraft operation, it is a critical consideration as part of a successful spacecraft design. While this short course does not focus on this aspect of radiation effects, it is worth mentioning, and worth taking the steps to mitigate charging effects. It is perhaps intuitively obvious that surface charging can occur due to high electron fluxes, but these electrons can also penetrate standard spacecraft shielding such that internal floating metal can charge. If the metal is not tied to a circuit or ground through leakage paths that can bleed off charge at a sufficient rate, these floating metal surfaces can build to very high voltage potentials relative to surrounding materials. At some point, if the breakdown potential for the surrounding dielectric material is reached, there can be an arc over event. These events can create damage and depending on the circuit, can even create the conditions for sustained arcs. The photos show examples of surface charging that created sustained arcing events.

Charging

At 100 mils of Al, electrons with energies greater than 1 MeV can penetrate the spacecraft shield



NASA-HDBK-4002A P. 28

- There are two main charging regimes; surface and internal
- This chart shows how deeply protons and electrons penetrate into aluminum and the energy dependence for a GEO orbit
 - Since these penetrate, *charging can occur within the spacecraft's Faraday cage*.
 - Electrons are deposited in a larger range around a given depth than protons.
 - The transition between surface charging and internal charging is around 50 to 100 keV (shielding thickness)
- For GEO orbits the practical ranges of interest for internal charging is 0.1MeV to 3 MeV (shielding, flux)



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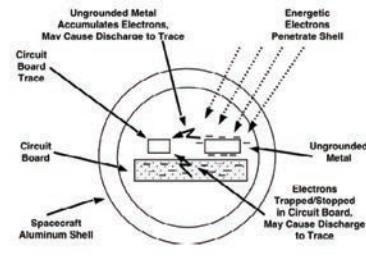
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There are two main charging regimes we deal with; surface and internal. The chart shows the penetration ranges for energetic electrons and protons and this shows how the penetration range (on the vertical axes with mils on the left and metric on the right) is a function of the particle energy. The top curve shows the electron penetration range, and the bottom curve shows the proton penetration range. The electron can penetrate further at a given particle energy up to about 200 MeV. The electron energy required to penetrate a 100 mil Al shield is around 1 MeV, but a proton needs about 20 MeV for the same penetration capability.

The electron energies trapped in our belts range up to 7 MeV in the outer electron belt and up to 30 MeV in the inner belt. (see P 17 Adell and Boch IEEE 2014 NSREC Short Course). Proton energies range from 1 keV to >500 MeV, but proton fluxes are much lower at higher energies. (see P. 45 Barth 1997).

For GEO orbits the practical range of interest for internal charging is electron energies that range from 0.1MeV to 3 MeV although some Earth missions will take this to higher depending on the orbit. Since proton fluxes are orders of magnitude lower in comparison to the electron fluxes for GEO, the real internal charging threat is due to energetic electrons.

Capacitor Model for Charging



Internal spacecraft floating metal and dielectrics can charge due to electron penetration.

- The figure shows energetic electrons penetrating the shell.
- The internal environment is determined by transporting the outside environment through the spacecraft wall shielding to determine a flux at different locations (dosimeter points).
- Note that all external forms of radiation must be transported through the material to determine the internal spacecraft environment
- Any ungrounded metal can accumulate charge due to energetic electron penetration during the life of the spacecraft – so can dielectrics
- For internal charging we build capacitance models of any floating metal so dielectric materials surrounding the metal, and their properties, must be identified.
- Ground metal lids, traces that are not connected to semiconductors, transformer and inductor cores



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Charging of floating metal can be thought of as the charging of a capacitor. Physical structures are examined where the floating metal forms the charge plate of the capacitor, and the distances and geometries of device features are measured to create a capacitance model. Important parameters include the electron flux that has penetrated the shield, the size of the floating metal, the distance to circuit traces or components (the capacitor's dielectric material thickness), the dielectric material properties including its resistivity and its dielectric constant. Once the effective capacitance is determined, the voltage build up due to the internal electron flux can be calculated. If the resulting electric field strength exceeds the material dielectric withstand voltage, mitigation measures to bleed charge must be taken, or circuit reactions need to be assessed to see if these are acceptable.

Common sources of floating metal include device lids, unconnected (remnant) circuit board traces, and transformer and inductor cores.

NASA-HDBK-4002A w/CHANGE 1

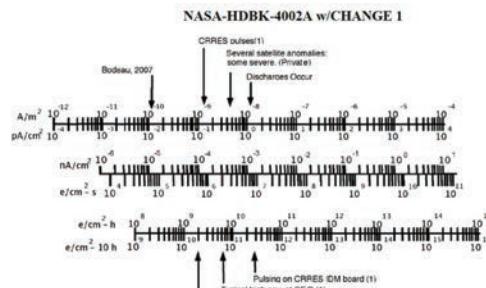


Figure 7—IESD Hazard Levels versus Electron Flux (Various Units) ⁽¹⁾Frederickson (1992)

NASA-HDBK-4002A P. 33

- As the electron flux increases, the Internal Electrostatic Discharge (IESD) risk substantially increases
- This flux can be translated as a current/cm² to examine floating metal charge impact using capacitive models of floating metals near dielectrics.
- Bodeau's paper cited discharges due to currents as low as 10 fA/cm²



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How Does Radiation Affect Spacecraft?

- Radiation Reaction Types:
 - Charging
 - ***Total Ionizing Dose***
 - ***Displacement Damage***
 - ***Single Event Effects***



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Electronic Devices are Affected by DDD, TID & SEE

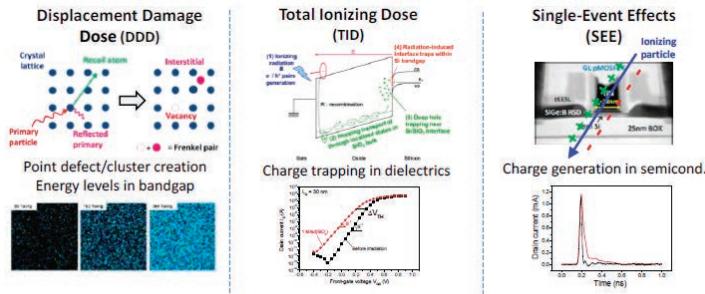


Figure 21: Summary of major radiation effects induced in electronic devices and ICs (images after [113,114,115,116,117,118,119]).

M. Gaillardin, IEEE 2018 Short Course P162

These were covered in the prior sections of the short course. To determine the impact to the mission, the space environment must be translated through the spacecraft shielding to determine the internal environment, and the impact of this is analyzed by radiation engineers.

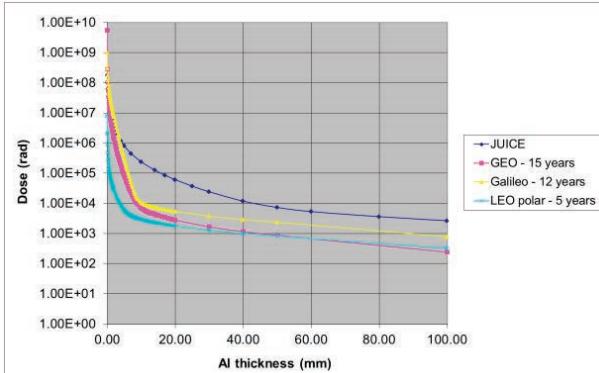


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There are three curves radiation engineers use to guide decision processes regarding system architecture and parts procurement decisions. These include Total Ionizing Dose (TID) dose depth curves, Displacement Damage dose depth curves, and the Integral Linear Energy Transfer (LET) Spectra. These curves give a translation of the external environment through shielding, typically as a function of aluminum shield thickness for TID and DD, to help designers determine working parameters for circuit design and for unit shielding. LET spectra are generated as a function of specific shield thickness. 100 mils of Al is often used as a reference shield thickness for mission comparisons.

Total Ionizing Dose Depth Curve



ESA Internal Course, EEE Component Radiation Hardness Assurance Tutorial, ESTEC, 4 November 2016

- This type of curve is used to determine the amount of radiation received behind aluminum shielding.
- As shielding is increased, its benefit plateaus (Bremsstrahlung). Typically spacecraft need around 5-10mm of Al for GEO 10 year missions to enable use of most electronics.
- The dose is mission and orbit dependent. We use this to guide part selection and shielding levels.



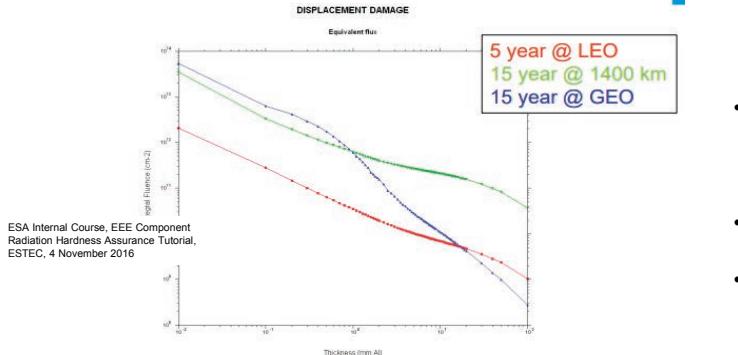
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The dose depth curve shows the dose in rads (radiation absorbed dose usually given for silicon) or krads vs the aluminum shield thickness in either mils of Al or mm of Al. It gives designers insight into the shielding needed and the total dose radiation levels for device procurement. Oftentimes a radiation design margin will be specified. For example, if we use a radiation design margin of 2, 20 mm of Al thickness for a 15 year GEO mission would get the dose down to 3 krads, so devices with $3 \times 2 = 6$ krad dose sensitivity would meet requirements. That would mean that relatively soft devices could be used. For the JUICE mission, the dose is close to 80 krads behind a 20 mm shield. That means parts procured would need to withstand a 160 krad dose for a design margin of 2. Design margin requirements are program specific.

DDE Environment Requirement

- Displacement Damage Effects (DDE) Curve provides the worst case estimate of neutron fluence as function of shield thickness for representative missions
- Derived from specified proton and electron fluence environments and converted to 1 MeV-equivalent neutron fluence (NOTE: neutrons are a convenient and inexpensive method to test for DD effects in electronics)



- For High LEO, MEO, GEO, HEO missions, DD requirement is dominated by intense, high energy solar protons
- Shielding is not an effective mitigation methodology
- Low LEO missions have low DDE environments (protected by the VA belts)



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The Displacement Damage Effects curve plots the integral fluence converted to 1 MeV equivalent neutron fluence vs Aluminum shielding thickness in either mils or mm of Al. 1 MeV neutrons are a convenient and inexpensive method to test for DDE in electronics.

Low LEO missions are more protected by the geomagnetic field and that is why the DDE is so much lower.

Integral Linear Energy Transfer (LET) Spectra

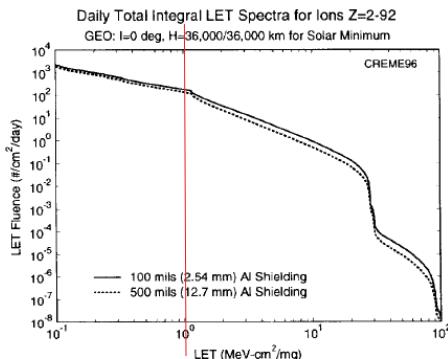


Figure 5.4.3.3: Total integral LET spectra for a geostationary orbit. Note the small decrease in LET fluence even though the shielding was increased by a factor of 5.

From Barth, J. 1997 IEEE NSREC Short Course P64

- The integral curve shows the total number of GCR particles that penetrate two different shielding thicknesses at GEO, 100 mils of Al (2.54 mm) and 500 mils of Al (12.7mm) at a given LET per day.
- For example, at an LET of 1, marked by the vertical red line, there are a total of just over 100 particles per cm² per day that have an energy of 1 MeV·cm²/mg and higher
- This shows how little benefit is achieved by shielding due to the high penetrating energy of GCRs
- Interestingly (and perhaps counterintuitively) shielding can slow down the particles and cause them to interact more with the material increasing their ability to deposit charge (Bragg peak)



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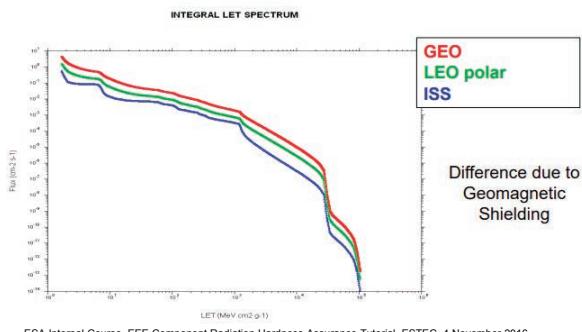
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This shows an integral LET spectra for ions with atomic numbers that range from 2 to 92. Integral means that the number of particles per cm² in one day includes all particles of that LET and higher. There are also differential spectra plots. These curves are generated based on specific shield thicknesses.

This model was generated for a GEO orbit for a solar minimum condition. Since solar minimum represents a maximum GCR flux condition, this serves as the environment to determine long term average conditions for upset rates.

Active solar conditions are treated where the mission defines the number of hours, days, and weeks for those conditions. Some systems will need to operate through these intense particle fluxes. TMR'd hardware in particular needs to be assessed for the probability of two chain impacts within critical timeframes.

SEE Environment Requirement



- “Heinrich” LET curves generated in CREME-MC
- Curves depend on:
 - Orbital parameters
 - Geomagnetic shielding and Earth shadowing effects
 - Solar conditions (average and peak)
 - “Quiet Model” for evaluating typical and long-term average particle fluxes and SEE rates
 - “Flare Model” for evaluating worst case and peak particle fluxes and SEE rates
- Includes galactic cosmic ray and solar heavy ions (LET spectra); solar and trapped protons (energy spectra)



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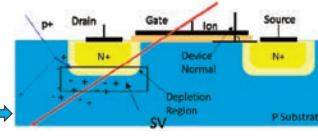
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Real differences in the SEE environment include those impacts due to geomagnetic shielding. For example, the ISS environment benefits from the geomagnetic field and this results in a lower particle flux.

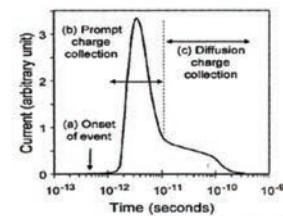
Once the internal environment has been determined the characteristics of the environment are translated using device heavy ion cross section curves from heavy ion characterization tests to determine device upset rates (as shown in previous sections of the short course). These device upsets are then categorized to determine system impacts and their criticality. If the upset type and rate does not meet requirements, mitigation is needed.

Single Event Effects (SEE)

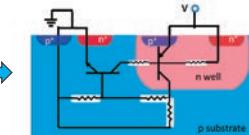
- Caused by charge deposition from *single high energy particle* (proton or cosmic ray) striking sensitive region
 - Heavy ions – direct ionization (shown in the red path)
 - Protons – primarily indirect ionization from nuclear reactions (spallation) (shown in the blue path)
- Effects on electronics – if Linear Energy Transfer (LET) of particle is greater than critical charge required $LET_{threshold}$
 - Non-destructive (soft errors):
 - Upsets (SEU): bit-flip in memory, change of state in logic circuit
 - Transients (SET): current/voltage spike causes output error
 - Correctable (reset device, rewrite data)
 - Destructive (hard errors)
 - Latchup (SEL): corruption of signal path, high current regenerative logic state destroys devices
 - Burnout (SEB): highly localized device destruction from high current flow (includes SEGR, SEDR)



R. Ladbury 2017 IEEE NSREC Short Course P. 80



R. Mangeret 2018 IEEE NSREC Short Course P114



R. Ladbury 2017 IEEE NSREC Short Course P. 94



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The types of reactions vary depending on the technology, technology node (device sizes), bias, application circuit, and temperature. The general reaction to particle strikes are known as Single Event Effects (SEEs). Ionized particle strikes can transfer charge directly leaving a trail of electrons and holes (direct ionization), or a particle, such as a proton or neutron, can hit a nucleus in the device that knocks the atom out of the lattice, and this scattered particle transfers charge generating electron-hole pairs in the device along the scattered particle's path. This is a nuclear spallation reaction, also known as indirect ionization, and typically, the cross section for a nuclear interaction is 4 to 5 OOM smaller than a direct ionization type of event.

A device will have a critical amount of charge required to affect its behavior. If the particle hit, directly, or indirectly through the scattered particle, has sufficient capability to deposit enough charge then a reaction can occur. The types of reactions, covered in the earlier short course sections by Daniel, Balaji, and Vincent, are shown here as a refresher and include both non-destructive and destructive effects.

Non-Destructive SEEs

Single Event Effects & Mitigation Strategies					
Non-Destructive	Impact	Vulnerable Device Types	Timescale	Mitigation Strategies	System requirements
SEU, MBU	SET	Transient Analog, buffers, regulators	ps to msecs	filtering, data integrity checks with retry, Temporal voting, multiple samples	System architecture to assume possible transients
	Data errors	digital	persists until re-written	detection of issue, TMR, EDAC	Acceptable Bit Error Rate
	Block Errors	memories	persists until re-written	detection of issue, TMR & error correction, two chains and reset if disagree	Availability
	Stuck Bits	memories	permanent	EDAC	EDAC architecture for level of mitigation required
SEFI	Interrupted Functionality	Digital	possible soft start	Detection and issue of soft start	System design requires detection technique for the SEFI mode with increasing degrees of autonomic interaction including reset and power cycle
			possible power cycle	Detection and power cycle	



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Non-destructive interactions include Single Event Upsets (SEUs), where logic states of memory elements such as flip-flops, shift registers, state machines, or RAMs, change logic level; and Single Event Transients (SETs) where buffers, clock paths, analog circuits, RF circuits, point of loads or regulators, see a transient pulse of various possible pulse widths and amplitudes depending on what gets hit. Transients can be ns to milliseconds long for analog circuits. The longest transients observed are typically in analog circuits that contain bistable start-up states in circuits like band gap references and these can be 100s of msecs (often temperature dependent). The non-destructive hits are evaluated for system impacts and recovery strategies required in a Single Event Effects Criticality Analysis (SEECA).

Destructive SEEs

Single Event Effects & Mitigation Strategies					
Destructive Effects (SEDE)	Impact	Vulnerable Device Types	Timescale	Mitigation Strategies	System Requirements
SEL, SEB, SEGR, etc	Usually a permanent failure if this occurs.	Various	Permanent	Cold-spare redundancy	Failed device isolation in cross-strapped functions
				avoid using vulnerable devices	restriction of vulnerable part usage
				controlled exposure time	bias device only when needed; avoid sneak path biasing
SEL	Possible failure, possible latent damage. Usually considered destructive unless reliability studies are performed	CMOS	Transient if below holding current	Current limiting; limit can bring out of latchup for some circuits	Passive or active limiting
			Current stays high until voltage decreases below holding voltage	power cycling	Increased current level detection and circuit restart
			Will not sustain if below holding voltage, uS to ms depending on voltage and temp		Assessment of power domain crossing during cycling
				controlled environment	lower voltage use, constrained temperature band



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Destructive effects include a whole host of alphabet soup reactions. Examples of destructive effects or potentially destructive effects include Single Event Latchup (SEL) in CMOS devices, Single Event Burnout, Single Event Gate Rupture (SEGR) in power devices, Single Event Dielectric Rupture (SEDR), Single Event Snapback (SEB), and Stuck Bits. Destructive effects demand strategic mitigation approaches, and for critical missions, parts that exhibit heavy ion destructive behaviors are often restricted from approved parts lists.

If a program permits the use of parts that exhibit destructive behaviors, redundancy strategies and operational strategies require careful consideration. Possible strategies include powering the device only when you really need to use it, or only operating the device at low enough voltages and/or temperatures where the destructive behavior will not happen. The safe operating regions are established as determined by device heavy ion characterization, often of a considerable number of device samples to understand the population.

Destructive SEEs

Single Event Effects & Mitigation Strategies					
Destructive Effects (SEDE)	Impact	Vulnerable Device Types	Timescale	Mitigation Strategies	System Requirements
SEGR	Failure	Power MOSFETs (typically hardened)	Permanent	operate in the safe operating area	Lower VDS, VGS
				redundancy	Failed device isolation in cross-strapped functions
SEB	Failure	Power MOSFETs (typically commercial), BJTs, FETs	Permanent	avoid using vulnerable devices	restriction of vulnerable part usage
				operate in the safe operating area	Design system using part at lower voltage
				redundancy	Keep redundant parts off/cross strap
SEDR	Failure	One Time Programmable FPGAs Caps used in linear bipolar devices	permanent	avoid using vulnerable devices	restriction of vulnerable part usage
			permanent		
SES (snap back also known as single transistor latch)	Possible failure, possible latent damage.	SOI	transient	Usually not destructive. Especially important for deep submicron devices	restriction of vulnerable part usage
Stuck Bits	Failure	Memories	can slowly anneal over many hours, days	EDAC	EDAC architecture for level of mitigation required
SEB	Failure	Schottky Barrier Diodes	permanent	Lower voltage applied across the diode	Derating requirements <50% rated voltage



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This table covers the types of parts that exhibit certain destructive effects and mitigation strategies. For example, hardened Power MOSFETs can exhibit SEGR, but if the voltage from the drain to source and gate to source are operated within a safe region, the part can successfully be used in space. Commercial Power MOSFETs often exhibit SEB, so it is wise to heavily characterize any commercial power MOSFET candidates for spacecraft power systems. If the devices can be safely used at a lower voltage, that can be a mitigation strategy. Otherwise restrict the part from program usage.

Although SEEs are usually thought of as effects on active, biased devices, one destructive effect, SEDR can actually damage the dielectric in capacitors used in linear bipolar devices. Vulnerable parts are usually restricted from space approved parts lists. SEDR can also occur in one time programmable FPGAs.

Silicon on Insulator (SOI) parts exhibit a single transistor latch structure called Single Event Snapback (SES) that can cause both latent damage and failures. Typically these parts are restricted from program usage.

Memories have such small transistors that particle strikes act as a localized radiation dose damage creating stuck bits due to leakage or threshold shifts. Some of these failures will slowly anneal over many hours and days, but these are considered failed bits for the purposes of designing adequate protection. Error detection and correction architectures are commonly employed to mitigate stuck bits since the number of overall stuck bits is low. The idea here is to assume that there will be failures and design the EDAC to handle the number of failed bits with appropriate encoding to correct for these failures.

Memories also employ logic to improve device yield using internal redundancy approaches. This control logic can get hit and cause the memory to point to failed columns or rows within the memory where the

number of failed bits can be considerably more than a few stuck bits. These failures are not due to the radiation environment – they are due to defects in the devices, but because of the internal redundancy logic that selects what portion of the memory is being used, SEUs affecting that logic can point to defective portions of the memory. Memory mode registers can also be hit and affect way more than a few bits. While these are not damaging events, it is important to understand that memory management must also deal with these types of events so that the EDAC architectures are appropriately chosen depending on the mission criticality.

A Special Word About Destructive Effects

- For Class A missions, most programs significantly restrict the use of devices that exhibit destructive behavior to heavy ion strikes.
- Some missions permit mitigation, such as keeping the device OFF if not normally used, to mitigate the exposure time and reduce the probability of failure.
- Some latch-up events are not immediately fatal – for high reliability mission requirements, there is often a requirement to demonstrate that the part will still meet mission requirements – it is usually easier to find a replacement part.
- A typical requirement is that devices must not demonstrate latchup or destructive SEE effects at less than an LET of 75 MeV-mg/cm² (testing to a fluence of 1E7 particles/cm²), or if destructive effects can occur, the reliability impact must be shown to be insignificant.



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Latch-up is traditionally considered a destructive abnormal high current event and its impact on the system reliability is a key consideration. Some devices that latch-up have latent damage where the subsequent failure does not occur during heavy ion testing, but manifests later (“walking wounded”). That is part of the reason life-testing post-latch is required to determine reliability impacts for high reliability missions, if you do use latchup susceptible devices. If these do not impact the reliability, then the system can design for the recovery from the latchup state.

The effort to prove latchup does not cause failure is considerable, so it is most common to weed out these devices. If there is no easily procurable replacement for the part, then the reliability characterization effort must be undertaken. However, the outcome of the characterization effort is not guaranteed and most programs will require a plan “b” such as hardening the device at the device level. The earlier talks in the short course have discussed some of these issues.

Most high reliability, high availability systems require that the latchup have little impact to the device’s basic reliability. This is incorporated in device requirements, where tests are done at high temperature (which exacerbates latchup), using a test particle fluence of 1E7, at high LETs (70-75 MeV-cm²/mg).

Why Do We Care About Destructive Events?

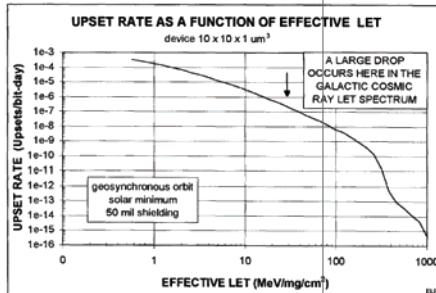


Figure 54 The upset rate calculated as a function of critical LET assuming that the cross section is a step function of LET.

Latchup rate (latchups/device-day)	Latchups during mission number	Failure hrs	FITS
1.00E-03	3.65E+00	2.40E+04	4.17E+04
1.00E-04	3.65E-01	2.40E+05	4.17E+03
1.00E-05	3.65E-02	2.40E+06	4.17E+02
1.00E-06	3.65E-03	2.40E+07	4.17E+01
1.00E-07	3.65E-04	2.40E+08	4.17E+00

IC typical FIT
rate range

- Assume the critical LET is an LET of 1
- Assume the cross section is 10^*10^*1 um^3 and that this represents a destructive event
- The GEO event rate behind 50 mils of Al is $2\text{E-}4$ upsets/device-day
- For reliability, we often talk of device failure rates in terms of a failure in 1 billion hours = 1 FIT
- Most ICs have reliabilities that are a few to 10s of FITs
- If the destructive event rate is higher than $1\text{E-}7$ events per device-day, *this starts to impact typical device reliability*
- If a device latches to protons, the rate will be so high mission reliability can be impacted*



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If the latch-up LET threshold is low, the failure probability goes up since the number of particles capable of latching the device goes up by orders of magnitude at lower LET thresholds. To get a feel for how the upset rates translate into reliability impacts, refer to the plot from Ed Peterson's 1997 IEEE NSREC short course that shows how a notional "brick wall" cross section would translate into upsets, or in our case, latchup events. In reality, the expectation is that the latchup would be fatal on the first latchup event, so it is not really technically correct to call this a rate, but this gives a way to notionally translate into hours to first failure.

The graph shows a notional upset rate plot of upset rate vs LET, assuming a step function cross-section of 100 square microns and charge collection depth of 1 micron, at a given LET. For example, at an LET of about 1.3 MeV-cm²/mg, the cross section would step up to 100um² with a 1 micron charge collection depth, and the resulting the latch-up "rate" is 1E-4 latch-ups per device-day for this GEO orbit at solar minimum (behind 50 mils of Al shielding). If we look at how long it would take for a failure, a random hit would take 2.4E5 hours. This translates to a FIT rate of 4170.

A typical IC FIT rate is much lower (1-100s of FITs) and depends on device complexity. Processors and memories can run into the 100's of FITs. If the latchup "rate" is around 1E-7 latches per day, that translates to a FIT rate of 4.17 which is on the order of the IC's baseline reliability number. If you look at using a device that has a threshold at an LET of around 75 MeV-cm²/mg (for our brick wall cross-section), that translates to roughly 2E-8 latchups per device-day and that is a FIT impact of around 1 FIT. The point here is that the program requirement of testing to high LETs means that a part tested that successfully passes that test criteria demonstrates a FIT rate impact that is essentially ignored. Higher FITs will likely impact the system reliability and availability and would have to be managed as part of the redundancy approach. It is usually easier (theoretically) to procure a better part, but there are trades in all designs.

Lower LET threshold latchup sensitive devices can also latch due to protons interacting with silicon or other atoms in the IC. This can drive rates substantially, even though it is a spallation reaction, due to the sheer number of protons during solar events or trapped in the proton belts. The bottom line? If you need your system to last, don't fly low LET threshold latchable devices if they must be continuously powered!

Reliability and Mission Duration

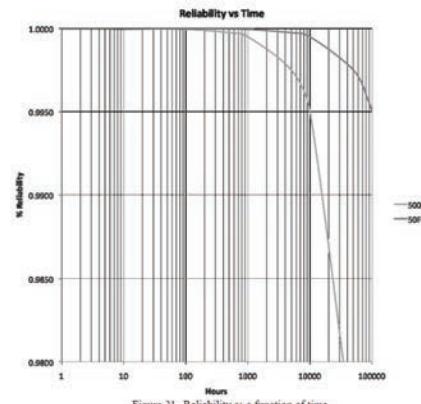


Figure 21. Reliability as a function of time.

Figure 21 shows reliability as a function of time for two different defect levels. Here, the exponential model is used. This means any defects will act independently in terms of how they cause a failure. Thus, a larger number of failures implies a higher failure rate. Failures as a function of time are measured in units of FIT's.

Sheldon IEEE NSREC 2009 Short Course



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- The mission duration intimately ties into the reliability requirements of the components selected. The plot shows an exponential model assuming that any defects will act independently in terms of failure cause.
- The 50 FIT device outlasts the 500 FIT device by a factor of 10.
- The 50 FIT device will have a 0.5% fail rate after 10 years vs 1 year for the 500 FIT device.
- Overall mission reliability requirements will dictate the allowable device FIT rate and redundancy strategy required
- This has implications for imposed requirements for single event destructive effects and program risk posture.

We looked at the impact of destructive events where we highlighted latchup's impact to the FIT rate of the part. This chart compares the percent reliability as a function of time for a part with a FIT rate of 50 vs a FIT rate of 500. A part that has a FIT rate of 50 has a 99.5% success rate for a 10 year mission whereas a part that has a FIT rate of 500 would only have a 99.5% success rate at 1 year, and the % reliability would drop off very quickly each year after that. Although not shown here, the failure rate for the 500 FIT part would be greater than 2% at 10 years. It would not take many of these devices cascaded in series to reduce the system reliability to lower than typical acceptable levels (e.g. 90% in a 10 year mission).

How to Make it Right? Mitigation Strategies

The environment (orbit), the type of mission, and the mission duration are key elements to understanding the limits of the design. Just because something has flown before does not mean that the “same” hardware is ok for the current mission. Beware the words “heritage” or, “this has flown before”. Find out if, and how, previous experience applies. We will review elements that help systems engineers manage space operation.

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Tools of the Trade

- Fault Tolerant Architecture
 - Design with function criticality in mind
 - Pick parts that help with hardware resilience
- Use monitoring & telemetry (i.e. watchdog timers, etc).
- Use redundant functions with cross-strapping
- Develop CONOPS
 - A **concept of operations** (abbreviated **CONOPS**, **CONOPs**, or **ConOps**) describes the characteristics of a proposed system from the viewpoint of an individual who will use that system.
 - This concept includes such system functions such as start-up, boot up, memory management, refresh, resets, diagnostic checks, scrubbing and recovery from hang-ups

Goal: Get your system to work well enough, and to recover when it doesn't.



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Systems are built with parts that will interact. When designing a system, the designer must understand the environment it will be in, the mission goals for availability, operational modes, durability and reliability. These key elements drive mitigation strategies, and certain functions demand higher system resilience. A command receiver, for example, will have a higher criticality than a unit that is primarily used for data processing.

The system designer must work with radiation engineers to understand what radiation will do to the system's building blocks. Radiation reactions can be identified and part technologies selected for applications based on system tolerance to upsets. Typically the radiation reactions are based on surveys of parts databases, but remember that any parts testing is done with certain parameters in mind. Key performance parameters need to be identified early to see if prior radiation tests adequately cover parameters required for a particular mission to be successful.

Many space systems have limited telemetry in terms of bandwidth and telemetered parameters. It is important to identify system parameters that can help anomaly investigations, because anomalies do happen! When an anomaly happens, the recovery process for system operation needs to be thought out as part of a flow diagram. What key parameters help determine what has happened? Has a failure occurred? How do you bring the system back online as fast as possible?

Most long term, critical mission systems provide redundant units and a means of cross-strapping interfaces between units in a system that will isolate a failed unit from a redundant cross strapped unit. The interfaces between cross strapped units are critical and must be carefully thought out for "what can go wrong?". Oftentimes these units involve the use of interface devices that are cold spare capable since most redundant units are not powered. Cold spare devices have specially designed ESD structures where interfaces can handle active inputs when no bias is present on a device. These prevent sneak power through ESD structures causing un-desired partial powering of the off unit.

Every system design team develops a concept of operations – how will this system be used and operated on a day to day basis? This includes a power up timeline for system startup and also includes processes for recovery of hang-ups or functional interrupts. There can be different types of system resets that occur at increasing levels of reset, including a hard power on reset as a “drastic” recovery measure. Any anomaly that occurs requiring this step is only done with much gnashing of teeth!

Operational Strategies

- The type of mission often defines acceptable strategies.
 - Complex systems will require a number of approaches to safeguard successful operation
- Know the environment.
 - Survival through harsher environments is easier to guarantee than operation through harsher environments.
- Some systems do not require that all elements are operated 100% of the time
 - Identify essential operations for the mission
 - For example, shut down power on sensitive hardware during critical environmental conditions in a particular orbit (such as the SAA or traversing the V-A Belts) for processors/devices that are sensitive.
- Systems can detect an elevated environmental condition by monitoring the SEU rate of sensitive detectors.
 - If high rates are observed, the system can set operation into an SEE safe mode for critical hardware.
 - Once the SEU rate falls below a predefined threshold, the system restores normal operation
 - Requires analysis of operational effects in harsher environments and process for handling the mode change including the threshold

IEEE 2017 NSREC Short Course, D. Roth P. 200



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Remember that the system goal is to get the system to work well enough to meet your mission requirements, and to have successful recovery strategies when it misbehaves. That means you must expect that you will need strategies to handle the system. Many systems do not require that all units operate at all times. That means these can be powered down if the environment is particularly harsh through different mission environmental regions. A good example of this strategy would be to power down a data processor while traversing the SAA to prevent annoying hang ups due to particle strikes.

Systems can use sensors to monitor the particle environment. The designer will establish thresholds so that any critical units can be put into a safe mode of operation (including powering it down) during high flux environments such as the SAA or Van Allen belts, or during harsh space weather conditions. Thresholds for resuming the function can also be established to return to safe operation. The safing and recovery process must be carefully walked through in detail by system and unit designers.

System Considerations

- Identify system vulnerabilities early in the program to establish critical functions and what each element of the architecture may be vulnerable to
- Identify where hardened technologies may be of value such as in command and control systems
 - The last thing you want is for the command receiver to shut down....
- Identify unusual requirements for parts performance to determine if standard radiation testing will be adequate
- Identify critical technology issues (thermal, reliability, radiation, packaging, floating metal) and work that early
- *Identify SEU impacts and strategies early and establish that as part of the system architecture*



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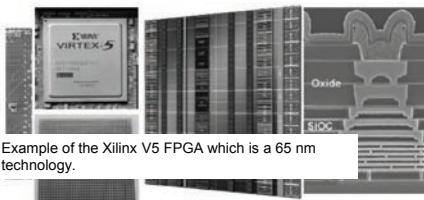
Robust system design starts early. Knowledgeable radiation engineers should work closely with designers to understand mission constraints and goal and determine viable system approaches and vulnerabilities. This should be done early in the program so that SEU impacts and parts strategies are identified early. This will also help determine parts procurement strategies.

Certain functions are so critical that they may require radiation hardened technologies. Command receivers are examples of units that must stay on since these act as the ears and brain of operating the satellite. The joke is that the last thing you would want a command receiver to do is to shut OFF! Obviously no command would ever be received again!

Why do I mention this? I was helping backfill two worn-out radiation engineers on a simple analog circuit heavy ion test. The two engineers had already been running beam for many hours characterizing other devices. We ran the first test so they could show me what they were looking to characterize on the circuit, where the output was expected to stay high. To their surprise, what we saw was that the output went low for a long period and then went high for a long period. I had them shut off the beam after the first reaction and we saw the state sustain. Long story short, the circuit was bi-stable and a particle strike could cause the function to lock up in either state, high or low. A particle strike would toggle the circuit. The circuit was used in the power distribution of a command receiver and it would actually cause it to shut down if the output went low. Obviously that was a big finding in the test and we changed the design to prevent the problem. The lesson? Examine transients and how they interact in your circuit and your system!

System Considerations

- There are other system concerns on top of the radiation impacts
- Packaging, thermal effects and local power distribution also impact system considerations
- How hard is it to provide safe biasing for the devices (absolute max)?
- How tightly controlled must these voltages be?
- What are the implications for single event transients and concomitant design requirements for power distribution?



Example of the Xilinx V5 FPGA which is a 65 nm technology.

Sheldon IEEE NSREC 2009 Short Course P86

Virtex-5QV FPGA DC Characteristics

Table 1: Absolute Maximum Ratings

Xilinx FPGA V5 Device specification

Symbol	Description	Value	Units
V_{CCINT}	Internal supply voltage relative to GND	-0.5 to 1.1	V
V_{AUX}	Auxiliary supply voltage relative to GND	-0.5 to 3.0	V
V_{CO}	Output drivers supply voltage relative to GND	-0.5 to 3.75	V
V_{BATT}	Key memory battery backup supply	-0.5 to 4.05	V
V_{REF}	Input reference voltage	-0.5 to 3.75	V
V_N	3.3V I/O input voltage relative to GND ^[1] (user and dedicated I/Os) 2.5V or below I/O input voltage relative to GND (user and dedicated I/Os)	-0.75 to 4.05 -0.75 to V_{CO} + 0.5	V
I_{IN}	Current applied to an I/O pin, powered or unpowered	± 100	mA
	Total current applied to all I/O pins, powered or unpowered	± 10	mA
V_{TS}	Voltage applied to S- and 3.3V pins (user and dedicated I/Os)	-0.75 to 4.05	V
	Voltage applied to state 3.3V or below output (user and dedicated I/Os)	-0.75 to 3.3V - 0.5	V
T_{STG}	Storage temperature (ambient)	-65 to 150	°C
T_{SOI}	Maximum soldering temperature ^[2]	+220	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.
2. For 3.3V I/O operation, refer to UG190: Virtex-5 FPGA User Guide, Chapter 6, 3.3V I/O Design Guidelines.
3. For thermal considerations, refer to UG120: Virtex-5QV FPGA Packaging and Pinout Specification.
4. 3.3V I/O absolute maximum limit applied to DC and AC signals.



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Power distribution for advanced systems includes many power forms for proper complex device operation. An example of a complex device is an ASIC or a Field Programmable Gate Array (FPGA) that use various biases. For example, Xilinx's V5 FPGA uses various voltage forms to properly operate the core internal supply, its IOs, analog blocks, clock distribution and clock management, etc. Oftentimes the voltage specifications for these devices are very tight to prevent device damage. The V5's absolute maximum ratings table shown on the lower right specifies that the core supply, for example, can only go to a maximum positive voltage of 1.1 V. That means that a POL or LDO that supplies that bias form, must be examined for single event transients and analyzed within the circuit context to determine if a transient will exceed the absolute maximum. If a transient exceeds this, further circuit mitigation is required.

System Mitigation

- Pick Your Parts
- Shielding & Materials selection
- SEE Mitigation
- Digital Systems with Flexible Platforms
- Power Systems
 - Power Distribution



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Key factors in system mitigation include picking the right parts, setting the right shielding levels (including the right materials for this), figuring out how to handle single event effects because those are not practically shieldable, handling radiation effects of flexible platforms, and determining safe power distribution including sequencing, and transient protection. Systems have other considerations beyond this, but these are heavy-hitters for most systems and will be touched upon in this section.

Learn Your System & Pick Your Parts

Table II: SEE Vulnerabilities of Electronics Technologies

SEL	SEGR	SEB	SEDR	Stuck Bit	SEU/MCU	SET	SEFI
CMOS	MOSFET	POWER MOSFET	One-time Prog. FPGA	SRAM	Digital/visible technologies	bipolar technology	Complex Microcircuits
Bipolar?	FLASH Schottky Diode	Power JFET Power BJT	Bipolar Microcircuits	DRAM FLASH	Deep submicron CMOS more MCU susceptible	Analog microcircuit Digital microcircuit	ADCs PWMs

Part-Level Consequences		How Common Is Issue?	
Catastrophic failure possible	Common in technology		
Destructive but limited	Catastrophic failure possible		
Nondestructive	Not seen but possible in principle		

R. Ladbury 2017 IEEE NSREC Short Course



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The table gives an overview of single event effects vulnerabilities for different hardware types. One of the most important strategies is to pick parts that are radiation resilient, and this means picking parts immune to destructive effects from particle strikes. Many CMOS devices, for example, have inherent latchable PNPN structures that cause high current flow and device damage. These types of structures were discussed in Balaji's and Daniel's talks on single event latchup (SEL). The danger of picking standard commercially available (cheaper) parts is that many of them will latch up with high current and destroy the device. Some devices will latch up and cause latent damage in heavy ion testing. This can be insidious if the conclusion drawn from device testing is that it survives the latchup condition without failing. There have been devices tested that initially survived the heavy ion test latchup condition only to fail early due to electro-migration from higher than normal currents in metallization structures. So while the part may appear to be a better choice because it is cheaper, an early mission failure is not often favorably looked upon.

Other types of damage due to particle strikes include single event gate rupture, single event dielectric rupture, and single event burnout. Procure power devices that are SEE hardened to mitigate SEGR and SEB concerns. Know what the safe operating areas are for power devices to prevent early system failures.

Pick Your Parts - Reliability

- If you can, pick parts you have flown before, or can get data on
- Parts are dominated by the requirements of the commercial marketplace (so buyer beware)
 - “Long Term” reliability for the commercial market is practically defined as 3-5 years and not the 10-15 years defined in certain space missions
 - Device design reliability decisions will be different for the commercial market
 - Commercial devices do not track process changes to the part for typical purchases
 - Process changes are designed to improve yield
 - ***Process changes can significantly impact the radiation responses***
 - Space missions typically use very low volume of parts and do not drive what the semiconductor industry is doing
 - Be aware of the processes used in your devices and understand the physics of failure
 - Look for packaging and thermal management issues



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The continuing scaling down of device features at new technology nodes presents challenge of creating reliability prediction models for known physics of failure mechanisms and may even introduce new failure mechanism peculiar to that technology. Smaller geometry devices operating at high speeds have higher current densities, higher electric field stresses, and tighter voltage tolerances than preceding generations. New materials and structures are being introduced as technologies scale. This poses a key question for space designers: how do the physics of failure models and reliability predictions match performance in the “real” world with real stresses in the application, as opposed to stresses introduced in accelerated life testing?

Long duration missions often require techniques to minimize the wear and tear on devices to extend the life of the part, or more advanced redundancy strategies will be required to bring spare parts online to backfill failed parts. Remember that redundancy does not reduce the SEE rates, but instead tackles the SEE consequences.

Pick Your Parts - Reliability

- To use commercial parts, it is best to buy the same wafer lot of parts and radiation characterize the lot.
- If this is not possible, a strategy might be to buy a number of device lots and look at radiation robustness over several lots.
- Characterization can start with cheaper tests and progress to more expensive tests
- Destructive mechanism tests can be used as discriminator tests to determine if the parts are useable



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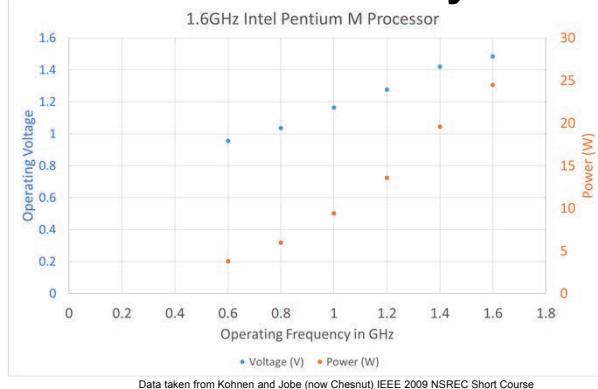
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Semiconductor manufacturers use device yield as a critical success parameter, and update their processes to improve yield. While these process tweaks are typically not an issue for terrestrial users, the impact of process tweaks to improve yield can cause huge impacts to radiation responses since radiation reactions are often due to parasitic structures that are not as well understood by the terrestrial designer (or manufacturer for that matter). For the space user that means the manufacturing lot (at the wafer level) can be critical in determining the radiation response. Prior lot data will not necessarily apply and each lot should be evaluated and characterized on its own merits.

Since these tests cost real dollars, tests can be performed as “weed out” tests where least costly tests are performed first. If the parts pass those tests, then more expensive characterization can be performed.

Reliability Strategies



- Operational frequency depends on the supply voltage
- Power depends on the square of the applied supply voltage * frequency*the number of switching gates*gate capacitive load (dynamic power) + voltage*leakage (static power)

Many integrated circuits are designed for a commercial market where the life of the product is 3-5 years. The spacecraft designer needs to understand the physics of failure and determine strategies to handle wearout mechanisms for any parts selected for the mission. The figure shows the impact of operating a processor at a reduced voltage. To determine successful system strategies, the device physics must be understood for critical applications.



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If a system needs to operate for an extended period beyond the intended design life of a product, an examination of lifetest conditions can be used to intelligently determine parameters that can be dialed down to reduce the wear and tear on the part given the physics of failures known. This plot of the Operating Voltage and Power vs. Operating Frequency of the 1.6 GHZ Intel Pentium M Processor shows how the processor can operate at lower voltage when the operating frequency is reduced.

Reducing the operating voltage by design can be a way of extending the life of a part if the operating voltage regime is well understood (if you go too low the device won't switch!). The advantage of such a strategy is that the power can be reduced significantly with this approach, and therefore the operating temperature. Temperature strongly impacts common failure mechanisms such as Temperature Cycling, Stress Migration, Time Dependent Dielectric Breakdown, and Electromigration. (P100 2009 IEEE NSREC Short Course, Sheldon and P.145 2009 IEEE NSREC Short Course, Kohnen)

Shielding and Materials Selection

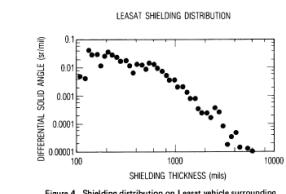


Figure 4. Shielding distribution on Leasat vehicle surrounding memory in attitude control electronics computer

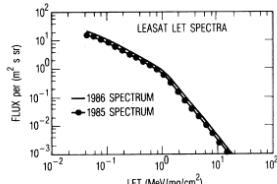


Figure 5. Calculated LET spectra based on heavy ion environment model and Leasat shielding distribution for two periods (early 1985 and mid-1986)

Verification of Single Event Upset Rate Estimation Methods with On-orbit Observations Shoga et al TNS 1987

Effects of Realistic Satellite Shielding on SEE Rates, Smith E. TNS 1994
distributions is given in Table I. As is evident, the customary assumption of 0.1 in. (0.686 gm/cm²) or less of shielding is

TABLE I
SATELLITE SHIELDING DISTRIBUTIONS
(Path lengths in inches)

SATELLITE	NUMBER OF RAYS/BINS	MINIMUM PATH	MEDIAN PATH	AVG PATH
TDRS-1	6000/450	0.07	0.25	0.55
LEASAT	1000/43	0.14	0.40	0.53
CRRES - 1	240/240	0.17	0.68	1.21
CRRES - 2	240/240	0.2	1.02	1.81

not a realistic estimate of the inherent shielding for these spacecraft.

Although our reference in our industry for upset rate comparison is 100 mils of Al, the average shielding of internal components can be much higher. For soft devices this can mitigate upset rates slightly, especially due to solar proton events, but in general:

Shielding helps for reducing TID, and IESD. Shielding is not typically an effective mitigation strategy for single event and displacement damage effects



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Typical spacecraft “reference” shielding is 2.5mm or 100 mils of Aluminum. This is often used for environment comparison purposes where the external environment is translated through the shield to get the internal environment for use in rate calculations. Often real spacecraft shielding is much higher than this, which can help mitigate TID and IESD. While shielding helps mitigate TID and IESD, it is not used for SEU or DD mitigation other than some mitigation of high proton rate conditions. SEU's must be handled using other techniques.

Rates Due to Different Environments Given Shields

DOBDS *et al.*: CONTRIBUTION OF LOW-ENERGY PROTONS TO THE TOTAL ON-ORBIT SEU RATE
IEEE 2015 TNS Partial table from P2450

Particle Type	Orbit	AI Shield thickness	# SEUs /bit-day		
			1a 20 nm UltraScale Config RAM, 0.95 V	1b 20 nm UltraScale Config RAM, 0.7 V	2 Vanderbilt FFs, design A
Low-Energy Protons	1400 km	GEO	100 mils 500 mils	3.5E-07 1.3E-08	5.5E-06 2.0E-07
		worst day	100 mils 500 mils	2.5E-09 9.4E-12	4.0E-06 2.9E-09
		ISS	100 mils 500 mils	3.7E-11 9.4E-12	7.8E-07 2.9E-09
	GEO solar min	100 mils 500 mils	4.5E-10 1.2E-12	7.0E-09 1.8E-11	1.4E-07 3.6E-10
		GEO	100 mils 500 mils	5.1E-13 1.2E-12	7.9E-12 1.6E-10
		worst day	100 mils 500 mils	1.4E-06 4.5E-07	6.8E-06 1.9E-07
High-Energy Protons	1400 km	100 mils 500 mils	3.6E-07 2.6E-07	4.9E-07 3.6E-07	1.6E-06 1.1E-06
		ISS	100 mils 500 mils	7.2E-09 5.3E-09	9.7E-09 2.3E-08
		GEO	100 mils 500 mils	1.2E-09 1.1E-09	1.5E-09 1.5E-09
	GEO solar min	100 mils 500 mils	4.3E-06 3.9E-08	— 4.5E-07	4.8E-05 4.8E-07
		GEO	100 mils 500 mils	5.1E-10 4.5E-10	7.5E-09 6.7E-09
		worst day	100 mils 500 mils	3.6E-10 3.1E-10	5.0E-09 4.5E-09
Heavy Ions	1400 km	ISS	100 mils 500 mils	— —	— —
		GEO	100 mils 500 mils	5.9E-09 3.6E-09	4.1E-08 3.0E-08
		solar min	100 mils 500 mils	— —	— —

- The environment can be quite dynamic and upset rates can change by orders of magnitude depending on the orbit
- Shielding has considerable impact on low energy protons for soft devices during worst day events but for a typical day would not offer much difference in performance.
- Shielding requirements may be driven by operational requirements for critical operation through coronal mass ejection events, depending on the technology.
- This table compares different 20 nm devices, CRAM at 0.95V and 0.7V, and 20nm Vanderbilt flip-flops. Note the upset sensitivity increase when the CRAM are at 0.7V.
- SRAM devices are known to be very sensitive to particle strikes and are often used to understand trends for heavy ion and proton radiation impact in new technologies



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This table compares upset rates of sensitive Configuration RAM (CRAM) bits and Flip Flops (FFs) at the 20nm CMOS technology node in different environments under different operating conditions and for different shielding levels. The first thing to note is how dynamic the environment can be, where rates change by OOM for different orbits, and for “flare” conditions shown for worst day vs. solar min at GEO. Shielding differences help slightly and are a higher factor for the worst day, but overall the rates with more shielding are comparable to less shielding; this points to the need for other mitigation techniques for single event effects. Note that shielding can benefit TMR’d architectures since that is very sensitive to flux.

While voltage can be lowered to extend the life of devices, lowering the operating voltage causes a concomitant increase in the single event upset sensitivity. That means that the upset cross section characterization should be performed at the minimum operating voltage for rate calculations. For example the upset sensitivity of CRAMs operated at 0.7V is a factor of 15 more sensitive for a GEO worst day.

Single Event Effects Mitigation

- Requirement: no SEE may cause permanent damage to a system or subsystem
- Implement SEE-Tolerant Circuit Design
 - SET mitigation: filtering, over-sampling, place high speed device with slow response time following circuit
 - SEL, destructive SEE mitigation: current limit and power cycle, use SOS/SOI technology (beware of SESB in SOI, but usually not destructive), limit operating windows for vulnerable parts, reduce operating voltage below latchup onset voltage, limit temperature range for SEL sensitive devices
 - SEU mitigation: redundancy (TMR), watchdog timers, EDAC, memory scrubbing, high refresh rates for SEU-susceptible memory
 - Derate Power MOSFET applications appropriately
 - non-SEE hardened Power MOSFETs derate to 20% of max V_{DSS} to mitigate SEGR & SEB

Ladbury 2017 NSREC Short Course



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The types of SEE mitigation strategies depend on what the effect is and what the system impact is. The details of how some of these are achieved has been covered by Balaji, Daniel and Vincent. To recap:

For SETs, the device reaction can be filtered, over-sampled, or a slower response time circuit can follow a high speed device.

For destructive events, some devices can be operated at lower temperature and voltage to keep the part operating in a safe operating area, or devices can be biased only when needed for the system function (i.e. limit the exposure time). Some systems use latchable devices where the current is limited and detected so autonomous cycling of power can keep the part from operating in a sustained high current (and life limiting) condition. This approach requires a lot of understanding of the structure and reliability impact.

SEU mitigation approaches include Triple Modular Redundancy, watchdog timers, Error Detection and Correction (EDAC), scrubbing of memory contents, and refreshing the contents of memories to avoid SEU error buildup.

Some devices require hardening of the device itself by altering the construction of the device. Techniques were covered in the earlier sections.

Digital Systems with Flexible Platforms

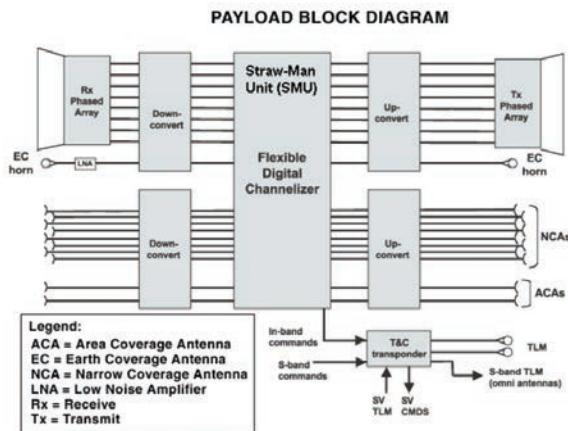


Figure 1. Hypothetical Digital Signal Processor.

Kohnen and Jobe 2009 NSREC Short Course

- Typical elements of a digital signal processor are shown, including a receive phased array antenna, through down-conversion to the flexible digital channelizer (SMU). This sends out the channelized data to the up-converter and then to the transmit phased array antenna for re-transmission.
- The SMU can contain ASICs and FPGAs to implement the function.
- Power must be distributed to the local circuits.
- These basic functions can be affected by radiation and radiation mitigation will be done at all levels.
- This will include parts selection, shielding, grounding of floating metal, and particle strike mitigation to handle upsets.



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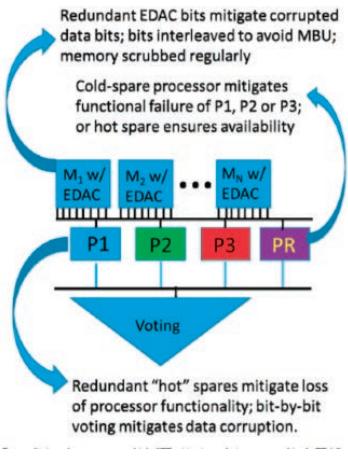


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The figure shows an example of a system that uses a digital signal processor to receive phased array data that is down-converted to a digital channelizer. The channelized data is sent to an up-converter and then retransmitted out the phased array transmission antenna. These units will contain ASICs and FPGAs to implement their functions where the operational mode is defined by a telemetry and command control transponder. Upsets to the different units will have a different impact and these impacts are assessed to determine how critical they are to the system function. Requirements for handling upsets are derived based on criticality. Some systems cannot have a down time (such as the previously mentioned command receiver).

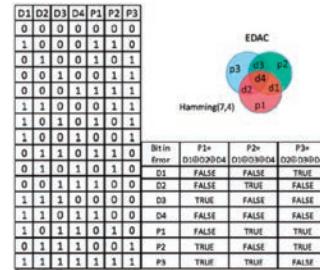
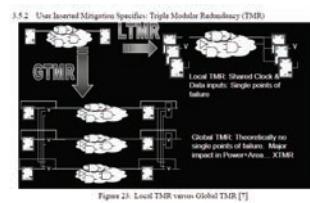
Every system will have clock and power distributions to support the operation. These elements must also be evaluated. This may seem obvious, but I have often seen only functional block diagrams where the supporting circuits are not even discussed. For “simple” systems, this omission could be literally catastrophic.

Radiation Tolerant Systems



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- Radiation tolerant systems combine multiple SEE mitigation techniques.
- The specifics of these techniques such as TMR, EDAC, scrubbing, and bit interleaving were covered in the early short course sections.
- Typical systems combine all of these.



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Within the functional blocks, each unit will require multiple mitigation techniques implemented at different levels of the hardware. The figure on the left shows three processors using independent memories to boot up the processor. The outputs are voted on where two out of three win the vote. This presumes that errors are independent in each TMR string.

A miss-compare requires a technique to restore the processor that is out of step with the other two, if the error cannot be tolerated. This can mean re-loading the data into the processor, or perhaps re-powering the processor depending on the nature of the issue. A full power on reset of all processors would be considered a major intervention, as would retiring the errant processor and bringing on a redundant processor (depending on the hit to system availability). If the system can maintain operation using two out of three of the processors while it recovers, this is not as "bad" as having to bring the system down and then re-boot where the operating condition is re-loaded.

TMR can be done with a global approach where all of the circuitry is replicated including the clocks, data, and control signals, or through a local TMR where shared paths exist. Shared paths are a source of upsets that can defeat the TMR and these will need rate calculations.

EDAC is used by augmenting the normal number of bits with auxiliary bits (known as parity bits) used to help decode if the data state is intact. The example shown has 4 data bits and 3 parity bits and is known as a Hamming 7,4 code. This particular example can detect and correct one error (SEC). The addition of one more parity bit allows the detection of two errors although the bit correction cannot be done with this approach (SECDED – single error correct, double error detect).

Isolating a Failed Path

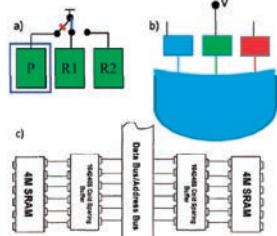


Figure 6-4 Reliability and availability are competing metrics with respect to redundancy. a) If a triple redundant scheme is configured with cold spares, only one device is susceptible to failure (both R1 & R2 at a time), and 2 out of 3 devices are available. b) For a triplicate system configured to maximize availability (and/or data integrity), all three devices are biased and available to failure (one R1). c) A cold spare system requires isolation of the failed device at the crew using a switch [16].

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- System availability is one of the key performance drivers for system architectures
- That often translates to a unit or module level redundancy plan that requires multiple instances of a function, where the function can get switched in if a failure or anomaly occurs
- One of the bigger issues with redundancy is the presence of a cold spare (unpowered) functional element.
- The separate power domains require the use of cold spare capable devices that can handle activity on the IOs prior to bias application to prevent sneak paths.
- Cold spare means that a device can handle input drive levels when the bias to the device is either floating or at ground.



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Spare functions can either be biased (“hot” spare) or unbiased (“cold” spare). The nature of the cold sparing techniques requires careful interface considerations to avoid sneak paths causing inadvertent biasing through IC IO ESD structures across power domains. If the part’s peculiarities require cold spare operation due to the type of single event reactions (such as destructive effects) then you need to make sure there is no power to the device, and it is truly OFF.

There will be devices designed with special ESD structures so that stimulus on IOs prior to the application of bias will have very low leakage levels (to within certain voltage ranges). Absolute maximum rating tables and IO descriptions can be very helpful in determining potential cold spare issues. Sometimes IO IV curves need to be generated to understand the impact of stimuli at IOs when the bias is not ON. A designer must pay close attention to the definition of cold spare since an operating condition that does not match that condition could represent a problem for the part to achieve a high impedance state for its IOs.

Flexible Platforms: Re-programmable FPGA

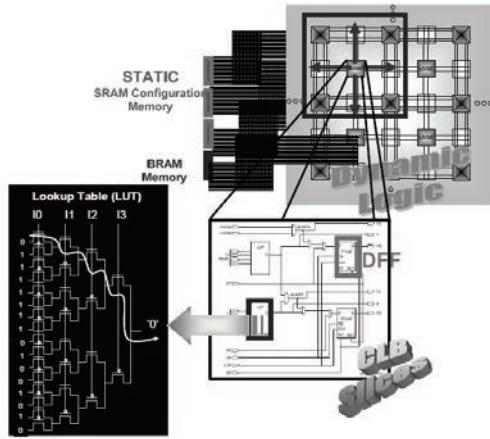


Figure 35. Xilinx Virtex-4 Architecture Containing SRAM Configuration Memory, Block RAM, and Dynamic Functional Logic blocks

From M Berg 2009 IEEE NSREC Short Course

- Many systems are moving to re-programmable FPGAs due to flexibility requirements
- The flexibility is due to the re-programmability of the FPGA, so the personality of the FPGA can be changed "on the fly" if a change in function is required.
- The functions are based on soft configuration memory (CRAM), so the CRAM bits can easily be upset by heavy ion and proton strikes.
- 10% - 15% of these CRAM are considered critical and if they change state, can create a fatal flaw
- The system must react to these in a safe fashion and design mitigation requires very careful consideration



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While re-programmable devices have the "sexy" feature of re-programmability, certain aspects of that re-programmability lead to concerns about "what could go wrong?" These devices use particle-strike soft devices called configuration RAM (SRAM that holds the configuration information) that are programmed to define the function of the part. These CRAM states connect hard-wired blocks such as look up tables (LUTs), dynamic functional logic blocks (Configuration Logic Block slices), block RAM memories and clock distribution systems.

System engineers work hard to determine the system effects of particle strikes to CRAM and approximately 10-15% of the FPGA CRAM bits are considered system critical. The system designer must determine what the reaction of the system will be to these critical upsets, and the recovery process required to bring the system back online. The system designer must also make sure that no upset results in damage to any downstream system or functions. How does the system designer make these determinations? One possible technique; fault injection testing, will be discussed in this section of the short course.

Re-Programmable FPGA Strategies, Continued

- To keep the function online, the CRAM contents must be checked to make sure they have not been corrupted, and if they have, the errors must be scrubbed
- This can be through a detection of a loss of critical CRAM state to flag re-writing to the CRAM
- The system must also be capable of possible power cycling to re-establish operation
- The recovery process must be carefully thought out and planned for levels of intervention required
- The reaction of the system must be analyzed to make sure no lock up conditions exist.

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The scrubbing process writes over configuration upsets with the correct bit information. Xilinx has developed an infrastructure wherein scrubbing can be performed during device operation without disrupting functionality. This can be used to clear accumulated errors. To support the scrubbing process means that the system will need a means of updating the CRAM with a “golden” image. That requires that the system have:

- Non-volatile memory access and control
- Possible Error Correction and Detection of non-volatile memory
- Configuration memory interface access and control
- Possible EDAC (such as a CRC checker) of configuration memory
- Supplemental non-volatile memory to support read back of the configuration

If the function is not critical, the scrubbing can be done based on detection of an issue, or at some periodic but manageable rate such as once a day. The overall scrubbing operation power required is reduced since scrubbing is done infrequently. The scrub rate must be determined based on the system requirements and the CRAM upset rate in the mission environment.

FPGA Design Strategies

- The SEU upset estimates can be calculated from a bottoms up estimate depending on the FPGA primitive blocks used.
- The table below shows an example rate estimate
- This design is dominated by CRAM upset rates
- Note that sections of the representative design are TMR'd and others are not. These are accounted for separately since TMR'd paths upset rates are very flux dependent (clobbering two chains)

Mitigation Technique	Primitive	# of Occurrences	Normalized Mitigated Upset Rate (CRAM Only) (upsets/year)	Normalized Mitigated Upset Rate (All) (upsets/year)	Upset Rate Contribution of CRAM	Device Feature (Includes Routing)	Approximate Number of Configuration Bits	
Using Fault Injection to Predict the Error Rate of a Large Complex Designs in a Non-Hardened SRAM-Based Xilinx 7-Series FPGA. Flanagan, P. et al 2020 SEE/MAPLD	TMR	CRAM FF DSP BRAM	1.09E+07 1.71E+05 1.44E+03 4.05E+02	0.71	0.71	95.84%	Logic Slice	1166
		CRAM FF DSP BRAM	1.07E+06 8.32E+03 0.00E+00 0.00E+00				Block RAM (36 Kb)	9396
	Non-TMR	BRAM MGT I/O Clock Generator (PLL and MMCM) Chip I/O	8.00E+00 3.00E+00 2.91E+02	0.93	1.00		Block RAM (18 Kb)	4698
		Total:	1.64	1.71			I/O Block	2850

CRAM estimate per FPGA feature from Xilinx SEM IP user guide



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The table shows bottoms up estimates of a design where sections of the design have been mitigated using TMR, and where some sections of the design cannot be TMR'd. For example, in this design 1.09E7 CRAM bits are used in the TMR'd portion of the design, and 1.07E6 CRAM bits have been used in the Non-TMR'd sections of the design. Note how the total number of CRAM bits dominates the number of occurrences of other elements in the design. Having a portion of the design reside in non-TMR'd sections is a common issue in system designs, for example, there may be limitations in the number of IO blocks available where TMR'd IO branches are not possible, or timing issues may cause limitations. TMR "clobber rates" are sensitive to particle flux and these types of designs should be closely reviewed for flare conditions.

For a standard assessment, the number of primitive functional blocks is determined and the resulting upset rates of the overall design can be determined against the upset rates of the CRAM bits themselves. The number of critical configuration bits can be estimated using user guides provided. This example shows how the CRAM bits contribute to almost 96% of the overall device upsets, although the criticality nature has not been determined here. The determination of system function criticality is a key component of the single event effects assessment.

Testing Re-Programmable FPGAs

- For devices **where the CRAM is soft** and upsets are dominated by CRAM upsets, a very useful fault injection test strategy has been proposed by P. Fleming, et al at the 2020 SEE MAPLD symposium based on tests of the Xilinx FPGAs.
- CRAM bit fault injection can be used to determine the number of critical bits and the system impact of the fault
- The design can more easily be modified to mitigate and then re-tested via fault injection prior to any beam run to save money
- Fault injection correlation to beam data has been demonstrated
- Fault injection's constant flux makes it especially useful for TMR designs with a flux dependency. These are difficult to test in the beam due to minimum flux limitations.
- Fault injection, in conjunction with prior beam tests and bottom up analysis is sufficient to demonstrate compliance to the SEU requirement for soft CRAM based FPGAs

Using Fault Injection to Predict the Error Rate of a Large Complex Designs in a Non-Hardened SRAM-Based Xilinx 7-Series FPGA, Fleming, P. et al 2020 SEE/MAPLD



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One of the “revolutionary” considerations for SEU soft programmable devices is that the dominant factor for upset rates for the function of the part is CRAM upset contributions as shown previously. Because these dominate, it is very useful to use fault injection to alter the contents of these configuration bits to determine the impact effect and if any of these effects are system critical.

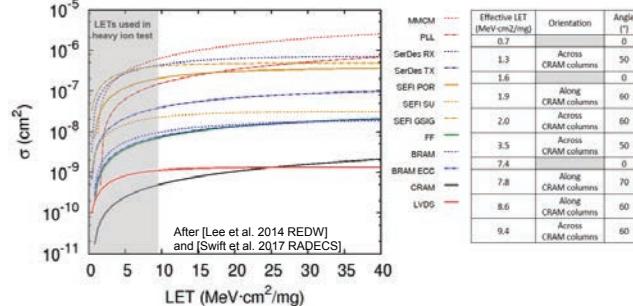
The fault injection tests can be used during beam test preparation for design mitigation strategies – this will help minimize the number of runs required to build a successful design.

Since TMR'd design success is very particle flux dependent, fault injection can be a strategy for parsing out the impact of the flux to the TMR'd portions and to help understand implications of beam testing where the beam's flux level will not be low enough to prevent impacting two TMR strings within a critical timing window. This creates a test artifact that would have a much lower probability of occurrence in a “real” space environment (other than possible flare conditions where the flux climbs by orders of magnitude).

Heavy Ion Test Conditions

Effects unique to beam testing have immeasurable impact on upset rate results

- XRTC flexible test platform
- Virtex-7 980T, delidded/unthinned die
- Nominal voltages
- Die temp ~30 °C
- Texas A&M 40 MeV/a.m.u. heavy ion cocktail
 - Ar, Ne, N ions used



Using Fault Injection to Predict the Error Rate of a Large Complex Designs in a Non-Hardened SRAM-Based Xilinx 7-Series FPGA, Fleming, P. et al 2020 SEE/MAPLD



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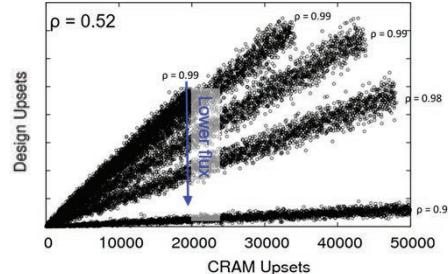
A particle beam can hit any element within the FPGA, and it can be very difficult to parse out what part of the IC causes a peculiar signature. Each design will combine the FPGA elements in a fashion that is unique to that design. Since the heavy ion test beam flux is very high compared to normal space particle fluxes, it can be difficult to determine the impact of the beam properties on the test results and true upset rates of the design given more normal particle strike rates. This is especially true for very soft devices where mitigation strategies have been employed.

The plot shows the heavy ion cross section curves for the various building blocks including SEFI types within the FPGA and shows that sensitivity depends on what you are hitting. The MMCM (mixed mode clock manager) for example, is a complex block that has a three OOM higher cross section than the CRAM. However, as seen in the previous charts, even though the CRAM has a lower cross section per bit, the sheer number of CRAMs used in the design will cause the CRAM upsets to dominate upset effects overall. In the previous bottoms up design example, 3 MMCM blocks are used, but over 1.2E7 total CRAM bits are used.

Virtex-7 fault injection methodology has been validated with beam data

Correlation analysis of design upsets to CRAM upsets validates fault injection methodology

- Monte Carlo simulation measures impact of flux on correlation
- CRAM upsets are the ONLY cause of design upsets in Monte Carlo simulation
- A dataset containing various CRAM upsets per scrub (analogous to flux):
 - Shows clear grouping by flux
 - Has increased scatter ($\rho < 1$)



Using Fault Injection to Predict the Error Rate of a Large Complex Designs in a Non-Hardened SRAM-Based Xilinx 7-Series FPGA, Fleming, P. et al 2020
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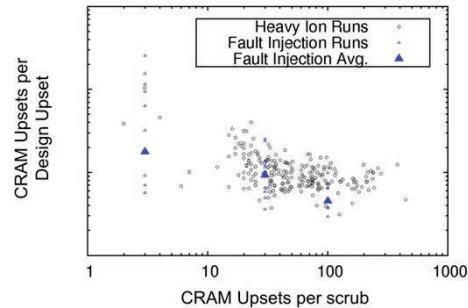
Because the CRAM upsets are so dominant, certain test strategies using fault injection can be used to determine the majority of upset impacts. This helps with impact determination and design modification for mitigation since these can be evaluated with bench testing. Designs can be refined and then brought to a heavy ion particle test in a more mature design state.

Fault injection clearly illustrates the impact of having more CRAM upsets per scrub which is analogous to higher particle fluxes. If the test's heavy ion particle flux cannot be brought low enough based on how many CRAM bits can be impacted per scrub cycle, then the design can upset in a fashion that is not probable in the lower particle flux environment in space. The chart shows how the lowest flux has the lowest design upset rate since the TMR'd function is able to successfully mitigate. If two chains can get clobbered, the design can be upset. Fault injection can be used to determine if a heavy ion test flux created a test artifact that is not likely given normal particle fluxes.

Virtex-7 fault injection methodology has been validated with beam data

Fault injection data compared to particle beam data

- Given the beam's flux variation, to measure the flux dependency one must use fluxes that span multiple orders of magnitude
- Large Block TMR designs exhibit flux dependency at low end of the heavy ion beam's flux capability
- While a beam test will include FF and BRAM hits, their impact is obscured by the flux variation



Using Fault Injection to Predict the Error Rate of a Large Complex Designs in a Non-Hardened SRAM-Based Xilinx 7-Series FPGA, Fleming, P. et al 2020 SEE/MAPLD



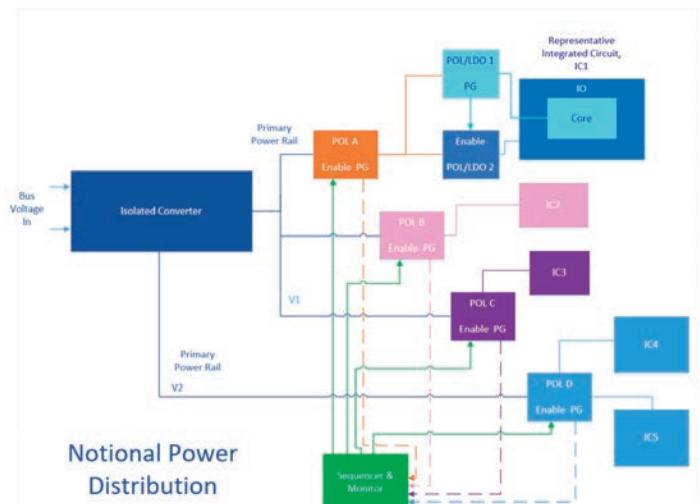
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For soft SRAM based FPGAs, the particle beam flux variability has a huge impact on heavy ion testing and will dominate flip flop and BRAM hits just because of the sheer numbers of CRAM devices present. This plot shows that the number of CRAM upsets per design upset varied considerably in the beam. Much of the variability was due to beam flux variations that cannot be controlled. Fault injection could be used to help understand flux impact and disentangle expected device impacts during “normal” rate conditions and “flare” conditions. Both are important when using soft devices.

Power Systems



- The Notional Power Distribution (NPD) shows elements of a conventional system that uses point of loads, load switches (not shown), and low dropout regulators to deliver biases to downstream integrated circuits and transistors.
- Many circuits require sequencers for power up and power down control.
- The sequencing requirements are driven by the specifics of each device used in the system
- Ask yourself:
 - What does the POL output do with my circuit?
 - What would happen if a sequencer control signal is hit?
 - Can an element drop out and create a bias concern for my circuit?



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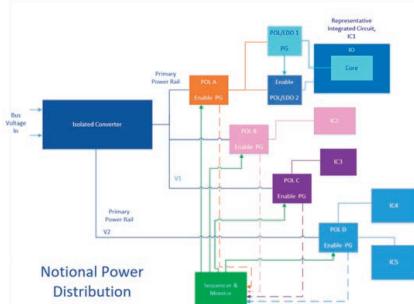
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All systems require some form of power distribution from the spacecraft bus (typically up to 100-110V) down to the specific voltages needed by complex integrated circuits. This has become even more critical with the advent of devices that have narrow supply ranges where the absolute maximum voltage requirements must be tightly controlled. Devices often have sequencing requirements to prevent damage or lockup modes, and these sequences must be adhered to for power up and power down (if this prevents device damage).

Lower level power distribution devices used include point of loads (POLs), low dropout regulators (LDOs), and load switches. These have control circuitry associated with them to enable sequencing and regulation. Many power distributions include a monitor circuit that shuts down the local distribution if an out-of-sequence event occurs.

Sequencing imposes derived single event effects system requirements to prevent events that can cause device damage. The reaction of each device in the power distribution must be evaluated to determine if the device behavior, due to a heavy ion strike, causes an out-of-sequence behavior. The impact of these need to be assessed for criticality and mitigation strategies.

Power Distribution Considerations



Virtex-5QV FPGA DC Characteristics

Symbol	Description	Value	Unit
V_{CO}	Internal supply voltage relative to GND	-0.5 to +1.1	V
V_{CCO}	External supply voltage relative to GND	-0.5 to 3.0	V
V_{DD}	Output drivers supply voltage relative to GND	-0.5 to 3.75	V
V_{KMR}	Key memory battery backup supply	-0.5 to 4.05	V
V_{SS}	3.3V IO input voltage relative to GND (user and dedicated I/Os)	-0.75 to 4.05	V
V_{IN}	2.5V or below IO input voltage relative to GND (user and dedicated I/Os)	-0.75 to $V_{CCO} + 0.5$	V
I_{IN}	Current applied to an I/O pin, powered or unpowered	<100	mA
V_{IO}	Voltage applied to 3-state 3.3V output ⁴ (user and dedicated I/Os)	-0.75 to 4.05	V
V_{O}	Voltage applied to 3-state 2.9V or below output (user and dedicated I/Os)	-0.75 to $V_{CCO} + 0.5$	V
T_{JMAX}	Silicon temperature (ambient)	-85 to 150	°C
T_{MAX}	Maximum soldering temperature ⁵	<200	°C

Notes:

- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time might affect device reliability.
- For 3.2V IO operation, refer to UG100: Virtex-5QV and Virtex-5QX Chapter 3.2V IO Design Guidelines.
- For 2.5V IO operation, refer to UG100: Virtex-5QV and Virtex-5QX Package and Pinout Information.
- 3.3V IO absolute maximum limit applied to DC and AC signals.



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- SEU requirements for Class A missions usually include “do no harm”, i.e. the part itself cannot die due to a radiation effect and *it cannot cause collateral device failures*.
- POL and LDO downstream devices often have very tight absolute maximum voltage requirements (e.g. the V5 core can only go to 1.1V maximum)
- The PD can have transients due to particle hits in the control logic and these need to be carefully assessed for the transient impact that could cause harm.
- Be aware that any vendor produced data is based on the test circuit that they used and *assess what that means for your application circuit*.

Device specifications include an absolute maximum table that guide the systems engineer for transient requirements. Some device inputs cannot safely be driven prior to the application of bias to the part. An example of this is shown in the table for the Xilinx V5 FPGA for Vin with a 2.5V IO where the lower voltage minimum is -0.75V and the maximum voltage is $V_{CCO} + 0.5$ V. This can be an important requirement for sequencing across different power domains, and for assessing single event effects.

POL, LDO and load switch single event transients must be analyzed and/or tested using the application circuit since the types of bypass capacitors used and their equivalent series resistances are key parameters that can really affect the transient amplitude. My favorite quote from a power system designer? “The power supply survives the transient just fine.” Remember: the last transient a system engineer wants to see is a “killer” spike affecting downstream devices!

Conclusions

- The history of space operation includes anomalies that expanded our knowledge of space and its radiation effects
- Based on what we have learned, we can apply design techniques from the material level to the device level, and then mitigate the system architecture to successfully harden our spacecraft systems. Techniques and specifics are mission driven.
- As technologies evolve, the missions will evolve, and we will have new problems to solve (it has never been boring....)

Thank you!



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We know that anomalies will happen in space; the environment is much harsher than the benign environment we have here on planet Earth and we already have anomalies enough with computer systems here! Remember, satellite hardening is not something that is “tossed over the fence” and painted on at the end of the program. It is a key system driver for system architectures and must be built into the design process from the very beginning. Even if a specific design has flown before, the requirements for that original mission may not apply to the new mission, so review these situations very carefully. The good news is that there are proven techniques for maximizing system availability even in harsh environments.

New missions will have new requirements based on new technology and new technology capabilities. Missions evolve creating new problems and these require new, creative solutions. We need to keep our ears and eyes open to new effects and think about what could go wrong...and more importantly, how to mitigate new effects and make it right!



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Short Course Chart	Title	First author	Source	Year	Page	location
1	no references					
2	no references					
3	The exhaust plume from space shuttle Atlantis is seen as it launches from pad 39A on Friday, July 8, 2011, at NASA's Kennedy Space Center in Cape Canaveral, Fla. Original from NASA. Digitally enhanced by rawpixel					
			https://www.rawpixel.com/image/440701/free-photo-image-nasa-florida-space-rocket			
4	Images from the central Milky Way	DNA	Rawpixel Public Domain	2011		
5	NSREC 2011 Short Course Ecotet	Robert Ecotet	Rawpixel Public Domain	2011	288	
5	Pictures of women who computed the Explorer I Trajectory general information		IEEE NSREC			
5	154354main/Vanalien_explorer_300.jpg [300x297] (nasa.gov)		http://www.nasa.gov/mission_pages/explorer/computers.html			
5	Explorer 3 geiger counter overwhelmed at top of belts					
6	Wikipedia SEU					
6,7	Satellite Anomalies From Galactic Cosmic Rays	Binder, Smith, Holman	IEEE TNS	1975		
6	Basic Mechanisms and Modeling of Single-Event Upset in Digital	Dodd and Massengill	IEEE TNS	2003	583	
6,7	Single Event Upset of Dynamic RAMs by Neutrons and Protons	Guenther	IEEE TNS	1979	5048-5052	IEEE Explore
8	NSREC 2011 Short Course, Garrett	Garrett, Hank	IEEE NSREC	2011	89	
9	Impact of Space Weather on Satellite Operations and Terrestrial Systems	Jokiah	AIAA			
9	solar flare picture	NASA.gov				
9	Space Weather Conditions During the Galaxy 15 and Telstar 401 Satellites Anomalies	Cid Consuelo	IEEE Explore	2017		
10	no references					
11	Risk Classification and Risk-based Safety and Mission Assurance	Leither	NASA	2014		
12	photos from various public domain sources					
13	Orbital Altitudes image		Wikimedia			
14	Orbital Belts with Satellites NASA		http://en.wikipedia.org/wikil/Satellite#mediaviewer/File:OrbitalAltitudes.jpg			
15	Catalog of Earth Satellite Orbits (nasa.gov)		https://www.nasa.gov/mission_pages/sunearth/news/gallery			
16	Catalog of Earth Satellite Orbits (nasa.gov)		Catalog of Earth Satellite Orbits (nasa.gov)			
17	Recent Progress in Space Radiation Environment Models	Xapsos, Barth Lauenstein	Space Power Working Group	2005	P. 12	
17	Dipolar magnetic field tilted and off center wrt Earth picture	Bourdaire	IEEE NSREC Short Course	2014	P. 11	
18	NSREC 2014 Short Course Adell and Boch	Philippe Adell and Jerome Boch	IEEE NSREC	2014	P. 45	
18	NSREC 2014 Short Course Adell and Boch	Philippe Adell and Jerome Boch	IEEE NSREC	2014	P. 42	
19	CONTRIBUTION OF LOW-ENERGY PROTONS TO THE TOTAL ON-ORBIT SEURATE	Dodds, Nathaniel A, et al	IEEE TNS	2015		
20	NSREC 1997 Short Course Barth	Janet Barth	IEEE NSREC Short Course	1997	PP. 18, 59	
20	Interaction depth see Kliwer/Cosmic_Rays/Interaction.htm	Kliwer, S.				
21	NSREC 1997 Short Course Barth	Janet Barth	IEEE NSREC Short Course	1997	P. 60	
22	no references					
23	NASA-HDBK-4002A MITIGATING IN-SPACE CHARGING EFFECTS –A GUIDELINE				P. 64	
24	no references					
25	NASA-HDBK-4002A MITIGATING IN-SPACE CHARGING EFFECTS –A GUIDELINE				P. 64	

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26	NASA-HDBK-4002A MITIGATING IN-SPACE CHARGING EFFECTS —A GUIDELINE				P.28	
27	NASA-HDBK-4002A MITIGATING IN-SPACE CHARGING EFFECTS —A GUIDELINE				P.30	
28	NASA-HDBK-4002A MITIGATING IN-SPACE CHARGING EFFECTS —A GUIDELINE				P.33	
29	no references					
30	Process variations and radiation effects in advanced transistors	Marc Gallardin	IEEE NSREC Short Course	2018 P.162		ESA Internal Course, EEE Component Radiation Hardness Assurance Tutorial, ESTEC, 4 November 2016
31	ESA Internal Course, EEE Component Radiation Hardness Assurance Tutorial, ESTEC, 4 November 2016	Hugh Evans	ESA	2016 P.48		ESA Internal Course, EEE Component Radiation Hardness Assurance Tutorial, ESTEC, 4 November 2016
32	ESA Internal Course, EEE Component Radiation Hardness Assurance Tutorial, ESTEC, 4 November 2016	Hugh Evans	ESA	2016 P.54		ESTEC, 4 November 2016
33	NSREC 1997 Short Course Barth	Janet Barth	IEEE NSREC Short Course	1997 P.64		
34	ESA Internal Course, EEE Component Radiation Hardness Assurance Tutorial, ESTEC, 4 November 2016	Hugh Evans	ESA	2016 P.62		
35	NSREC 2017 Short Course Ladbury, R.	Ray Ladbury	IEEE NSREC	2017 P.80		
35	NSREC 2018 Short Course Mangeret, R.	Renaud Mangeret	IEEE NSREC	2018 P.114		
35	NSREC 2017 Short Course Ladbury, R.	Ray Ladbury	IEEE NSREC	2017 P.94		
36	NSREC 2017 Short Course Ladbury, R.	Ray Ladbury	IEEE NSREC	2017 P.100		Original table generated from Ray's short course
37	NSREC 2017 Short Course Ladbury, R.	Ray Ladbury	IEEE NSREC	2017 pp. 93-99		Original table generated from Ray's short course
38	NSREC 2017 Short Course Ladbury, R.	Ray Ladbury	IEEE NSREC	2017 pp. 93-99		Original table generated from Ray's short course
39	no references					
40	NSREC 1997 Short Course Petersen	Ed Petersen	IEEE NSREC Short Course	1997 P.224		
41	NSREC 2009 Short Course Sheldon	Doug Sheldon	IEEE NSREC Short Course	2009 P.111		
42	no references					
43	Concept of operations - Wikipedia					Concept of operations - Wikipedia
43	NSREC 2017 Short Course Ladbury, R.	Ray Ladbury	IEEE NSREC Short Course	2017		
44	NSREC 2018 Short Course Roth, D.	David Roth	IEEE NSREC Short Course	2017 P.200		
45	NSREC 2017 Short Course Ladbury, R.	Ray Ladbury	IEEE NSREC Short Course	2017		
45	NSREC 2018 Short Course Roth, D.	David Roth	IEEE NSREC Short Course	2017 P.200		
46	NSREC 2009 Short Course Sheldon	Doug Sheldon	IEEE NSREC Short Course Xilinx	2009 P.86		
46	Xilinx V5 FPGA data sheet Absolute Max specifications			2016 P.1		
47	no references					
48	NSREC 2017 Short Course Ladbury, R.	Ray Ladbury	IEEE NSREC	2017 P.105		
48	NSREC 2017 Short Course Ladbury, R.	Ray Ladbury	IEEE NSREC	2017 pp. 124-126		
49	Integrated Circuit Reliability Prediction Based on Physics-of-Failure Models in Conjunction With Field Study	Hava, Avishalom	dfr Solutions	P2		
49	Accurate Quantitative Physics-of-Failure Approach to Integrated Circuit	Edward Wyrwas	dfr Solutions			https://www.dfrsolutions.com/hubs/Resources/services/PoF_Approach_Integ
50	NSREC 2009 Short Course, Kohnen and Jobe	Kirk Kohnen and Kay Jobe (now Che)	IEEE NSREC Short Course	2009		
51	NSREC 2009 Short Course, Kohnen and Jobe	Kirk Kohnen and Kay Jobe (now Che)	IEEE NSREC Short Course	2009 P.145		
51	NSREC 2009 Short Course, Sheldon, D.	Doug Sheldon	IEEE NSREC Short Course	2009 P.100		
52	Effects of Realistic Satellite Shielding on SEE Rates	Ed Smith	IEEE TNS	1994 P.2397		
52	Observations	Munir Shoga	IEEE TNS	1987 P.1258		
53	CONTRIBUTION OF LOW-ENERGY PROTONS TO THE TOTAL ON-ORBIT SEE RATE	Nathaniel Dodds, et al	IEEE NSREC Short Course	2015 P.2450		
54	NSREC 2017 Short Course Ladbury, R.	Ray Ladbury	IEEE NSREC Short Course	2017		
55	NSREC 2009 Short Course, Kohnen and Jobe	Kirk Kohnen and Kay Jobe (now Che)	IEEE NSREC Short Course	2009 P.129		
56	NSREC 2017 Short Course Ladbury, R.	Ray Ladbury	IEEE NSREC Short Course	2017 P.131		
56	NSREC 2009 Short Course, Berg, M.	Melanie Berg	IEEE NSREC Short Course	2009 P.189		
56	NSREC 2017 Short Course Ladbury, R.	Ray Ladbury	IEEE NSREC Short Course	2017 P.128		
57	NSREC 2017 Short Course Ladbury, R.	Ray Ladbury	IEEE NSREC Short Course	2017 P.129		

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58	NSREC 2009 Short Course, Berg, M.	Melanie Berg	IEEE NSREC Short Course	2009	P.206	
59	NSREC 2009 Short Course, Berg, M.	Melanie Berg	IEEE NSREC Short Course	2009		
60	Using Fault Injection to Predict the Error Rate of a Large Complex Designs in a Non-Hardened SRAM-Based Xilinx 7-Series FPGA (presentation)	Patrick Fleming	SEE/MAPLD 2020	2020	P. 3	
61	Using Fault Injection to Predict the Error Rate of a Large Complex Designs in a Non-Hardened SRAM-Based Xilinx 7-Series FPGA (presentation)	Patrick Fleming	SEE/MAPLD 2020	2020		general information of power point report
62	Using Fault Injection to Predict the Error Rate of a Large Complex Designs in a Non-Hardened SRAM-Based Xilinx 7-Series FPGA (presentation)	Patrick Fleming	SEE/MAPLD 2020	2020		
63	Using Fault Injection to Predict the Error Rate of a Large Complex Designs in a Non-Hardened SRAM-Based Xilinx 7-Series FPGA (presentation)	Patrick Fleming	SEE/MAPLD 2020	2020	P. 6	
64	Using Fault Injection to Predict the Error Rate of a Large Complex Designs in a Non-Hardened SRAM-Based Xilinx 7-Series FPGA (presentation)	Patrick Fleming	SEE/MAPLD 2020	2020	P. 8	
65	An SET-Free, Fully-Digital Point-of-Load Regulator for Next-Generation Spacecraft Power Systems	Nijjad Anabtawi and Rabih Chamour	IEEE Explore	2016	P. 1	Figure 1 of paper used to generate original graphics for short course
66	Xilinx V5 FPGA data sheet Absolute Max Specifications	Xilinx	Xilinx	2016	P. 1	Figure 1 of paper used to generate original graphics for short course
66	An SET-Free, Fully-Digital Point-of-Load Regulator for Next-Generation Spacecraft Power Systems	Nijjad Anabtawi and Rabih Chamour	IEEE Explore	2016	P. 1	Figure 1 of paper used to generate original graphics for short course