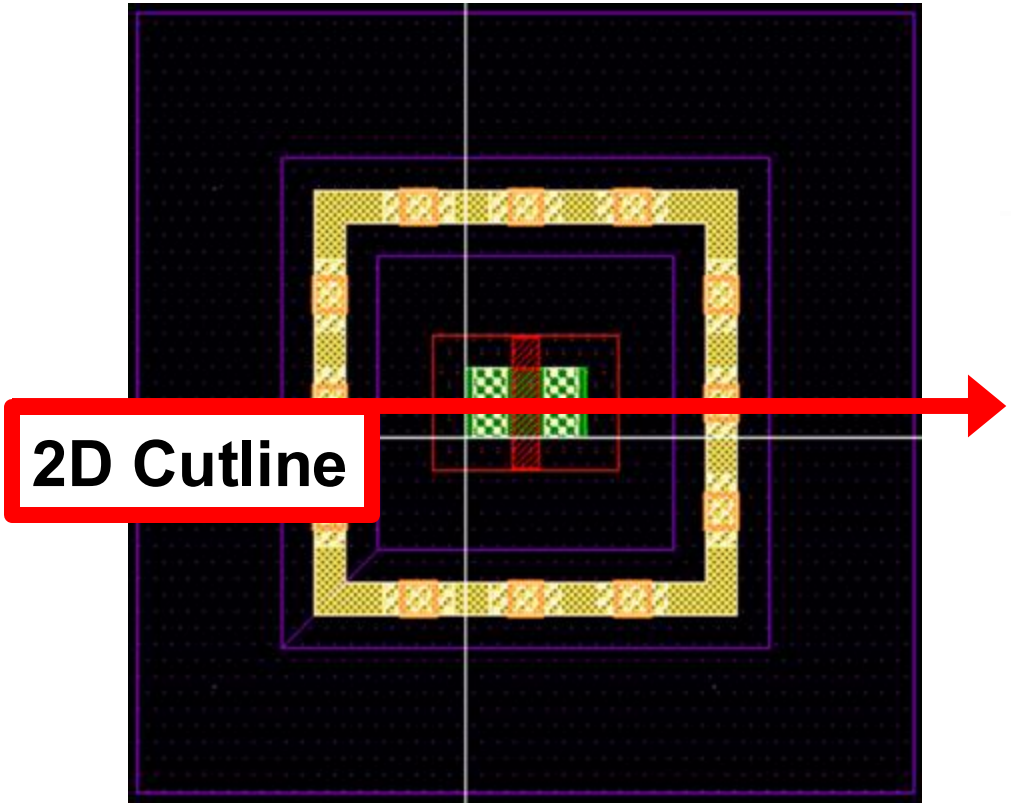
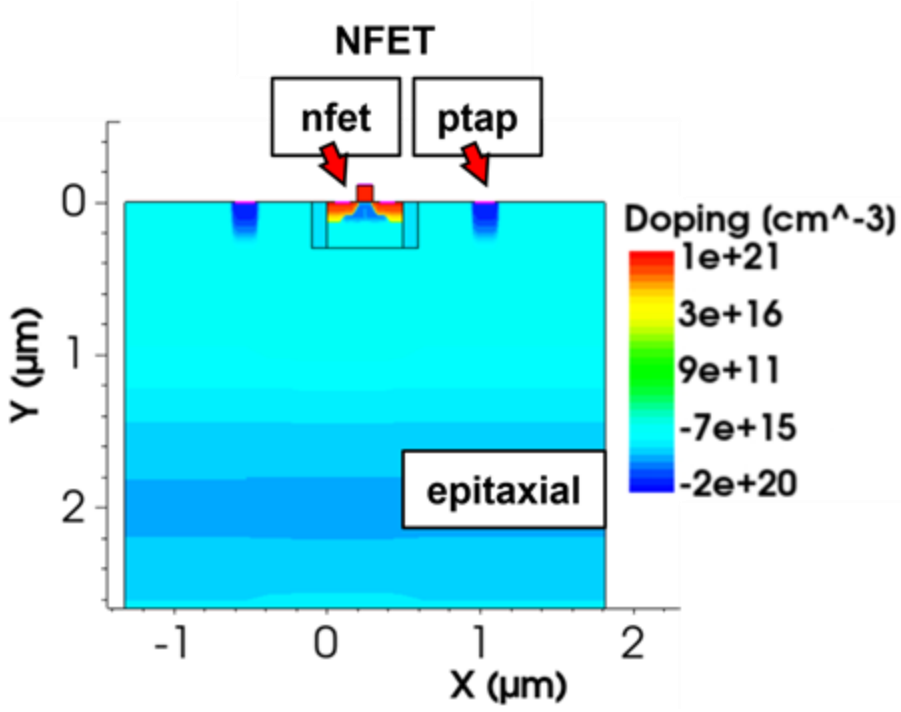
TCAD Modeling of SEE in a 90 nm Blk CMOS Process

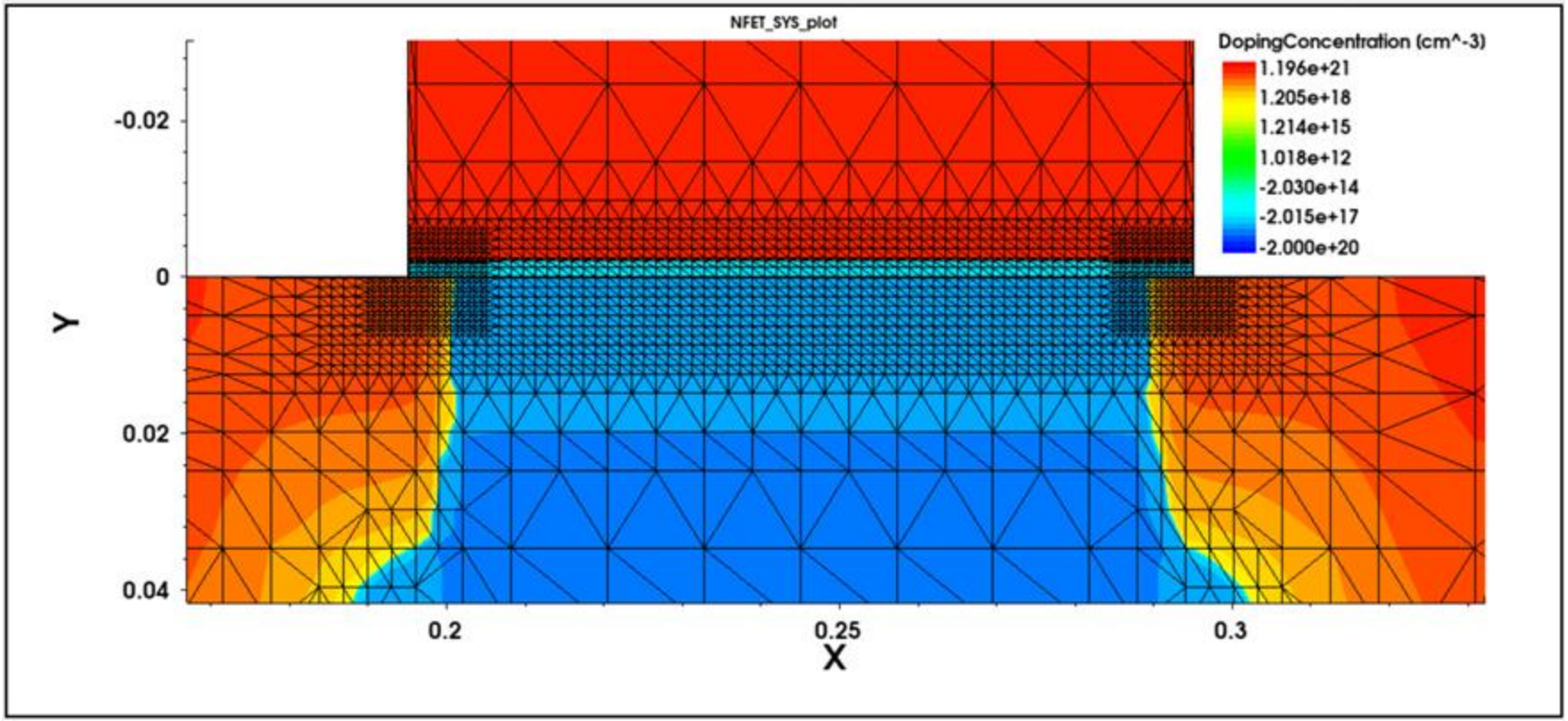
Courtesy John Barney | barneyjo@iu.edu

Layout (left) & TCAD Model (right)

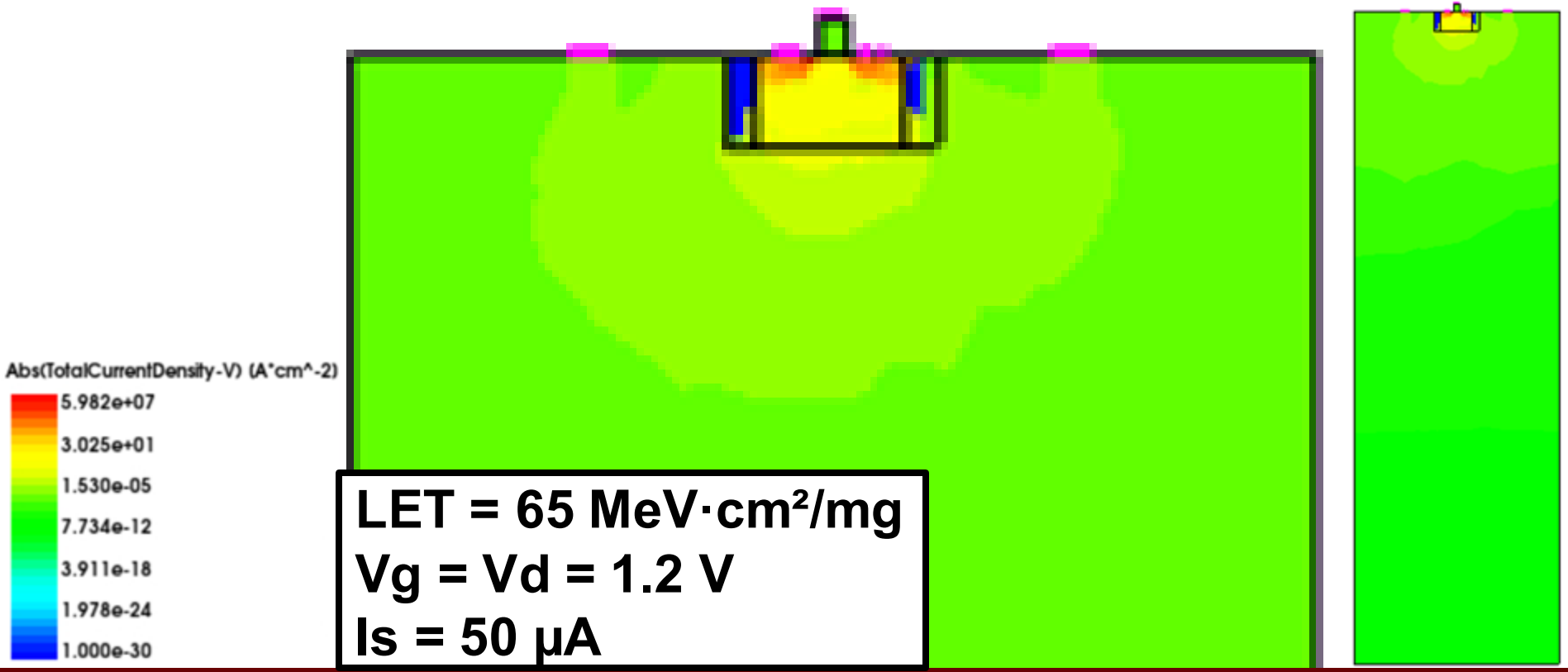




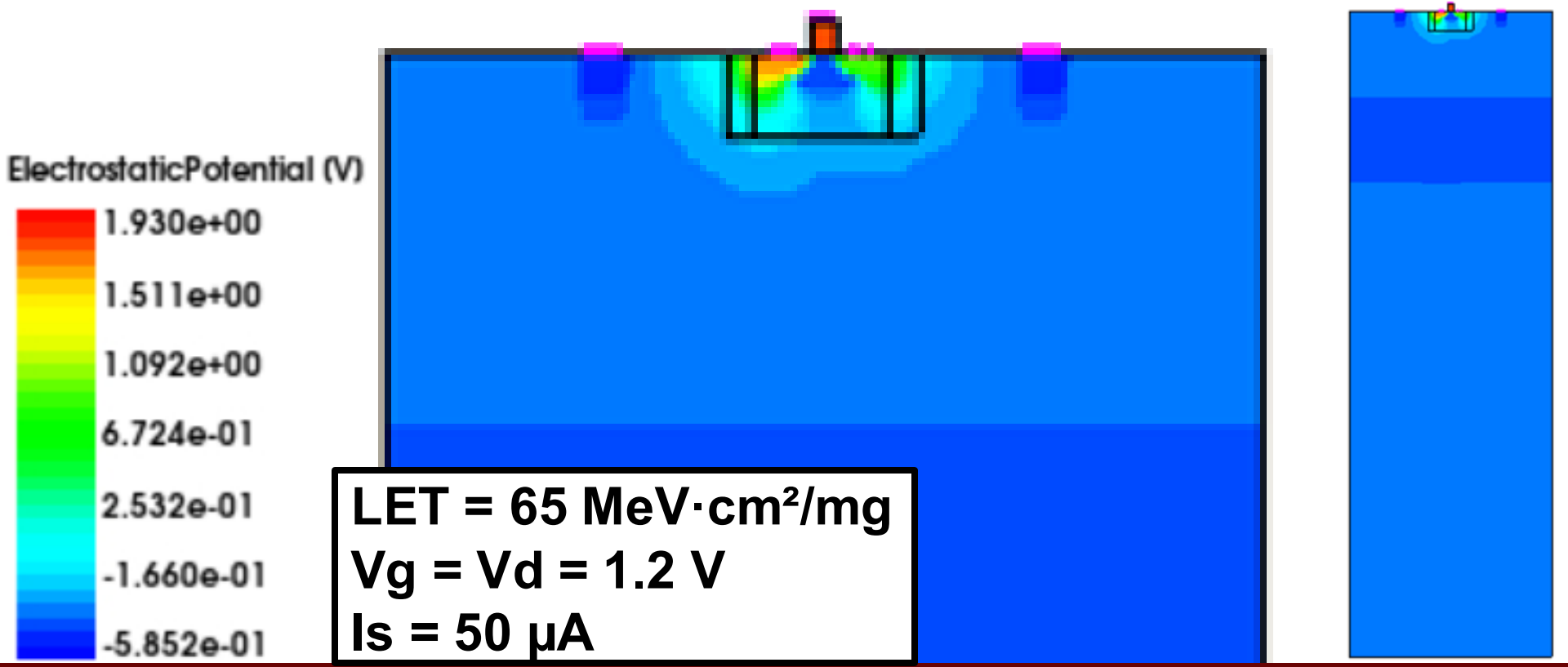
Channel Region Meshing for Simulation



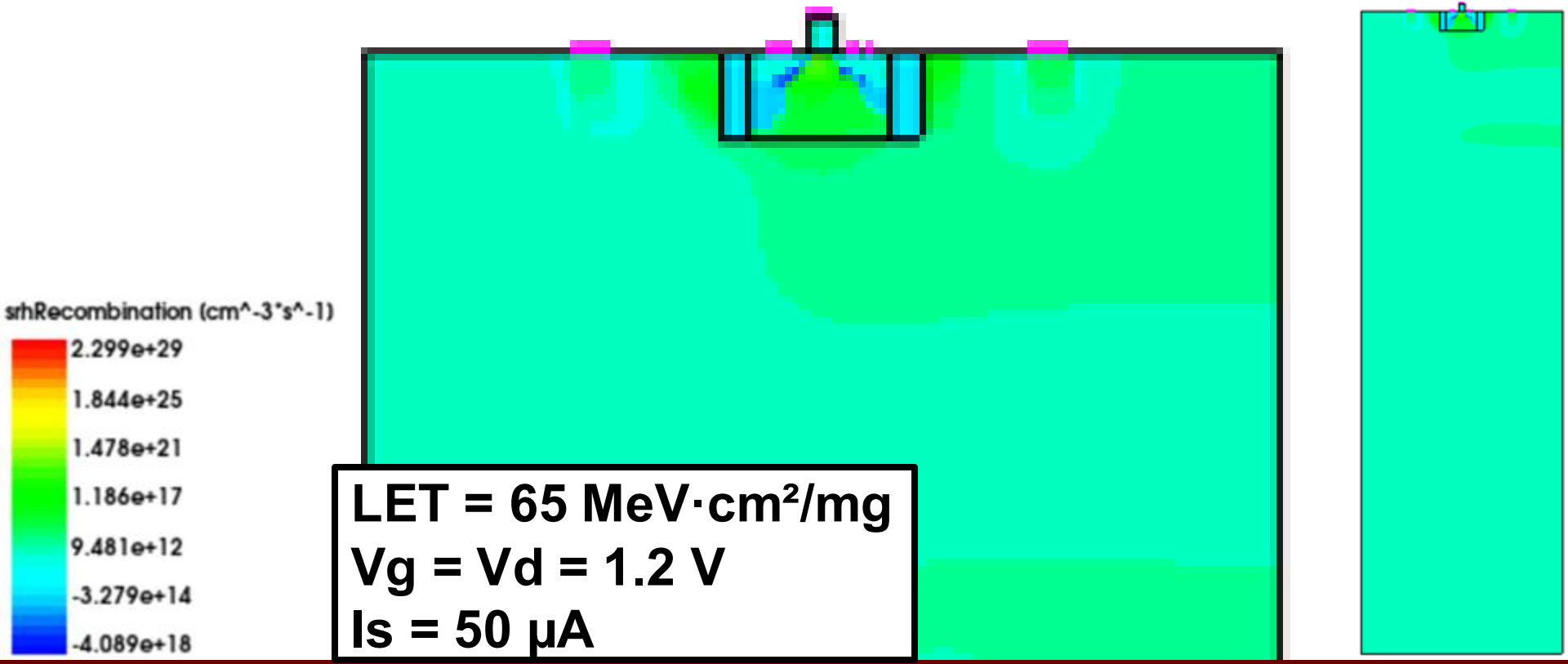
NFET: HI Strike - TotalCurrentDensity



NFET: HI Strike - ElectrostaticPotential

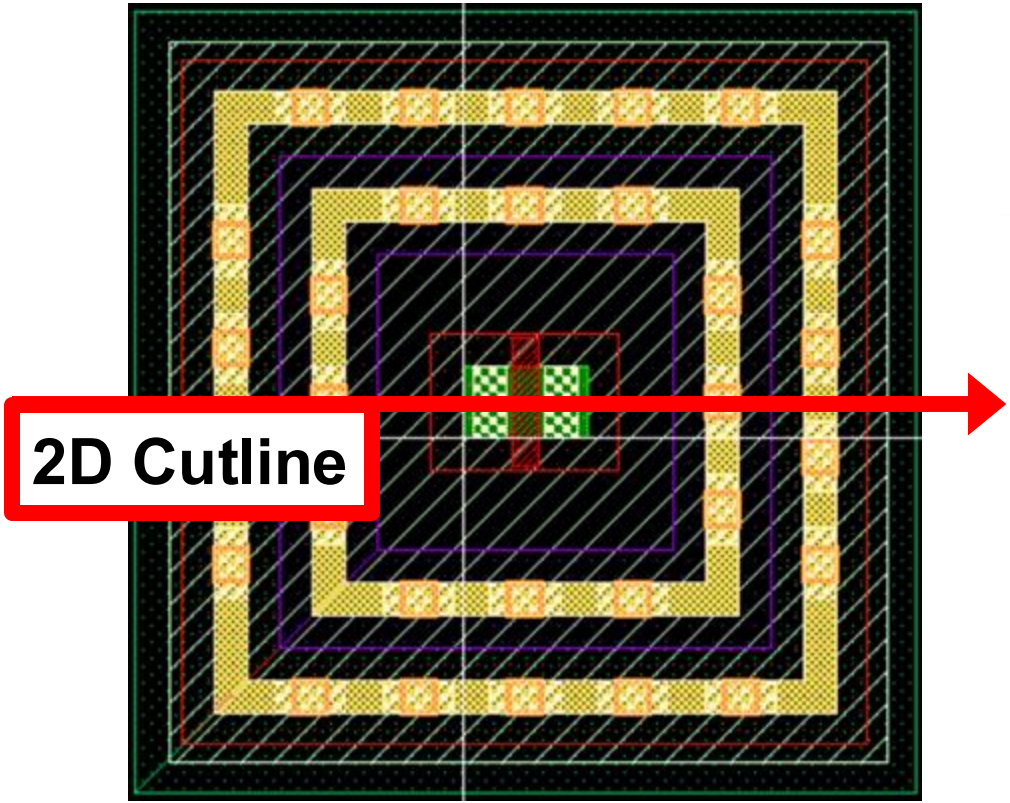


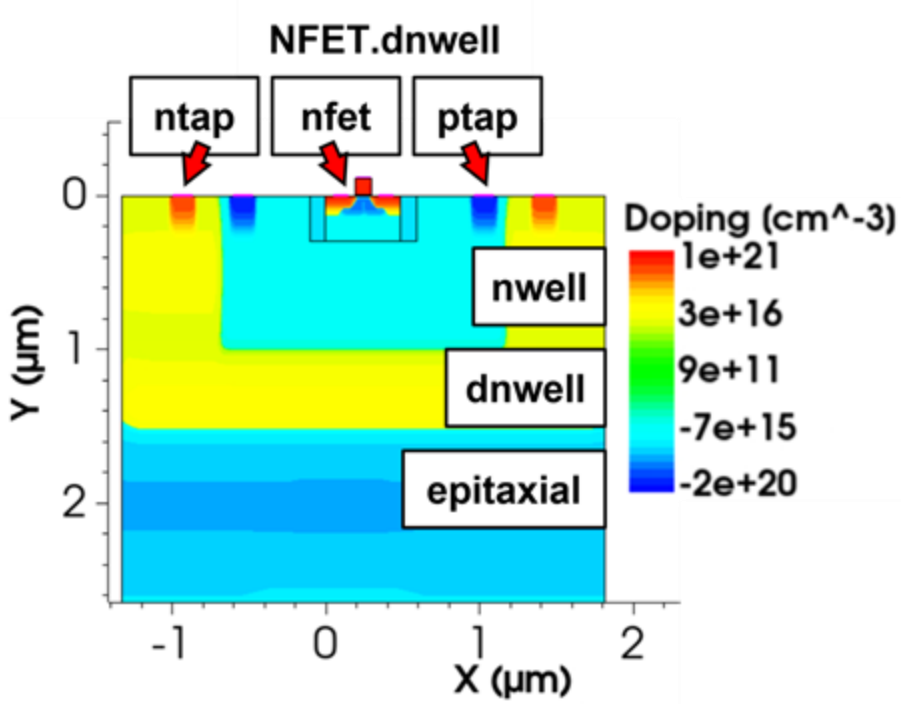
NFET: HI Strike - srhRecombination



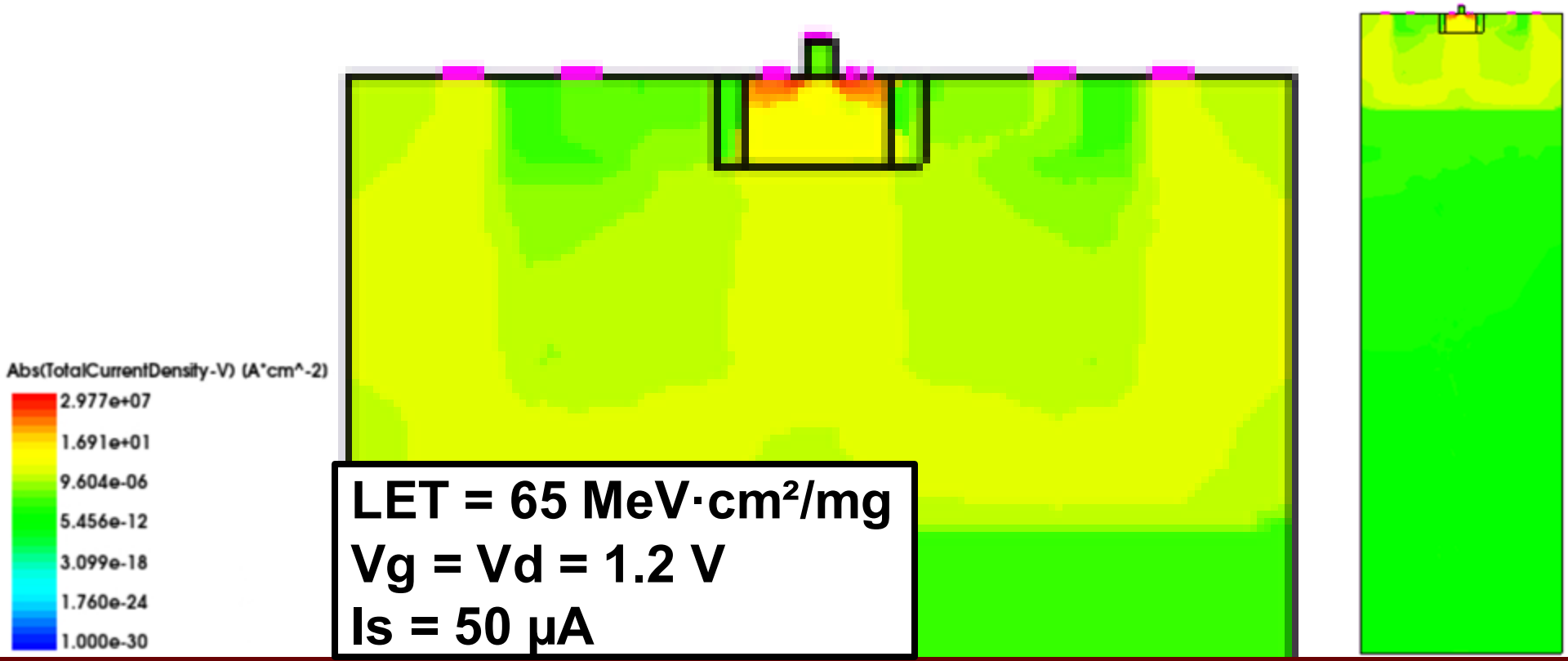
LET = 65 MeV·cm²/mg
Vg = Vd = 1.2 V
Is = 50 µA

Layout (left) & TCAD Model (right)

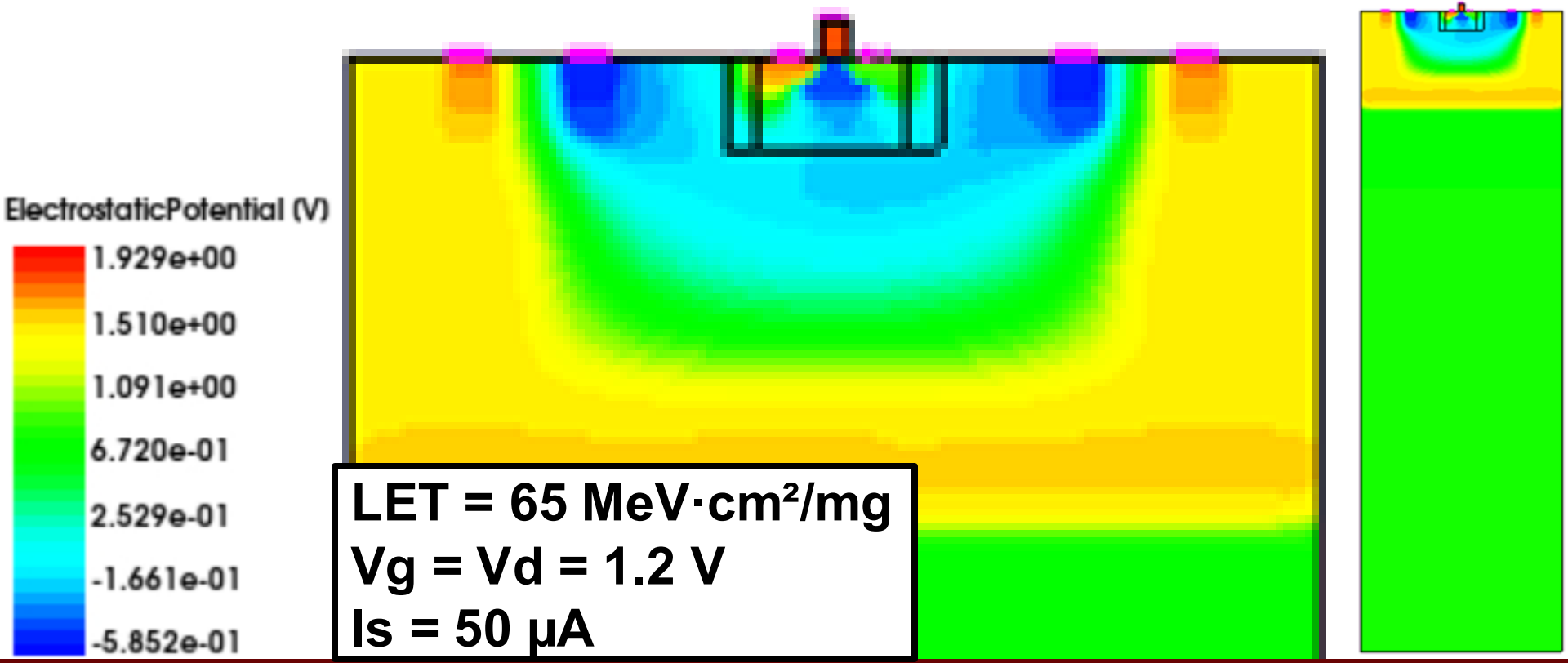




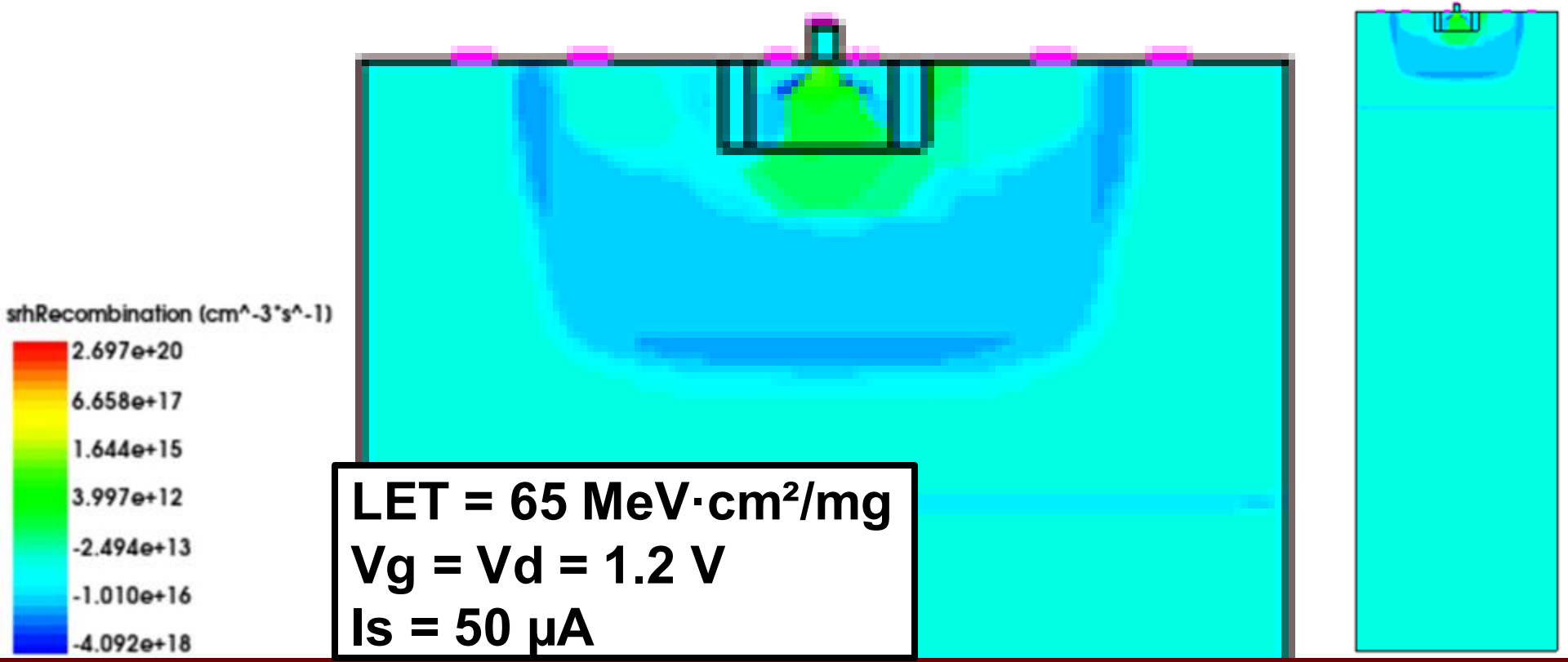
NFET.dnwell: HI Strike - TotalCurrentDensity



NFET.dnwell: HI Strike - ElectrostaticPotential



NFET.dnwell: HI Strike - srhRecombination



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