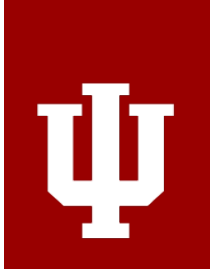


Microelectronics Radiation Effects and Reliability

HW 3

Simulation of Single-Event Effects

Issue 1.0

1 Introduction

This HW introduces you single-event effects (SEE) simulation using the LTSpice IV simulation software. Single-event transients (SET) and single-event upsets (SEU) will be analyzed on basic combinational and sequential logic cells.

LTSpice IV can be downloaded here: https://www.analog.com/en/resources/design-tools-and-calculators/ltspice-simulator.html. Before beginning the assignment, it is recommended that you complete the Getting Started Tutorial, and review the LTSpice IV tutorials from class.

In the first part of this HW assignment, you will draw transistor-level schematics of an inverter gate and a D Flip-Flop cell. In the second part of the assignment, you will explore the SET and SEU responses of the cells. Finally, you will propose and demonstrate a mitigation solution.

2 Learning Objectives

At the end of this lab, you should be able to:

- Draw transistor-level cell schematics using LTSpice IV
- Simulate transistor-level schematics using SPICE
- Simulate SEE in combinational and sequential logic
- Design and demonstrate SEE mitigation solutions

3 SPICE Models

This assignment uses the following custom LEVEL 3 SPICE models:

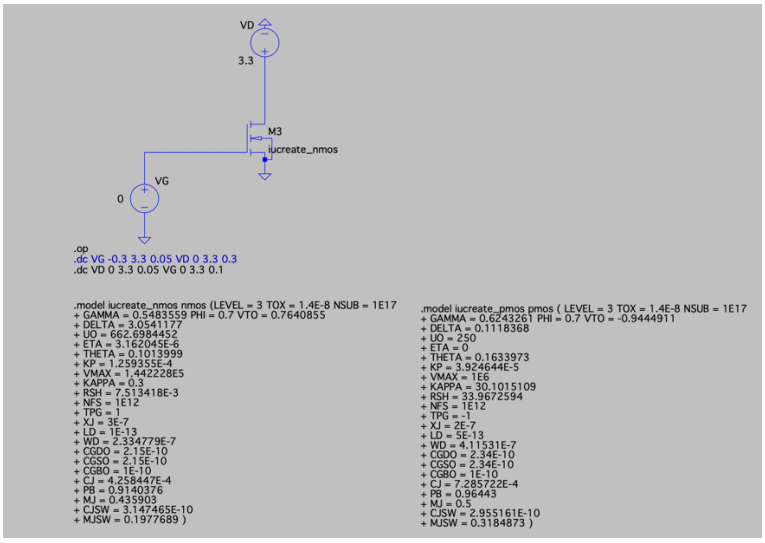
```
.model iucreate_nmos nmos (LEVEL = 3
+ TOX = 1.4E-8
+ NSUB = 1E17
+ GAMMA = 0.5483559
+ PHI = 0.7
+ VTO = 0.7640855
+ DELTA = 3.0541177
+ UO = 662.6984452
+ ETA = 3.162045E-6
+ THETA = 0.1013999
+ KP = 1.259355E-4
+ VMAX = 1.442228E5
+ KAPPA = 0.3
+ RSH = 7.513418E-3
+ NFS = 1E12
+ TPG = 1
+ XJ = 3E-7
+ LD = 1E-13
+ WD = 2.334779E-7
+ CGDO = 2.15E-10
+ CGSO = 2.15E-10
+ CGBO = 1E-10
+ CJ = 4.258447E-4
+ PB = 0.9140376
+ MJ = 0.435903
+ CJSW = 3.147465E-10
+ MJSW = 0.1977689 )
```

```
.model iucreate_pmos pmos (LEVEL = 3
+ TOX = 1.4E-8
+ NSUB = 1E17
+ GAMMA = 0.6243261
+ PHI = 0.7
+ VTO = -0.9444911
+ DELTA = 0.1118368
+ UO = 250
+ ETA = 0
+ THETA = 0.1633973
+ KP = 3.924644E-5
+ VMAX = 1E6
+ KAPPA = 30.1015109
+ RSH = 33.9672594
+ NFS = 1E12
+ TPG = -1
+ XJ = 2E-7
+ LD = 5E-13
+ WD = 4.11531E-7
+ CGDO = 2.34E-10
+ CGSO = 2.34E-10
+ CGBO = 1E-10
+ CJ = 7.285722E-4
+ PB = 0.96443
+ MJ = 0.5
+ CJSW = 2.955161E-10
+ MJSW = 0.3184873 )
```

The custom technology can be assumed to be generally reflective of a 0.5 µm CMOS technology node with the following specifications:

Parameter	Value
Gate Length (minimum), Lmin	0.5 µm
Gate Width (minimum), Wmin	1.5 µm
NMOS Threshold Voltage (VTN)	0.9 V
PMOS Threshold Voltage (VTP)	-1 V

In LTSPICE IV, the models can be copied and pasted into a SPICE directive in a schematic as shown below, or saved as a .model file and referenced in a .include SPICE directive statement. Be sure to use the **nmos4** and **pmos4** symbols in LTSpice IV when creating your schematic. Once a device is placed, right-click the device and change the **Model:** field to point to the appropriate model (iucreate_nmos or iucreate_pmos). You may adjust the Length and Width parameters of each instance as well.



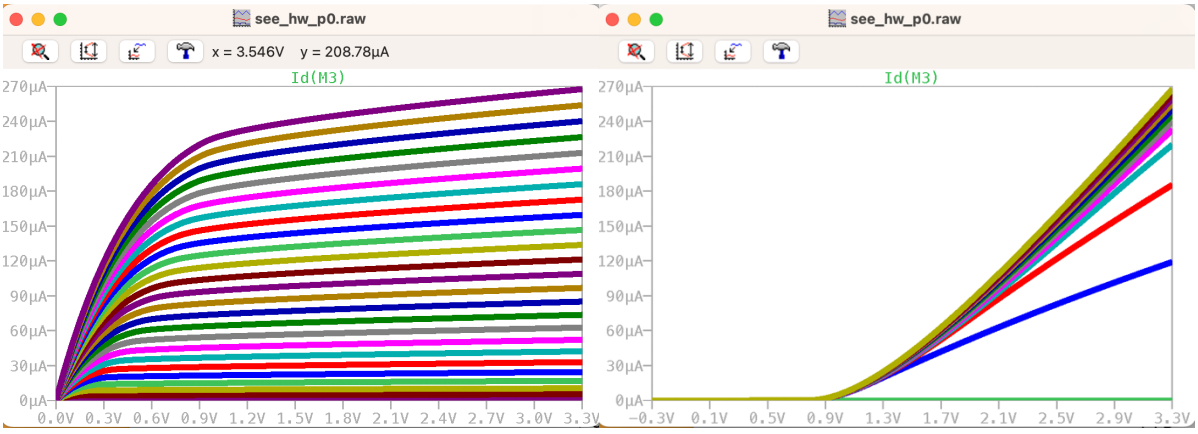
The following SPICE files are required for this HW:

- see_hw_p0
- see_hw_p1
- see_hw_p2
- see_hw_p3
- see_hw_dff_p0
- see_hw_dff_p1

4 Combinational Logic

Before proceeding, download the LTSPICE IV examples and ensure that you are comfortable with .OP, .DC, and .TRAN simulations.

- see_hw_p0: In this simulation deck, explore the various nested DC sweep simulation settings, reproducing the IDS-VDS and IDS-VGS curve families:

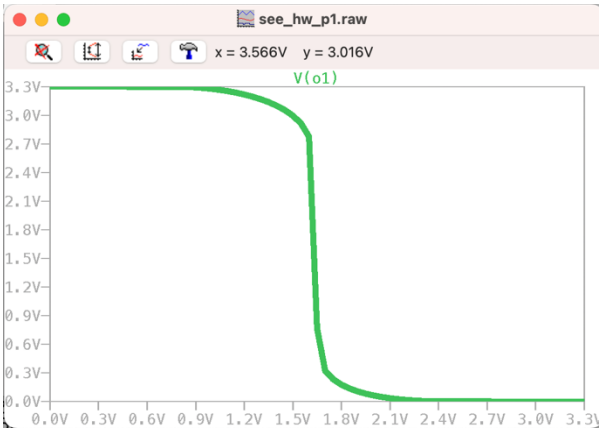


IDS vs VDS (left) and IDS vs VGS (right) examples

QUESTION 1: According to the IDS vs VGS simulation, what is the approximate threshold voltage of the minimum size NMOS device? Does this agree or disagree with the noted specification? Why?

QUESTION 2: Reproduce the ISD-VSD and ISD-VSG curves for a PMOS device (minimum dimensions). What is the approximate threshold voltage?

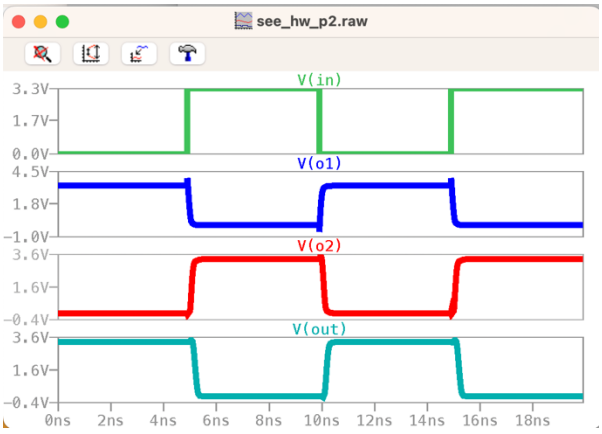
- see_hw_p1: In this simulation deck, simulate the voltage transfer curve (output voltage versus input voltage) of the inverter combinational logic gate.



Output voltage vs. Input voltage for minimum sized inverter

QUESTION 3: A "matched" inverter is said to have Vout=Vin when Vin=VDD/2. Is this the case for the provided inverter? If you make the NMOS gate width twice as large, how much do you have to increase the PMOS gate width by to ensure that the device is "matched"?

- see_hw_p2: In this simulation deck, simulate the transient response, showing a sequence of pulses propagating through the chain of three inverters.



Output voltage vs. Time for the chain of 3 inverter gates

QUESTION 4: Propagation delay is defined as the time between the output signal and input signal when the values equal 50% of VDD. Measuring the delay between signal o2 and o1, what is the propagation delay (measured from a rising input edge to a falling output edge)? Measuring the delay between signal o2 and o1, what is the propagation delay (measured from a falling input edge to a rising output edge)? Why should you use signals o1 and o2 to make this measurement?

- see_hw_p3: In this simulation deck, simulate SET by injecting a double exponential current pulse at node o1. Note that the default file simulates an ion strike on NMOS transistor M3. For the simulation, TP (Rise Tau) should be 10ps, TN (Fall Tau) should be 1ns, the Rise Delay should be 8ns and the Fall Delay should be 8.001ns. The only parameter you should adjust is the Vpulsed parameter, representing the peak of the current pulse.

QUESTION 5: What is the critical charge required to create a transient that propagates to OUT (with an amplitude of at least 90% of VDD) when transistor M3 is struck?

Note that the collected charge can be determined by integrating ISET. If the following SPICE directive is used, the integrated value will be reported in the .log file:

```
.meas TRAN QCOL INTEG I(ISET)/1e-15
```
(the units will be in fC)

What is the resulting pulse width?

If the amount of deposited charge is doubled, by what percentage does the pulse width increase?

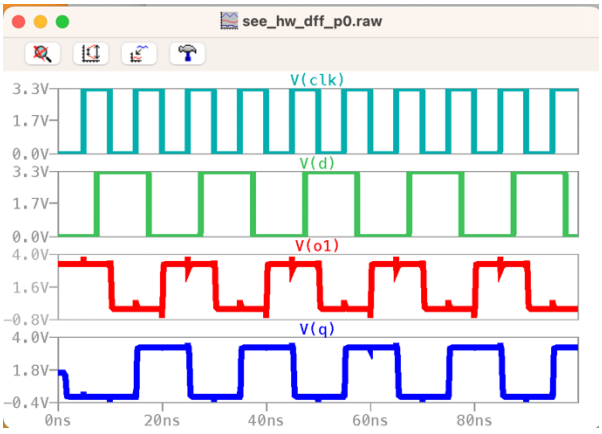
QUESTION 6: What is the critical charge required to create a transient that propagates to OUT (with an amplitude of at least 90% of VDD) when transistor M4 is struck? Note that you must adjust the terminal connections for the source ISET when simulating a PMOS hit.

What is the resulting pulse width?

If the amount of deposited charge is doubled, by what percentage does the pulse width increase?

5 Sequential Logic

- see_hw_dff_p0: In this simulation deck, reproduce the transient response of the D Flip-Flop (DFF) over a 100 ns period.



Transient response of the DFF

QUESTION 7: The initial simulation deck tests the design at a 100 MHz clock frequency. What is the maximum clock frequency for which the DFF can properly sample the input data?

- see_hw_dff_p1: In this simulation deck, a SET is injected into node o1 by simulating a strike on transistor M1.

QUESTION 8: What is the critical charge required for this SEE to result in an observable SEU at the DFF output (Q)? Do not change any of the timing parameters.

QUESTION 9: What is the critical charge required for a SEE on transistor M3 to result in an observable SEU at the DFF output (Q)? Note that you may have to change timing parameters of the event to ensure that transistor M3 is OFF when you simulate the strike!

6 For Independent Practice

We just scratched the surface. On your own, explore the various sensitivities in the DFF – there are a lot of nodes and transistors, all at various states during an SEE. What does this mean about critical charge?

7 What to Turn In

A single document uploaded to Canvas containing the following:

1. Please indicate how many hours you spent on this HW. This will not affect your grade but will be helpful for calibrating the workload for the future.
2. Answers to the 9 questions, along with supporting work. Results in the form of simulation printouts are encouraged – with supporting statements.