Total-Ionizing-Dose Effects in Modern CMOS Technologies

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***Abstract*—This review paper discusses several key issues associated with deep submicron CMOS devices as well as advanced semiconductor materials in ionizing radiation environments. There are, as outlined in the ITRS roadmap, numerous challenges ahead for commercial industry in its effort to track Moore's Law down to the 45 nm node and beyond. While many of the classical threats posed by ionizing radiation exposure have diminished by aggressive semiconductor scaling, the question remains whether there may be unknown, potentially worse threats lurking in the deep submicron regime. This manuscript provides a basic overview of some of the materials, devices, and designs that are being explored or, in some cases, used today. An overview of radiation threats and how radiation effects can be characterized is also presented. Last, the paper provides a detailed discussion of what we know now about how modern devices and materials respond to radiation and how we may assess, through the use of advanced analysis and modeling techniques, the relative hardness of future technologies.**

***Index Terms*—1/f noise, high-k, interface traps, oxide trapped charge, radiation, RILC, shallow trench isolation, silicon-on-insulation (SOI), total ionizing dose.**

I. Introduction

THE combined effects of advances in microelectronic materials and device structures have resulted in more changes to underlying integrated-circuit technologies over the past five years than have occurred in the previous forty years. Some of these changes are still in research labs, but many of them are now beginning to appear in mainstream products. These changes have profound implications for radiation hardness. Energy absorption, carrier generation, carrier transport, charge trapping, and defect formation and dynamics depend on the specific materials and devices used in the ICs. Sensitivity to the electrostatic effects of radiation-induced trapped charge, lifetime degradation, and device-edge and interdevice leakage depend on the detailed device geometries and doping profiles.

There are, as outlined in the International Technology Roadmap for Semiconductors (ITRS), numerous challenges ahead for commercial industry in its effort to track Moore's Law down to the 45 nm node and beyond. While many of the classical threats posed by radiation environments have been diminished by aggressive semiconductor scaling, the question remains whether there may be unknown, potentially worse threats lurking in the deep submicron regime. This paper reviews a portion of what is known today about how emerging materials and CMOS devices respond to ionizing radiation, from physical mechanisms at the atomic-scale to the current–voltage characteristics of modern devices and circuits.

The paper is broken down into three sections. The first section focuses on some of the novel technologies, materials, and devices that are the subject of intense research and development today. These technologies, identified in the ITRS, will be critical to maintaining the phenomenal growth experienced in the electronics industry for the past half century. However, the development and practical implementation of these processes will depend strongly on addressing the numerous practical, commercial challenges, which are for the most part, totally divorced from radiation effect concerns. The technologies considered here are as follows:

— ultra-small bulk CMOS;
— fully depleted silicon-on-insulator (SOI);
— ultra-thin gate oxides;
— high-k gate dielectrics.

The second section provides an overview of mechanisms for radiation damage, which will include a review of the physical nature of the defects associated with total ionizing dose (TID). Radiation-induced displacement damage and single event effects in electronics will not be discussed in this paper. Following the TID effects overview, the paper will provide examples and explanations for how these mechanisms manifest themselves in modern technologies. Indeed, while the basic physical processes leading to radiation damage have remained essentially unchanged, the manner in which the damage impacts the quality of materials or the function of devices is somewhat different in today's advanced technologies.

II. Emerging Materials and Devices

A. CMOS Technology Drivers

The quickening pace of MOSFET scaling is accelerating the introduction of new technologies to extend CMOS beyond the 45 nm technology node [1]. This acceleration requires the industry to simultaneously intensify research in two highly challenging thrusts, scaling CMOS into an increasingly difficult manufacturing domain well below the 90 nm node while extending existing or inventing fundamentally new approaches to electronic signal processing and control that sustain functional scaling beyond the domain of traditional CMOS [1]. The ITRS, which is primarily interested in how Moore's law is tracked, has been focused on CMOS as its defining technology for the past several years. This is because CMOS, with its ability to be aggressively scaled, has represented the benchmark for

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state-of-the-art microelectronics. It is for this reason that we generally begin by considering ways in which classical CMOS can be extended through the use of advanced semiconductor materials or devices when discussing new commercial technologies. In the next decade, CMOS field effect transistor (FET) technologies will most likely continue to dominate the semiconductor industry. This paper therefore focuses on FET technologies, specifically deep submicron bulk CMOS and SOI.

In 1965, Gordon Moore predicted that the number of components per integrated function would double every 2–3 years [2]. By keeping pace with Moore's prediction, the semiconductor industry has not only seen an exponential increase in component density and circuit complexity over time but an exponential increase in speed (performance) and corresponding reductions in the power needed to drive integrated circuits as well. Simultaneous optimization of power and performance is best achieved by reducing both the power supply voltage (V_{DD}) and the horizontal dimensions of MOS transistors (e.g., gate length and width, drain/source area) [3]. Unfortunately, the scaling of horizontal features below micron dimensions increases the transistor's susceptibility to short channel effects (SCE). One of the best ways to keep SCEs under control is to reduce the vertical dimensions of the transistor (e.g., gate insulator thickness, drain/source junction depth) while proportionally increasing the device body doping [4].

B. Ultra-Small Bulk CMOS

The majority of ultra-small CMOS technologies are still fabricated in bulk processes. In 2004, most of the major IC manufacturers began high volume production of bulk 90 nm CMOS. For this technology node, the minimum physical gate length of the transistors (L_{min}) is 53 nm [1]. Reducing critical device features to these deep-submicron dimensions (technology scaling) not only has obvious cost advantages, but also leads to reduced power and increased speed (performance). The first steps in scaling have traditionally relied on mapping a current process to a smaller node by "shrinking" features set by the limits of photolithography (e.g., L_{min}, contact windows). Changes to the process are made accordingly to ensure appropriate specifications such as threshold voltage and off-state drain current are met. Examples of these process changes include reduced gate insulator thickness (t_{ox}), tuned threshold voltage implants, planarization, and reactive etching to improve quality of isolation structures. Deep-submicron bulk CMOS processes use shallow trench isolation (STI) structures to establish electrical isolation between devices in today's densely packed integrated circuits.

As mentioned above, the move into the deep submicron regime has increased device susceptibility to short channel effects. Among the worst of these SCEs are drain-induced barrier lowering (DIBL) and subsurface punch-through. The DIBL phenomenon is illustrated in Fig. 1. As the figure indicates, when the channel length is short, the barrier to carrier flow across the source-body pn junction is lowered via the impact of reverse bias across the drain-body junction [5]. This will lead to an increase in off-state drain current and a reduction in threshold voltage. Punch-through is also caused by the influence of the drain voltage on the source junction; however, the difference in this effect is that it occurs in the substrate, away from the surface [5]. Punch-through occurs when the drain-body depletion region reaches the source-body junction and creates a depletion region across the device (Fig. 2). This leads once again to coupling between the source and drain, increased leakage current, and a breakdown in the saturation current at high drain-to-source voltages. These problems may be mitigated by increasing doping in the body. Many advanced bulk CMOS processes now use selective implants (halo and δ-doping) to create nonuniform doping profiles that reduce susceptibility to SCEs. Nonuniform doping through retrograde and epitaxial processes has also been shown to mitigate latch-up. While technology innovations such as these have largely enabled manufacturers to control latch-up and the deleterious impact of SCEs, bulk CMOS is still saddled with other drawbacks. One drawback is the parasitic junction capacitance below the drain/source regions. This capacitance limits the performance of bulk technologies. Other drawbacks include a subthreshold swing that is too high (~90 mV per decade [6]) and a channel mobility that is too low. These inherent limitations have led to the development of fully depleted SOI CMOS technologies.

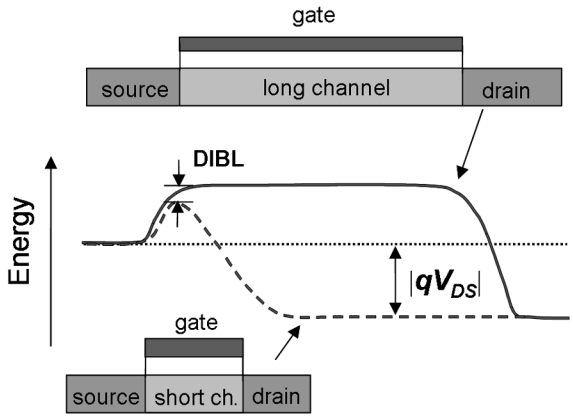

Fig. 1. Illustration of drain-induced barrier lowering (DIBL) short channel effect.

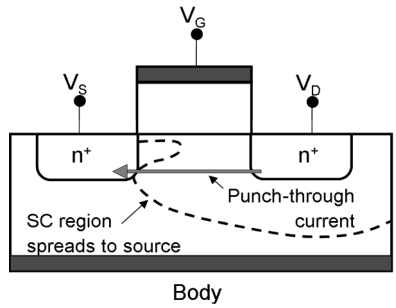

Fig. 2. Illustration of the punch-through short channel effect.

C. Fully Depleted Silicon-on-Insulator (SOI)

1) Basic Structure: In fully depleted silicon-on-insulator (FDSOI) technologies, a thin silicon film is grown or deposited on top of a buried oxide known as the BOX. In this structure, illustrated in Fig. 3, the highly doped drain and source regions extend from their contacts on the top-side of the silicon film to the BOX on the bottom of the film, thereby removing the

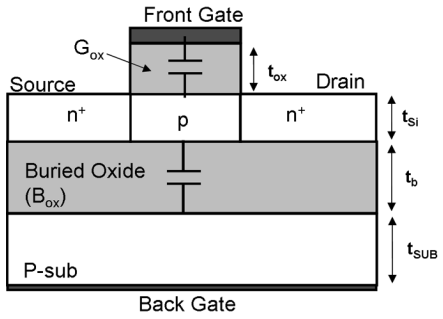

Fig. 3. Schematic illustration of FDSOI cross-section.

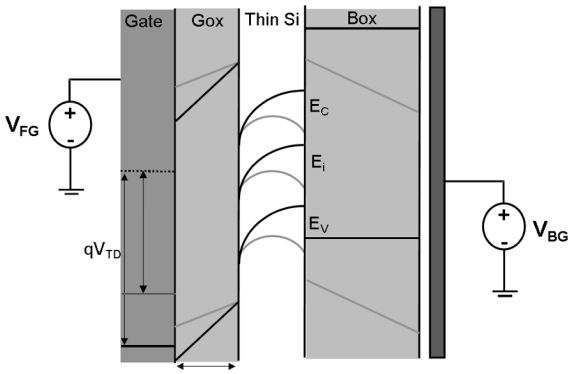

Fig. 4. Illustration of the impact of back gate voltage on the Si thin film energy bands.

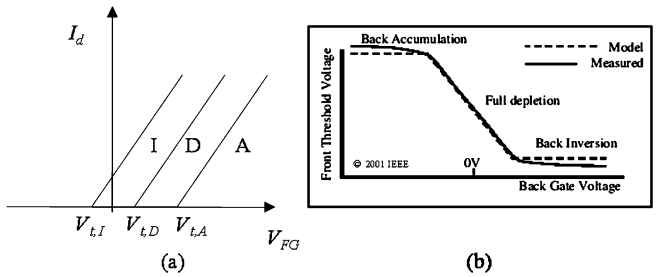

Fig. 5. Impact of back gate bias on the *I–V* characteristics of FDSOI devices [6].

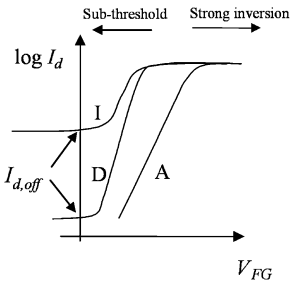

Fig. 6. Illustration of the impact of back gate bias of the I_D versus V_{GS} properties of FDSOI nFET [7].

parasitic junctions below the drain/source regions. This significantly reduces the drain-body and source-body junction area. Thus, these transistors can also operate at higher speeds due to reduced junction capacitance.

The drawback to the widespread implementation of SOI in years past was the problem of achieving quality interfaces, especially between the silicon epitaxial layer and the BOX. However, with the advent of new techniques and technologies for fabricating SOI, including SIMOX and UNIBOND, these fabrication problems have mostly disappeared [7].

The key feature of the FDSOI MOSFET is that the Si film is depleted across the entire body region. That is, under equilibrium conditions the energy bands in the Si film are bent so that the sum of the free carrier densities is less than the doping concentration. This effect is illustrated in Fig. 4, [6]. In addition to reduced capacitance, another advantage to the FDSOI structure is that it mostly eliminates the need for body contacts or body ties, although in some applications, body contacts may still be recommended. Another advantage to FDSOI is that it enables control of the channel from both the front gate and back gate. This "dual gate" operation can enable control and optimization of threshold voltage, subthreshold voltage swing, and small signal transconductance.

2) Dual-Gate Operation: As Fig. 3 illustrates, the SOI MOSFET has a front and back gate. The front gate is equivalent to the conventional gate control terminal. Voltages applied to this gate $(\mathrm{V_{FG}})$ are applied across the thin front gate capacitor, $\mathrm{G_{ox}}$, to modulate the carrier concentration of the Si film. However, unlike bulk MOSFETs, there is a backside contact to the device, which can also act as a gate. Voltages applied to the back gate $(\mathrm{V_{BG}})$ are applied across the BOX to modulate the energy bands and carrier concentration of the Si film but from the opposite side. Thus, in FDSOI, carrier modulation in the Si film is a function of both the front and back gate biases. This effect is also illustrated in Fig. 4. It is this coupling that allows three critical specifications, threshold voltage, subthreshold swing, and small signal transconductance, to be optimized in FDSOI technologies.

Fig. 5 shows the impact of back gate voltage on threshold voltage (V_t) [6]. Fig. 5(a) represents the linear drain current (I_d) versus front gate gate-to-source voltage $(\mathrm{V_{FG}})$ characteristic of an n-channel device for back gate voltages that put the back channel surface in either accumulation (A), depletion (D), or inversion (I). As the figure indicates, through back channel control, the threshold voltage can be modulated with appropriate biases. Fig. 5(b) summarizes this effect by showing how V_t is modulated by back gate biasing [6]. The ability of $\mathrm{V_{BG}}$ to alter V_t is explained by charge control, i.e., the back gate voltage controls the amount of charge that must be compensated by the front gate potential. In the case of accumulation, the positive charge on the back gate must be offset by a greater amount of negative charge on the front gate, hence the higher V_t. In inversion, the negative charge on the back gate minimizes the compensation voltage needed to invert the front gate.

An inverting back gate voltage increases the off-state leakage current, $\mathrm{I}_{d,\mathrm{off}}$ (I_d at $\mathrm{V_{FG}} = 0$ V), between the drain and source. This is illustrated in Fig. 6, [7]. High $\mathrm{I}_{d,\mathrm{off}}$, increases the static power specification of the CMOS digital applications. Another important phenomenon shown in Fig. 6 is the relative steepness of the subthreshold response for a back gate bias that depletes the back channel. A steep subthreshold curve is typically desired for optimizing power and performance in CMOS technologies. In standard bulk operation, which is similar to the way the

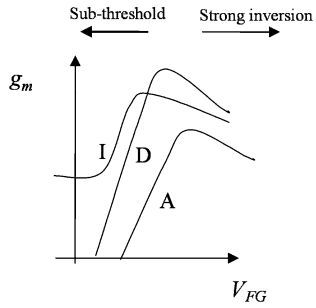

Fig. 7. Illustration of the impact of back gate bias on small signal transconductance in an FDSOI nFET [7].

FDSOI device operates with an accumulated back channel, subthreshold current is primarily due to the diffusion of minority carriers from the source to drain. In general, current is not only a function of the diffusion of carriers from high to low concentrations but is also a function of the local electric field, which causes carrier drift. When the FDSOI body is depleted by the back gate bias, both the carrier and electrics field from drain to source are modulated in a way that increases the sum of carrier diffusion and drift from drain to source, thereby increasing $\mathrm{dI}_d/\mathrm{dV}_{\mathrm{FG}}$. This causes subthreshold voltage swing to be minimized with depleted back gate bias. Depletion mode operation will also increase small signal transconductance, particularly in strong inversion, as shown in Fig. 7. Transconductance in strong inversion can be expressed as

$$g_m = \sqrt{2\mu_x G_{\mathrm{ox}} \frac{W}{L_{\mathrm{min}}} I_d} \tag{1}$$

where μ_x is the channel mobility. Since the drain current (I_d) in strong inversion is roughly the same regardless of how the device's back gate is biased, the advantage of a depleted back gate comes from its effect on μ_x. A depleting back gate bias reduces the vertical field in the body, which increases the mobility of carriers transporting from source to drain [7].

In summary, through the use of back gate control, key parameters of a MOSFET manufactured in an FDSOI process may be optimized for both power and performance. These parameters include: threshold voltage, off-state current, channel mobility, subthreshold voltage swing, and transconductance.

D. Ultra-Thin Oxides

The reduction in gate dielectric thickness is one of the most important parameters in scaling. The maintenance of a constant electric field across the gate dielectric (constant-field scaling) has been a widely accepted guideline for technology scaling [4]. Thus, reductions in power supply voltage are typically accompanied by simultaneous reductions in gate dielectric thickness. Electrical oxide thickness is reduced by roughly 50% every five years, correlating to the exponential rates originally predicted by Moore [8].

SiO_2, or nitrided SiO_2, have been the gate dielectrics primarily used by the semiconductor industry for over 30 years. The thickness limit is the same for both materials and is not limited by manufacturing control. Today, it is technically feasible to manufacture oxides that are less than 1 nm thick [9].

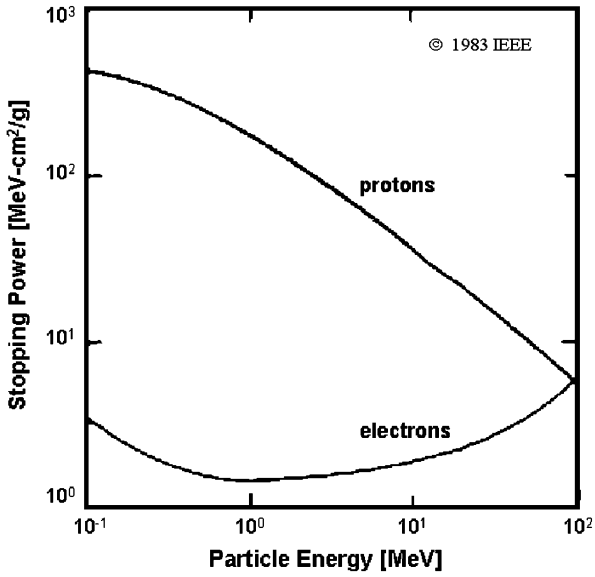

Fig. 8. Stopping power for electrons and protons as a function of particle energy [12].

Indeed, for the next CMOS technology node, 65 nm, the electrical oxide thickness will be 0.9 nm [1]. The thickness limit for SiO_2 is set instead by gate-to-channel tunneling leakage. As the thickness of the gate oxide decreases, direct tunneling of carriers through the potential barrier can occur, causing gate leakage current [9]. According to prediction, the SiO_2 thickness limit should already have been reached if the limit was defined as the point where the gate-to-channel tunneling current is equal to the off-state source to drain subthreshold leakage (currently $\sim$1 nA/μm). Only through the utilization of some important stop gap measures related to gate stacking and tunnel barriers has the problem of leakage been somewhat avoided today. However, it is widely accepted that the problem of gate leakage is unavoidable. Thus, new techniques for gate leakage mitigation are being developed.

E. High-k Dielectrics

One of the most important advanced material techniques today is the use of dielectric materials with higher dielectric constants than SiO_2. The reason for the choice of high-k materials is to reduce gate leakage current caused by direct tunneling through ultra thin materials. The most straightforward way of achieving this is to "thicken" the dielectric. However, simply increasing the gate dielectric thickness $(\mathrm{t}_{\mathrm{dielectric}})$ will violate rules for constant-field scaling. These rules require that the gate dielectric capacitance should be reduced by the same factor as $\mathrm{t}_{\mathrm{dielectric}}$. Since

$$C_{\mathrm{dielectric}} \propto \frac{k_{\mathrm{dielectric}}}{t_{\mathrm{dielectric}}} \tag{2}$$

increased $\mathrm{t}_{\mathrm{dielectric}}$ can be achieved without violating rules if a material is used that has a higher dielectric constant $(\mathrm{k}_{\mathrm{dielectric}})$. There are several high-k dielectrics being considered today. Among these are Al_2O_3 (aluminum oxide$-\mathrm{k}_{\mathrm{dielectric}} = 9$), ZrO_2 (zirconium-oxide$-\mathrm{k}_{\mathrm{dielectric}} = 25$), and HfO_2 (hafnium

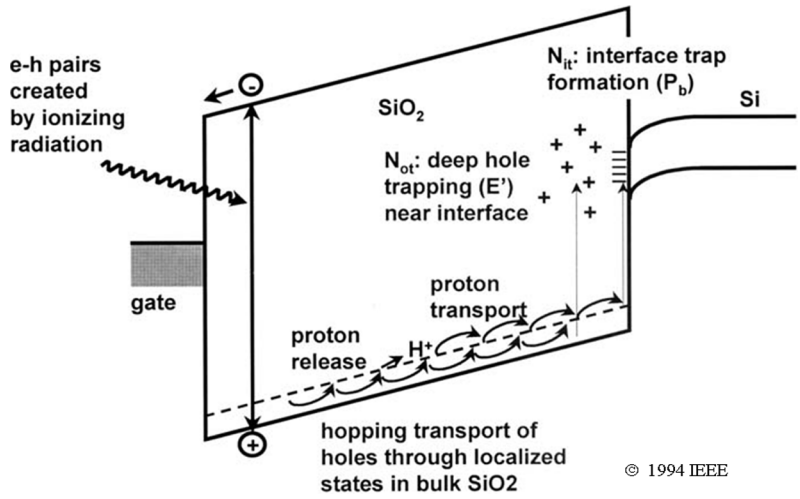

Fig. 9. Illustration of the main processes in TID damage [14].

oxide$-k_{dielectric}\sim 25$). Ensuring a stable interface between these materials and silicon is one of the most important issues related to the use of these materials. For us, understanding their radiation properties is also critical.

III. Total Ionizing Dose (TID) Effects

A. Ionization Damage Overview

Ionization of a target material is caused by the interaction of high energy photons or charged particles (i.e., protons, electrons, or energetic heavy ions) with the atoms of that material [10]. Photon-induced ionization damage is initiated when electron-hole-pairs (ehps) are generated along the track of secondary electrons emitted via photon-material interactions. Protons and other charged particles also generate ehps that lead to ionization damage.

The density of ehps generated along the tracks of charged particles is proportional to the energy transferred to the target material [11]. Stopping power or linear energy transfer (LET) expresses the energy loss per unit length (dE/dx) of a particle and is a function of the mass and energy of the particle as well as the target material density [12]. The units of LET are commonly expressed as MeVcm^2/g. Fig. 8 is a plot of LET versus particle energy for electrons and protons [12]. The LET for protons is considerably higher than that of electrons for lower energies, but it decreases rapidly with increasing energy. Electrons show a nonmonotonic response, decreasing as a function of particle energy before increasing for energies above 1 MeV. The total amount of energy deposited by a particle that results in ehp production is commonly referred to as TID. The typical unit of TID is the rad, which denotes the energy absorbed per unit mass of a material. One rad(material) is equivalent to 100 ergs absorbed by one gram of the target material.

The physical processes that lead from the initial deposition of energy by ionizing radiation to the creation of ionization defects are: 1) the generation of ehps, 2) the prompt recombination of a fraction of the generated ehps, 3) the transport of free carriers remaining in the oxide, and either 4a) the formation of trapped charge via hole trapping in defect precursor sites or 4b) the formation of interface traps via reactions involving hydrogen [13]. These processes are summarized graphically in Fig. 9, [14].

TABLE I
Relationship Between, Ionization Energy, Material Density, and Generated Carriers [10]

Material	Mean E_p (eV)	Density (g/cm^3)	Pair density, generated per rad, κ_g (pairs/cm^3)
GaAs	~4.8	5.32	~7x10^{13}
Silicon	3.6	2.328	4x10^{13}
Silicon Dioxide	17	2.2	8.1x10^{12}

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In ehp generation (process 1), a fraction of the kinetic energy of the incident particle is lost to ehp creation. The mean energy, E_p, needed to ionize a material is dependent on the bandgap of the target material. The number of ehps generated for a given dose is thus strongly dependent on E_p as well as the material density. The relationships between ionization energy, material density, and generated carriers are listed in Table I for three materials: GaAs, Si, and SiO_2 [10]. The ehp density per rad, denoted as κ_g (column 3 in Table I), is obtained using the following conversion formula:

$$\kappa_g\left[\frac{\#\text{ehp}}{\text{cm}^3\text{rad}}\right] = 100\left[\frac{\text{erg}}{g}\right]\left[\frac{1}{\text{rad}}\right] \bullet \frac{1}{1.6\times 10^{-12}}\left[\frac{\text{eV}}{\text{erg}}\right] \bullet \frac{1}{E_P}\left[\frac{\#\text{ehp}}{\text{eV}}\right] \bullet \rho\left[\frac{g}{\text{cm}^3}\right]. \quad (3)$$

Once generated, a fraction of the ehps are annihilated through either columnar or geminate recombination (process 2) [11]. The ehps that escape this initial recombination process divided by total number of ehps generated is the fractional charge yield, denoted by f_y. Fig. 10 plots f_y as a function of the radiation type [14], [15]. The figure also indicates that electron-hole pair recombination is a function of the electric field within the material [16]. The fractional yield of ehps increases monotonically

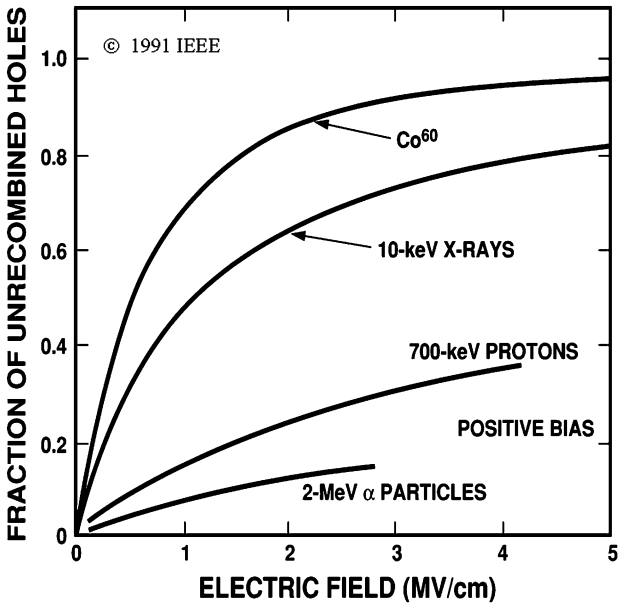

Fig. 10. Fractional yield of holes generated in SiO_2 as a function of electric field in the material [14], [15].

as the local electric field increases. It is generally believed that electrons, having a much higher mobility than holes in oxides, are rapidly swept out of the dielectric [17]. The surviving holes will undergo polaron hopping transport via shallow traps in the SiO_2 (process 3) [17]. A fraction of these transporting holes may fall into deep traps in the oxide bulk or near the Si/SiO_2 interface, thereby forming trapped positive charge (process 4a) [17]. The hole trapping efficiency (f_{ot}) is also a function of the electric field in the oxide [10]. The trapped hole defect may, depending on its proximity to the interface, exchange charge with the underlying Si via electron tunneling [18], [19]. Reactions between holes and hydrogen-containing defects or dopant complexes can also lead to the formation of a second type of ionization defect: the interface trap (process 4b) [20], [21]. The following two subsections provide a more detailed discussion of the nature of oxide trapped charge and interface traps.

B. Oxide Trapped Charge

1) Nature of Defects: Oxide trapped charge is typically net positive due to the capture of a hole in neutral oxygen vacancies and the subsequent formation of oxygen vacancy defects, or E' centers [22]–[27]. There are primarily two types of E' defects: E_δ', and E_γ'. The E_δ' center is a "dimer" vacancy, which forms a relatively shallow trap for holes in the oxide. Most of the E_δ' centers have energies located in the SiO_2 bandgap within 1.0 eV of the oxide valence band [25]. The shallow trap level of the E_δ' makes it a good candidate for the defect type responsible for hole transport through SiO_2 (process 3) [25]. The E_γ' center is a significantly deeper trap then the E_δ' defect, residing at energy levels greater than 3 eV above the oxide valence band [23], [25]. While E_γ' centers may be located throughout the oxide, most are found near the Si/SiO_2 interface [17]–[19].

Both types of E' centers can exchange charge with an adjacent Si layer [23]. The ability of the E' defect to "communicate" with the Si is a strong function of its proximity to the interface [18]. E' centers that readily capture carriers from or emit carriers to the adjacent Si are often called border traps or switching states. They are generally located within 3 nm of the Si/SiO_2 interface and can exchange charge via electron tunneling on time scales of microseconds to seconds [18], [19]. E_γ' centers located at distances greater then 3 nm from the interface (i.e., in the oxide bulk) may capture and emit carriers, but the probability of this process occurring is low. Thus, E_γ' defects in the oxide bulk are generally treated as fixed (i.e., bias independent) positive oxide charge (N_{ot}). Removal or compensation of N_{ot} may require elevated temperature and/or biased anneals over relatively long periods of time. A schematic illustration of the location of border traps (switching states) and oxide trapped charge (fixed states) in the MOS system is illustrated in Fig. 11. The buildup of N_{ot} in an oxide can be expressed as [28], [29]

$$\Delta N_{ot} = D\kappa_g f_y f_{ot} t_{ox} \tag{4}$$

where D is the total ionizing dose deposited. As (4) shows, ΔN_{ot} is proportional to the thickness of the oxide.

2) Impact on CMOS DC Response: Fixed oxide trapped charge can have a significant impact on the dc parameters of CMOS devices and integrated circuits. One of the most important and well-studied effects is the negative shift in the dc drain current versus gate-to-source voltage (V_{gs}) for both n- and p-channel MOSFETS. This effect is illustrated in Fig. 12. The figure shows that for a fixed I_d, the radiation-induced buildup of N_{ot} shifts the V_{gs} bias point more negative (i.e., by ΔV_{ot}). In n-channel MOSFETs, this shift leads to a reduction in threshold voltage and an increase in off-state and drive currents. In p-channel MOSFETs, V_t increases negatively, while off-state and drive currents are reduced.

Radiation-induced dc voltage shifts can be calculated using the following equation:

$$\Delta V_{ot} = -\frac{t_{ox}}{k_{ox}\varepsilon_0} q \Delta N_{ot} \tag{5}$$

where k_{ox} is the dielectric constant of SiO_2 and ε_0 is the permittivity of free space [5]. Given (4) and (5), the theory predicts that negative threshold voltage shifts caused by fixed oxide trapped charge buildup are proportional to the square of oxide thickness, i.e.,

$$-\Delta V_t(N_{ot}) = -\Delta V_{ot} \propto t_{ox}^2. \tag{6}$$

This theoretical relationship has been verified through numerous experiments [29]. The relationship in (6) indicates that as the gate oxides of advanced CMOS technologies are scaled to thinner dimensions, the threat of shifts in dc parameters due to N_{ot} buildup in the gate oxide is reduced [30], [31]. Instead, hole trapping in the thicker shallow trench isolation dielectrics is now a greater radiation threat in modern CMOS technologies. Typical STI trenches are much thicker than gate oxides. For advanced CMOS technologies the thicknesses range from 300 to 450 nm [32]. The impact of fixed positive oxide trapped charge buildup in STI structures will be discussed in detail in the third section of the paper.

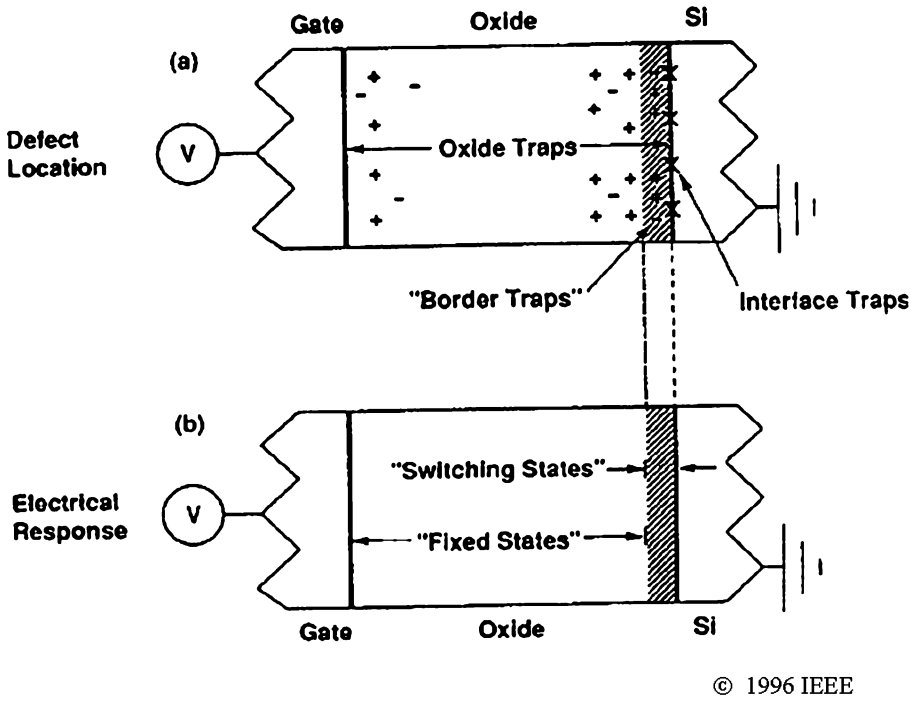

Fig. 11. Location and stability of trapped charge in SiO_2[19].

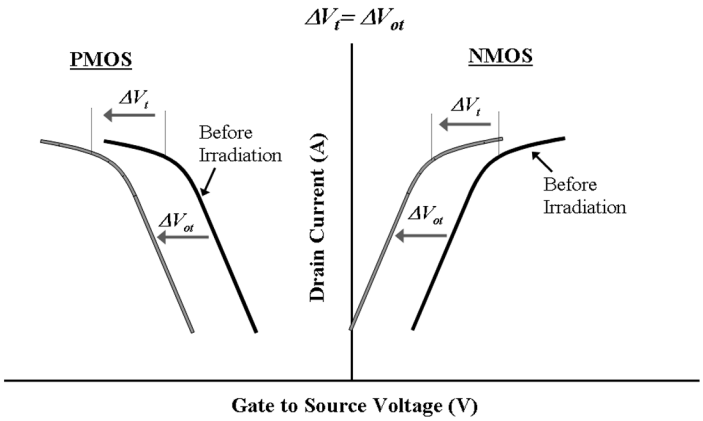

Fig. 12. Illustration of the effect of fixed oxide trapped charge on n- and p-MOS devices.

3) Switching Oxide (Border) Traps: As noted above, depending on their proximity to the Si/SiO_2 interface, E' centers can "communicate" with an adjacent Si layer [18], [19], [23]. Most of these switching defects are located within 3 nm of the interface and can exchange charge on time scales between 0.01 s to 1 s [19]. The mechanism of charge exchange is dependent on the nature of the oxide trap. For example, the E_δ' defect can simply capture and reemit trapped holes [23]. This process has been shown to be more likely in pMOS transistors [23]. In pMOS transistors, the E_δ' defect has a high hole capture cross section and a relatively low barrier for reemission relative to nMOS devices [23]. For E_γ' defects, the mechanisms are somewhat more complex. Most theories contend that the acting carriers for charge transfer in and out of the E_γ' defect are tunneling electrons. It is now widely held that the positively charged E_γ' centers can trap an electron, forming a highly stable dipole structure [17]–[19], [23], [33]. While it is possible for these trapped electrons to be reemitted, the dipole will also act as a shallow electron trap that is relatively easy to fill or empty depending on the surface potential of the underlying Si [17], [33]. For a more detailed examination of the processes related to switching oxide traps, readers may want to consult [17]–[19], [23], and [33].

The impact of switching oxide (border) traps on CMOS dc parameters is different than the impact of fixed oxide charge discussed in the previous section. Unlike N_{ot}, the charge state of the switching trap can vary with bias. As such, the signature effect of border traps on MOSFET dc parameters is similar to the effect of interface traps. This will be discussed in the following subsection.

C. Interface Traps

1) Nature of Defects: Like border traps, a second type of ionization defect, the interface trap will also exchange charge

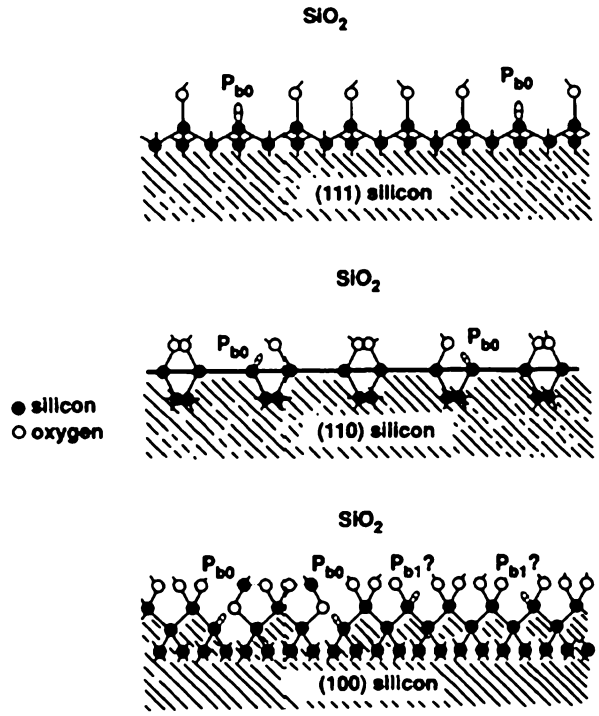

Fig. 13. Schematic illustration of P_{b0} and P_{b1} interface trap defects on (111), (110), and (100) silicon [35].

with an adjacent Si layer. However, unlike border traps, interface traps (N_{it}) are located exactly at the interface. Thus, there is essentially no barrier to trapping and detrapping of carriers in the near-surface Si. Interface traps can therefore have a significant effect on carrier mobility and recombination rates of carriers at the semiconductor surface.

Interface traps are primarily dangling bond defects called P_b centers [34]. The most important and abundant of these centers is called the P_{b0} center. A secondary contribution is provided by a closely related defect called P_{b1}. Schematic illustrations of P_{b0} and P_{b1} defects on (111), (110), and (100) silicon are shown in Fig. 13, [35].

The three initial processes that lead to N_{it} formation are similar to processes that lead to the formation of oxide trapped charge (i.e., ehp generation, recombination, and transport). However, the final formation of dangling bonds relies on several other reactions. The first reaction is between transporting holes and hydrogen containing oxide defects (D'H), which releases protons (H^+) [20]. Although it has been contended that direct reactions with holes can create interface traps, it has been shown experimentally that (near and above room temperature) most interface traps are created by protons [36]. Moreover, density-functional theory calculations confirm that the formation of interface traps by direct hole interaction is not energetically favorable under most conditions [37]. Thus, the creation of a P_b center primarily relies on the presence of H^+ near the interface. Other potential sources of protons that have recently been identified are dopant-H complexes in the Si bulk [21]. In their 2005 paper, Tsetseris *et al.* reported that hole interactions with these hydrogen complexes can lead to the creation of protons that move toward the interface under negative gate biases [21]. These effects seem to share a common origin with a growing reliability threat in advanced CMOS technologies, i.e., negative bias temperature instability (NBTI) [21].

Protons diffusing or driven by the electric field to the SiO_2 interface can remove hydrogen atoms from H-passivated dangling bonds (D) via the simple reaction [20], [37]

$$SiH + H^+ \Rightarrow D^+ + H_2. \tag{7}$$

The resulting defect (D^+) is the interface trap. Further details regarding the formation of radiation-induced interface traps may be found in [20], [21], [34], and [37].

2) Impact on CMOS DC Response: One of the principle effects of interface trap buildup is an increase in the subthreshold swing of a CMOS device. This effect is illustrated in Fig. 14, which shows a characteristic stretch out (ΔV_{it}) in the I_d versus V_{gs} response for both n- and p-channel devices. The mechanism for this effect is the bias-dependent trapping or detrapping of charge at the interface as the device surface is swept from accumulation to inversion by the gate voltage. Fig. 14 shows that the threshold voltage is also impacted by N_{it} buildup. It should also be noted that depending on the preirradiation characteristics of the MOSFET, interface trap buildup may also increase off-state drain current.

As discussed in the previous section, switching oxide (border) traps can also change charge state as the dc gate-to-source bias is varied. Thus, in dc measurements, it is difficult to distinguish the effects of interface traps (P_b centers) and switching oxide traps (near interface E' centers). The key difference between the two defect types is that the charge exchange frequency at switching E' centers is low (<100 Hz) compared to P_b centers (>1 kHz) [38], [39]. Therefore, independently measuring the effects and/or densities of either defect type requires ac or noise measurement techniques (e.g., ac conductance, charge pumping, or 1/f noise).

D. 1/f noise in MOS Devices

The radiation-induced build-up of switching states (interface traps and border traps) can significantly increase flicker or 1/f noise in CMOS devices [28], [40]. An increase in 1/f noise is detrimental to the phase noise of high frequency transceiver front-end circuits (e.g., mixers and voltage controlled oscillators) as well as base band communications applications such as data converters and filters [41]. In 1990, Meisenheimer and Fleetwood presented 1/f noise data on irradiated n-channel MOSFETS with relatively thick (48 nm) gate oxides [40]. These data are shown in Fig. 15, [40]. As the figure indicates, for TID exposures up to 500 krad, the noise spectrum, S_v, increases over an order of magnitude. The gate bias during the irradiations was fixed at 6 V. The 1/f low noise spectra can be related to frequency (f) with the following equation:

$$S_v \approx K_n \frac{V_{ds}^2}{(V_{gs} - V_t)^2} \frac{1}{f} \tag{8}$$

where K_n is the normalized noise power factor [40]. For these measurements, the source is grounded while the drain and gate

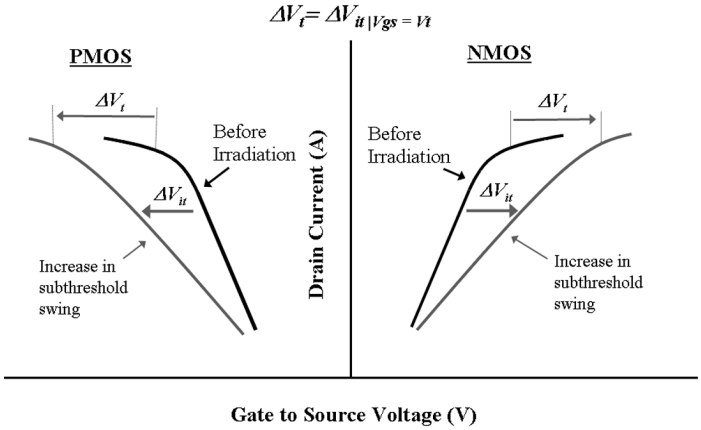

Fig. 14. Illustration of the effect of interface traps on n- and p-MOS devices.

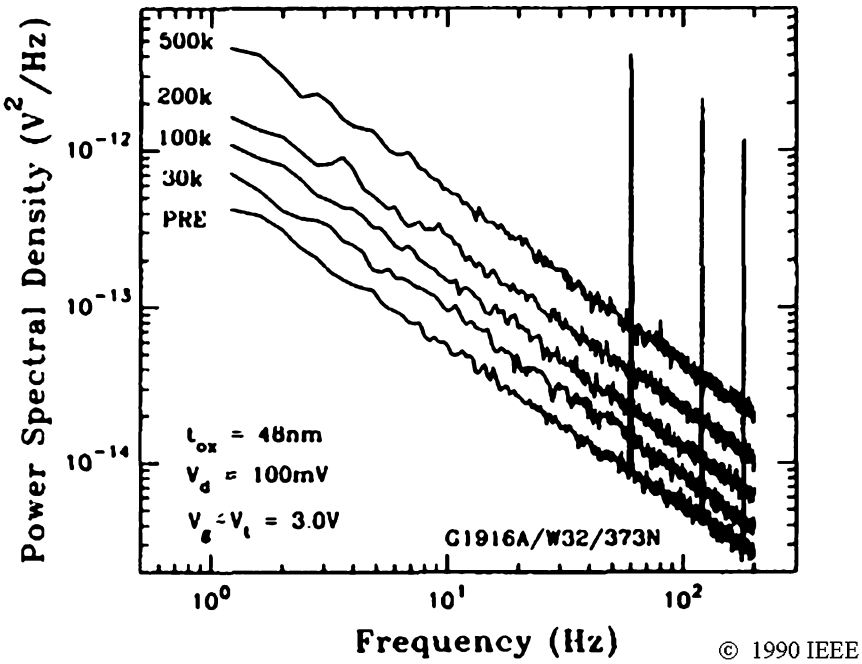

Fig. 15. 1/f noise spectra, S_v, of irradiated n-channel MOSFETS [40].

terminals are biased such that the device is operating in its linear regime [40]. The noise power factor can be expressed as

$$K_n = \frac{q^2 kT}{WL}\frac{N_{ss}}{E_g}\left(\frac{t_{ox}}{k_{ox}\varepsilon_0}\right)^2\left[\ln\left(\frac{t_{max}}{t_{min}}\right)\right]^{-1} \quad (9)$$

where k is Boltzmann's constant, T is absolute temperature, W and L are the gate width and length of the MOSFET, respectively, N_{ss} is the areal density of switching states, E_g is the SiO_2 bandgap, and t_{max} and t_{min} are the presumed maximum and minimum "cutoff" times associated with noise processes [28].

Subsequent analysis on this and other 1/f noise data sets revealed a proportional relationship between the K_n and the hole trapping efficiency factor f_{ot} [28], [40], [42], [43]. Unlike interface traps, border traps are created as a result of hole trapping. As a result, switching oxide (border) traps and not interface traps are typically assumed to be the defects responsible for increased low frequency noise in irradiated CMOS devices [28]. Thus, the switching state density, N_{ss}, in (9) is typically replaced with the variable N_{bt}, i.e., the areal density of border traps.

IV. Radiation Effects on Modern Technologies

A. Ultra-Small Bulk CMOS

1) Radiation Damage in Isolation Oxides: In the 1980s, Saks and Ancona predicted that technology scaling would reduce a MOSFET's susceptibility to radiation-induced damage in gate oxides [44]. This is due primarily to the fact that, to first order, defect buildup in gate oxides scales with t_{ox} (4). Radiation tolerance in thin gate oxides is further enhanced by the increased likelihood of positive charge annihilation or compensation by tunneling elections from the adjacent materials [45]. Inherent gate oxide hardness was demonstrated at the 0.25 μm technology node [46]. At this node, the oxide thickness is typically less than 6 nm, which is less than twice the approximate distance for high probability electron tunneling (i.e., $\sim$3 nm) [18], [45]. Gate oxide hardness trends have continued to be observed in subsequent smaller technologies, e.g., 0.18 μm ($t_{ox} = 3.2$ nm) and 0.13 μm ($t_{ox} \sim 2$ nm) [47]. As discussed in the previous section, defect buildup in thicker isolation oxides is typically the dominant

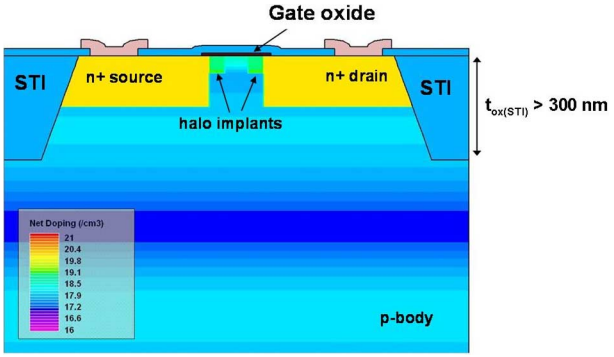

Fig. 16. Representative cross-section of an n-channel MOSFET in a modern CMOS technology.

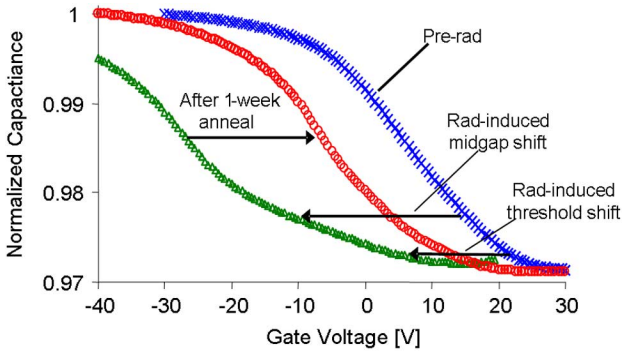

Fig. 17. *C–V* response of the FOXCAP for worst-case bias conditions.

cause of radiation-induced degradation in the dc parameters of modern CMOS devices and integrated circuits. A representative cross-section of a modern n-channel MOSFET is shown in Fig. 16. As the figure illustrates, the STI structures enclosing the active device are much thicker (by more than two orders of magnitude) than the gate oxide. In advanced CMOS technologies the STI oxide thickness is typically greater than 300 nm.

In order to quantify TID defect build-up in advanced CMOS isolation structures, radiation exposures and capacitance-voltage (C-V) measurements were performed on STI field oxide MOS capacitors (FOXCAPs) fabricated in a commercially available 130 nm process. The FOXCAP was built with an array of single capacitor cells placed in parallel. Each cell integrates an n-type poly-Si top gate over the STI, which is deposited into the p-well (body). C-V measurements were taken prior to radiation exposure, after irradiations up to 1 Mrad (SiO_2), and after an elevated temperature postirradiation anneal (1 week at 100 °C). A gate bias of either 0 or 1.32 V was applied to the structures with all other pins grounded during exposure. The radiation source used for the experiments was the Co^{60} GammaCell at Arizona State University. Fig. 17 shows the *C–V* responses of the FOXCAP for the worst-case irradiation bias conditions (i.e., $V_G = 1.32$ V) prior to radiation, after 1 Mrad (SiO_2), and after the postirradiation anneal.

As shown in Fig. 17, the FOXCAP exhibits the characteristic negative shift in the *C–V* response after irradiation [10], [48]. This response indicates a build-up in radiation-induced defects. The positive shift in the *C–V* curve after the one week anneal indicates a moderate amount of defect removal or compensation

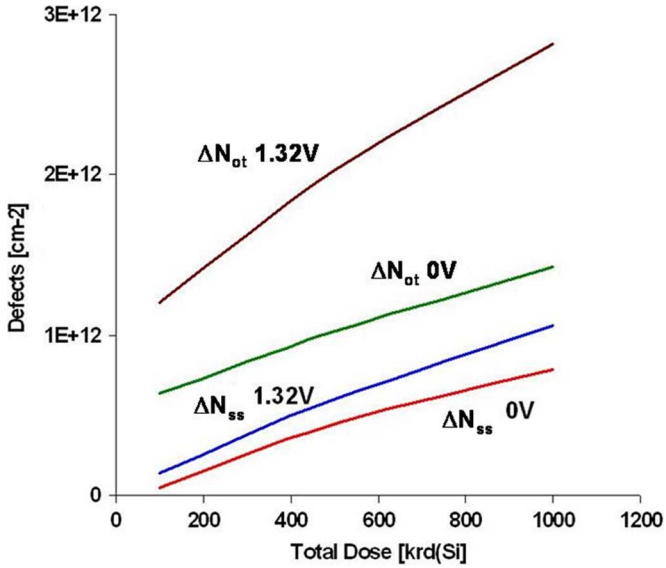

Fig. 18. Buildup of N_{ot} and N_{ss} as a function of radiation bias and exposure level.

occurs in these oxides as a result of time and/or temperature dependent processes. The build-up of oxide trapped charge in the STI oxide can be computed as

$$\Delta N_{\rm ot} = -\frac{k_{\rm ox}\varepsilon_0}{qt_{\rm ox(STI)}}\Delta V_{\rm mg} \tag{10}$$

where ΔV_{mg} is the change in the midgap gate voltage (i.e., ΔV_{ot}). The build-up of switching states (interface traps and border traps) above midgap can be approximated as

$$\Delta N_{\rm ss} = -\frac{k_{\rm ox}\varepsilon_0}{qt_{\rm ox}({\rm STI})}(\Delta V_t - \Delta V_{\rm mg}) \tag{11}$$

where ΔV_t is the change in the gate voltage at threshold [10], [48]. Using (10) and (11), the build-up of N_{ot} and N_{ss} in the STI can be computed at each dose level. Fig. 18 plots the buildup of each defect type as a function of radiation bias and exposure level. As the figure indicates, radiation bias has a strong effect on the buildup of trapped charge and to a lesser extent, the buildup of switching states. The results in Fig. 18 suggest that as with older CMOS technologies, radiation-induced increases in TID defects in modern STI structures is linearly related to the exposure level.

In order to assess the relative hardness level of the 130 nm isolation oxide, the results of the FOXCAP experiments are compared to the responses of MOS capacitors with similar dielectric thicknesses, but manufactured in different technologies [49]. Using (4)–(6), a damage factor constant, K, relating ΔV_{ot} to dose (D) can be obtained using the following equation [10]:

$$\Delta V_{\rm ot} = -D \times K \times t_{\rm ox}^2 \tag{12}$$

where $K = ((q)/(k_{ox}\varepsilon_0))\kappa_g f_y f_{ot}$ is the damage factor constant associated with the exposed oxide.

Since the parameter f_{ot} is the primary factor that can alter the damage factor constant, a higher value for K signifies greater trapping efficiency in an oxide. In Table II, the damage factors are compared for the STI (FOXCAP), base oxides (XFCB and RF25), a thermal oxide (E4403/W21), and an SOI buried

TABLE II
COMPARISON OF 130 NM STI, BASE, THERMAL, AND SOI BURIED OXIDES

Device	t_{ox} (nm)	Type	Area (cm^2)	ΔV_{ot} (V)	K (x 10^3)
FOXCAP	320	p	0.0023	6.5	63.5
RF25	600	p	0.0012	4.175	11.6
XFCB	600	p	0.0070	6.12	17
E4403/W21*	1080	n	0.030	7.7	33.01
SIMOX	370	n	0.022	2.2	16.07

*data taken after 20 krad(SiO_2) exposures
**radiation bias is 0V for all devices

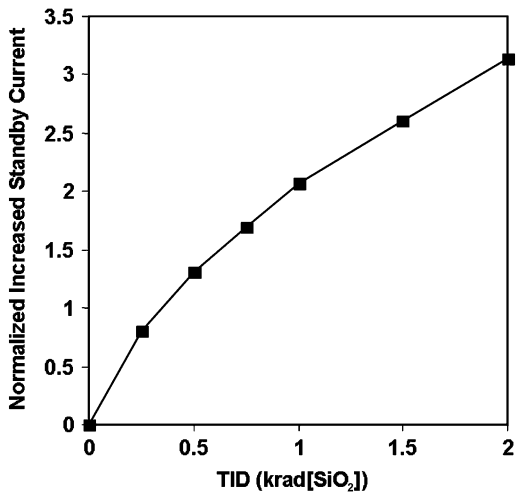

Fig. 19. Normalized increased standby current versus total dose in shift registers fabricated in 130 nm process [51].

(SIMOX) oxide. All results in the table, except for E4403/W21, were obtained for total dose levels of approximately 100 krad(SiO_2) with 0 V bias conditions during exposure. The E4403/W21 data is for a total dose of 20 krad(SiO_2). In the table, it is seen that the STI has the largest damage factor and thus has the greater trapping efficiency. This may be due to either a higher density of hole trapping defects or a greater trapping cross-section for holes in the STI. The results suggest that the radiation tolerance of modern trench isolation structures may actually be worse than other isolation technologies.

2) Leakage Paths: Radiation-induced degradation in shallow trench isolation oxides is typically caused by exposure to high fluxes of ionizing radiation. Micro-doses of damage brought on by a single ion strike have also been observed in ultra small CMOS technologies [50]. Damage to the STI can cause a significant increase in the standby current in modern CMOS integrated circuits. Fig. 19 plots the normalized increase in standby current in CMOS shift registers manufactured in a commercial 130 nm process [51].

The causes of increased standby current are leakage paths created as a result of TID defect buildup in the shallow trench isolation structures of the 130 nm technology. These leakage paths include: 1) drain-to-source leakage in a single n-channel MOSFET, 2) drain-to-source leakage between two different devices, and 3) source-to-well leakage between two different devices. The basic mechanisms for all field leakage phenomena

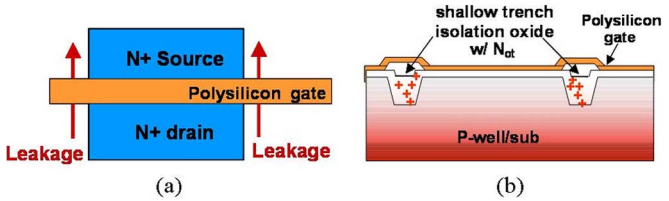

Fig. 20. (a) Illustration of drain-source leakage path in n-channel FETs and (b) its cause; oxide trapped charge buildup in the isolation oxide [53].

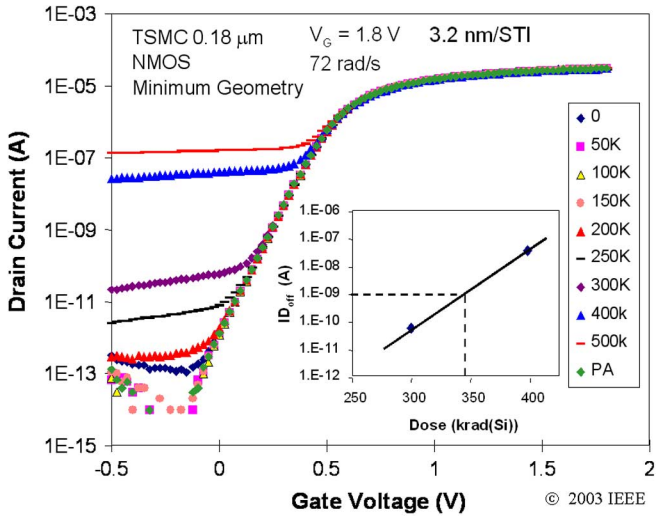

Fig. 21. Impact of STI radiation damage on the current-voltage characteristics of nFET fabricated in TSMC 0.18 μm CMOS [47].

are the same. Positively charged oxide defects invert an adjacent p-type Si layer, which enables the flow of current from one isolated region to another.

a) Drain-to-Source Leakage: Charge trapped in the isolation dielectric, particularly at the Si/SiO_2 interface along the sidewalls of the trench oxide, creates a leakage path which becomes the dominant contributor to off-state drain-to-source leakage current in n-channel MOSFETs (n-FET) [52]. This effect is illustrated schematically in Fig. 20, which shows a) the edge leakage path from drain-to-source on the planer (top) view of the n-FET and b) the device cross-section with fixed oxide trapped charge buildup in the STI [53].

The impact of STI radiation damage on the n-FET current-voltage characteristics of one deep submicron technology is shown in the experimental data in Fig. 21, [47]. These data were obtained from total ionizing dose (TID) measurements on 0.18 μm n-channel MOSFETs fabricated by the Taiwan Semiconductor Manufacturing Company (TSMC) [47]. The data

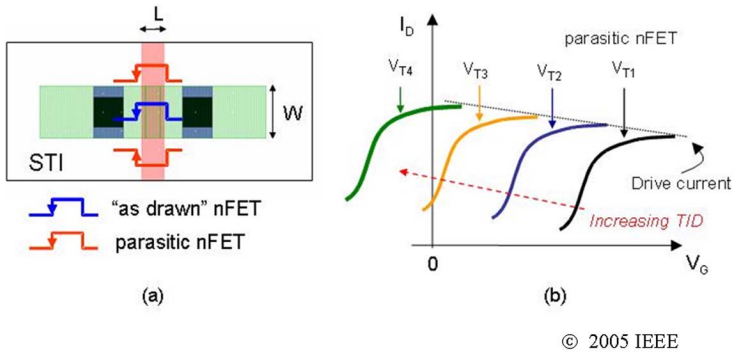

Fig. 22. (a) Illustration of the circuit-level models associated with the n-channel MOSFET with parasitic nFETs, and (b) the effects of increasing total ionizing dose (TID) radiation exposure on the threshold voltage and drive current of the parasitic nFET [53].

show that off-state leakage current, $I_{d,off}$, shows a significant monotonic increase above 200 krad(SiO_2), reaching a level above 100 nA at 500 krad(SiO_2) of total dose [47].

The primary cause of increased $I_{d,off}$, is the reduction in threshold voltage and increase in drive current in the parasitic n-FET formed along the two edges of the "as drawn" device Fig. 22(a). Prior to radiation exposure, the threshold voltage is high and drive current is low for the parasitic device relative to the "as drawn" structure. Upon exposure to ionizing radiation, the threshold voltage of the parasitic device is reduced significantly relative to the "as drawn" transistor Fig. 22(b). This is because the "gate" oxide of the parasitic structure is formed from the STI, which is much thicker than the "as drawn" gate dielectric. In addition to negative voltage shifts, the drive current of the parasitic n-FET also increases significantly Fig. 22(b). This is due to the fact that the effective width of the parasitic transistor $(W_{eff.})$, to which drive current is proportional, increases as surface along the STI sidewall inverts in response to N_{ot} buildup [53]. The degree to which ΔN_{ot} can invert this surface is also inversely proportional to the doping concentration along the sidewall [53]. Thus, a higher doping concentration in the p-type body will typically mitigate the effects of fixed oxide trapped charge in the STI.

In order to examine the scaling trends of drain-to-source leakage, the pre- and postirradiation I_d versus V_{gs} characteristics of a commercial 130 nm CMOS technology are shown in Fig. 23, [51]. These data indicate that negative voltage shifts in the parasitic edge devices are significantly smaller than the 180 nm TSMC technology (Fig. 21). The increased radiation tolerance of the 130 nm technology may be due to the aggressive use of halo implants. In advanced CMOS technologies, highly-doped halo implants (Fig. 16) are used to suppress SCEs. Like the thinning of gate oxides, this deep-submicron processing technique seems to be fortuitously increasing the radiation tolerance of modern CMOS devices. At the 130 nm node, where the physical gate length is below 100 nm, the halo doping may extend across the entire channel for minimum gate length devices. This significantly increases the p-type doping concentration along the entire STI sidewall, between the drain and source of the n-channel MOSFETs. The increased doping will inhibit the impact fixed oxide charge, thereby increasing the inherent radiation hardness of ultra-small bulk CMOS devices.

b) Interdevice Leakage: Unlike drain-to-source leakage, where the leakage path is associated with one n-channel device, interdevice leakage pertains to paths that are created between the n+ drains and sources of two adjacent n-FETs or between the n+ drain/source of one n-FET and the n-type well of an adjacent p-channel MOSFET. A schematic illustration of the n-FET device-to-device leakage mechanism is illustrated in Fig. 24. A schematic illustration of the n-FET drain/source-to-n-well leakage mechanism is illustrated in Fig. 25.

The impact of interdevice leakage on the supply current can be observed in the following inverter chain example, shown in Fig. 26 below. Path (a) represents the leakage path caused by n-FET device-to-device leakage. The bold line corresponds to the radiation-induced parasitic path between two n-FET drains. The current path from V_{DD} to ground is completed via the second stage p-FET and first stage n-FET, both biased in their linear region in this example. Path (b) represents the leakage path caused by n-FET drain/source-to-n-well leakage. The bold line corresponds to the radiation-induced parasitic path between the first stage n-FET drain and the n-well of the first stage p-FET. Here the current path from V_{DD} to ground is completed via the first stage n-FET biased in its linear region in this example.

At the present time, interdevice leakage does not seem to be a great TID-threat in modern CMOS technologies. Recent experiments on field oxide transistors fabricated in two separate commercial 130 nm processes indicate that off-state current per unit width remains below 1 nA/μm after 500 krad(SiO_2) of total dose. Thus, interdevice leakage at the 130 nm technology node is more than a factor of two less than single device drain-to-source leakage (Fig. 22). Whether these trends continue when technologies scale to smaller feature sizes is unknown at the present time.

B. Total Dose Effects in Fully Depleted SOI

1) FDSOI DC Response: Modern FDSOI MOSFETs have been shown to be significantly more susceptible to total ionizing dose effects than their bulk counterparts [54]–[56]. In 2005, Paillet *et al.* presented the I_d versus V_{gs} (front gate) dc characteristics of irradiated n-channel FDSOI MOSFETS with minimum gate lengths below 100 nm [56]. These responses are shown in Fig. 27, [56]. The FDSOI n-FET used for these experiments was fabricated with a p-type UNIBOND substrate, a

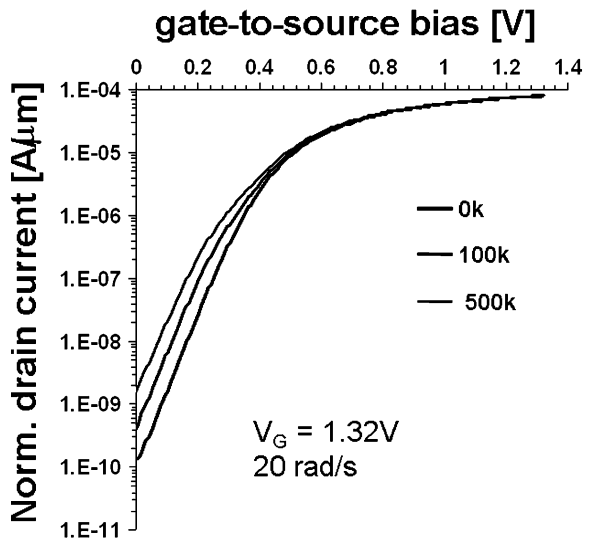

Fig. 23. Impact of STI radiation damage on the current-voltage characteristics of nFET fabricated in 0.13 μm CMOS [51].

BOX thickness $(\mathrm{t_b})$ of 100 nm, and an 11 nm thick p-type Si body $(\mathrm{t_{Si}})$. During irradiation, the gate and body biases were fixed at 0 V while the drain and source terminals were biased at 1.2 V (i.e., a transmission gate bias condition). As the data in Fig. 27 reveal, these ultra-small SOI devices exhibit significant negative voltage shifts in response to TID exposures. Indeed, the threshold voltage shifts are greater than -300 mV after 500 krad of total dose [56]. By comparison, the 130 nm bulk technology exhibits negligible $\mathrm{V_t}$ shifts at this dose level (Fig. 23).

It is unlikely that the cause of these shifts is due to radiation damage to the front gate oxide. This is because the front gate oxide $(\mathrm{t_{ox}})$ in this FDSOI technology is very thin (1.8 nm). Instead, radiation defect buildup in the much thicker BOX layer is the more probable cause of dc parametric degradation. A schematic illustration of the FDSOI device indicating the location of TID defects in the BOX (plus symbols) is provided in Fig. 28. Fixed positive charge $(\mathrm{N_{ot}})$ buildup in the BOX will, as with all MOS systems, lead to negative shifts in the threshold voltage of the back gate transistor, which is denoted as $\mathrm{V_{tb}}$. The impact of radiation damage, BOX thickness, and transistor gate length on $\mathrm{V_{tb}}$ can be observed in Fig. 29, [54]. These data were obtained from radiation experiments on different FDSOI MOSFETs, having BOX thicknesses between 80 and 410 nm [54]. After 1 Mrad TID exposures, shifts in $\mathrm{V_{tb}}$ range from -2.5 V and -42.5 V depending on the BOX thickness. Furthermore, the data suggest a sublinear relationship between threshold voltage and oxide layer thickness, which is consistent with the square root dependence described previously (6). Studies have shown that a reduction in back gate threshold voltage can lead to back-channel drain-to-source leakage, an enhanced latch effect, and a reduction in front gate threshold voltage due to electrostatic coupling between the two gates [54]–[57]. It is this later effect which is the likely cause of the degradation in the dc characteristics observed in Fig. 27.

In the discussion of dual gate operation in FDSOI technologies provided in the first section, a qualitative explanation of the relationship between back gate bias on the front gate threshold voltage was presented. Quantitatively, this relationship is best understood by means of a "coupling" coefficient $\mathrm{k_c}$, which is the proportionality constant between $\mathrm{V_{tb}}$ and the threshold voltage of the front gate $(\mathrm{V_{tf}})$ [54], i.e.,

$$V_{\mathrm{tf}} = k_c V_{\mathrm{tb}}. \tag{13}$$

Through an analysis of the electrostatics of dual gates, it is readily shown that $\mathrm{k_c} \approx \mathrm{t_{ox}}/\mathrm{t_b}$ [54]. The reduction in $\mathrm{V_{tb}}$ caused by the buildup of $\mathrm{N_{ot}}$ in the BOX leads to a reduction in $\mathrm{V_{tf}}$ by $\Delta\mathrm{V_{tb}}/\mathrm{k}_c$. The coupling effect can be observed in the experimental data shown in Fig. 30, [54]. Negative voltage shifts in the dc response of modern FDSOI n-FETs can therefore be explained as the combined effects of damage to the thick BOX layer and back gate coupling.

2) FDSOI 1/f Noise Response: As explained in the previous section, border trap buildup as a result of ionizing radiation can increase the low frequency 1/f noise in CMOS devices [28], [40]. Moreover, given the discussion above, the "thick" buried oxides of commercial FDSOI MOSFETs tend to exhibit measurable increases in oxide trapped charge with radiation. Thus, it seems reasonable that radiation damage to the BOX layer may have an impact on 1/f noise in SOI devices. In 2004, Xiong *et al.* presented data on radiation-induced excess back channel noise [58]. These data are shown in Fig. 31. The BOX thickness of the SOI transistor used in these experiments was 170 nm. As the data in Fig. 31 show, there is no more than a factor of two increase in the normalized noise power factor $(\mathrm{K_n})$ after 2 Mrad of total dose. This increase is significantly smaller than the order of magnitude increase observed in 48 nm gate oxides irradiated to 500 krad (Fig. 15). Although the 48 nm gate oxides were fabricated in a much older bulk technology, the authors of [58] contend that it is unlikely that the different responses may be explained by the greater hardness of the BOX. On the contrary, it is suggested that the slow increase in SOI back channel noise is likely due to a high BOX defect density before irradiation [58]. Thus, at least for the present, radiation damage in the buried oxide may not pose a great threat to the noise performance of SOI devices. However, with further improvements to the quality of BOX layers and back-channel interfaces, radiation damage to buried oxides may yet have a deleterious impact on noise performance in future SOI technologies.

C. Ultra-Thin Oxides

1) 1/f Noise: A recent examination of the effects of commercial technology scaling revealed that MOSFETs can exhibit more than an order of magnitude increase in 1/f noise as CMOS technology is shrunk from 350 nm to 130 nm [41]. The study by Chew *et al.* reported that the increase was most likely due to the near order of magnitude jump in oxide traps in ultra thin gate oxides prior to radiation exposure [41]. As (9) shows, the noise power factor $(\mathrm{K_n})$ is proportional to the density of switching oxide defects, specifically border traps. While this rise in border trap density is not uniform across all CMOS technologies, the results are somewhat troublesome, especially for designers of modern communication systems where low noise is critical [41]. Fortunately, radiation damage to thin oxides does not seem to significantly add to the problem. In their comparison of TID effects in 350 nm, 250 nm, and 180 nm CMOS technologies,

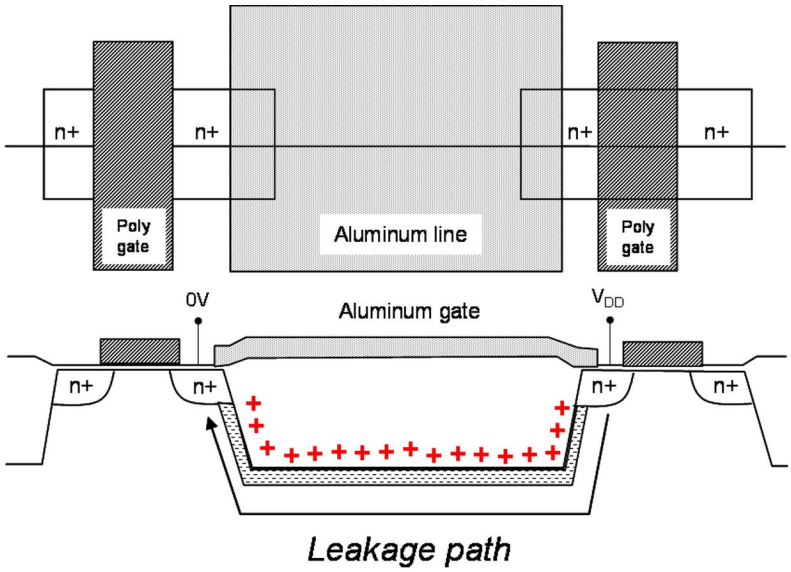

Fig. 24. Schematic illustration of n-FET device-to-device leakage.

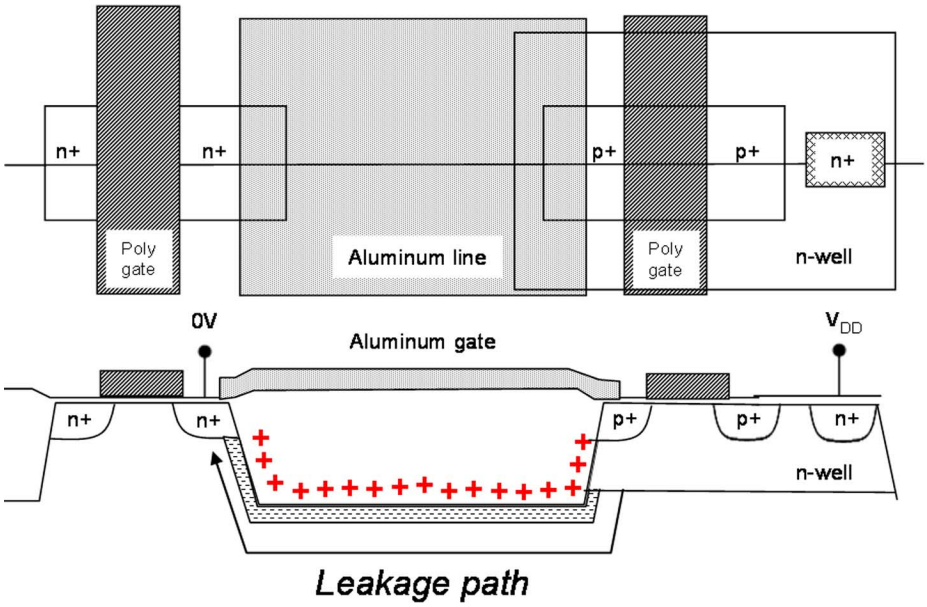

Fig. 25. Schematic illustration of n-FET drain/source-to-n-well leakage.

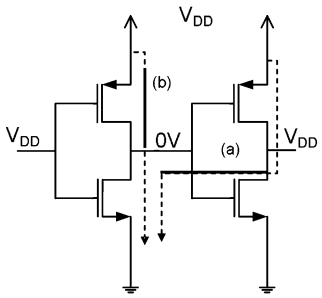

Fig. 26. Example of how interdevice leakage can increase the supply current of inverter chain. Path (a) represents the leakage path caused by n-FET device-to-device leakage. Path (b) represents the leakage path caused by n-FET drain/source to p-FET n-well leakage.

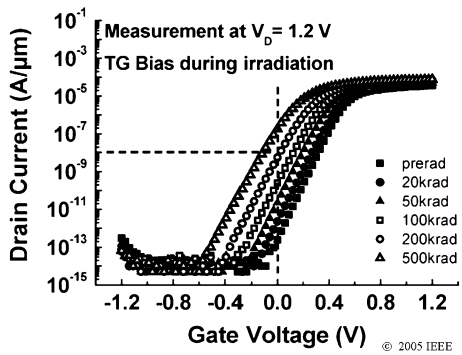

Fig. 27. Normalized drain current versus front gate voltage on an 80 nm FDSOI n-FET [56].

Manghisoni *et al.*, reported that after 10 Mrad of total dose the worst case increase in K_n was only a factor of two for both n-FETs and p-FETs biased in saturation during radiation exposure [59]. Moreover, this increase was observed only at the

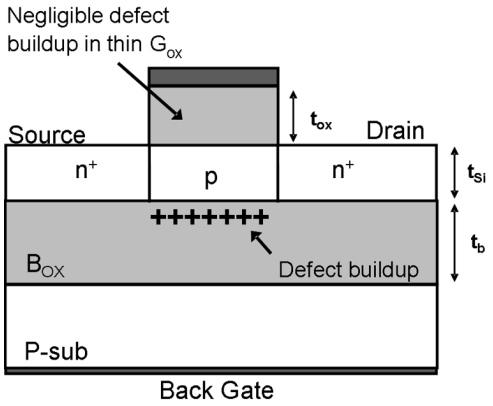

Fig. 28. Schematic illustration of FDSOI cross-section indicating location of TID defects (red plus symbols) in the BOX layer.

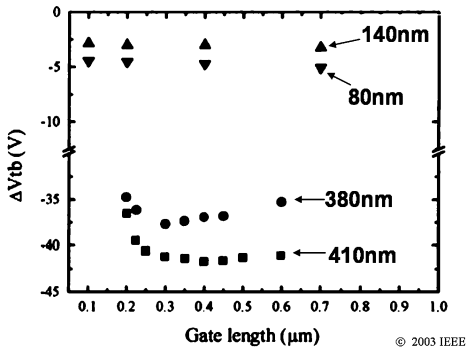

Fig. 29. Comparison of back gate V_t shifts after 1 Mrad for BOX layers of different thicknesses [54].

350 nm node. Indeed, subsequent generations exhibited a reduction in power factor enhancement. For the 130 nm node, the increase in K_n was 1.3 for n-FETs and 1.4 p-FETs after 10 Mrads [60]. This improvement in the postirradiation noise performance of CMOS technologies scale is likely due to reduced defect buildup in thinning oxides.

2) Radiation-Induced Leakage Current: One of the greatest threats to deep submicron CMOS today is the reliability of the gate oxide. Due to its extremely small thickness (around 2 nm for most 130 nm nodes), the oxides are easily damaged leading to increased carrier leakage from gate into the underlying substrate. The impact of radiation only exacerbates the gate leakage problem.

Radiation Induced Leakage Current (RILC) was reported in oxides below 8 nm in the late 1990s. RILC is characterized by electron tunneling via neutral traps created in the oxide layer by radiation exposure [45], [60]. RILC is a function of the electric field in the oxide during radiation exposure, as exhibited by the data shown in Fig. 32, [61]. In this plot, the abscissa is the electric field in the oxide during irradiation and the ordinate is the magnitude of gate current density through the oxide. The white circles and black squares denote the leakage response for 2 V and -2 V, respectively applied to the gate during measurements. This strong field dependence suggests that the radiation-induced oxide traps are not generated directly by radiation interactions but rather by field dependent processes similar to those related to hole trapping in the oxide [45]. Some researchers contend that the neutral traps involved in RILC behave very much like electron compensated E_γ' defects [45]. As discussed in the previous section, these dipoles form neutral electron traps that are highly stable and shallow. In ultra thin oxides, where the tunneling distance is less than 3 nm, these oxide (border) traps are relatively easy to fill or empty [17], [33].

In addition to the radiation field and measurement bias dependence, RILC increases nearly linearly with dose and is not surprisingly a function of oxide thickness. These dependencies can be seen in Fig. 33, [61]. As the data in this figure indicate, the gate current density for these technologies is a near linear function of dose and increases significantly as the oxide thickness is scaled from 6 nm to 4 nm. The higher leakage for the thinner oxide is likely due to the increased probability of electron tunneling into and out of the radiation-induced border trap defects [45].

The data presented in Figs. 32 and 33 seem to suggest that RILC may be a significant emerging radiation threat in ultra thin oxides. However, in a study by Wang *et al.*, 3.2 nm oxides were exposed to high energy gamma rays up to 30 Mrad. The results, shown in Fig. 34, indicate that total dose exposures on this technology do not have a significant impact on gate leakage up to 30 Mrad [62]. It should be noted that the researchers who published this work caution that these measurements were performed on a specific process at a specific thickness (3.2 nm), which is relatively thick by today's standards [62]. Further reductions in oxide thickness may increase a gate oxide's susceptibility to high-energy photons, electrons, or protons due to increased tunneling probabilities. Another open question is whether or not RILC susceptibility will be large relative to preirradiation leakage specification in more advanced, aggressively scaled technologies.

D. High-k Dielectrics

Alternative dielectrics for conventional SiO_2 films are of great interest in future CMOS technologies because they enable the use of thicker materials without compromising rules for constant field scaling. As can be seen from the above discussion, thicker oxides are desirable because they reduce gate leakage current and other reliability threats.

Radiation-induced charge buildup in gate oxides was a major concern when gate oxide thicknesses were greater than 50 nm [63]. Due to aggressive scaling, this concern has almost been eliminated. Indeed, excellent total-dose hardness is a supplementary benefit of aggressive gate oxide scaling [64]. The end result is that thermally grown gate oxides in advanced commercial technologies are radiation hard, withstanding accumulated doses in excess of 1 Mrad (SiO_2) with little threshold voltage shift [63]. High-k gate materials use potentially much thicker dielectrics to obtain the equivalent capacitance of much thinner SiO_2 gates while reducing gate leakage susceptibility. Due to the strong dependence of TID damage with dielectric thickness, gate oxide radiation response could be an issue once again if high-k dielectrics are used in place of SiO_2[63].

There is increasing interest in the radiation hardness of the high-k dielectrics under consideration for replacing SiO_2. The radiation hardness of several candidate high-k gate insulators

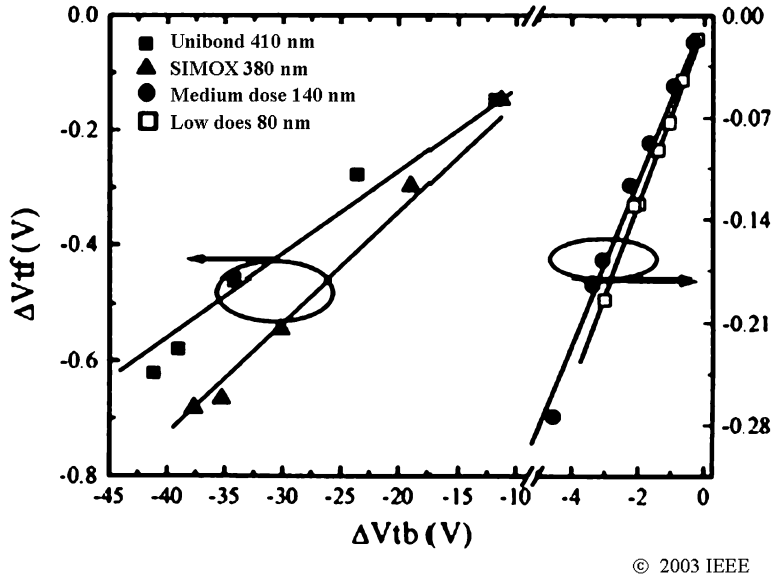

Fig. 30. Proportional relationship between radiation-induced front gate threshold voltage and back gate threshold voltage shifts [54].

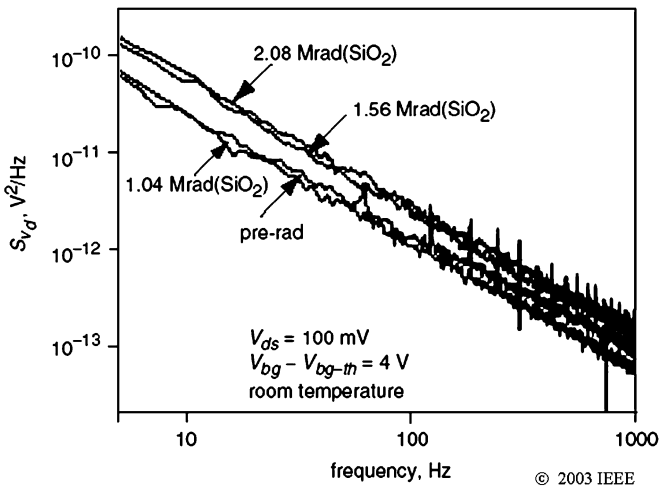

Fig. 31. SOI back gate transistor 1/f noise spectra prior to and after radiation exposure [58].

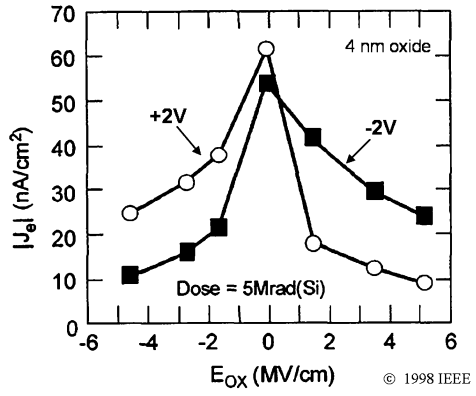

Fig. 32. Post-irradiated gate current density as a function of oxide field during radiation exposure and gate bias during measurement [61].

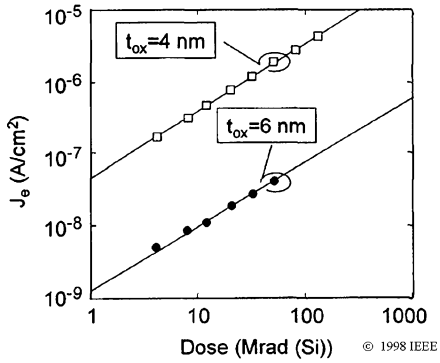

Fig. 33. Gate current density versus dose for 6 nm and 4 nm oxides [61].

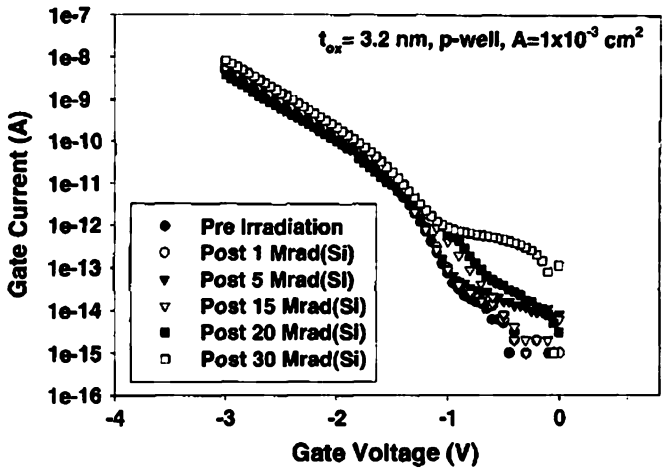

Fig. 34. Radiation-induced leakage current characteristics following γ-ray exposures for 3.2 nm oxides [62].

are reviewed here, including nitrided oxides (RNO) [65] and hafnium silicate dielectrics [66].

1) Nitrided and Reoxidized Nitrided Oxides (RNO): Fig. 35 is a plot of the midgap voltage shift for p-channel transistors fabricated with a hardened oxide and with an RNO oxide versus dose [65]. As can be seen in the figure, oxide trapped charge

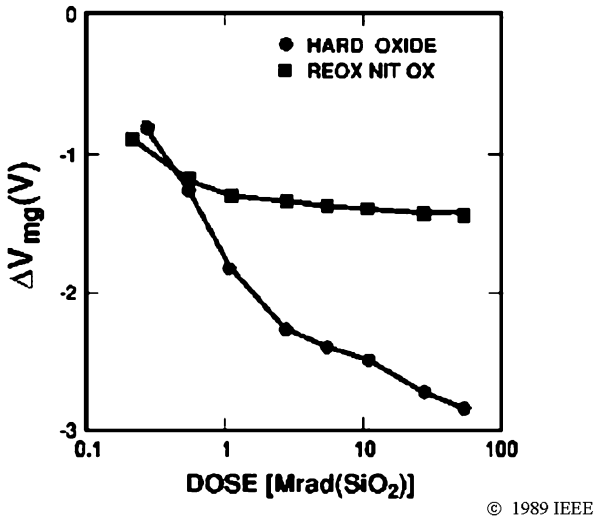

Fig. 35. Midgap voltage shift for p-channel transistors fabricated with a hardened oxide and with a RNO oxide versus dose [65].

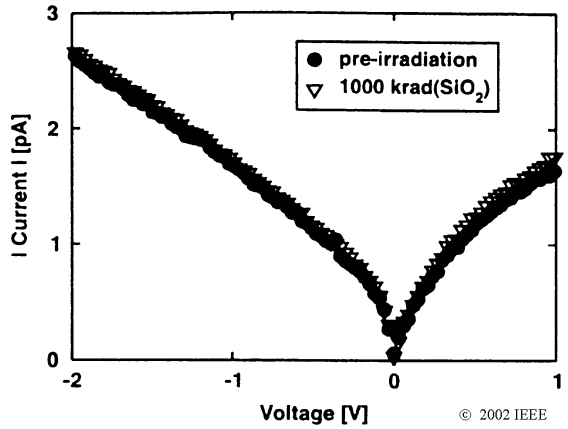

Fig. 36. Pre- and postrad oxide leakage current in a hafnium-silicate capacitor with dielectric thickness of 29 nm ($\mathrm{EOT} = 4.5$ nm) [66].

buildup, which is proportional to $\Delta \mathrm{V_{mg}}$, is significantly lower for RNO compared to hardened thermal oxides. Additionally, the authors of [65] showed that RNO dielectrics exhibit essentially no interface trap buildup when compared with thermal SiO_2 [65]. In fact, RNO dielectrics can be fabricated such that there is no measurable interface-trap buildup for transistors irradiated to total doses in excess of 50 Mrad(Si) [65]. Thus, based on recent studies, the conclusion is that the radiation hardness of ultra-thin RNO dielectrics should be extremely good [65].

2) Hafnium Dielectrics: Hafnium-silicate has a high dielectric constant (~ 25) compared to SiO_2. It has also been shown to be more resistant to stress and TDDB and is less reactive with polysilicon than many of the other dielectrics being pursued. Fig. 36 is a plot of gate oxide leakage current in a hafnium-silicate capacitor with dielectric thickness of 29 nm (effective oxide thickness-EOT, of 4.5 nm). As the figure indicates, there is a negligible change in leakage current for parts irradiated with 10 keV X rays up to 1 Mrad (SiO_2). Thus, photon exposures up to 1 Mrad(SiO_2) do not have an impact on leakage in these high-k dielectrics.

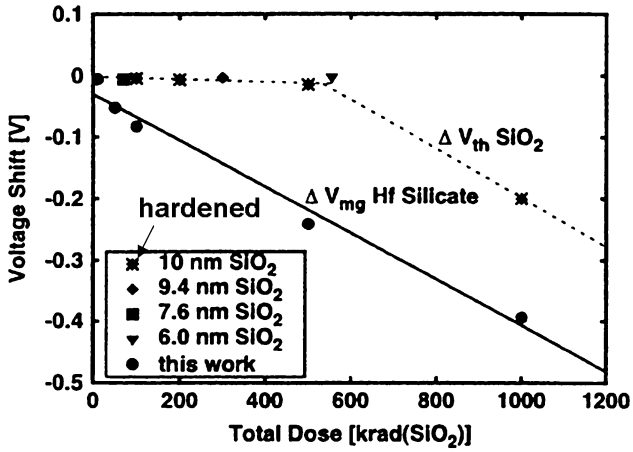

Fig. 37. Voltage shift versus dose for 2 V irradiation of the 4.5 nm EOT (29-nm physical thickness) hafnium-silicate devices compared to shifts seen in SiO_2 from several processes [66].

More detailed studies on the hafnium silicate capacitors have revealed that these dielectrics show significantly higher hole trapping efficiencies compared to radiation hardened SiO_2. Hole trapping efficiency $(\mathrm{f_{ot}})$, as discussed in the previous section, is a measure of the probability of hole capture in precursor defects in the dielectric. For SiO_2 dielectrics, hole trapping efficiency may be derived from (12) as

$$f_{\mathrm{ot}} = -\frac{\Delta V_{\mathrm{ot}} k_{\mathrm{ox}} \varepsilon_0}{q D \kappa_g f_y t_{\mathrm{ox}}^2}. \tag{14}$$

For high-k dielectrics the formula for trapping efficiency must be adjusted to account for the difference in κ_g and the physical thickness of the dielectric. A reasonable estimate of κ_g (high-k) is

$$\kappa_g(\mathrm{high}-k) = \kappa_g(\mathrm{SiO_2}) \frac{E_g(\mathrm{high}-k)}{E_g(\mathrm{SiO_2})} \tag{15}$$

where E_g (SiO_2) and E_g (high-k) are the bandgaps of SiO_2 and the high-k dielectric, respectively [66]. Given (14) and (15), the trapping efficiency for high-k dielectrics can be estimated as

$$f_{\mathrm{ot}}(\mathrm{high}-k) = -\frac{\Delta V_{\mathrm{ot}} k_{\mathrm{ox}} \varepsilon_0}{q D \kappa_g(\mathrm{SiO_2}) \frac{E_g(\mathrm{high}-k)}{E_g(\mathrm{SiO_2})} f_y t_{\mathrm{ox}} t_{\mathrm{phys}}} \tag{16}$$

where $\mathrm{t_{phys}}$ is the physical thickness of the high-k dielectric [66]. In their 2002 paper, Felix *et al.* reported that the effective trapping efficiency of the hafnium-silicate dielectric was more than 20 times larger than a hardened oxide [66]. This difference in trapping efficiency was determined as the primary contributor to the relative radiation "softness" of hafnium silicate compared to hardened SiO_2. A comparison of the total dose response of hafnium-silicate and hardened SiO_2 is plotted in Fig. 37. While the results seem to suggest that the high-k material may be more prone to radiation damage then SiO_2 films, it should be noted that the high-k data were taken from relatively new processes and that the quality and hardness of these dielectrics would be expected to improve with process improvements and optimization [66].

V. Conclusion

This review paper provides an overview of some of the prominent material and device technologies being developed for or implemented in microelectronics today. After a brief introduction, a study of the selected technologies and their key parameters are provided. In the subsequent section, we provide a detailed discussion of how ionizing radiation interacts with materials to degrade both materials and devices used in integrated circuits. In the last section, we present a small subset of the data (and some analysis) that is now available in the open literature regarding total ionizing dose damage in advanced integrated circuit technologies. This review gives a brief synopsis of what is known today and may be able to be predicted in the future regarding the viability of advanced electronics in harsh radiation environments. The data and analysis presented suggests that, with respect to total ionizing dose susceptibility, the future of electronics is for the most part positive. However, testing and analysis of new technologies must continue in order to justify these claims. In particular, questions concerning the total ionizing dose hardness of gate oxides, SOI, and deep submicron CMOS when scales hit their extremes must still be addressed.

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