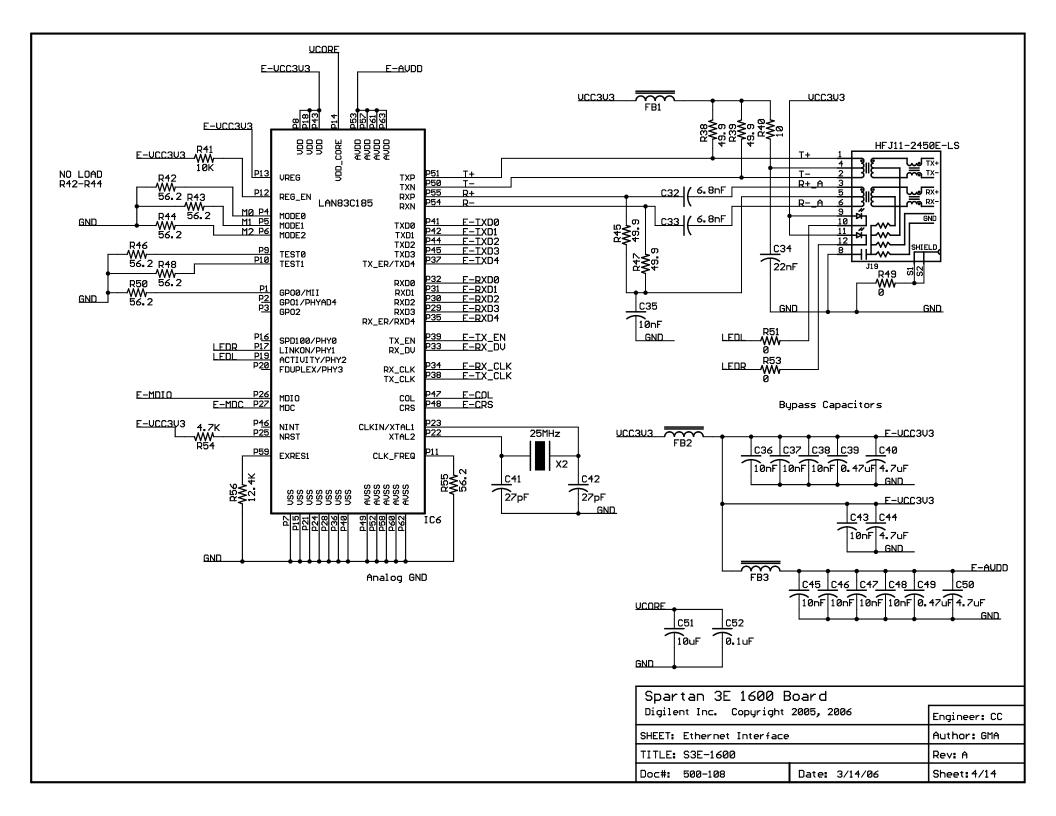
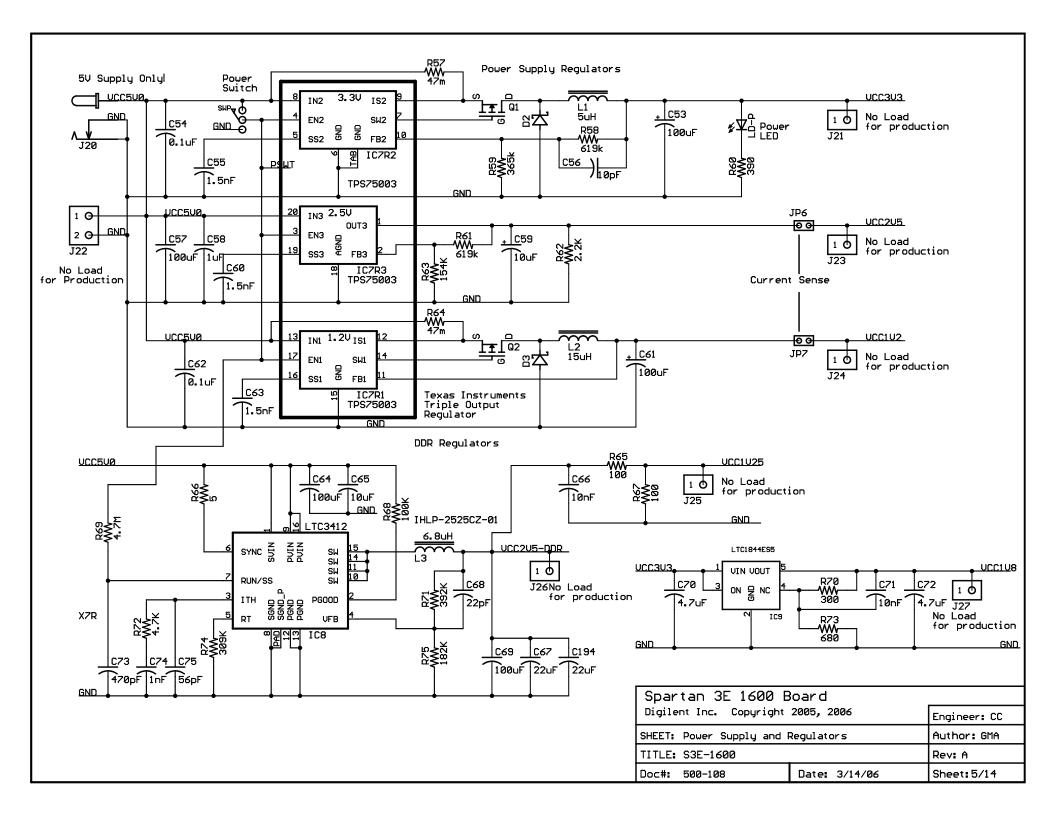
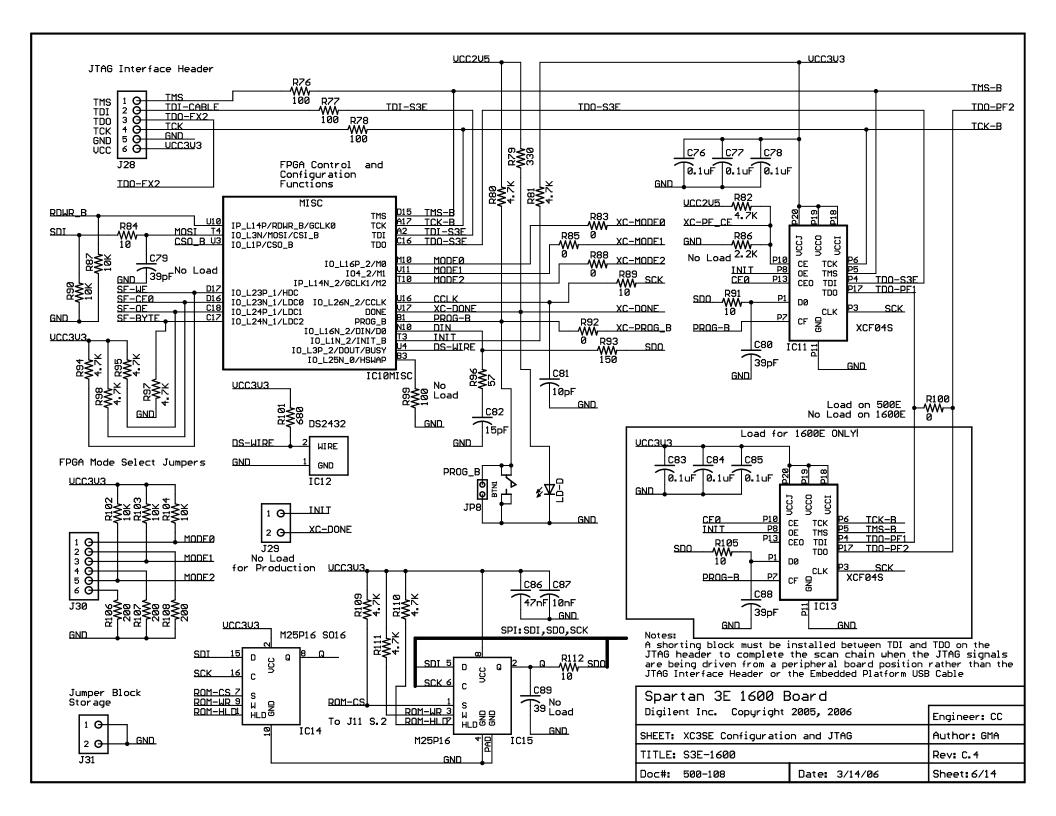


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(This page outlines the Xilinx ® proprietary USB 2.0 layout/interface.)



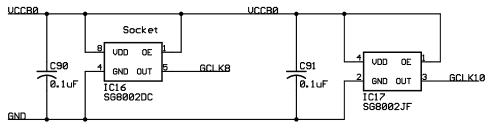






VCC for Bank 1 = 3.3V

IP2 A3 EX2-I040 C15 FX2-I035 A7 FX2-I036 D13 IP3 B15 IP4 A15 IP5 C12 IP6 D12 IP7 F10 IP8 G10 IP9 C8 IP10 D8 IP11 A5 IP12 B5 IP1 A12 FX2-I038 D6 FX2-I037 E6	IPI 10 IP3 103/VRE IP4 * IO IP5 * IO IP5 * IO IP_L2P IO IP_L2N IO IP_L7P IO_L1 IP_L7N IO_L1 IP_L10P IO_L3 IP_L10P IO_L4 IP_L16P IO_L4 IP_L16P IO_L4 IP_L16N IO_L4 IP_L22P IO_L5N/VRE IP_L22N IO_L5N/VRE IO_L6 IP_L22N IO_L5N/VRE IO_L6 IO_L15 IO_L15 IO_L15 IO_L15 IO_L17	SII	SF-STS B18 AMP-D0 E18 ROT-B G18 EAST H13 SOUTH K17 WEST D18 ROT-A K18 SW0 L13 SW1 L14 SW2 H18 SW3 N17 XC-TRIG R17 J1-I01 N15 J1-I02 N14 J1-I03 E15	104	E16 XC-CPL D_EN E17 IP13 P16 F-TX_EN P15 IP14 U18 SF-A16 T17 SF-A15 R18 SF-A14 T18 SF-A13 R15 SF-D8 R16 SF-D9 M14 TXD M14 TXD M14 TXD M15 SF-D10 P18 XC-CMD0 M15 SF-D11 M16 SF-D12 N18 XC-CMD1 M18 XC-CMD1 M18 XC-CMD1 M18 XC-CMD1 M18 XC-CMD1 M18 XC-CMD1 L16 SF-A12 L15 SF-A11 L17 LCD_F L16 SF-A12 L17 LCD_RW J12 SF-A2 J13 SF-A1
FX2-CLKOUT D10 FX2-CLKIN E10 XC-CPI D_FN B10 XMA-CLK A10 R113 GCLK8 B8 WW SD-CK P/F B9 45 GCLKIA C9 FX2-CLKIO D9	IO_L17 IO_L18 IO_L18N/URE IO_L19	F8 FX2-I011 C7 FX2-I010 D7 FX2-I09 F7 FX2-I08 E7 FX2-I07 B6 FX2-I06 A6 FX2-I06 C5 FX2-I04 D5 FX2-I03 B4 FX2-I01 C3 FX2-I01 C3 FX2-I03	SF-A10 K13 SF-A9 K12 SF-A8 K15 SF-A7 K14 SF-A6 J17 SF-A5 J16 SF-A4 J15 SF-A3 J14	10_L16P 10_L16N/A0 10_L17P 10_L11P/A10/RHCLK0	H16 XC-GCKØ



AD - A/D Converter (11) AMP - Gain Amplifier (11) DAC - D/A converter (11)

E- Ethernet (4) FX2 - Hirose FX2 Connector (1)

ROM - M25P16 (6) SD- SD RAM (12) SF - StrataFlash (12)

ST - Soft Touch Connector (1) U - USB (3)

XC - XC9572 (10)

* Notes are for pins that very between 500/1200/1600 dies

Spartan 3E 1600 Board			
Digilent Inc. Copyright	Engineer: CC		
SHEET: XC3SE Banks 0 and 1, Clock ICs		Author: GMA	
TITLE: \$3E-1600		Rev: A	
Doc#: 500-108	Date: 3/14/06	Sheet: 7/14	

Vcc for Bank 2 = 3.3V

VCC vor Bank 3 = 2.5V DDR

	BANK2)	1	
E-RX DU V2	IP1	IO1/UREF	U5 R9	E-MDIO
CENTER V16	IP2	I02/D5	R9	SF-D5
E-COL U6	ID3 *	103	P9	E-MDC
E-CRS U13	IP4 *	105	R11	E-TXDØ
NORTH V4	IP_L2P	IO6/UREF	T15	E-TXD1
E-RX_CLK	IP_L2N	IO_L 1 P	R5 T5	E-TXD2
	IP_L8P	IO_L 1 N	R6	E-TXD3
RXD R7 RXD-A U8	IP_L8N	IO_L5P	K0	<u>E-TXD4</u> SE-D13
E-RXDØ V8	IP_L11P	IO_L5N	NZ	AMP-CS
E-RXD1 T11	IP_L11N/VREF	I0_L7P	P6 N7 P7	AMP-SHDN
E-RXD2 U11	IP_L17P	IO_LZN	P8	DAC-CLR
E-RXD3 V14	IP_L17N	IO_L9P	N8	DAC-CS
E-RXD4 U14	IP_L23P	IO_L9N	R8	SF-D14
	IP_L23N	IO_L10P IO_L10N	R8 T8	SF-D15
		IO_LIBN IO_LIBP	P11	AD-CONU
J1-I04 V7	IO4 *	IO_L18P	N11	SF/XC-A23
J2-I01 V5	IO_L6P *	IO_L19P	V12	SF/XC-A22
J2-I02 V6	IO_L6N/UREF*	IO_L19N/VREF	V13	SF/XC-A21
J2-I03 N12	IO_L21P *	IO_L20P	T12	SF/XC-A20
J2-I04 P12	IO_L21N *	IO L20N	R12	SEL
	_	-	L.	
SF-D7 N9		IO_L22P/A23	P13 R13	<u>J4-I01</u> .I4-I02
<u>SF-D7 N9</u> SF-D6 M9	IO_L12P/D7/GCLK12	IO_L22N/A22	T14	J4-102 J4-103
SF-D6 U9	IO_L12N/D6/GCLK13	IO_L24P/A21	R14	
SF-D3 V9	IO_L13P/D4/GCLK14	IO_L24N/A20	V15	US2 SF-A19
SF-D2 R10	IO_L13N/D3/GCLK15	IO_L25P/VS2/A19	U15	US1_SF-A18
SF-D1 P10	10_L15P/U2/GCLKZ	IO_L25N/US1/A18	T16	US0 SF-A17
<u></u>	IO_L15N/D1/GCLK3	IO_L26P/VS0/A17		<u> </u>
			J	
	·	IC10B2		

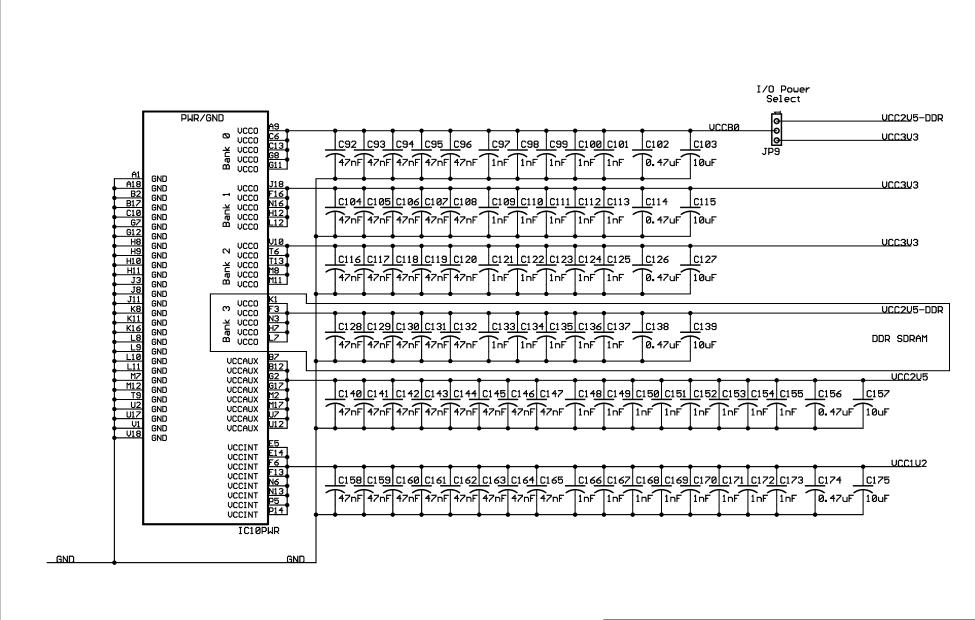
	BANK3	* IO1	D4	LEDØ
D3	IP1	* 102	F4	
0 <u>3</u> F <u>5</u> UCC1U25 Je	IP3	* IO L4P	E4	SD-A4
UCC1U25 Je	IP4/UREF	* I03/VREF	R 1	UCC1U25
GI	IPT/OREF	··· 103/ OREF	C1	SD-RAS
J 7	1 125	IO_L1P	C2	SD-CAS
ΚZ	IP6	IO_L1N	D1	SD-WE
K7	IP7	IO_L2P	D2	UCC1U25
91 17 17 18 19 19 19 19 19 19 19 19 19 19 19 19 19	IP8	IO_L2N/VREF	E2	SD-DQ8
NI NI	IP9	IO_L3P	F1	SD-DQ9
N <u>1</u> N2	IP10	IO_L3N	F1	SD-DQ10
RI		IO_L5P	F2	SD-DQ11
<u></u>	1712	IO_L5N	G3	SD-UDQS
<u>~</u>	IP13	IO_L6P	G4	UCC1U25
		IO_L6N/VREF	G6	SD-DQ12
		IO_L7P	G5	SD-DQ13
		IO_L7N	H6	SD-DQ14
		I0_L8P	H5	SD-DQ15
		IO_L8N	H 4	SD-A5
LCD-/RET E3	TO 14N *	IO_L9P	H3	SD-A6
LCD-CS1 P3	1 IU_LTN	IO_L9N	H2	SD-A8
LCD-CS2 P4	1 IU L22P	IO_L10P	H1	SD-A7
LUD-USZ F	IO_L22N *	IO_L10N	Li	SD-DQ1
		IO_L15P	L2	SD-DQI SD-DQQ
		IO_L15N	L3	SD-DQ0 SD-DQ2
		I0_L16P	L3 L4	SD-DQ2 SD-DQ3
		IO_L16N	L6	SD-LDQS
		I0_L17P	L5	UCC1U25
		IO_L17N/VREF	M4	SD-DQ5
		I0_L18P	M3	SD-DQ5 SD-DQ4
		IO_L18N	M5	SD-D04 SD-D06
SD-CK P JS		IO_L19P	M6	SD-DQ6 SD-DQ7
SD-CK_P JS SD-CK N J4	1 IO_LIIP/LHCLNU	IO_L19N	N 1	
SD-UDM J	1 IU_LIIN/LHCLKI	IO_L20P	N5	<u>SD-</u> A9
	1 IU_LIZP/LHULKZ	IO_L20N	P2	_SD-A11
		I0_L21P	P2 P1	_SD-A12
	1 10_L13P/LHCLK4/1RD12	IO_L21N	R3	_ <u>SD-</u> A3
		I0_L23P	R2	_SD-A1
		IO_L23N	T2	SD-A2
SD-BAO K	IO_L14N/LHCLK7	I0_L24P	T1	<u>SD-</u> A10/AP
		IO_L24N	 	_SD-A0
		IC10B3	_	
		1CI0B3		

AD - A/D Converter (11)
AMP - Gain Amplifier (11)
DAC - D/A converter (11)
E- Ethernet (4)
FX2 - Hirose FX2 Connector (1)
ROM - M25P16 (6)
SD- SD RAM (12)
SF - StrataFlash (12)
ST - Soft Touch Connector (1)
U - USB (3)
XC - XC9572 (10)

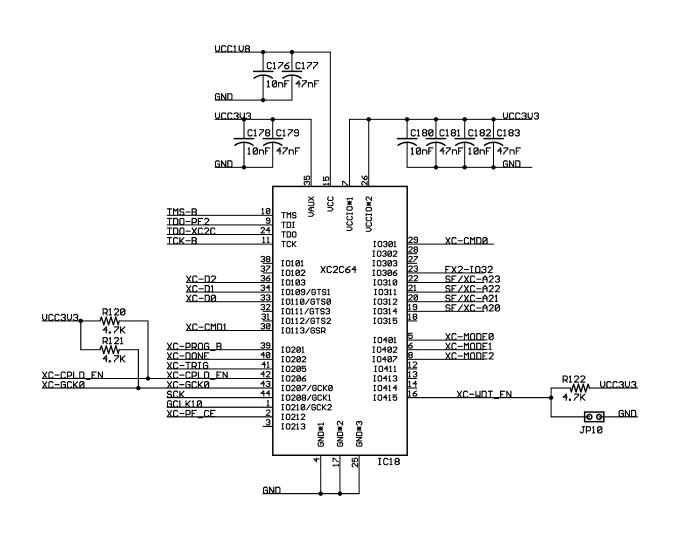
USD_SF-A17
USD_SF-A17
USD_SF-A17
USD_SF-A18
USD_SF-A18
USD_SF-A19

* Notes are for pins that very between 500/1200/1600 dies

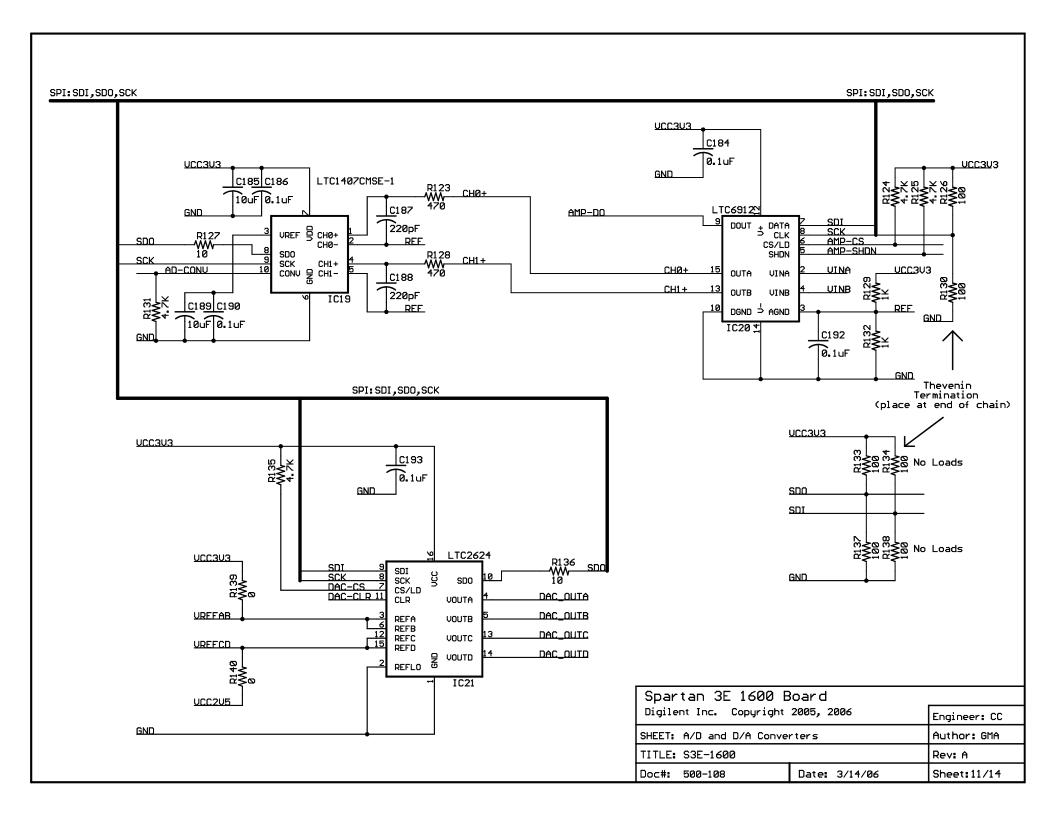
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SHEET: XC3SE Banks 2 and 3		Author: GMA	
TITLE: \$3E-1600		Rev: A	
Doc#: 500-108	Date: 3/14/06	Sheet: 8/14	

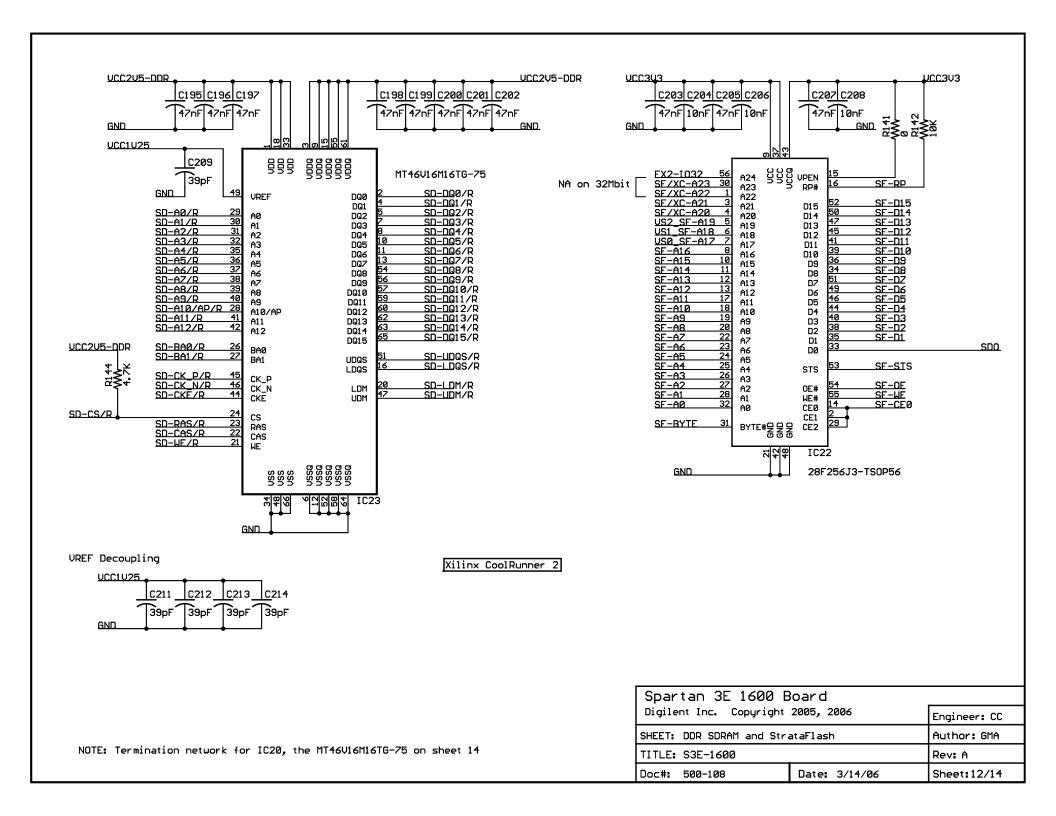


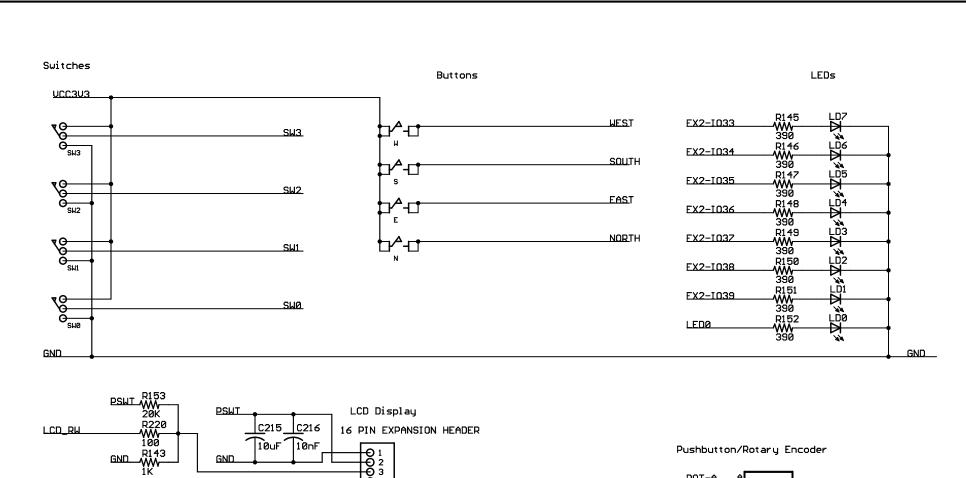
Spartan 3E 1600 Board		
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SHEET: XC3SE Power Decou	Author: GMA	
TITLE: S3E-1600	Rev: A	
Doc#: 500-108	Date: 3/14/06	Sheet: 9/14



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SHEET: XC2C64 CPLD	Author: GMA		
TITLE: S3E-1600	Rev: A		
Doc#: 500-108	Date: 3/14/06	Sheet:10/14	





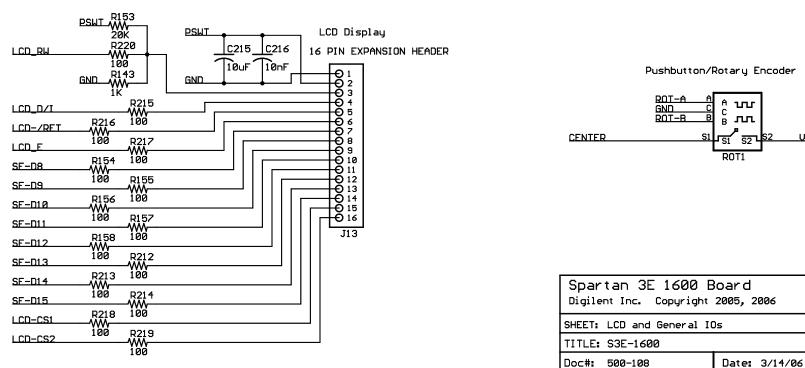


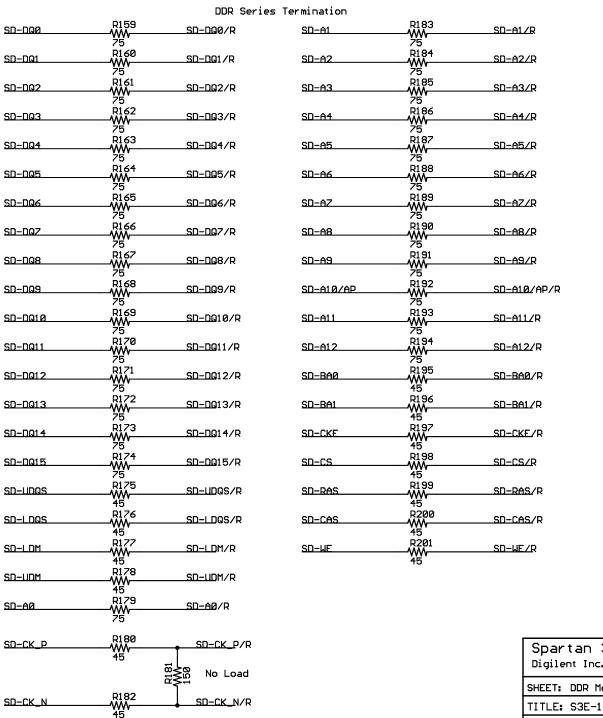
Engineer: CC

Author: GMA

Sheet: 13/14

Rev: A





FX2 Differential Termination Not Loaded				
EX2-I017	R202 - W	FX2-I018		
FX2-I019	100 R203 - WW 100	FX2-I020		
FX2-I021	R204 	FX2-I022		
FX2-I023	100 R205 - /W/	FX2-I024		
FX2-I025	100 R206 - WW	FX2-I026		
FX2-I027	100 R207 -W	FX2-I028		
FX2-I035	100 R208 - WW	FX2-I036		
FX2-I037	1000 R2009 - VW	FX2-I038		
FX2-CLKIN	100 R210 - WW	FX2-CLKOUT		
	100			

Spartan 3E 1600 Board			
Digilent Inc. Copyright 2005, 2006			Engineer: CC
SHEET: DDR Memory Signals			Author: GMA
TITLE: \$3E-1600		Rev: A	
Doc#: 50	0-108	Date: 3/14/06	Sheet:14/14