LSI Circuit Design

Behavior of MOS transistors Fundamentals to LSI circuit design
Low power circuit technologies

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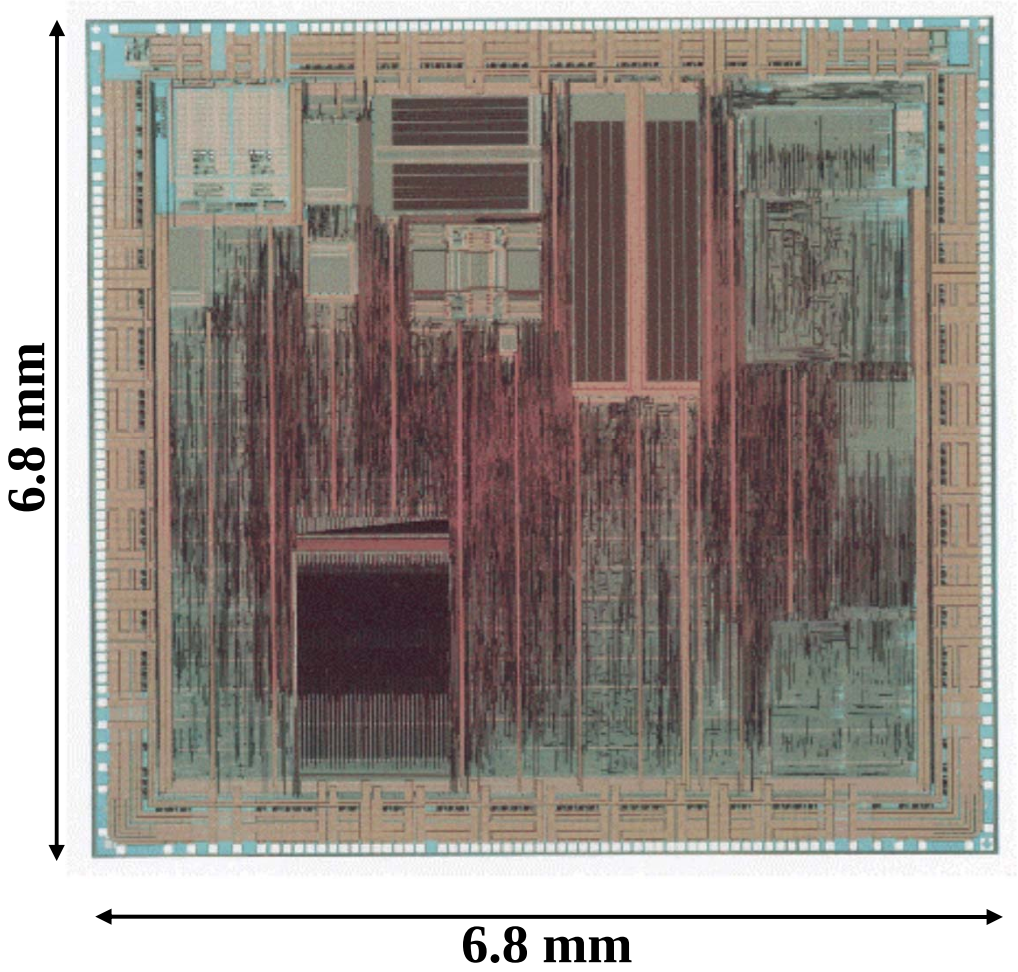
Chip Micrograph of SH4 Microprocessor



Technology	0.2µm
Tr. Count	3.3 M
Threshold Voltage	0.5V
Frequency	133-200 MHz
Power Supply	1.5-1.8V, 3.3V
Active Power	780 mW
Standby Current	100 µA

Designed in 1997
First SoC in Hitachi

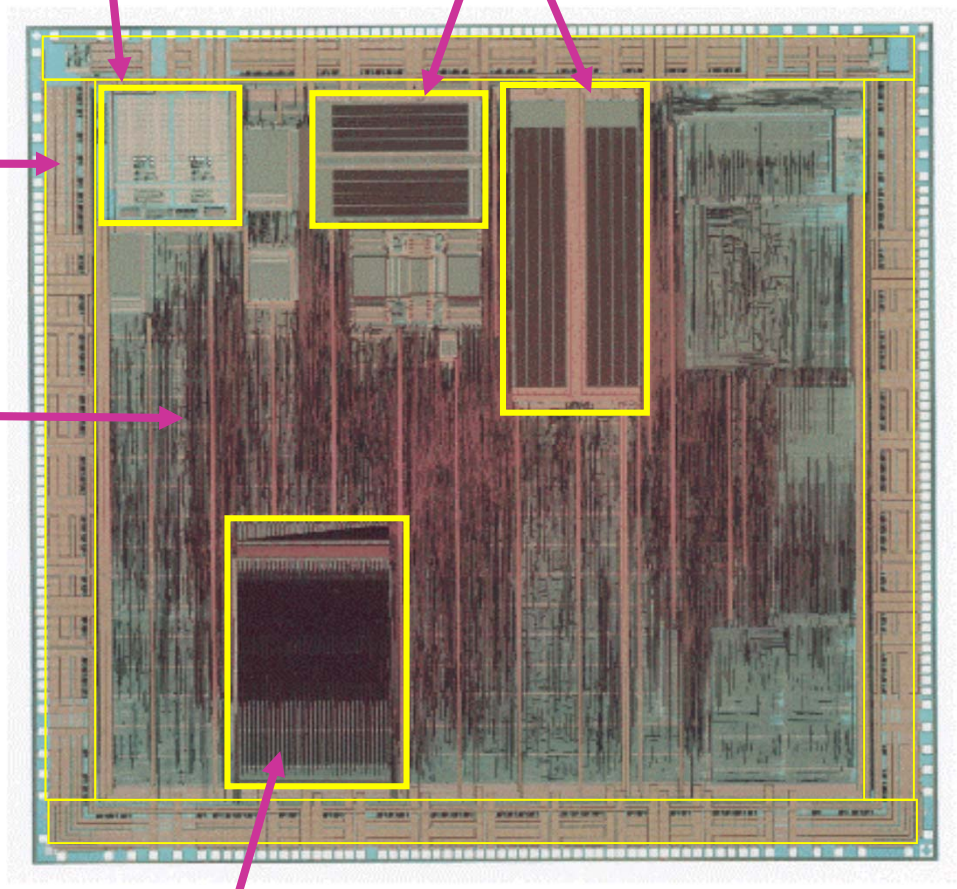
Location of Circuit Blocks in SH4

Cache Memories are kind of RAM that temporarily store instruction and data

PLL that generates clock signals

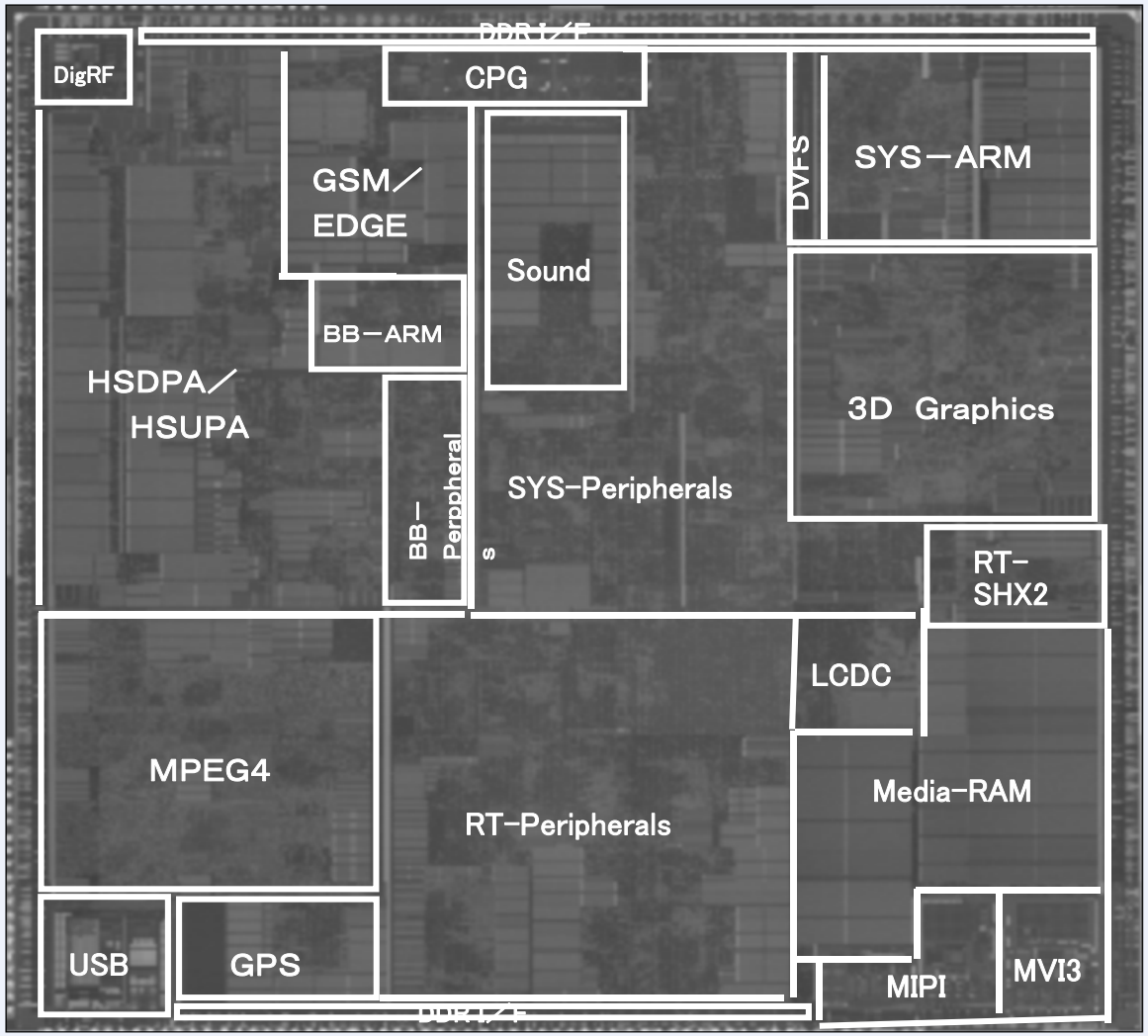
IO Circuits
that receive or send data

Logic Circuits



Data Path that executes calculation

Chip Micrograph of Mobile G4



Technology 45 nm

Contents 45 M Gate
48.3M bit RAM
6.3Mbit ROM

Tr. Count 600M

CPU
- ARM A8 600 MHz
- SHX2 400 MHz

Power Supply:
- Power domain 25
- Core 1.15V – 1.0V (DVFS)

IO LPDDR2
USB2.0

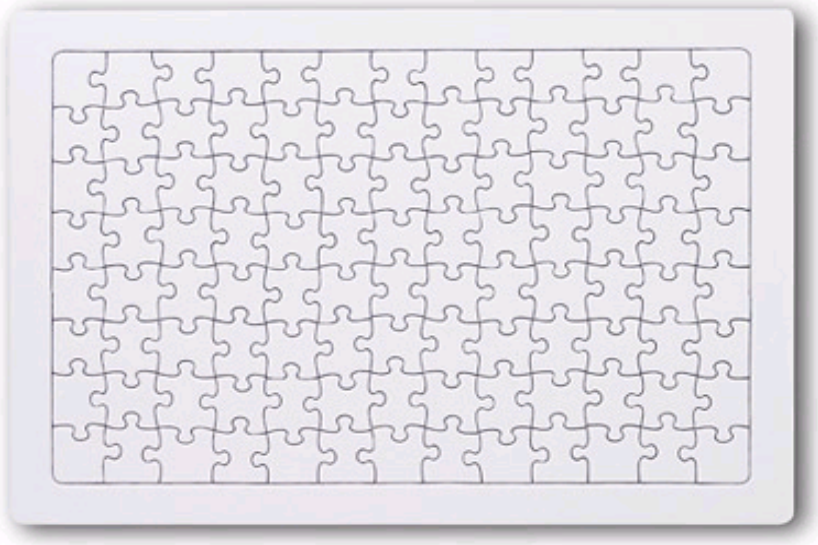
(DVFS: *Dynamic voltage-frequency scaling*)

Designed by Renesas in 2009

SoC Design and Jigsaw Puzzle

- **Jigsaw puzzle: assemble whole picture from many of interlocking pieces**

- **SoC design: assemble whole chip from components in circuits libraries, place and route them, so that they function harmoniously**



1. **Logic Cell library**
2. **Memory library**
3. **Analog Circuit library**

Circuit libraries on SoC

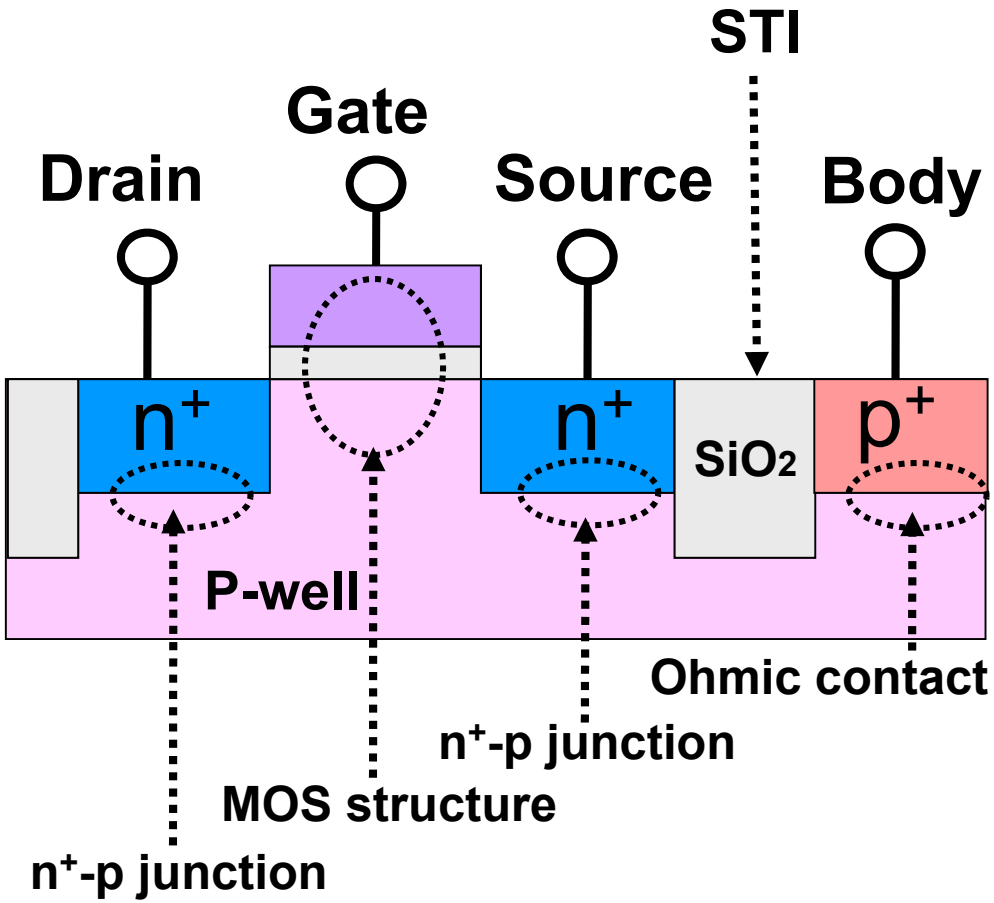
1. Logic cell library
   - Primitive cells (Inverter, Buffer, NAND, NOR, FF, etc.)
   - Data Path (Execution unit, selector, multiple-bit width)
   - Clock Buffer
   - Power Control Circuits (Power Switch, Substrate Bias Controller)
2. Memory library
   - Register File
   - RAM (Random Access Memory)
   - ROM (Read Only Memory)
3. Analog Circuit library
   - IO (Input and Output Buffer, Level Shifter)
   - PLL (Phased Locked Loop)
   - ADC (Analog to Digital Converter)
   - RF (Radio Frequency Circuit)
   - PA (Power Amplifier)

Note: Circuit blocks which indicated the red letters are implemented in SH4

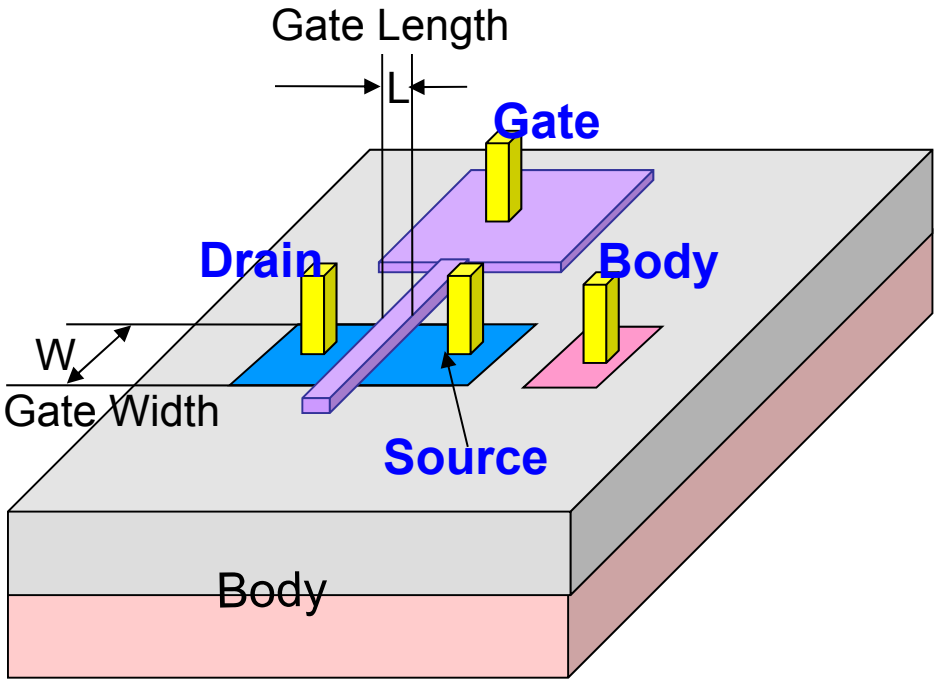
Contents

NMOS FET Structure

<Cross Section view>

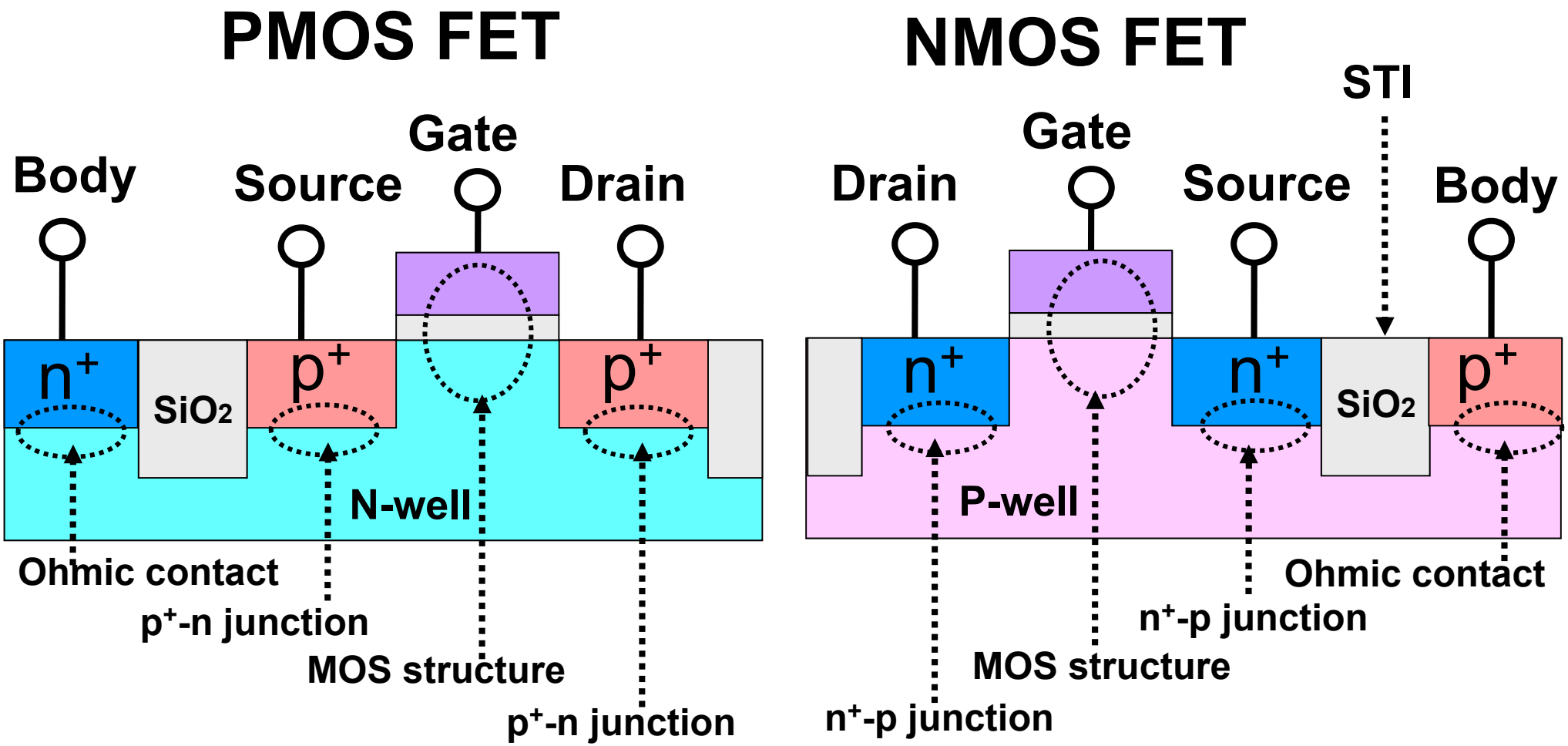


<Bird eyes view>



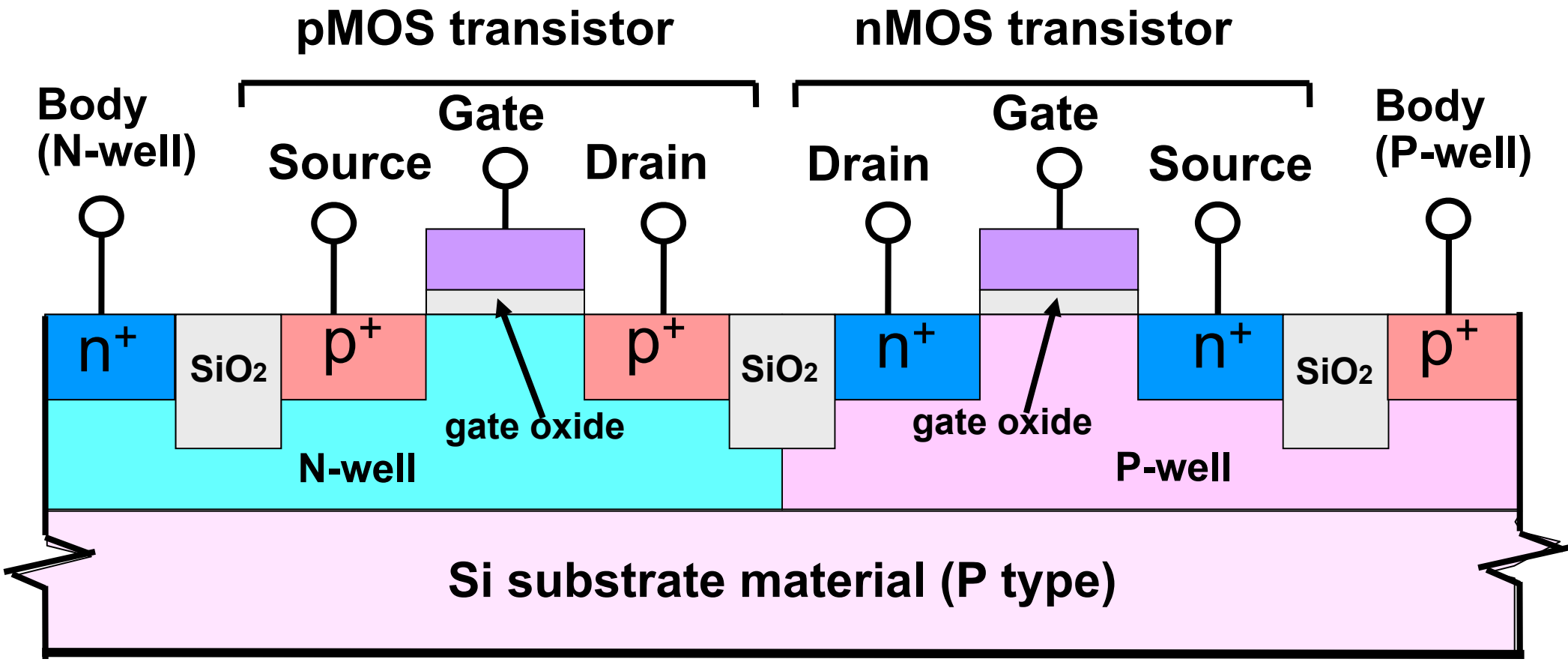
MOS: Metal-Oxide Semiconductor
STI: Shallow Trench Isolation

NMOS and PMOS FET Cross Section

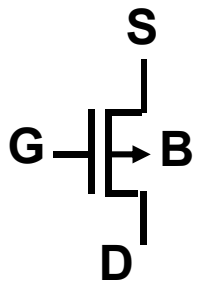
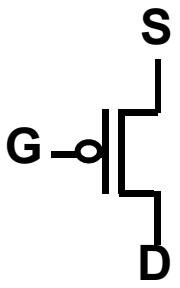
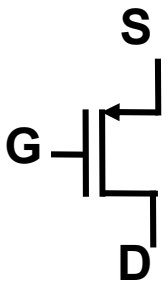
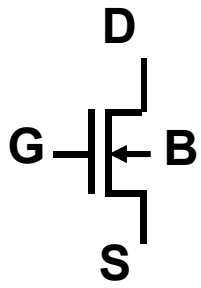
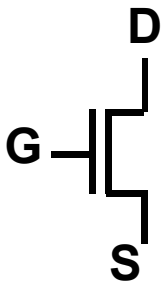
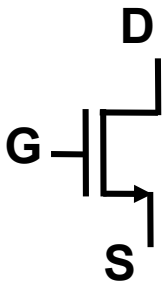


MOS : Metal-Oxide Semiconductor
STI : Shallow Trench Isolation

Structure of CMOS

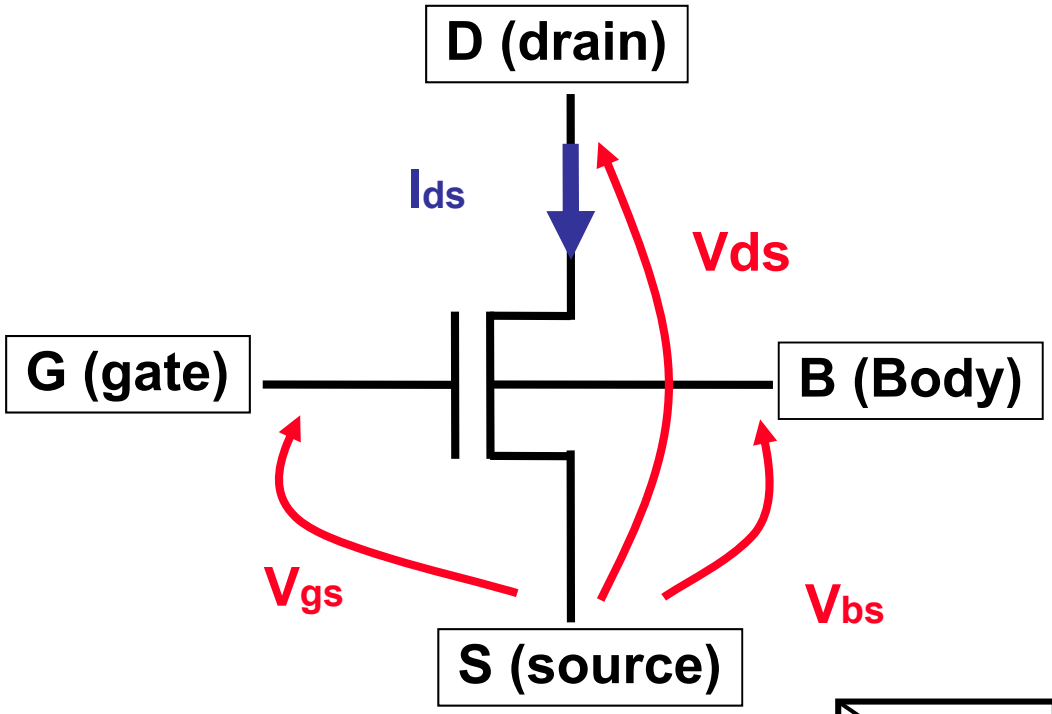


Notations and Operations of MOS Transistors

	Notations			Operations
pMOS transistor				When negative gate voltage (Vgs) is applied, Holes are injected from Source and reach to Drain.
nMOS transistor				When positive gate voltage (Vgs) is applied, Electrons are injected from Source and reach to Drain.

All three notations are commonly used.

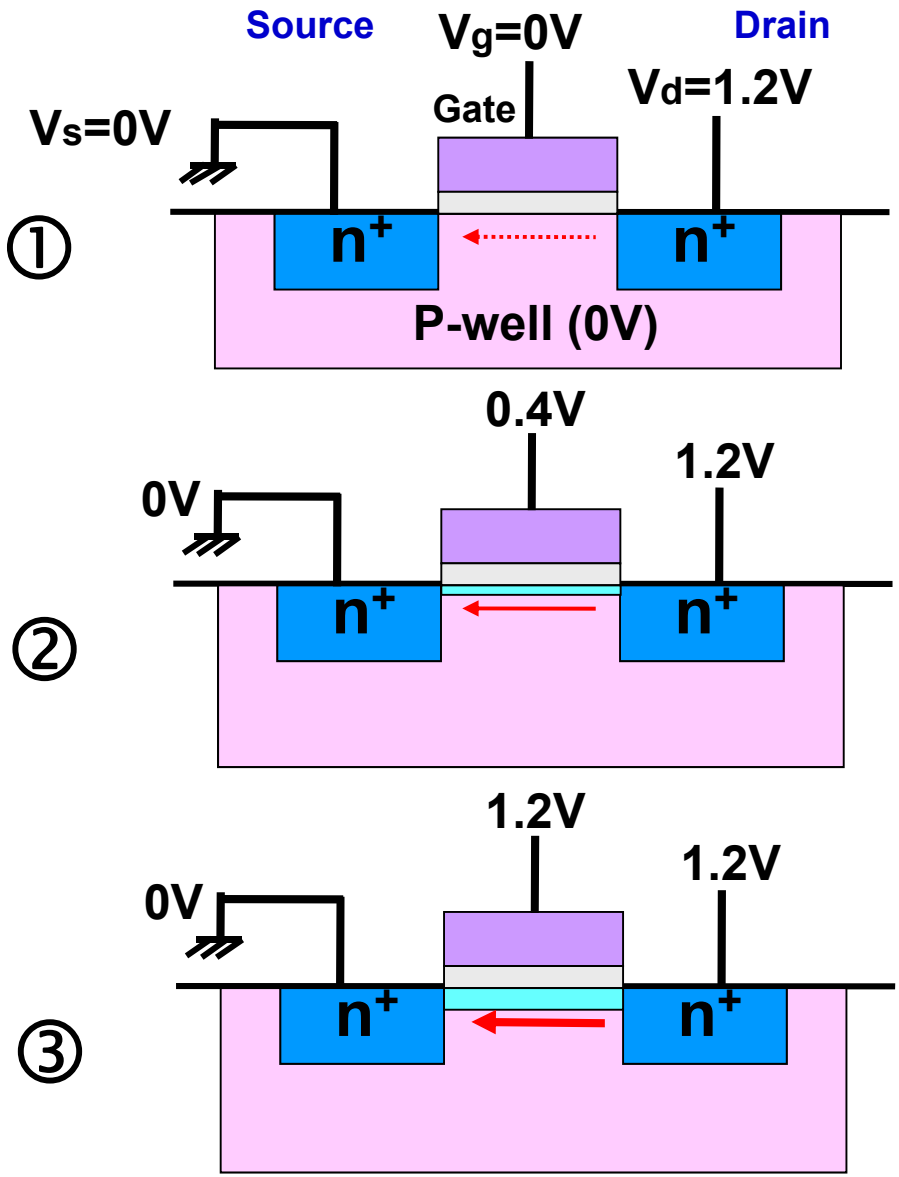
Naming Convention of MOS Transistor



Sometimes “s” is eliminated, such as V_g, V_d, I_d, and V_b.

	Polarity			
	V_{gs}	V_{ds}	I_{ds}	V_{bs}
nMOS	+	+	+	-
pMOS	-	-	-	+

Operations of NMOS Transistor



<Characteristics of drain current >

Only leakage current flows

Electrons are generated in the channel and current starts flowing

Number of electrons in the channel increases and current increases

Operations of NMOS Transistor

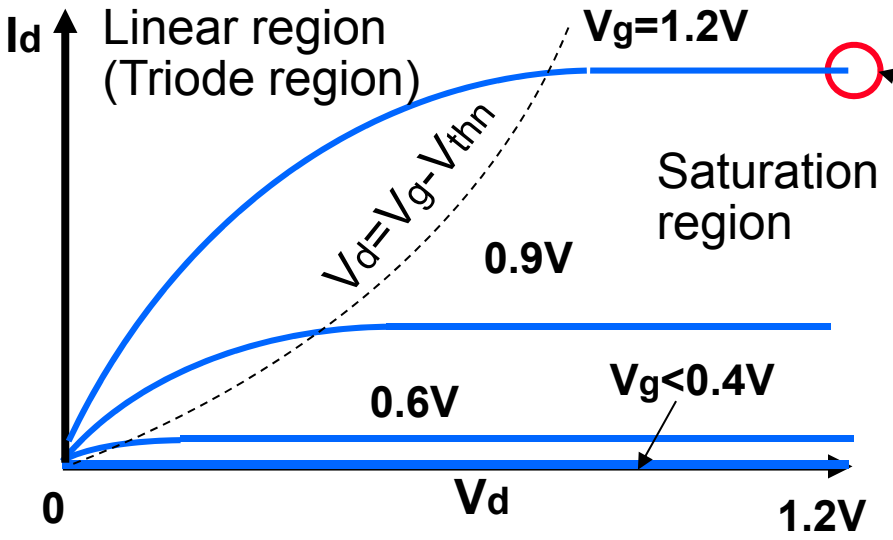
<Fundamental Formula of drain current>

$$I_d = \begin{cases} \beta_n \{V_d(V_g - V_{thn}) - V_d^2/2\} & (\text{Linear region } 0 \leqq V_d \leqq V_g - V_{thn}) \\ \beta_n/2\,(V_g - V_{thn})^2 & (\text{Saturation region } V_d > V_g - V_{thn}) \end{cases}$$

$\beta_n = \mu C_{ox} W/L$

μ: Electron Mobility
C_{ox}: Gate capacitance per unit area
W: Gate width
L: Gate length
V_{thn} : Threshold voltage of NMOS
(gate voltage required to switch ON transistor)

<Characteristics of drain current >



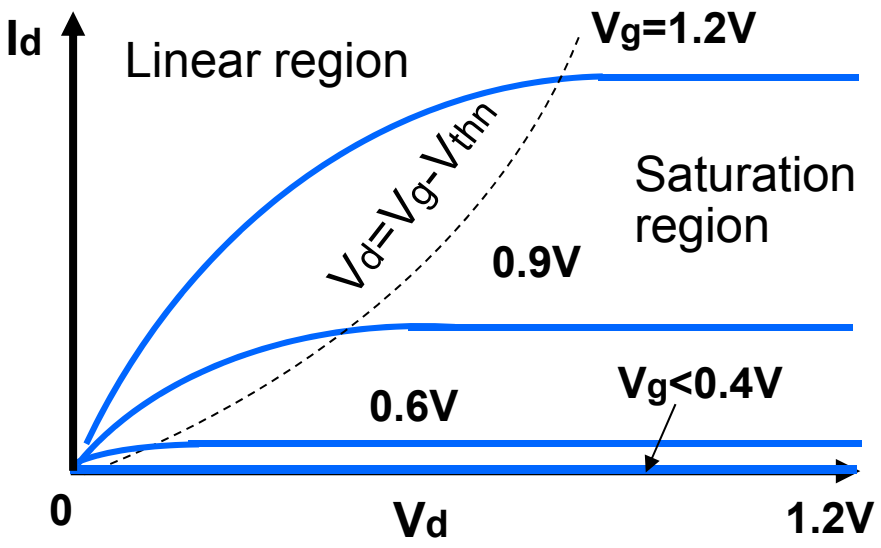
Drain current at *Vg=Vd=Vdd* is called as Saturation Conditions:

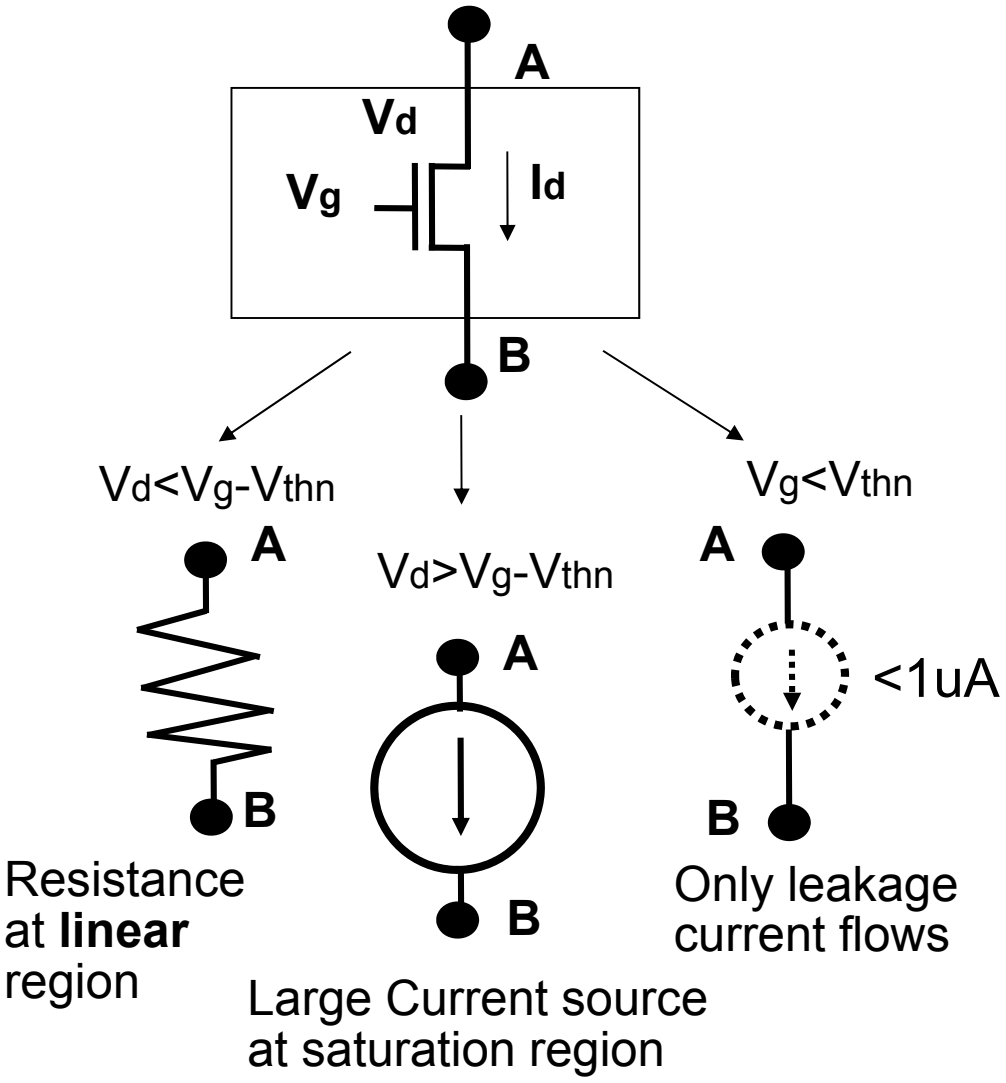
$V_{gs} - V_{th} > 0$

$V_{ds} > V_{gs} - V_{th}$

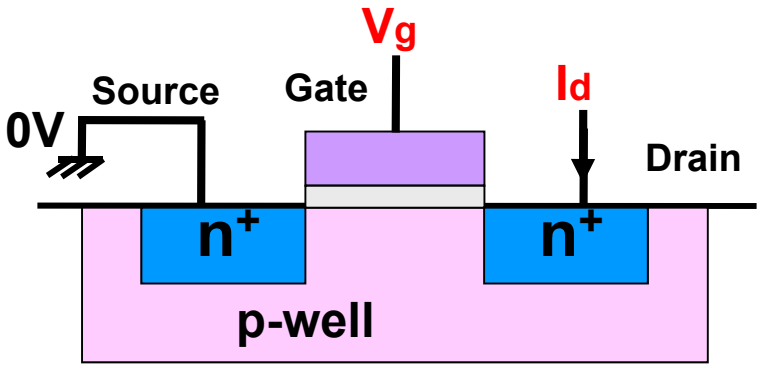
Transistor acts as a two-terminal element depending on gate voltage

<Characteristics of drain current >

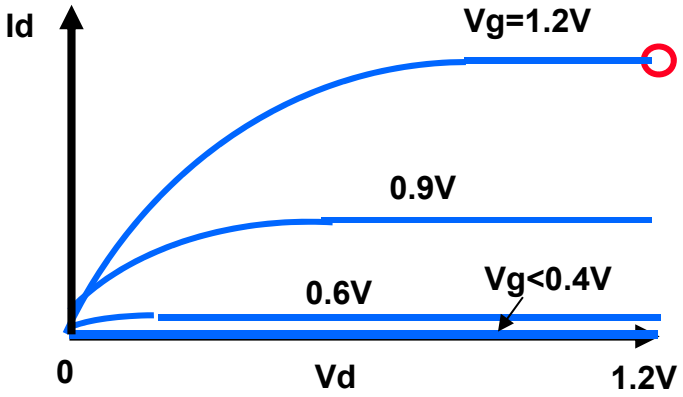


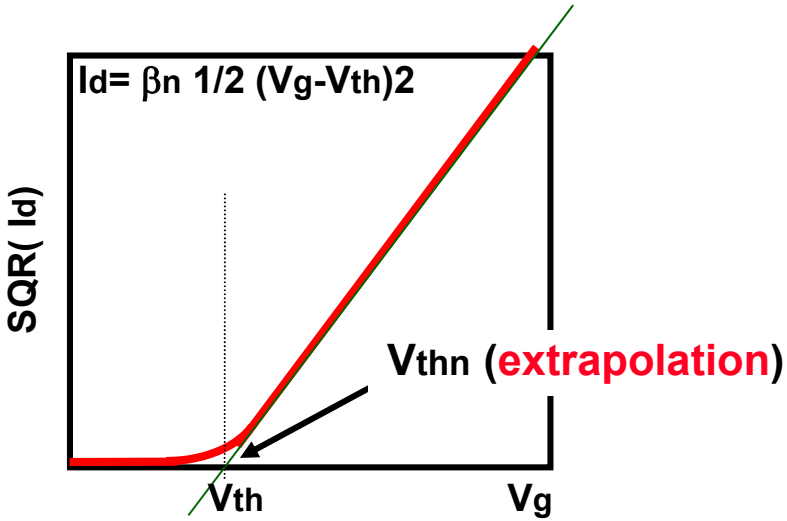


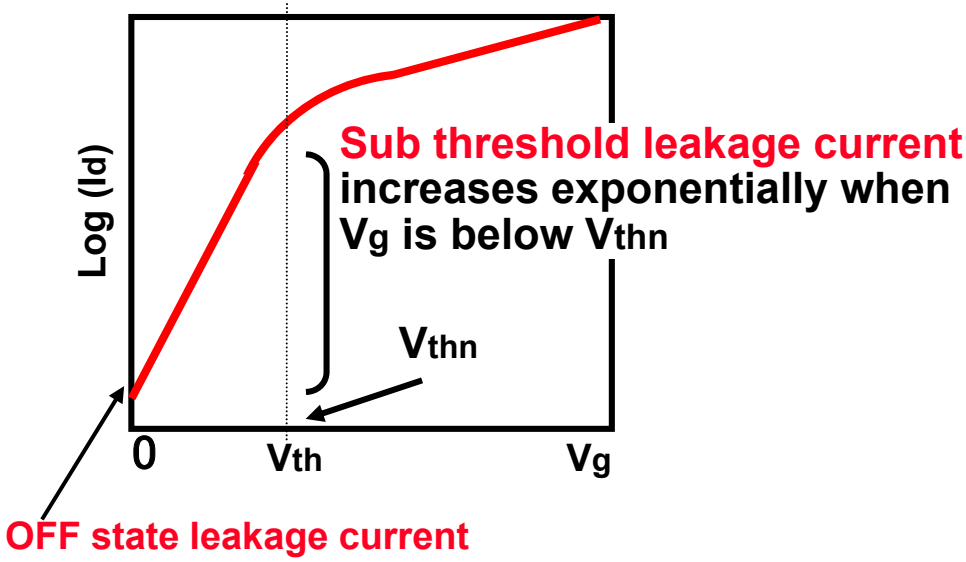
Threshold Voltage of NMOS (Vthn)



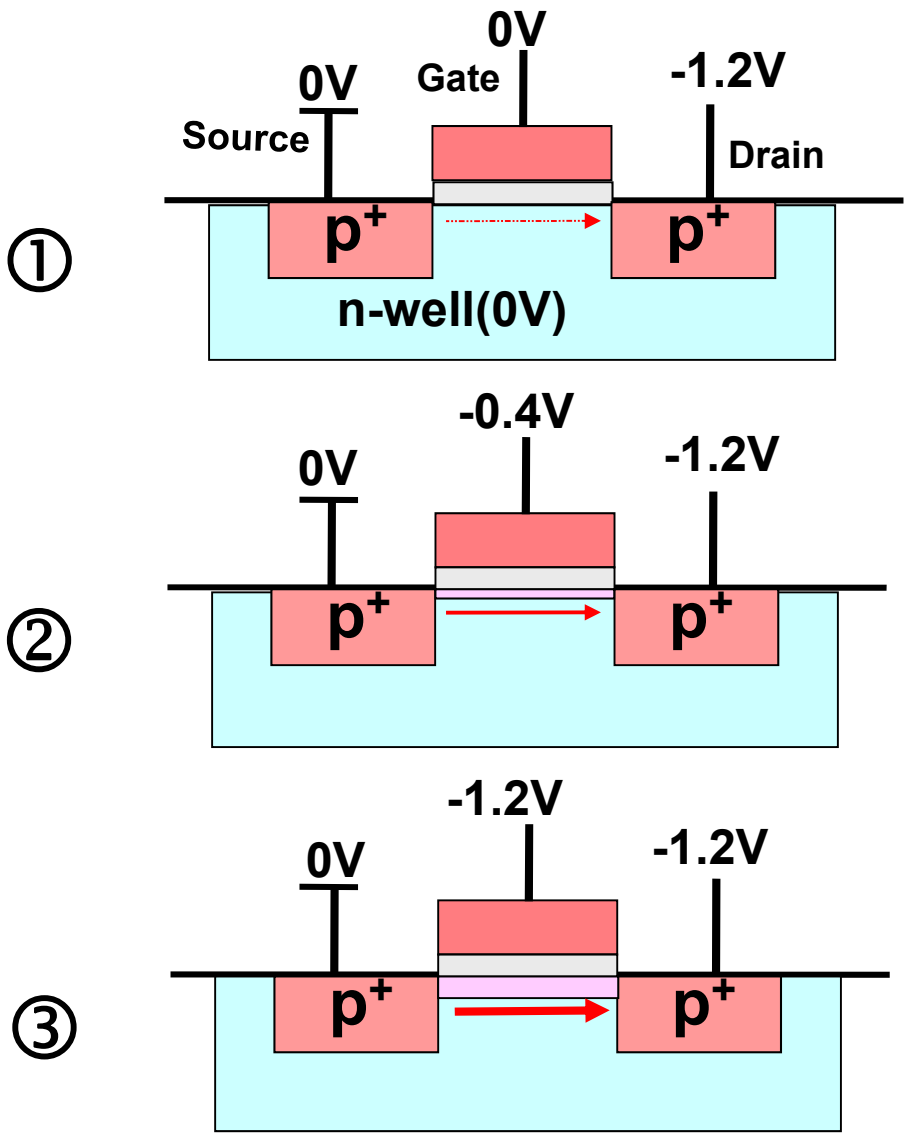
<Characteristics of drain current>



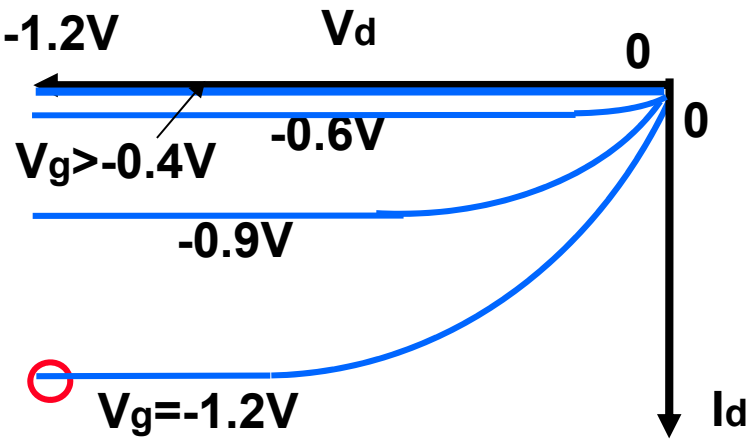




Operations of PMOS Transistor



<Characteristics of drain current >



① Only leakage flows

② When holes are generated in the channel and current starts flowing

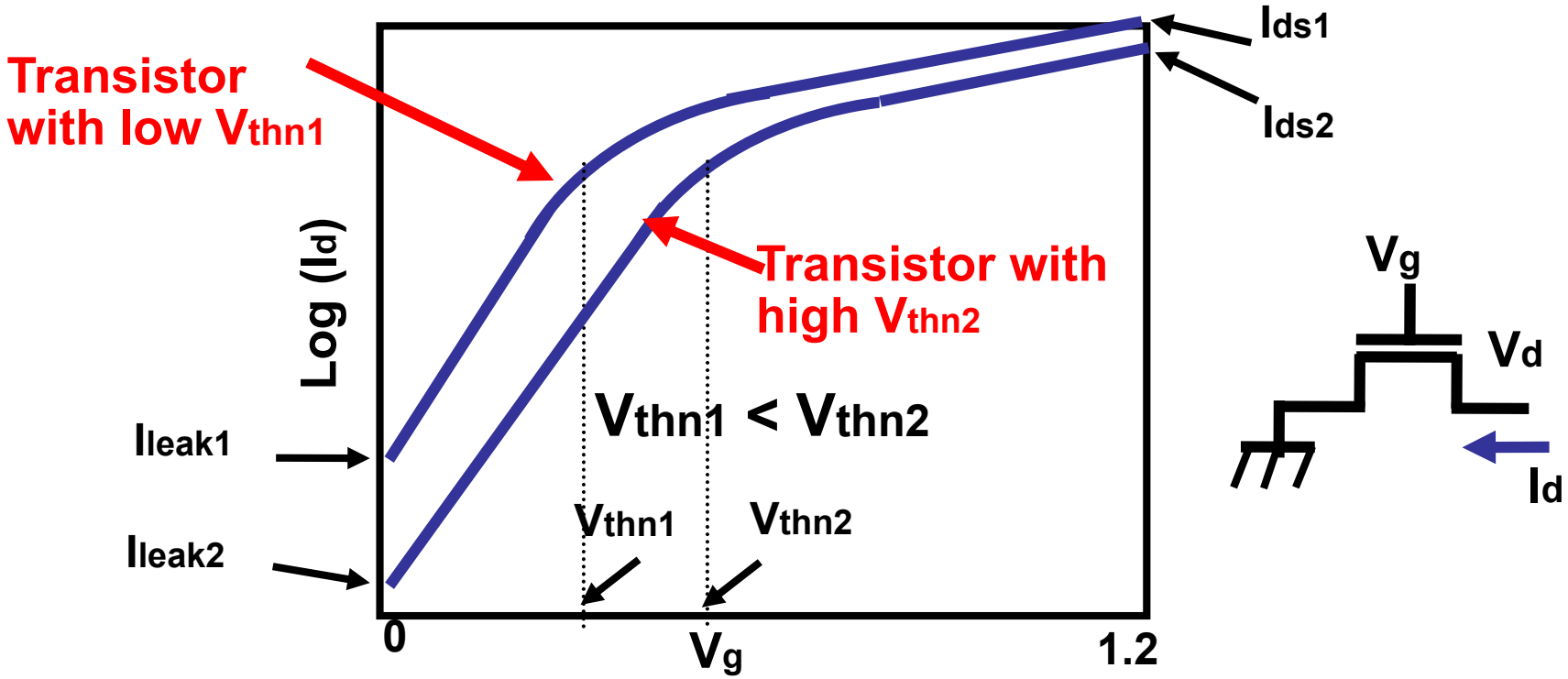
③ Number of holes increases and current increases

Question 1

Current flows from drain to source for NMOS, while it flows from source to drain for PMOS.

Why are the directions of currents different between NMOS and PMOS?

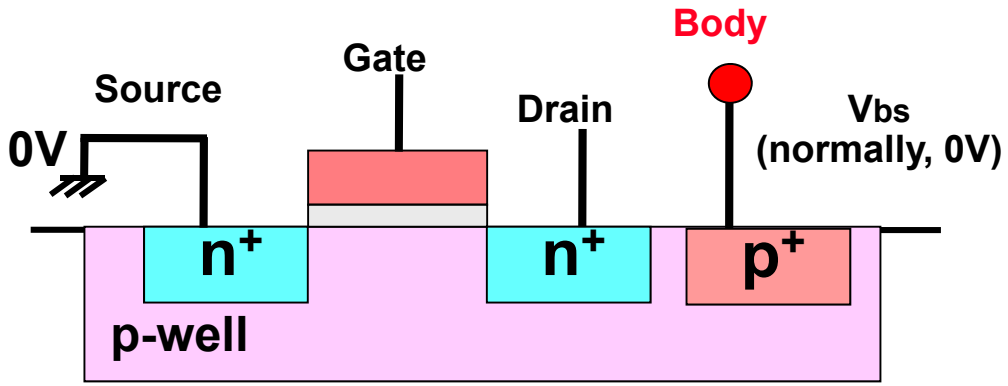
Threshold Voltage affects Id and Leakage



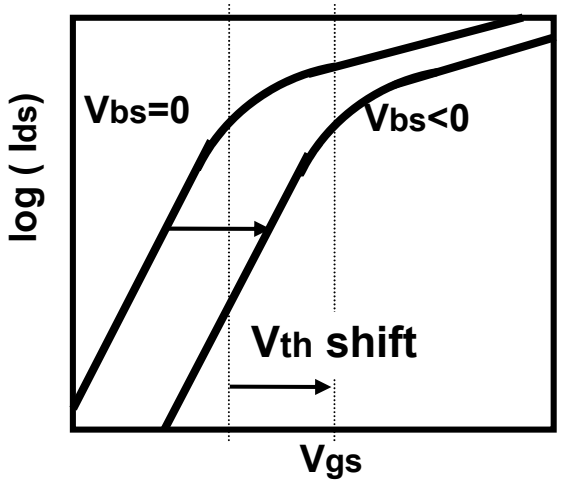
- Vth can be tuned during fabrication by ion implantation.
- Transistor with lower V_{th} can flow large drain current at V_g=1.2V, but has large leakage at V_g=0V ($I_{leak1} > I_{leak2}$)

Substrate (Body) Node Potential

○ Electrical potential of body (formed by WELL structure) as 4th electrode also affects transistor characteristics.



<nMOS transistor>



< threshold voltage dependency on body voltage >

$$V_{thn} = V_{t0} + k^*(\sqrt{-V_{bs}+ 2\phi} - \sqrt{2\phi})$$

V_{t0}, k, ϕ: constants

Body Effect

<nMOS>
- V_{bs} <<0, then V_{thn} increases.
- low speed, low leakage

<pMOS>
- V_{bs} >>0, then $|V_{thp}|$ increases.
- low speed, low leakage

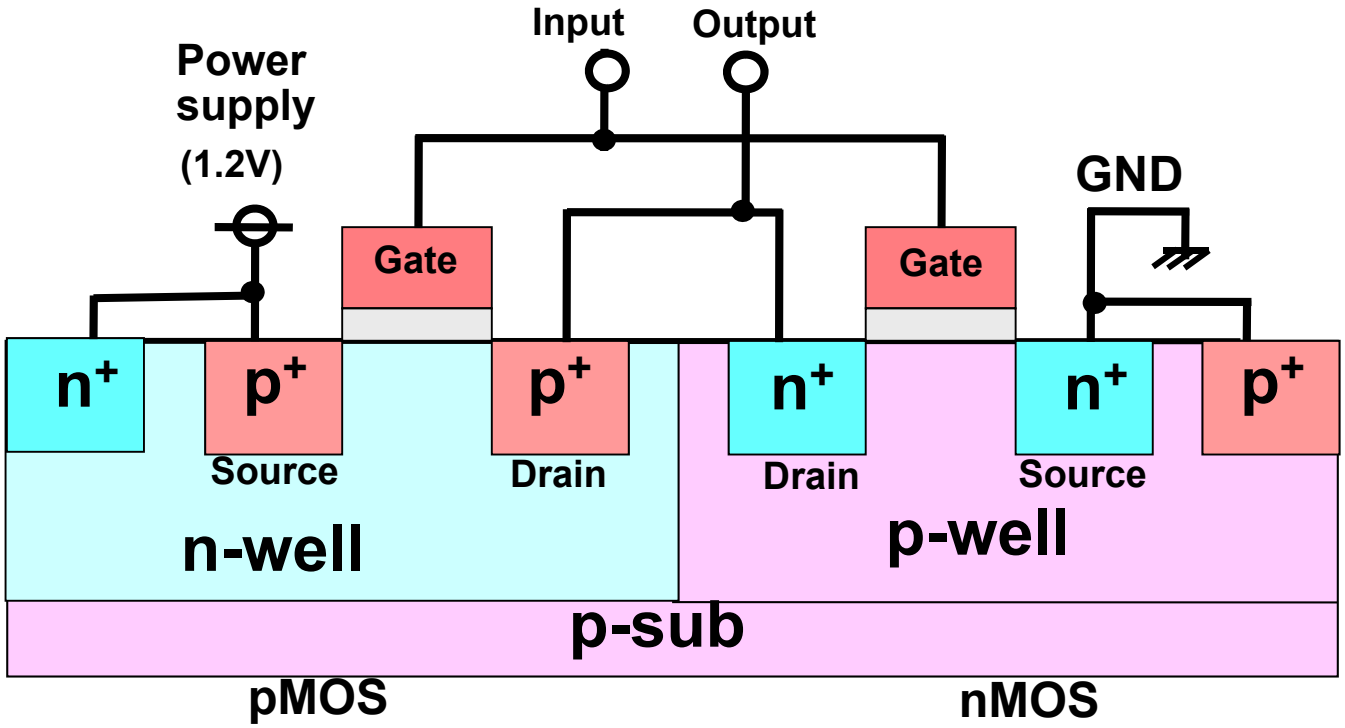
Summary of MOS Transistor

- Characteristics of nMOS and pMOS transistors are symmetrical, and polarity of signals is opposite.
- I_d/V_d curves are divided into linear and saturation regions, where their boundary is $V_d = V_g - V_{th}$.
- I_d/V_g curve is divided into normal and sub threshold regions, where boundary is $V_g = V_{th}$.
- Vth affects I_d and leakage current:
  When V_{th} is low, I_d becomes large but leakage also becomes large.
- Body electrode acts as 4^{th} terminal, and body voltage V_{bs} affects V_{th}.

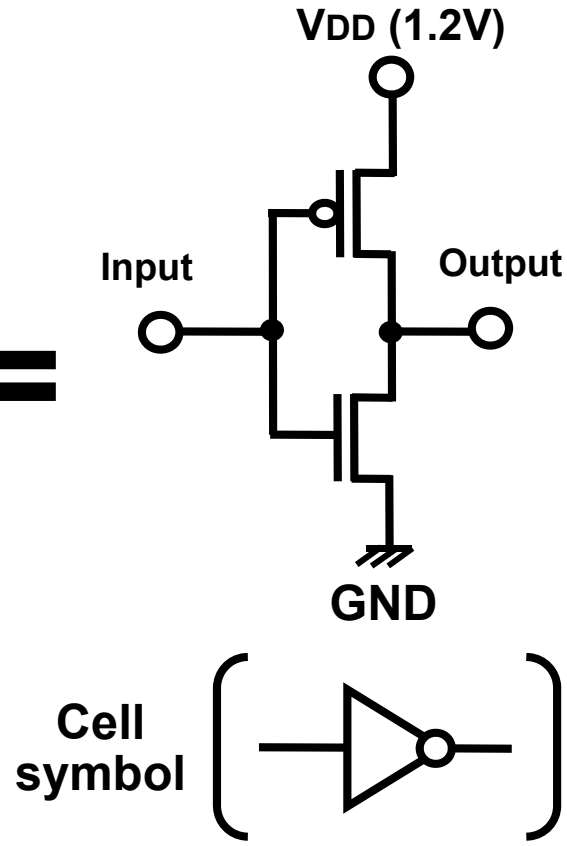
Contents

Inverter

< CMOS inverter Cross Section >



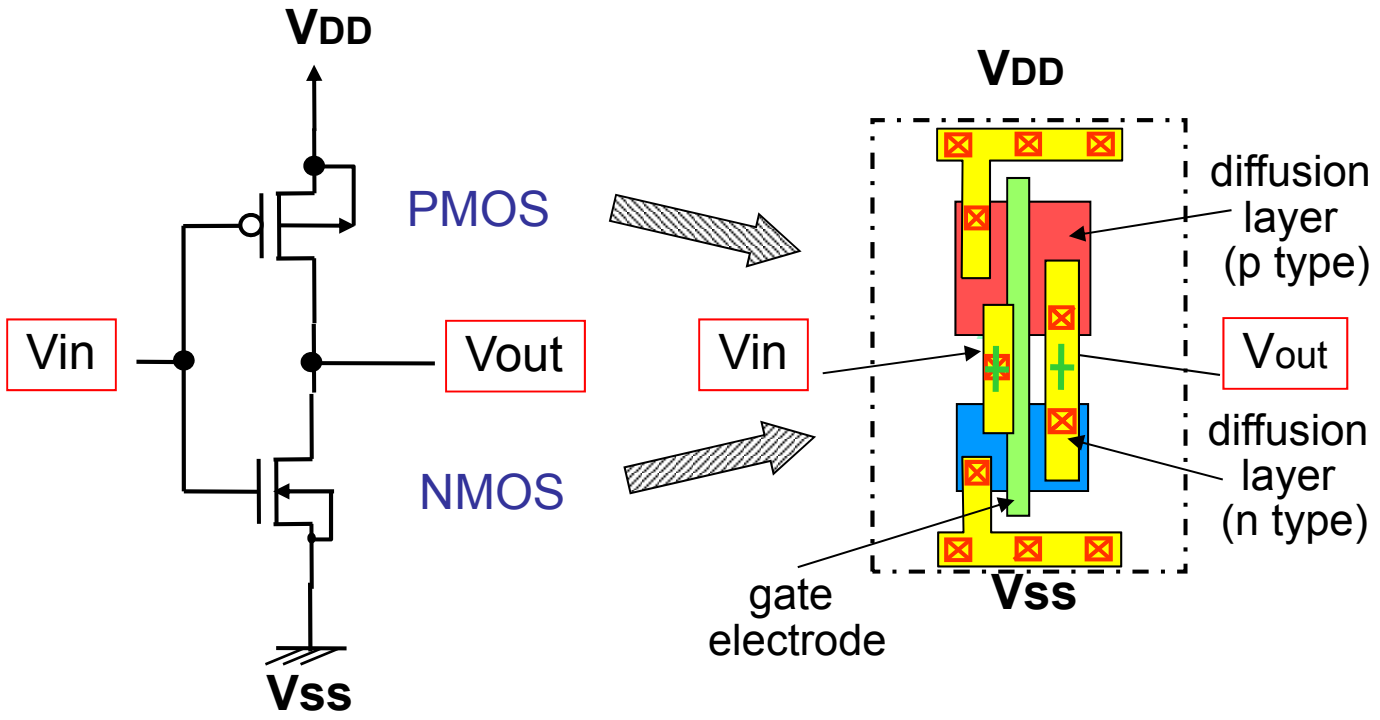
< Circuit Schematic >



The most simple logic circuit with a pair of pMOS and nMOS transistors .

Inverter Design

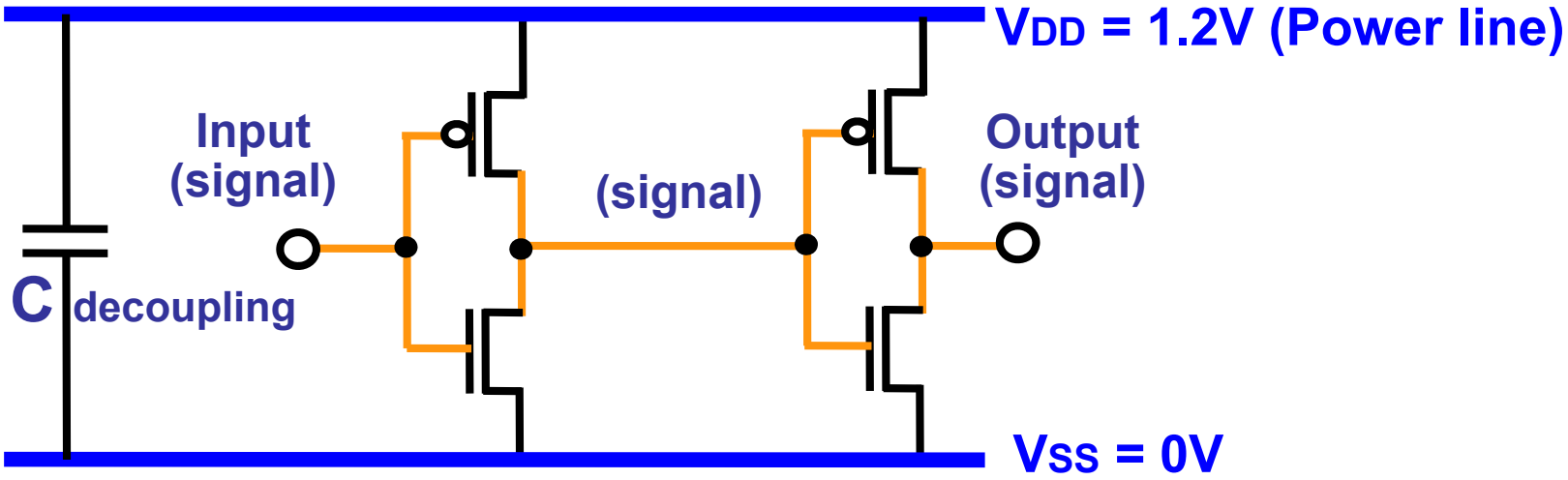
<circuit schematics> <Over View Layout>



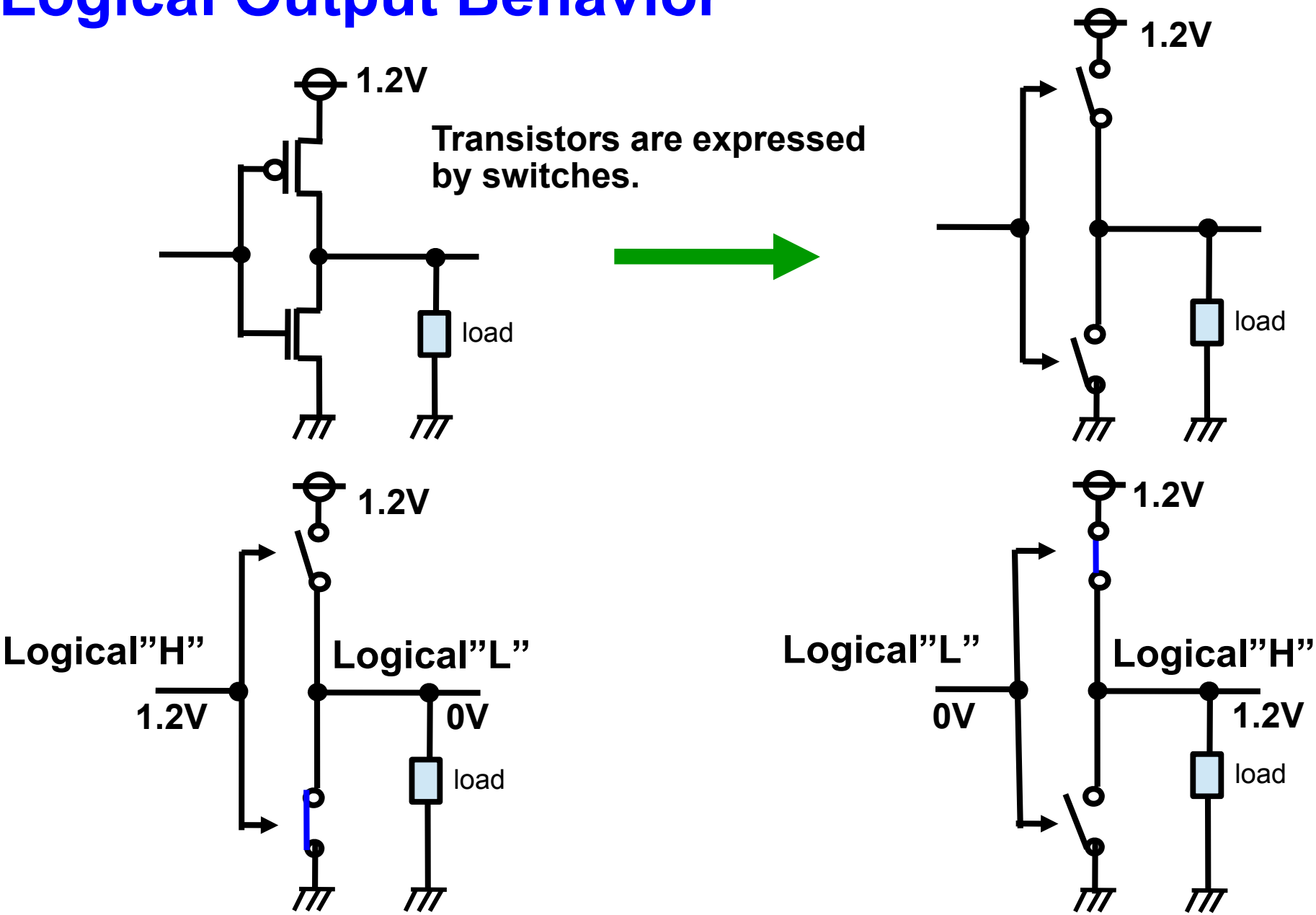
INV Circuit Design: Define W and L of NMOS & PMOS depending on speed and drive-ability!

Wiring

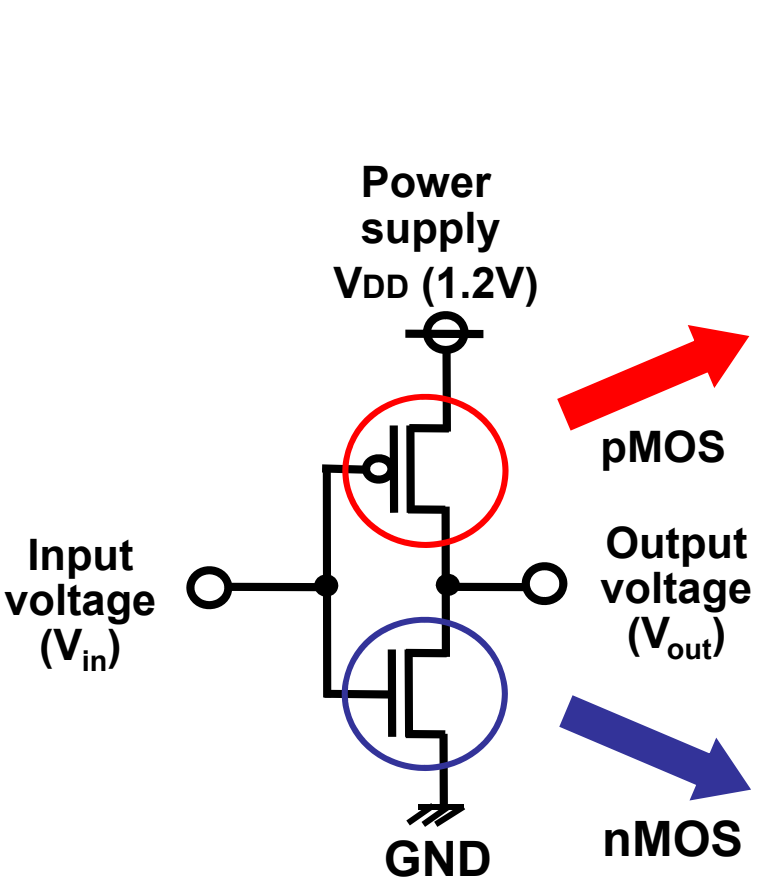
1. Power lines
   - Constant voltage lines
   - Common to many transistors
   - They prefer large capacitance to be stable
     (Decoupling capacitance)
2. Signal lines
   - Wiring which transmits signals
   - They prefer small parasitic capacitance to achieve short delay time

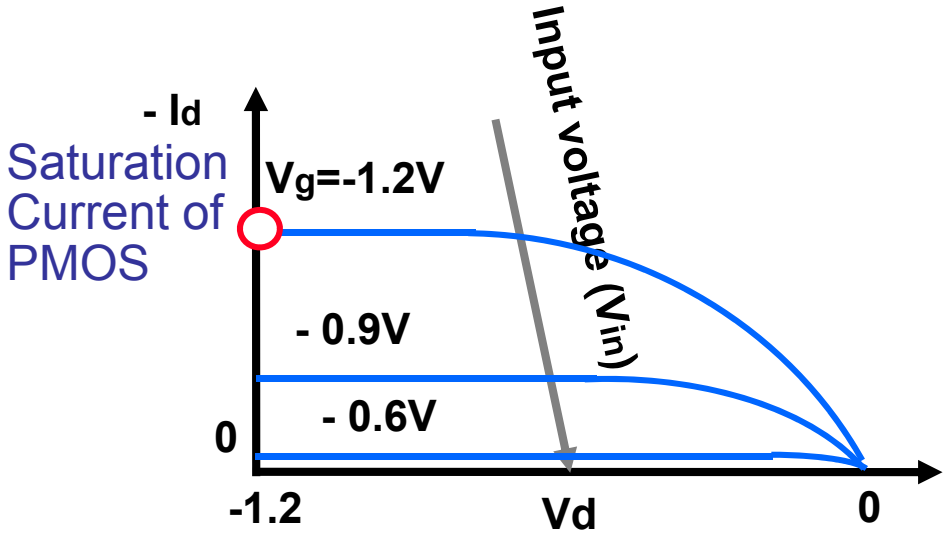


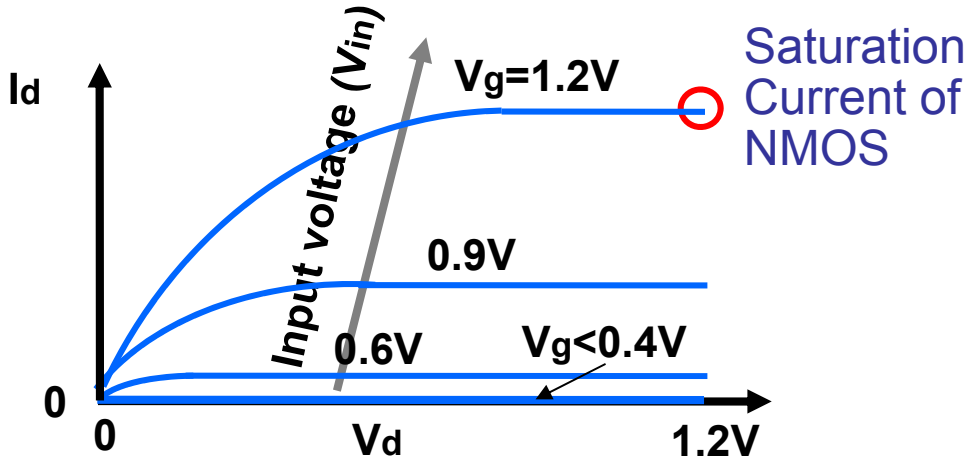
Logical Output Behavior



Drain Current Characteristics



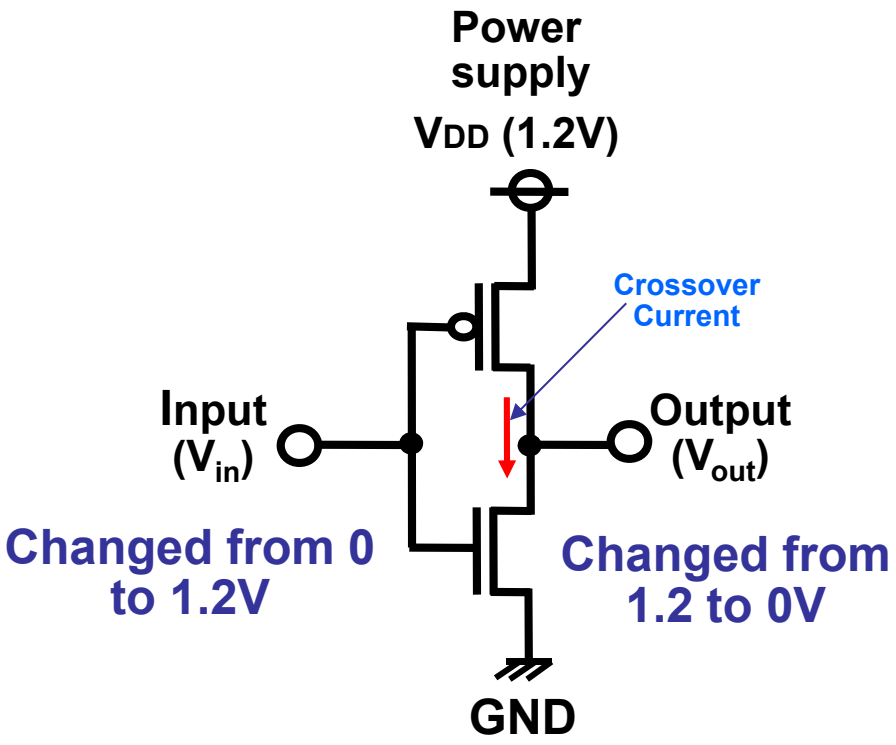


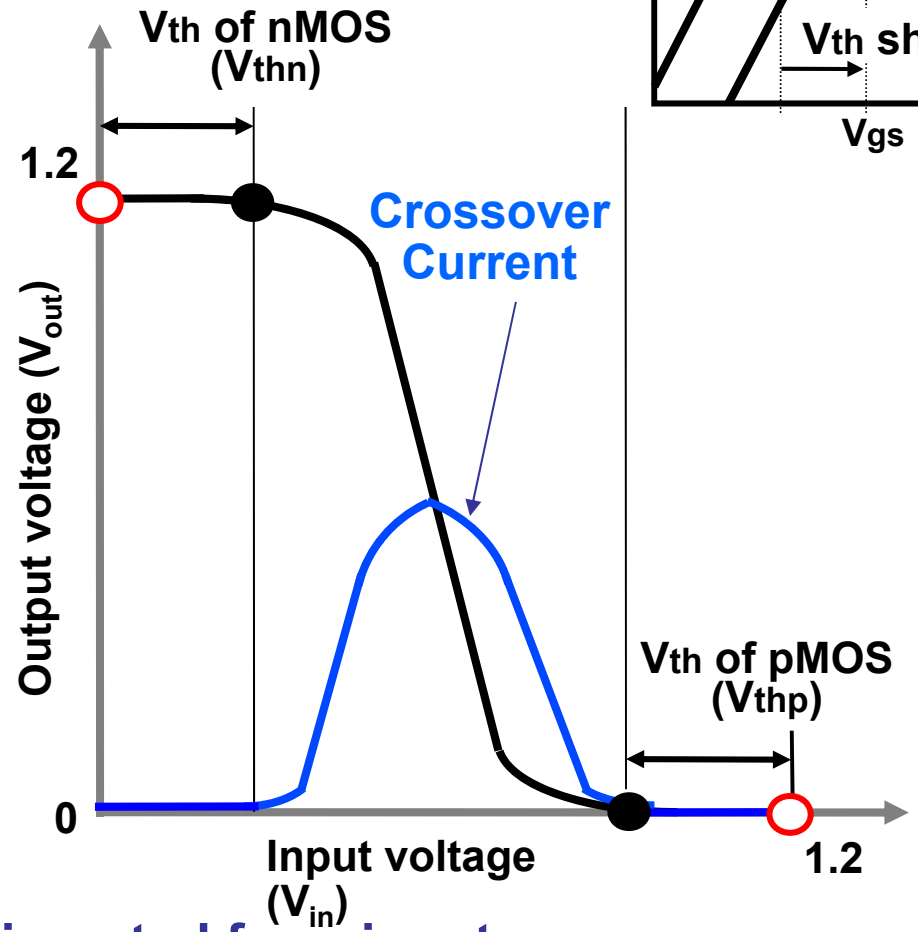


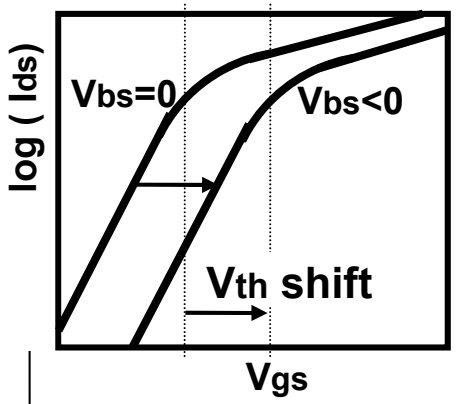
Inverter performance is determined by saturation currents of both transistors.

Output voltage is determined by intersection point of NMOS & PMOS current curves.

Output Characteristics



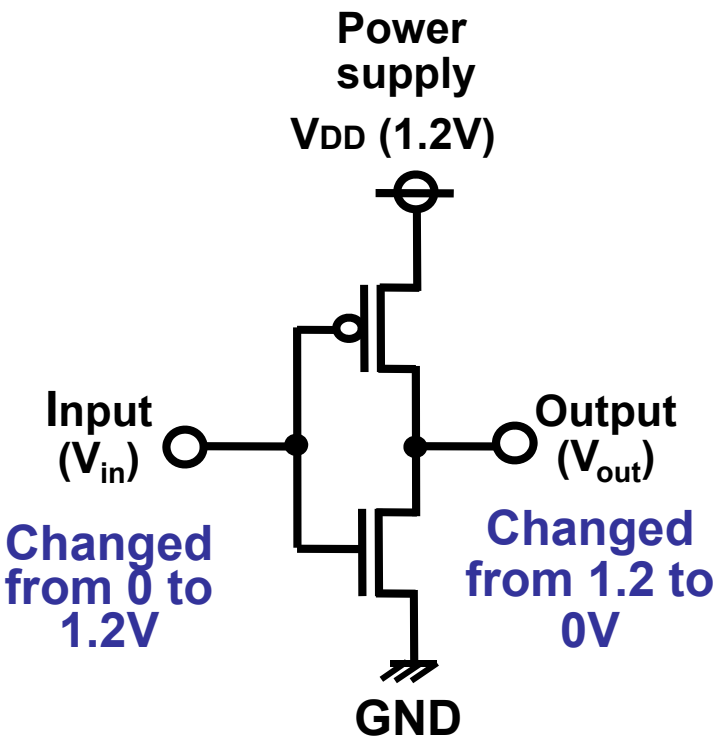


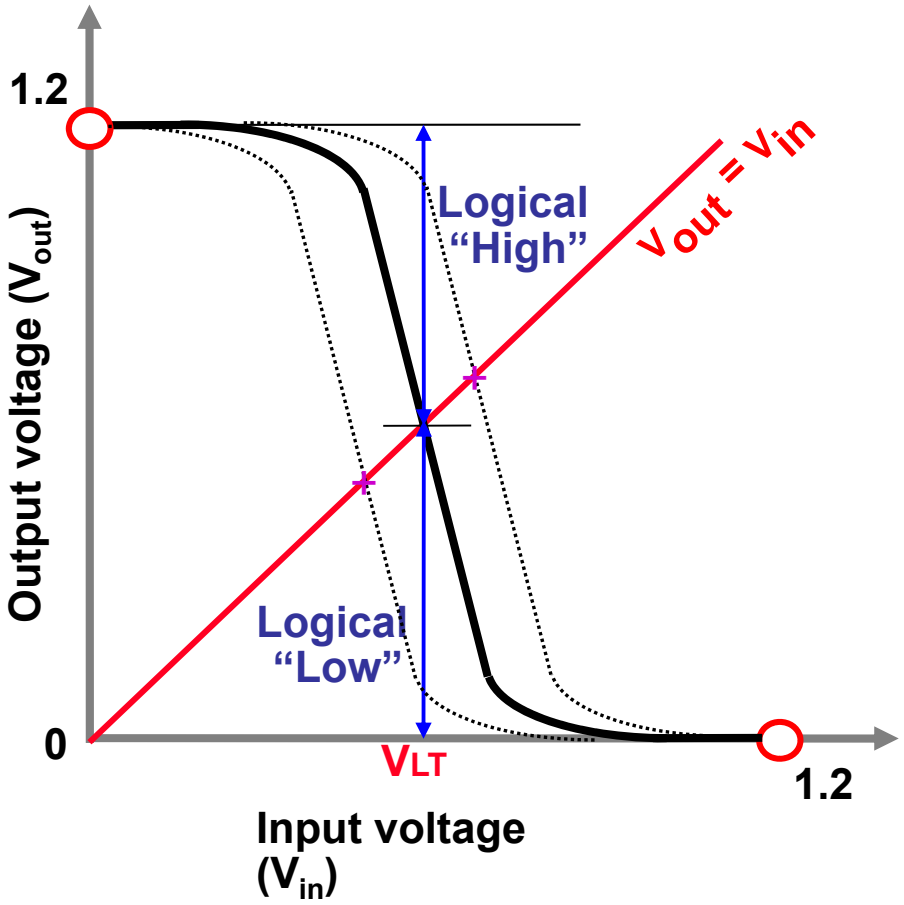


inverter: Signal at output is logically inverted from input

Neither NMOS or PMOS is ON (in steady state), no direct current flows;
No crossover current flows at stable states;

Logical Threshold Voltage





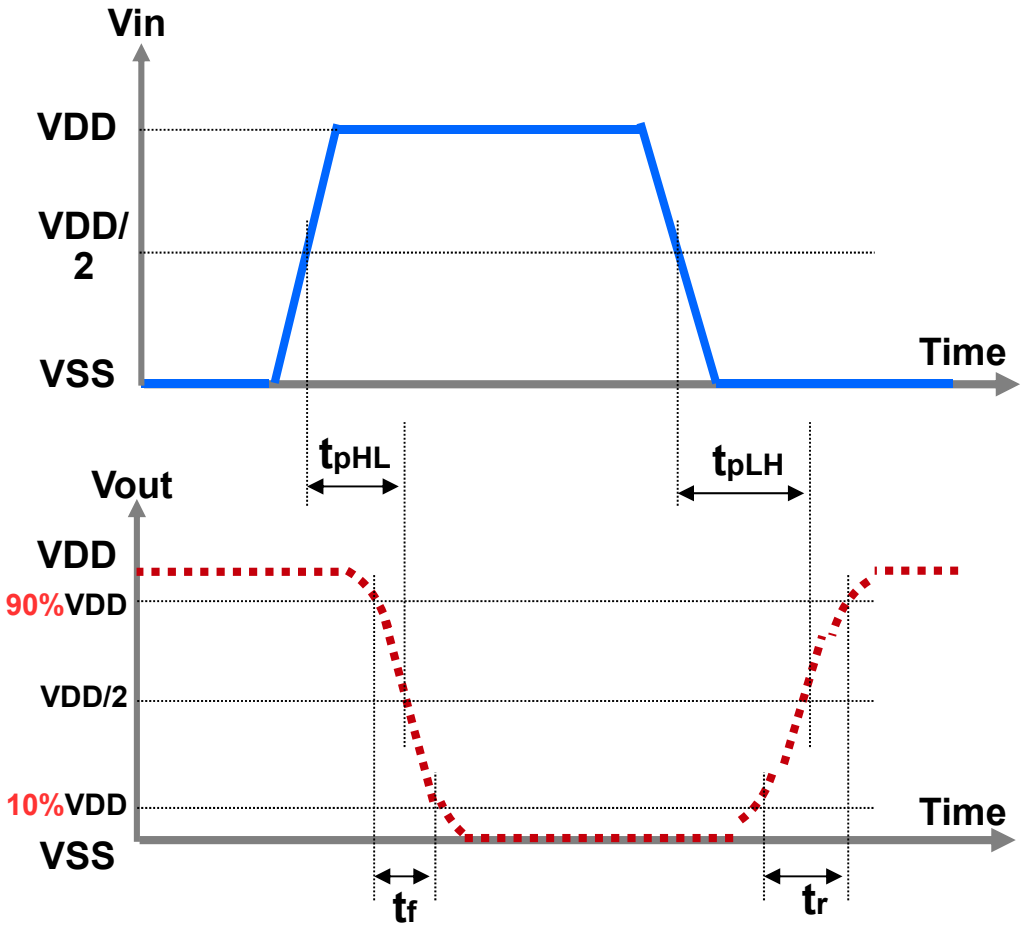
At V_{LT}, logic level is divided between "H" and "L". To set logical threshold voltage of each gate at the same level is important to secure noise margin: $V_{LT} = V_{DD}/2$;

Delay Definitions

Logic delay through a gate is conveniently described by the propagation delay time, t_p. This is average time needed for the output to respond to a change in the input logic state:

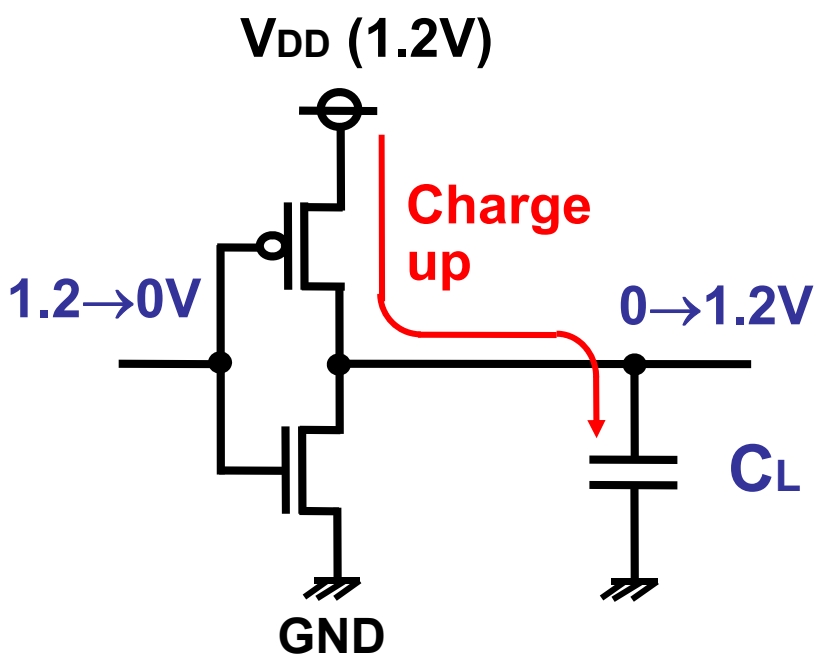
$$t_p = \frac{1}{2}(t_{pHL}+t_{pLH})$$

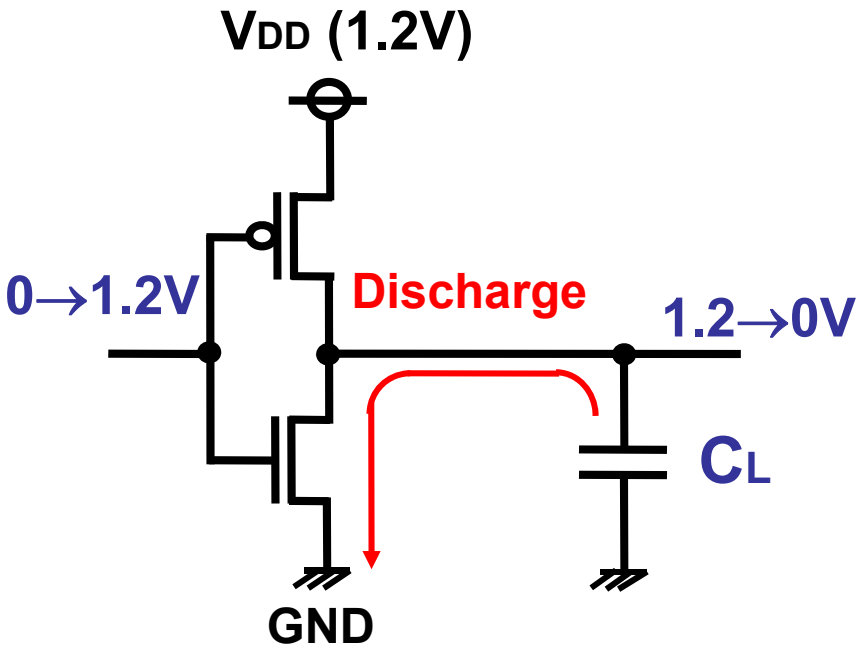
- **Falling propagation delay** (t_{pHL}):
  Time for output to fall by 50% of V_{DD} references to input changes by 50% of V_{DD};
- **Rising propagation delay** (t_{pLH}):
  Time for output to rise by 50% of V_{DD} references to input changes by 50% of V_{DD};
- **Fall time** (t_f):
  Time for output to fall from logical level "1" to level "0";
- **Rise time** (t_r):
  Time for output to rise from logical level "0" to level "1";



Logical level:
- Level "0": From V_{SS} to 10% of V_{DD};
- Level "1": From 90% of V_{DD} to V_{DD};

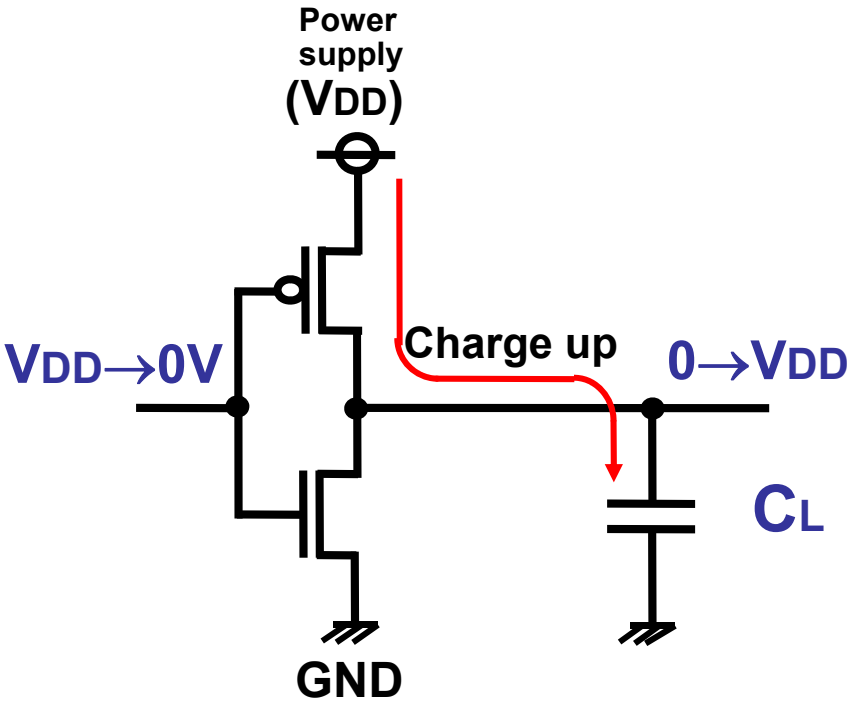
Charge up and Discharge





Rise time and fall time: Times required to charge or discharge the load capacitor. Large load capacitance results in large delay.

Rise time - Delay for Charge up



Note: Assume at initial state, C_L was fully dis-charged to 0V!

◆ Current flows when pMOS is ON,

$$I_s = |I_{ds}| = (\beta_p/2)\cdot (V_{DD} - |V_{thp}|)^2$$

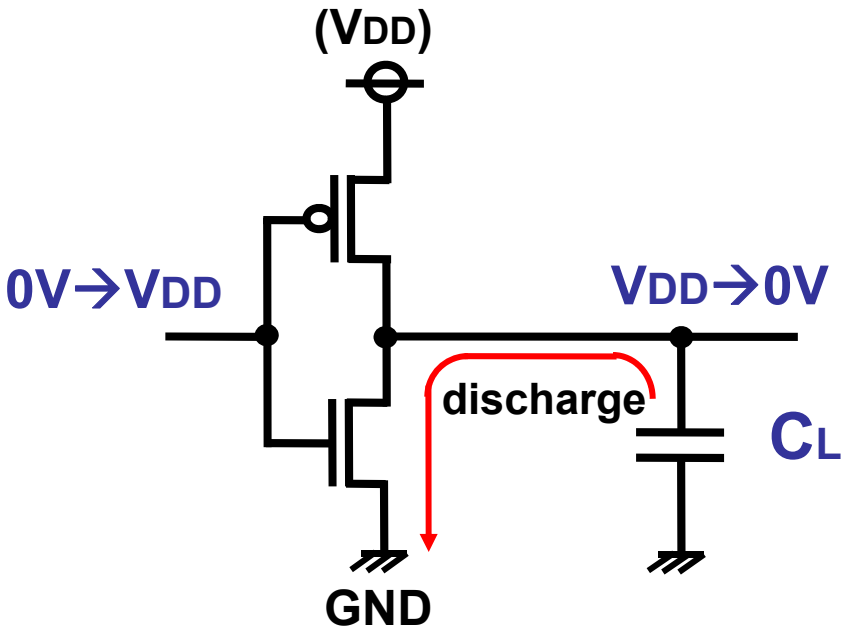
◆ Electric charge to be charged

$$Q = C_L \cdot V_{DD}$$

Rise time is:

$$t_r = Q/|I_{ds}| = \frac{C_L \cdot V_{DD}}{(\beta_p/2)\cdot (V_{DD}-|V_{thp}|)^2}$$

Fall time - Delay for Discharge



Note: Assume at initial state, C_L was fully charged to V_{DD}!

♦ Current flows when nMOS is ON,

$$I_{ds} = (\beta_n/2)\cdot(V_{DD}-V_{thn})^2$$

♦ Electric charge to be discharged

$$Q = C_L \cdot V_{DD}$$

Fall time is:

$$t_f = Q/I_{ds}$$

$$= \frac{C_L \cdot V_{DD}}{(\beta_n/2)\cdot(V_{DD}-V_{thn})^2}$$

Summary of Delay Time

$$\text{Delay time} = \begin{cases} \dfrac{C_L \cdot V_{DD}}{(\beta p/2)\cdot(V_{DD}-|V_{thp}|)^2} & \text{: rise time} \\ \dfrac{C_L \cdot V_{DD}}{(\beta n/2)\cdot(V_{DD}-V_{thn})^2} & \text{: fall time} \end{cases}$$

$\beta = \mu * C_{ox} * W/L$ ⇒

- Faster, if gate length L is shorter
- Faster, if gate width W is wider

Mobility

Capacity of gate oxide per unit area

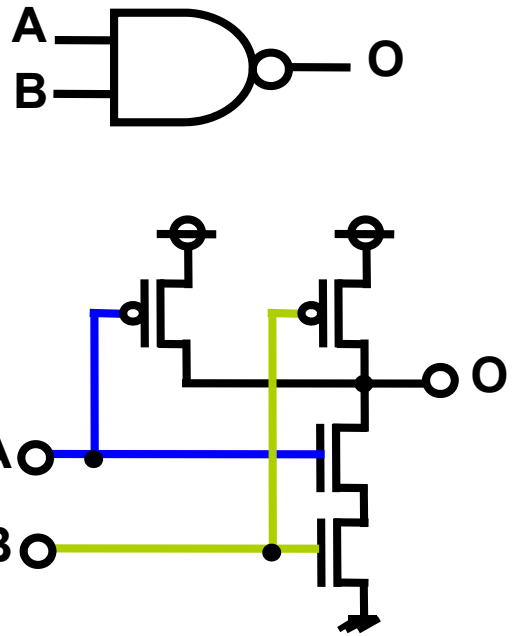
Question 2

What are the schemes to shorten delay time of the inverter?

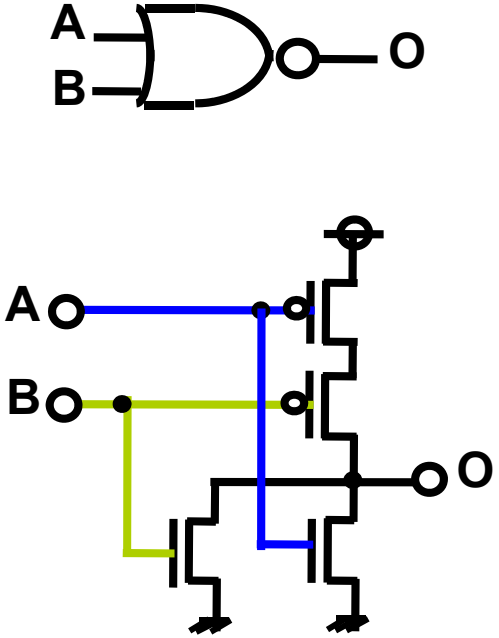
Other Logic Gates

Examples of logic gates

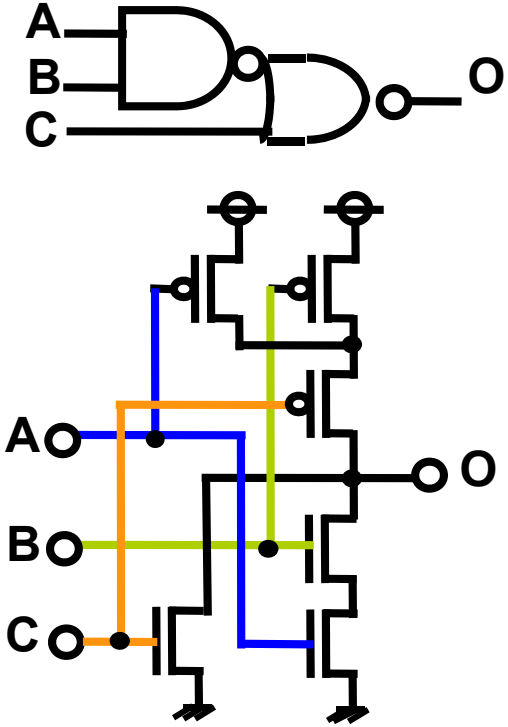
- 2 input NAND ($O=\overline{A \cdot B}$)



- 2 input NOR ($O=\overline{A+B}$)



- Combinational gate ($O=A \cdot B \cdot \overline{C}$)

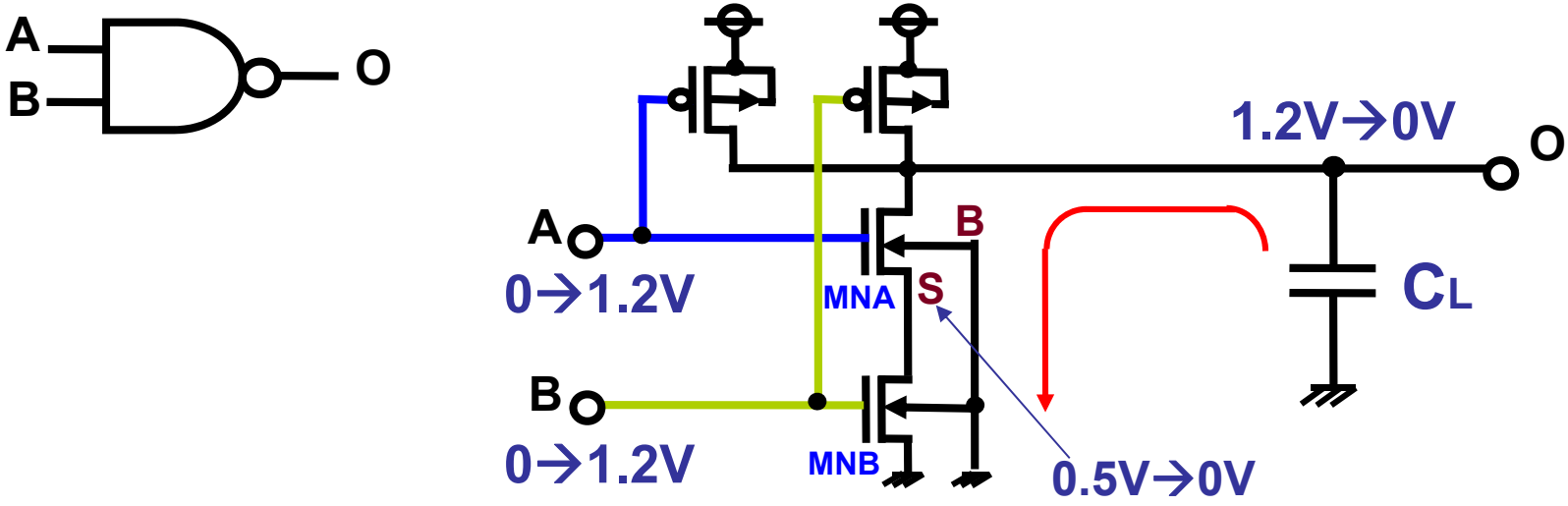


With complementary transistor configurations, all logic circuits can be implemented. Basically their complementary operations are similar to those of an inverter.

Body effect in Logic Gate

Examples of logic gates

- 2 input NAND ($O=\overline{A \cdot B}$)

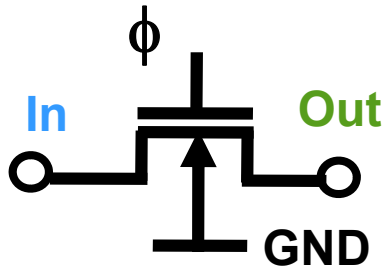


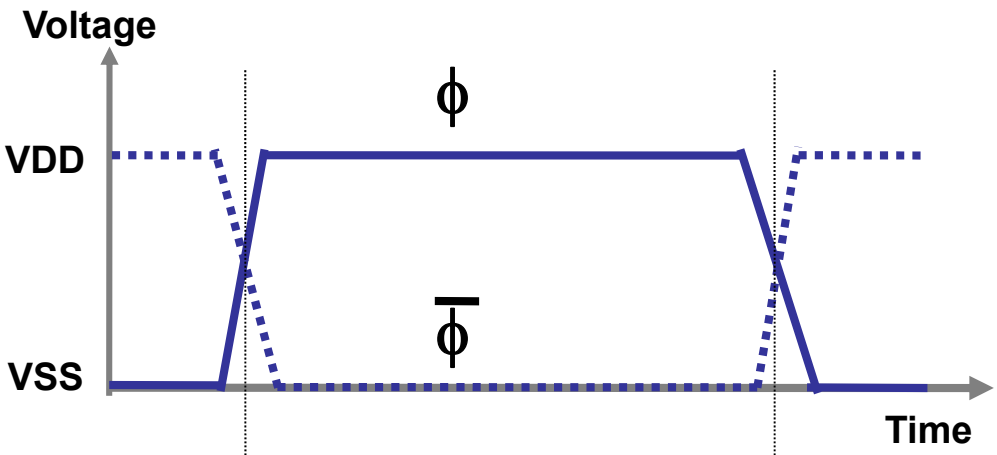
Vthn of NMOS transistor MNA is increased because V_{bs} becomes negative at discharge operation.

→ Delay timing will be increased!

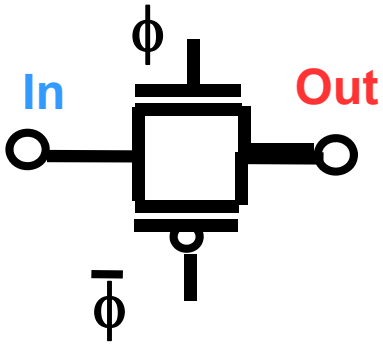
Various Circuit Elements

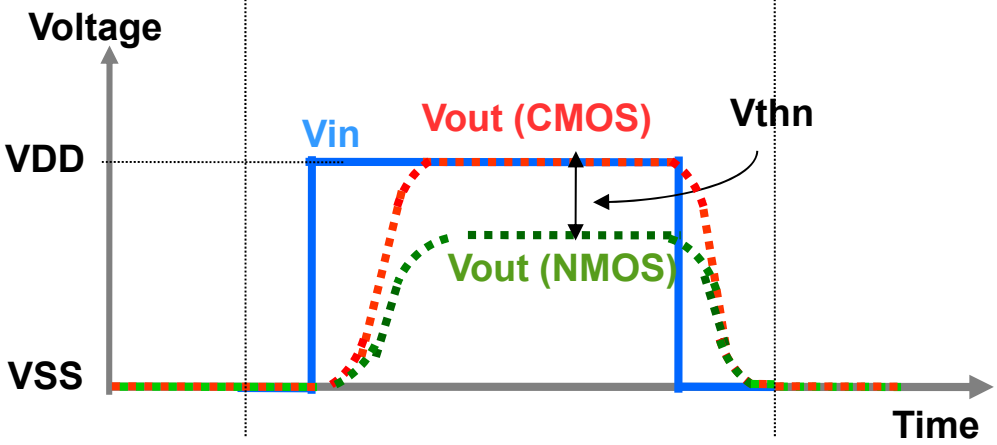
NMOS Transmission Gate





CMOS Transmission Gate

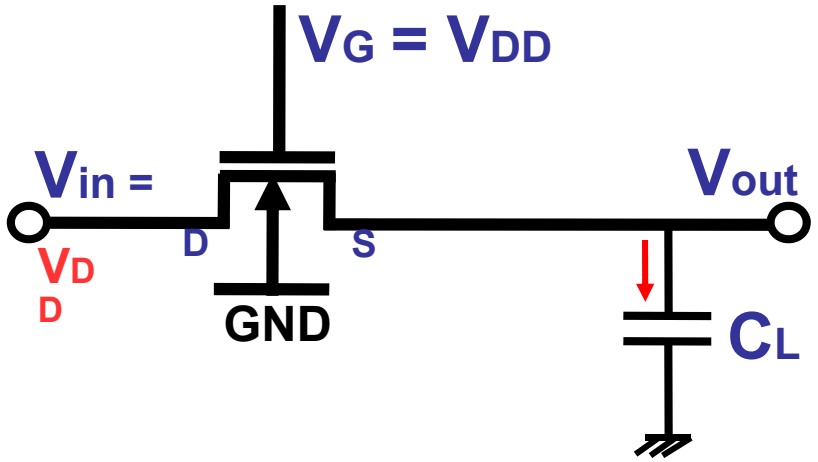




Operation principle: NMOS Transmission Gate

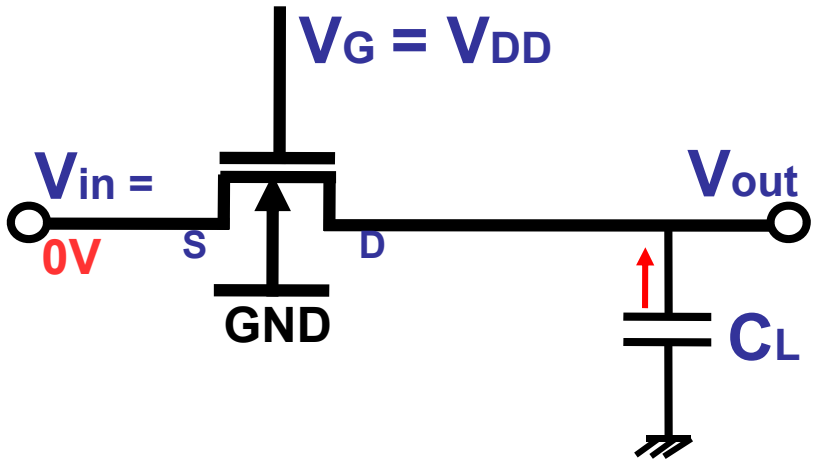
V_{in} is at logical "1" (V_{DD}), assume at the initial state (t=0), V_{out} = 0V. Then:
$V_{GS} = V_{DD} > V_{thn}$;
$V_{DS} = V_{DD} >= V_{GS} - V_{thn}$;
→ NMOS operates in Saturation region;

C_L is charging → V_{out} is increasing;
Condition for NMOS is ON: $V_{GS} >= V_{thn}$;
→ $V_{out} <= V_{DD} – V_{thn}$
→ V_{out} can only swing to $V_{DD} – V_{thn}$;



V_{in} is at logical "0" (0V), assume at the initial state (t=0), $V_{out} = V_{DD}$. Then:
$V_{GS} = V_{DD} > V_{thn}$; (always satisfied)
$V_{DS} = V_{DD}$; → NMOS is in Saturation region;

C_L is discharging → V_{out} is decreasing;
When $V_{DS} = V_{out} < V_{GS} – V_{thn}$, NMOS turns into Triode mode.
C_L continues to discharge until V_{out} = 0V;

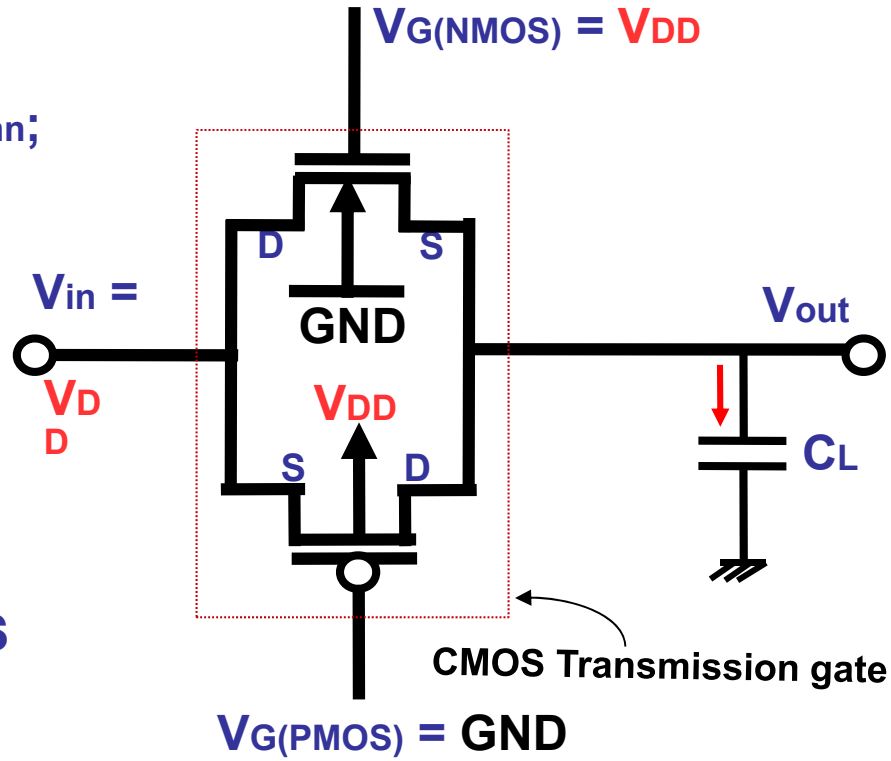


In case of disable mode (V_G=0V), output of NMOS Transmission gate becomes floating or high impedance.

Operation principle: CMOS Transmission Gate

V_{in} is at logical "1" (V_{DD}), assume at the initial state (t=0), V_{out} = 0V. Then:
* For NMOS: $V_{GS} = V_{DD} > V_{thn}$; $V_{DS} >= V_{GS} – V_{thn}$;
→ NMOS in Saturation mode;
* For PMOS: $V_{SG} = V_{DD} > |V_{thp}|$; $V_{SD} >= V_{SG} - |V_{thp}|$. → PMOS in Saturation mode;

C_L is charging → V_{out} is increasing;
* PMOS is in SATURATION region only when:
(1) $V_{SG(PMOS)} >= |V_{thp}|$ (always satisfy); and,
(2) $V_{SD(PMOS)} >= V_{SG(PMOS)} - |V_{thp}|$
→ $V_{OUT} <= |V_{thp}|$
→ At V_{out} is slightly greater than $|V_{thp}|$, PMOS turns to Triode region.



* NMOS is ON when: $V_{GS(NMOS)} >= V_{thn}$;
→ $V_{out} <= V_{DD} – V_{thn}$

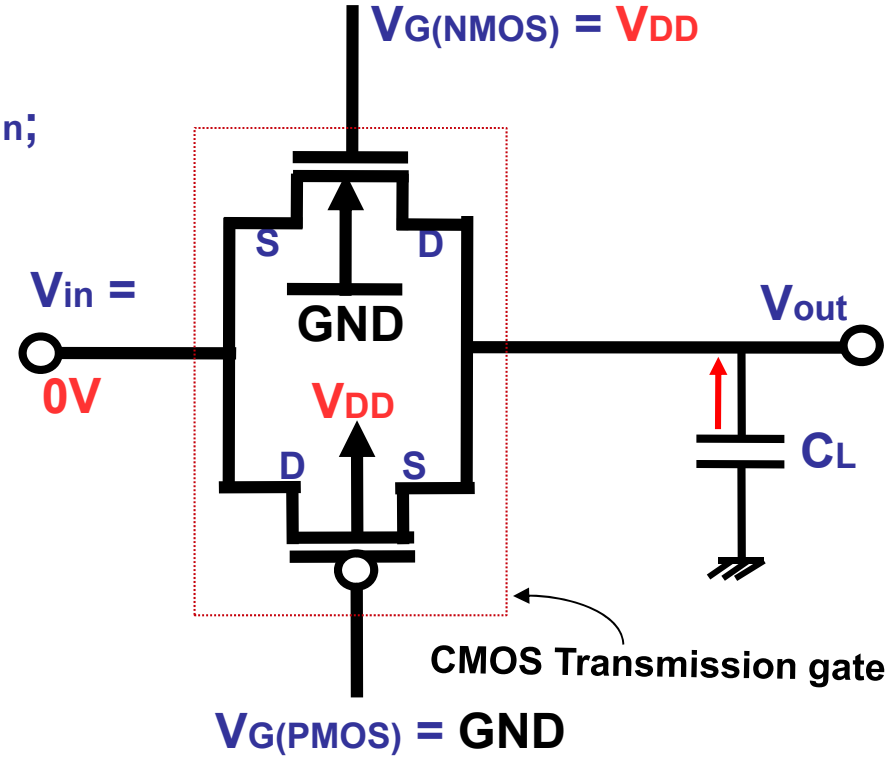
→ At V_{out} is slightly greater than $V_{DD} – V_{thn}$, NMOS turns to OFF state;

But, PMOS is still in Triode region so, C_L continues to charge until $V_{out} = V_{DD}$.

Operation principle: CMOS Transmission Gate

V_{in} is at logical "0" (V_{SS}), assume at the initial state (t=0), $V_{out} = V_{DD}$. Then:
* For NMOS: $V_{GS} = V_{DD} > V_{thn}$; $V_{DS} >= V_{GS} – V_{thn}$;
→ NMOS in Saturation mode;
* For PMOS: $V_{SG} = V_{DD} > |V_{thp}|$; $V_{SD} >= V_{SG} - |V_{thp}|$. → PMOS in Saturation mode;

C_L is discharging → V_{out} is decreasing;
* NMOS is in SATURATION region only when:
(1) $V_{GS(NMOS)} >= V_{thn}$ (always satisfy); and,
(2) $V_{DS(NMOS)} >= V_{GS(NMOS)} – V_{thn}$
→ $V_{out} >= V_{DD} – V_{thn}$
→ At V_{out} is slightly lesser than $V_{DD} – V_{thn}$, NMOS turns to Triode region.



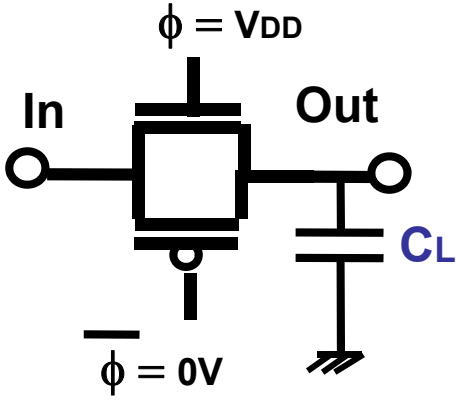
* PMOS is ON when: $V_{SG(PMOS)} >= |V_{thp}|$;
→ $V_{out} >= |V_{thp}|$;
→ At V_{out} is slightly lesser than $|V_{thp}|$, PMOS turns to OFF state;

But, NMOS is still in Triode region so, C_L continues to dis-charge until V_{out} = 0V.

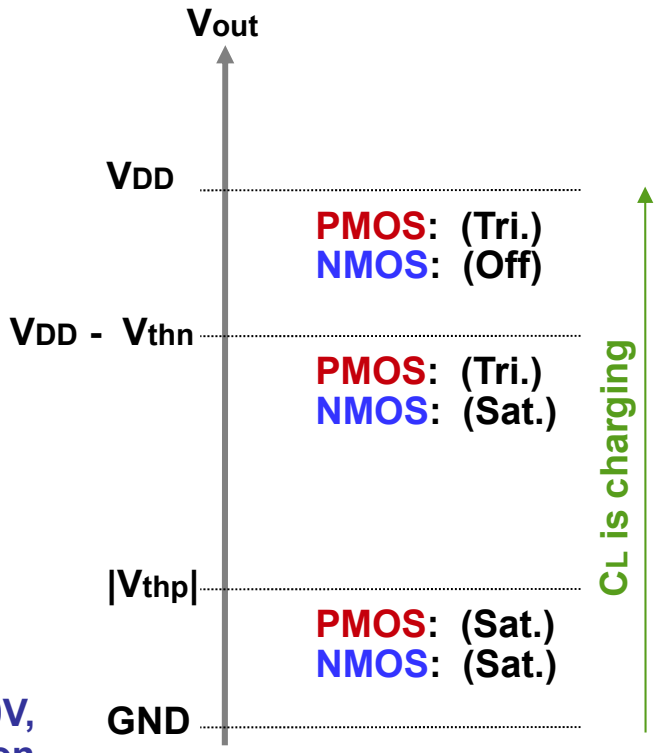
In case of disable mode ($V_{G(NMOS)}$=0V, and $V_{G(PMOS)}$=V_{DD}), output of CMOS Transmission gate becomes floating or high impedance.

Summary Operation: CMOS Transmission Gate

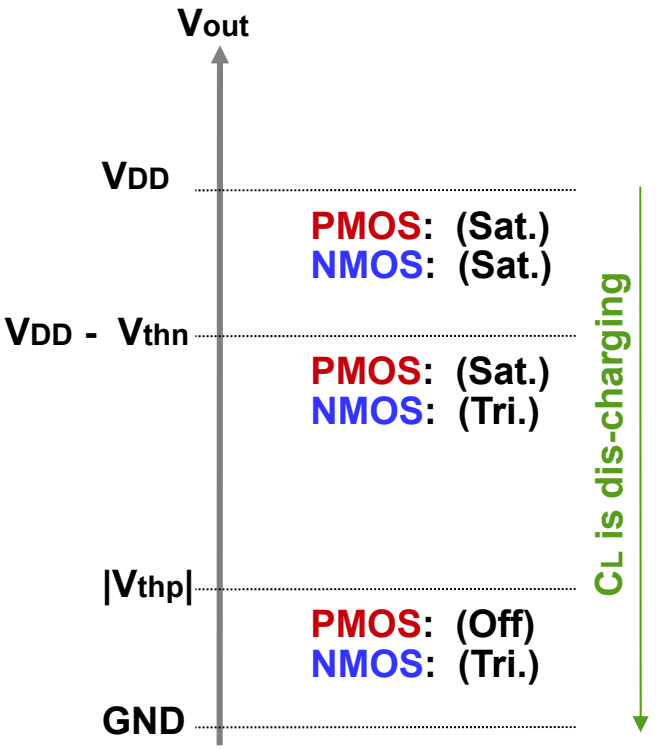
Operation principle of CMOS Transmission gate can be summarized into two charts. First chart is for $V_{in}=V_{DD}$ where C_L is charging up; and other is for $V_{in}=0V$ where C_L is discharging.



In case of disable mode ϕ=0V, output of CMOS Transmission gate becomes floating or high impedance.

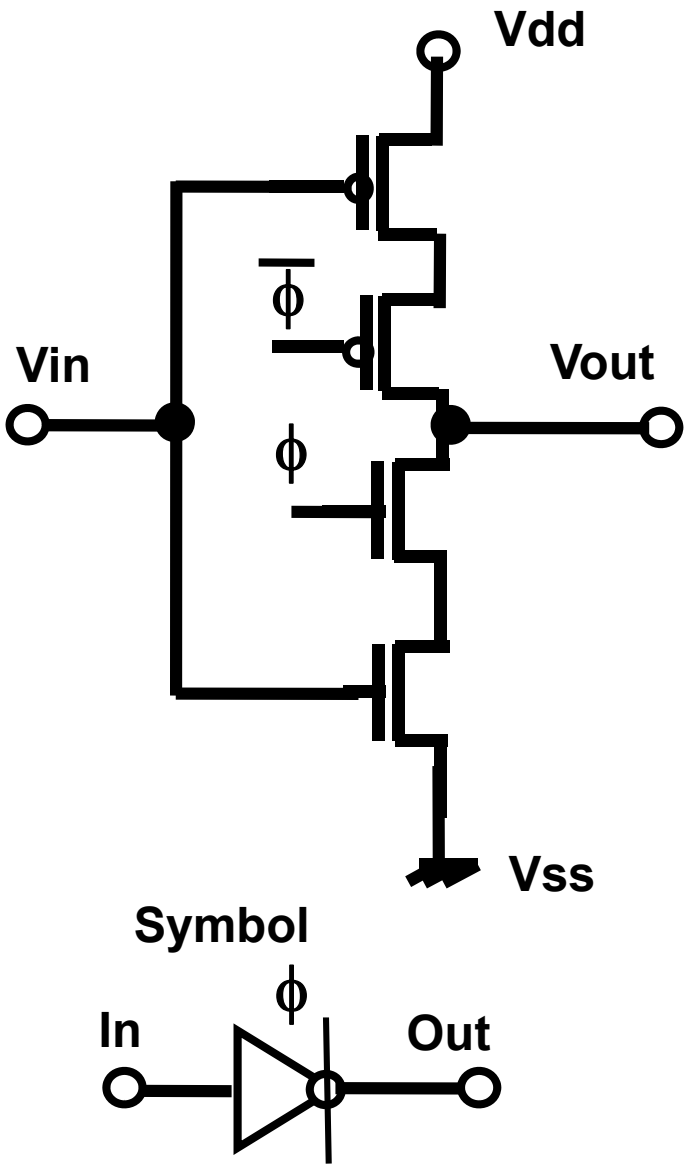


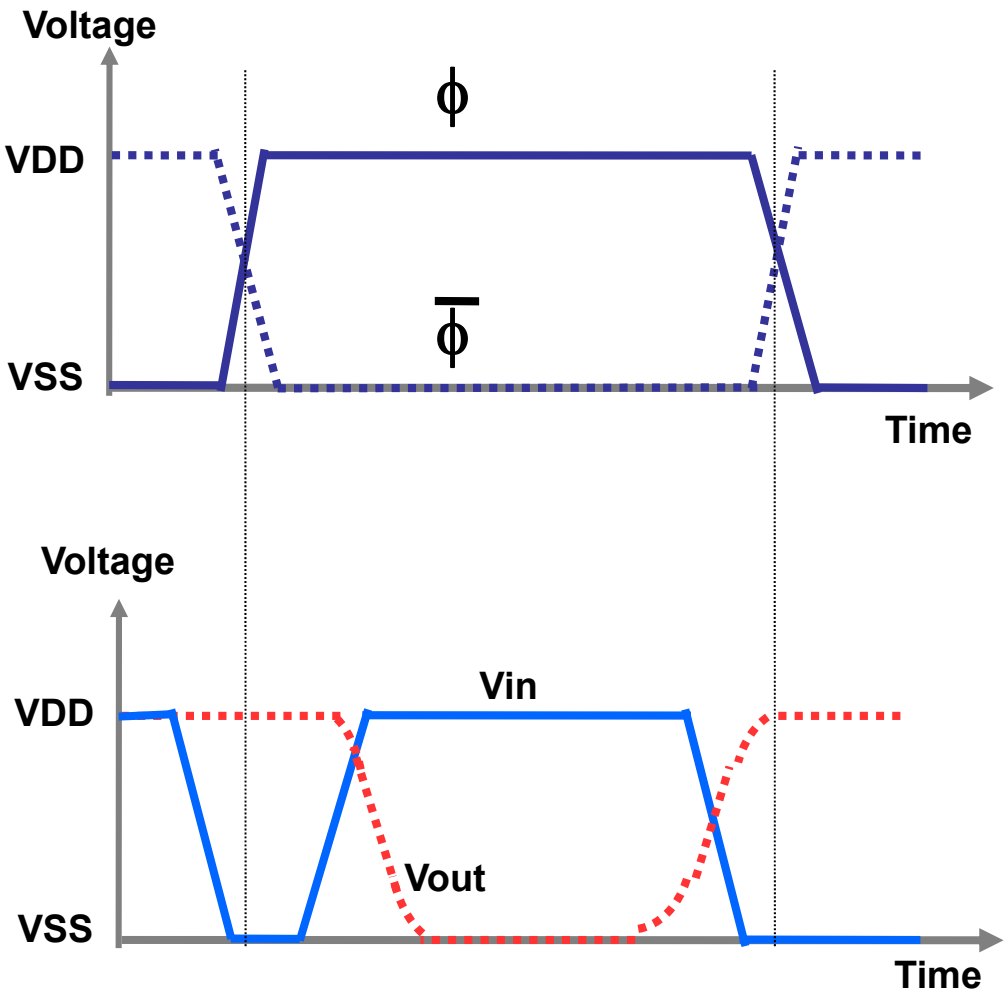
V_{in} = V_{DD}; C_L = 0V at initial state;



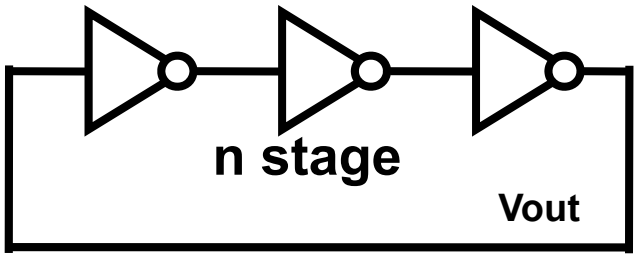
V_{in} = 0V; C_L = V_{DD} at initial state;

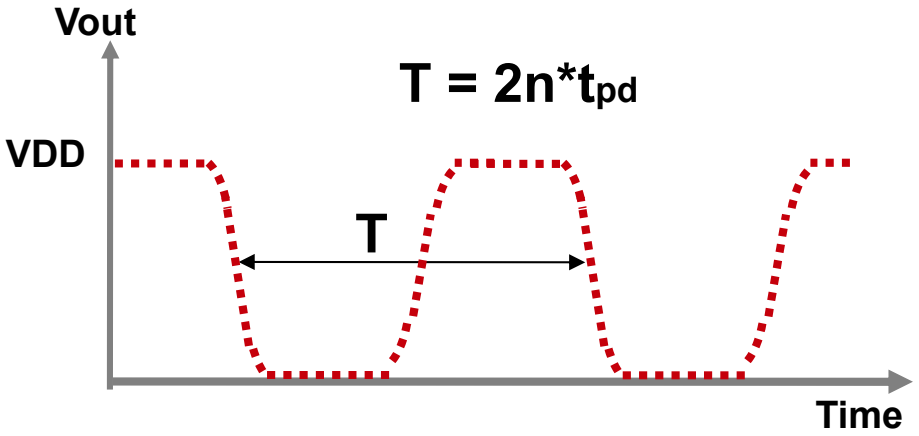
Tri-state CMOS Inverter





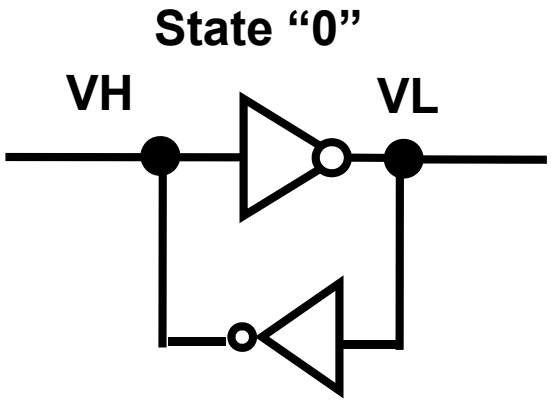
Ring Oscillator

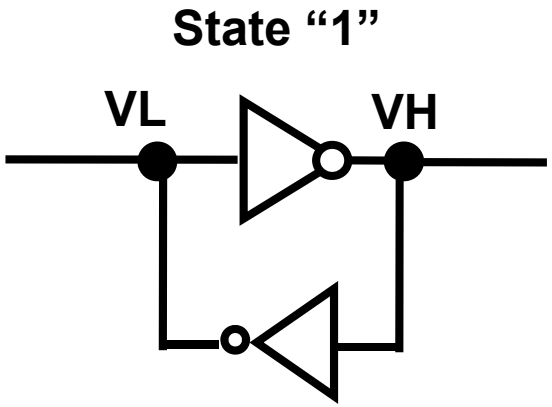




Connect odd number of inverter in ring configuration, the circuit oscillates.

Latch Circuit

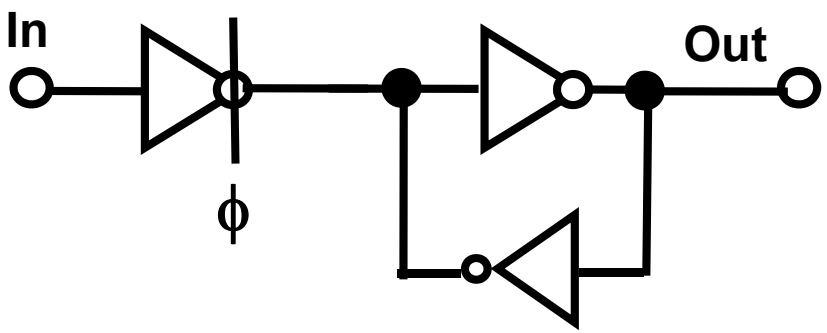




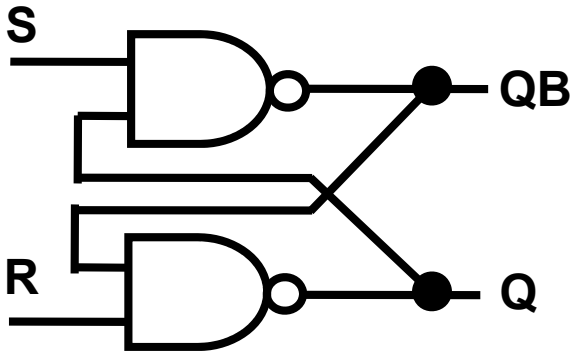
Latch circuit can store data.

Various Latch Circuits

Tri-stage CMOS inverter type Latch

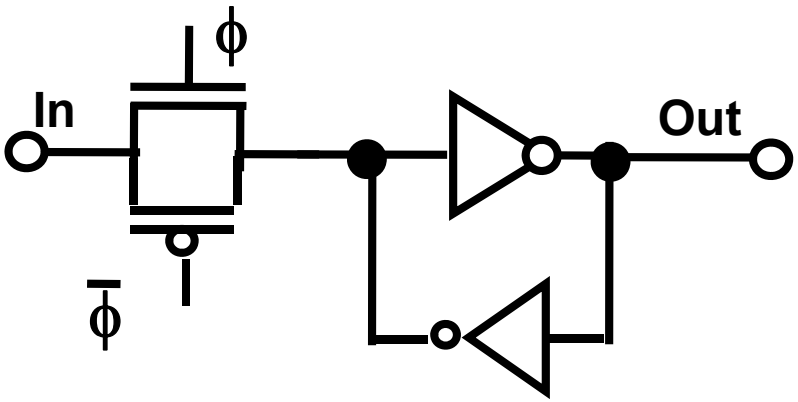


SR Latch Circuit

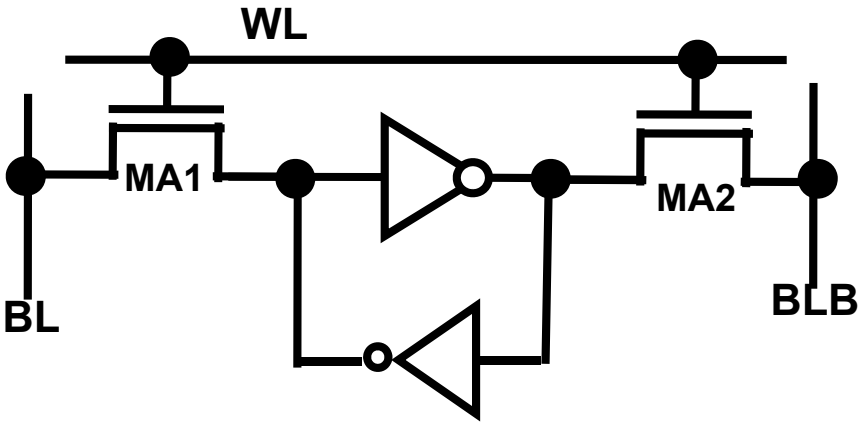


S	R	Q	$\overline{Q}$
0	0	1	1
1	0	1	0
0	1	0	1
1	1	Q	$\overline{Q}$

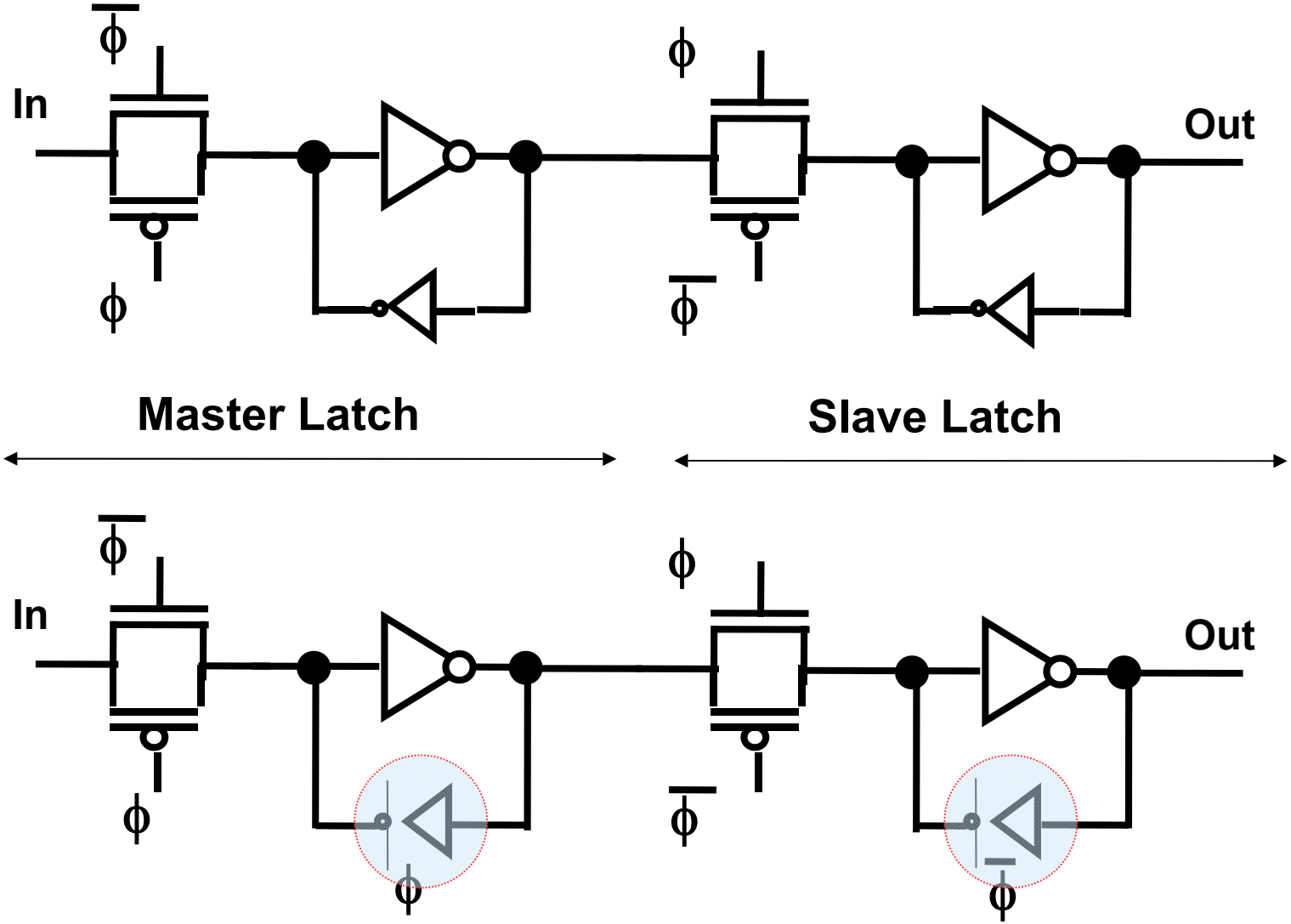
CMOS transmission gated type Latch



SRAM cell

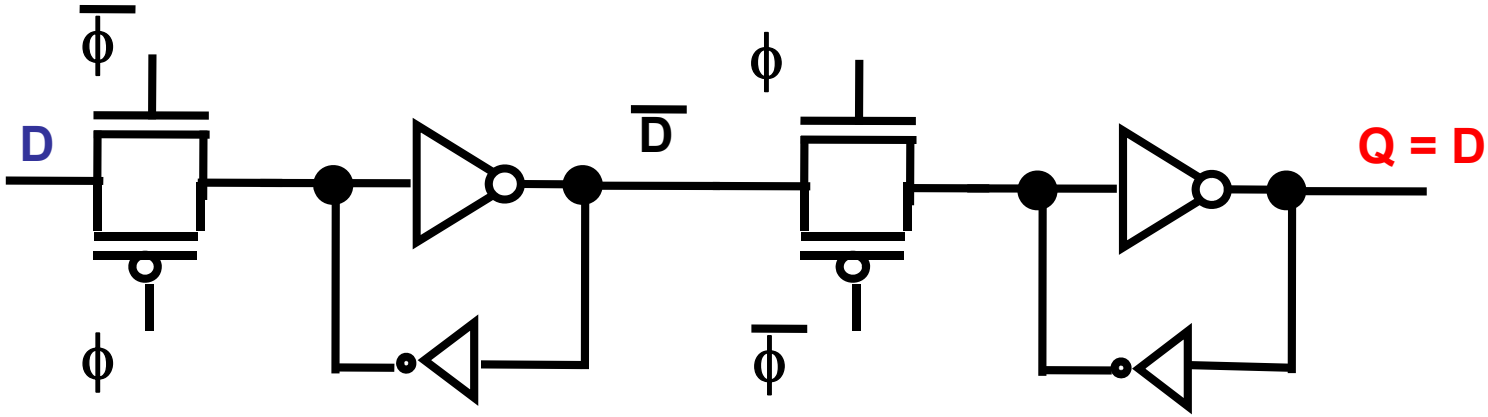


Master Slave Flip Flop (FF) Circuit



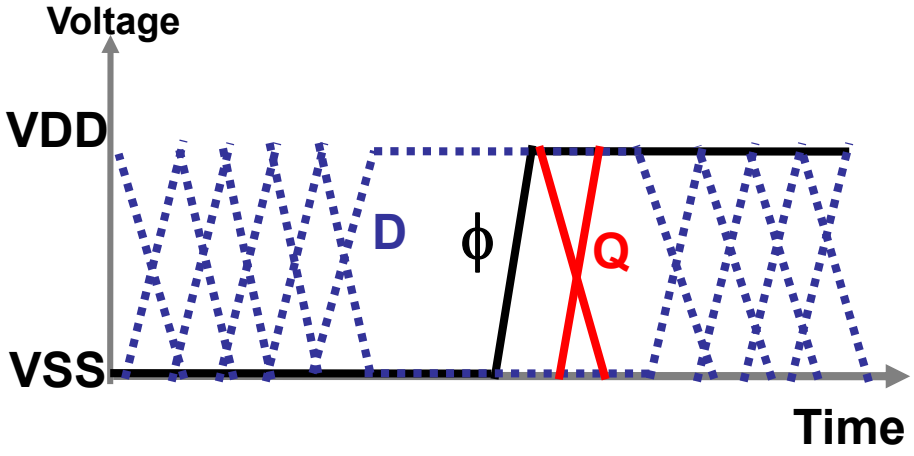
Operation principle of FF

Principle of operation

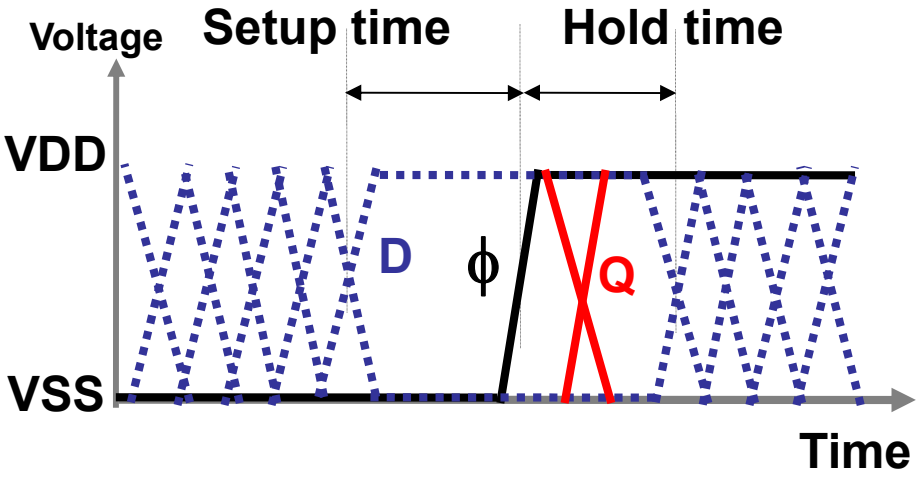


1. When ϕ becomes "Low" data "D" is taken into the first latch and the data "$\overline{D}$" appears at output of the first latch

2. When $\overline{\phi}$ becomes "High" data "$\overline{D}$" is taken into the second latch and the data "D" appears at output of the second latch as a data of Q.



Setup and Hold Time of FF



(1) Data must be arrived to FF setup time before the clock edge.

(2) Data must be kept until hold time after the clock edge.

Setup and hold time is determined depend on FF circuit, and PVT conditions.

Question: What problem will happen if setup time, hold time are violated?

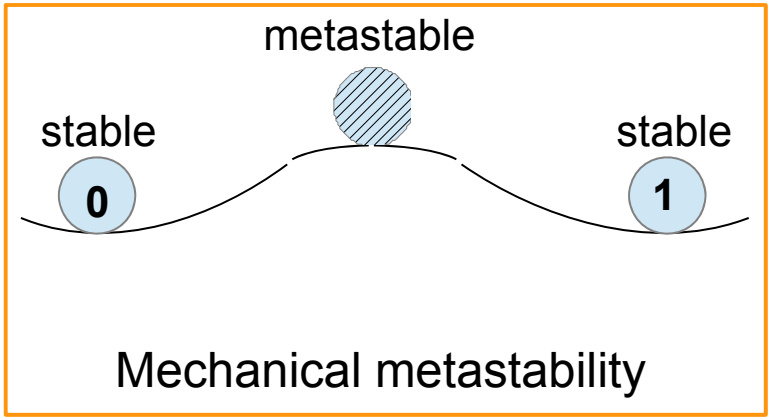
Metastability of FF (1/2)

What is metastability?

In picture, two bottom balls take up a stable state. They can leave only with the supply energy.

But the upper ball is different. Its state remains in unpredictable time and might fall down to unpredictable flank at unpredictable point of time by even very small and unknown influences.

State of this ball (upper ball) is metastable.

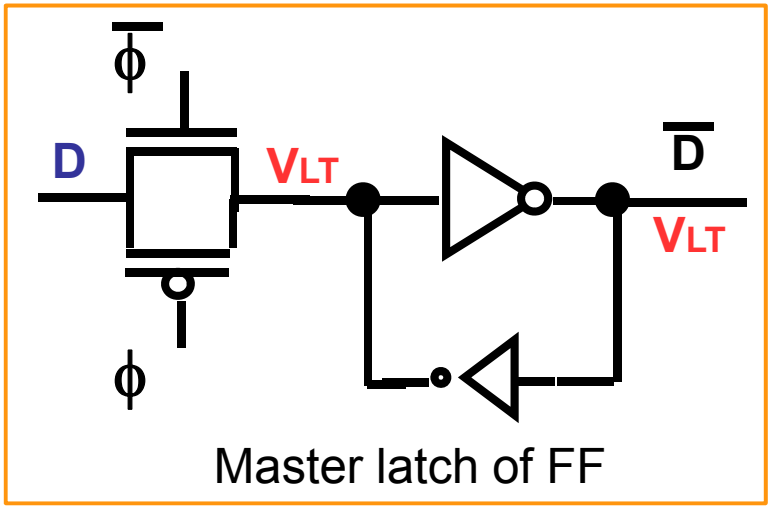


Mechanical metastability

In FF, metastability means indecision of whether the output should be "0" or "1".

How does FF enter metastability?

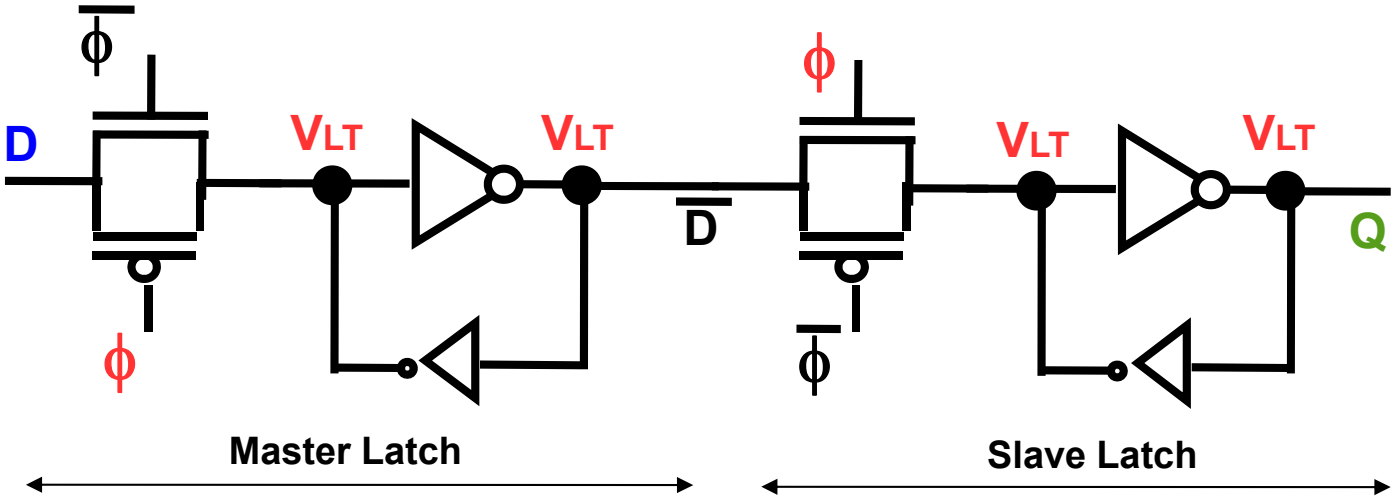
When input D is rising (or falling) to V_{LT}, then ϕ become high. The value of $\overline{D}$ might be this level (V_{LT}) for unpredictable periods. This is called metastability.

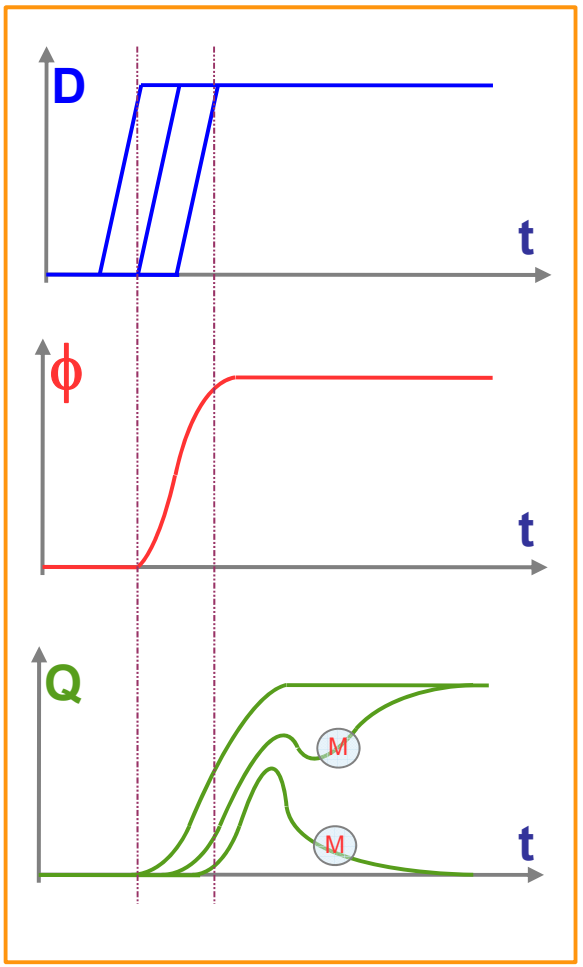


Master latch of FF

Metastability of FF (2/2)

How does FF output (FF/Q) response while FF is in metastability?





When Φ is rising (and assume that master latch is entering to metastability), slave latch is active. Then, value of $\overline{D}$ is transferred to the inverter loop. So, the FF output (FF/Q) will be also V_{LT}.

FF/Q will keep this potential level for unpredictable time and the final value is also unpredictable as shown on waveform picture.

Analog block: Operational amplifier (Op-amp)

An op-amp is a high gain voltage amplifier with differential inputs; and a single-ended output;

<u>Circuit configuration:</u>

- Biasing circuit: outlined in blue;
- Differential input stage: outlined in red;
- Output amplifier: outlined in green;

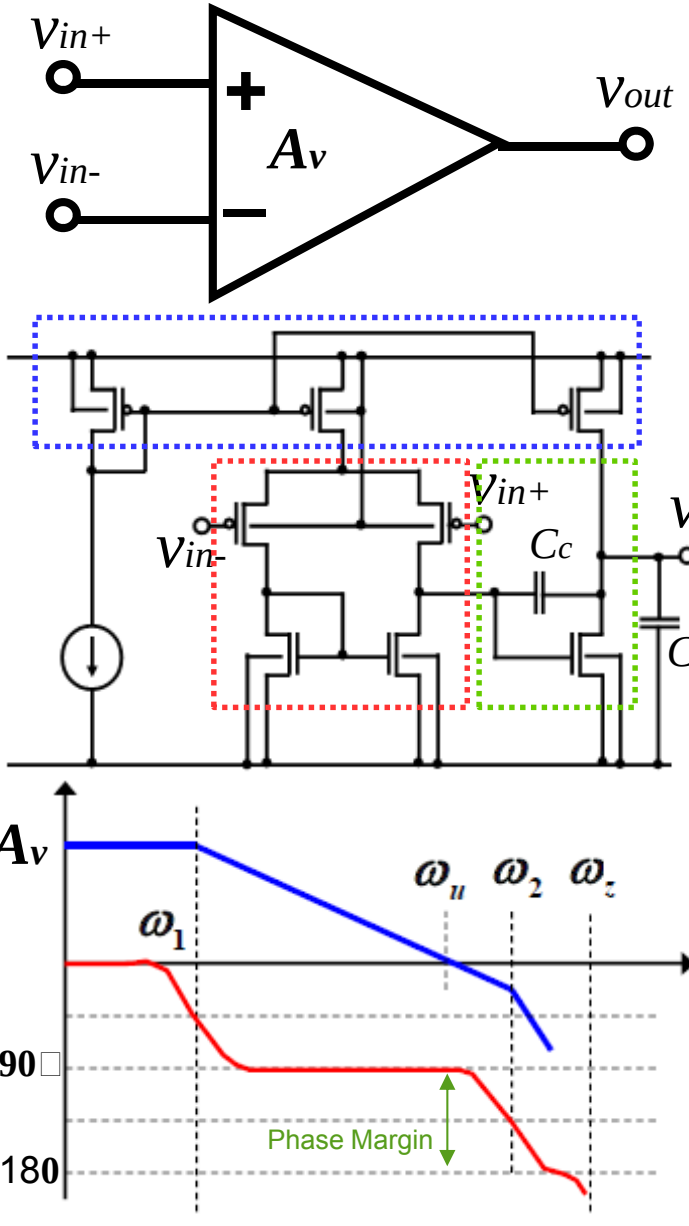
<u>Bode plot:</u>

Bode plot indicates frequency dependence of magnitude and phase;

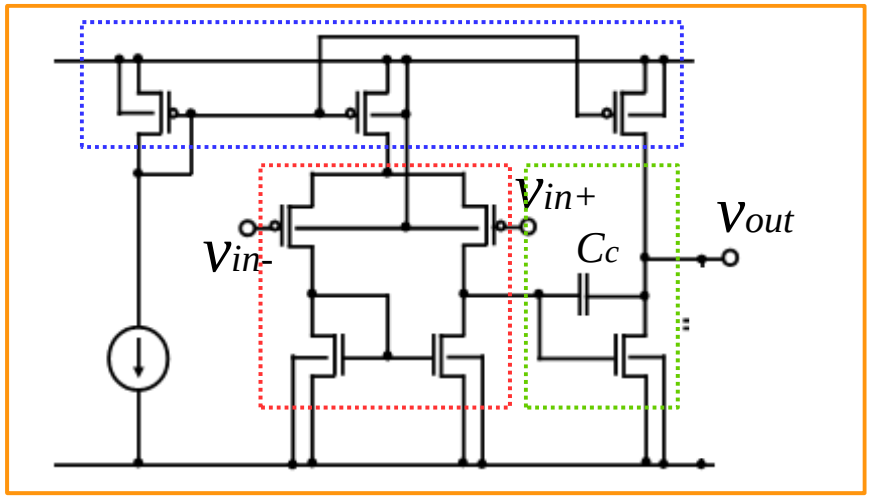
- ω_1, ω_2: Frequency at pole1 and pole2 points;
- ω_u: Frequency at unity gain (Av=1);
- ω_z: Frequency at zero point;

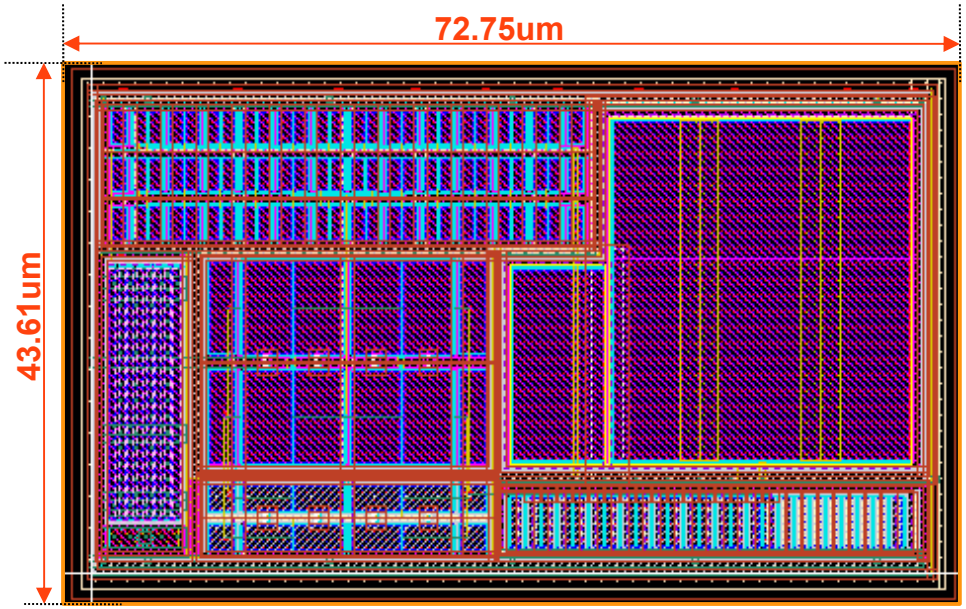
<u>Applications of op-amp:</u>

- Voltage comparator;
- Schmitt Trigger; Triangle wave oscillator;
- Inverting/Non-inverting amplifiers;
- Differentiators and integrators; peak detectors;



Layout of Operational amplifier (Op-amp)



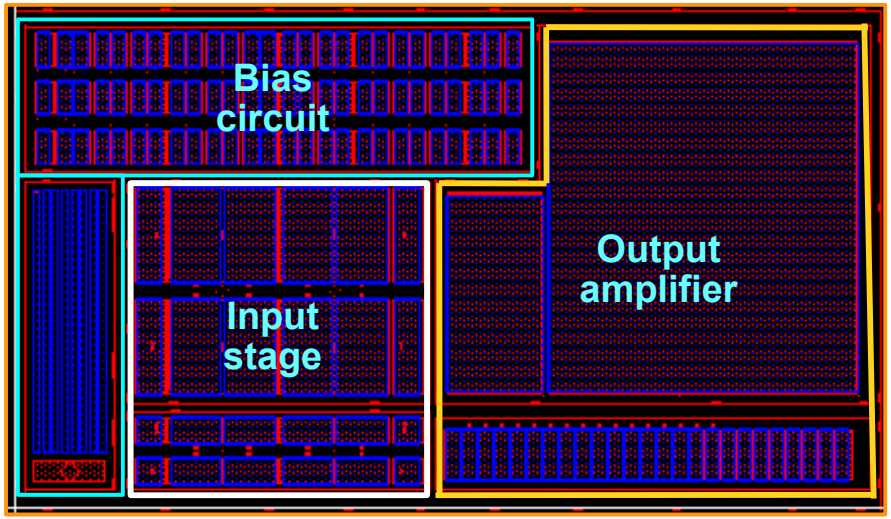


A sample layout of two-stage op-amp is designed in TSMC 40nm, size:
- width: 72.75um;
- height: 43.61um;

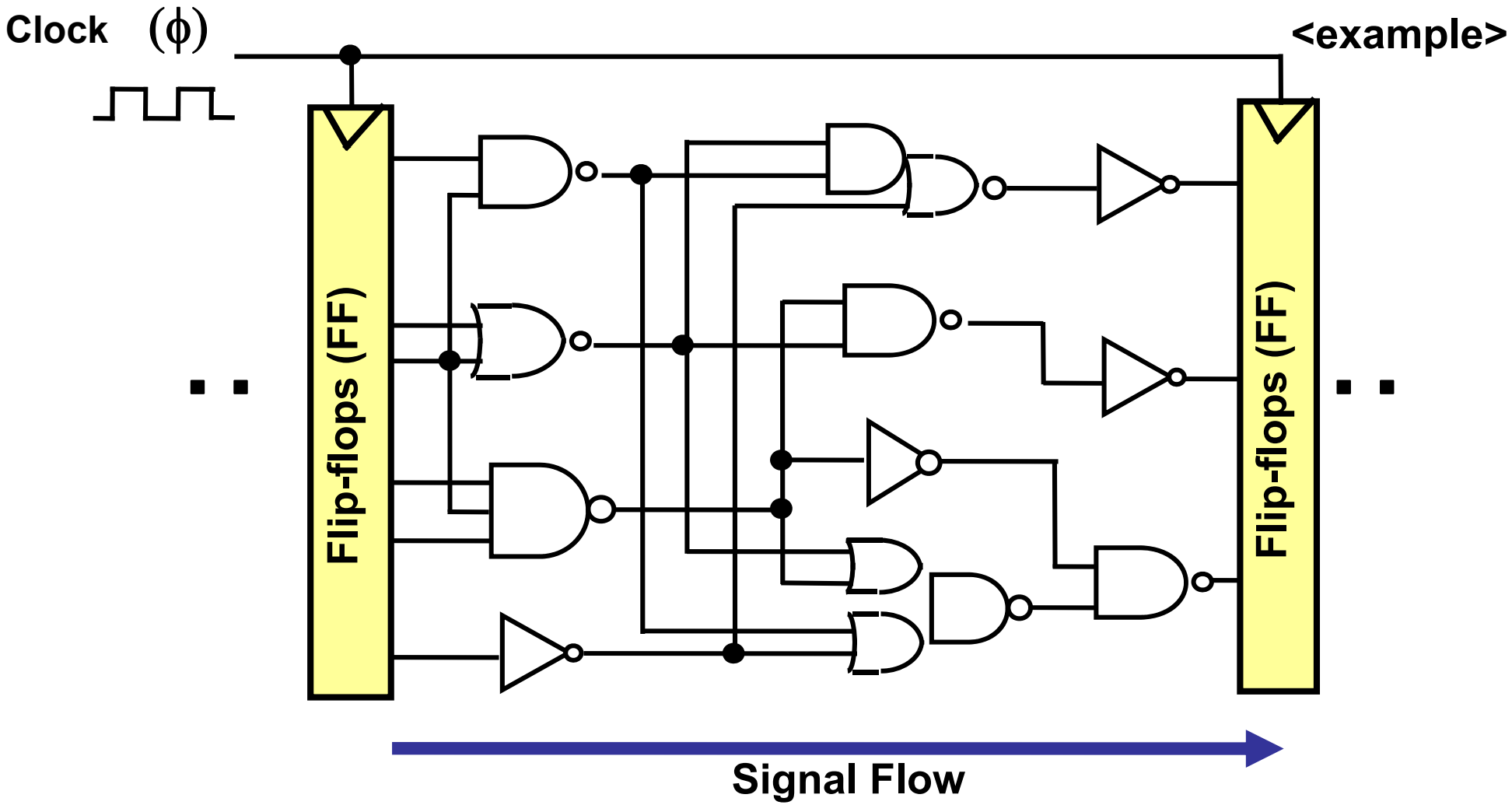
It is different compares to standard cell. Layout size of analog block does not have any standard, it depends on its position in whole placement of upper level.

It will be fabricated at whole chip level.

Block placemen:

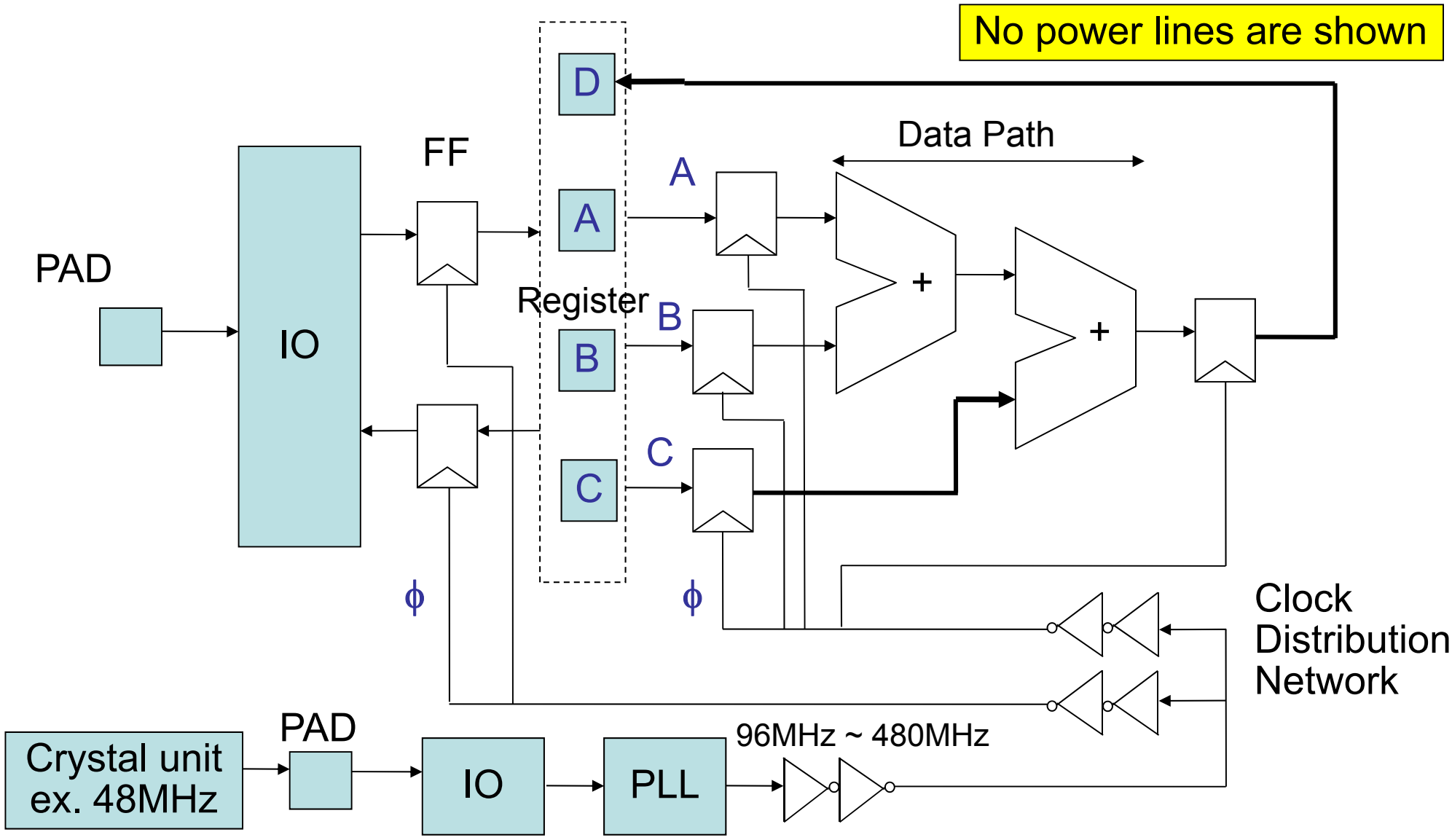


Standard Organization of Logic Block



Standard logic block is composed of combination logic sandwiched by 2 rows of FF

Basic Structure of SoC Synchronous Circuit

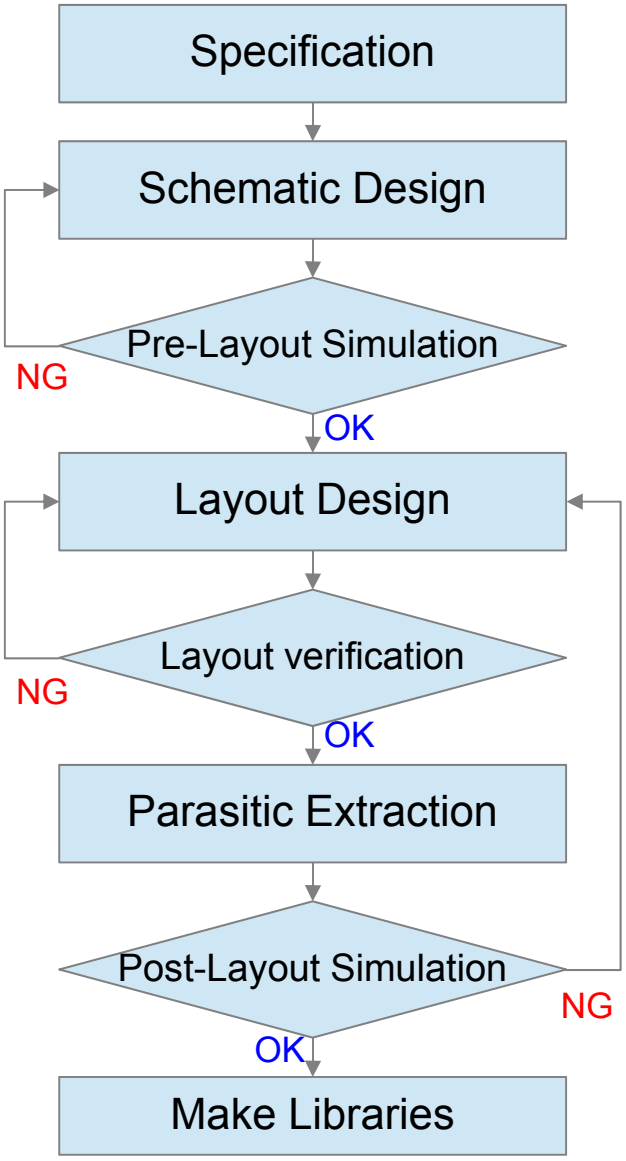


Frequency multiplication is carried out by PLL (Phased Locked Loop)

Summary for Logic Circuits

- Inverter, a fundamental logic circuit, is composed of a pair of nMOS and pMOS transistors, where both gates are commonly connected to input, and both drains to output.
- Output voltage is GND or V_{DD}, and no crossover current flows from V_{DD} to GND at stable conditions.
- Logical threshold voltage: $V_{LT} = V_{IN} = V_{OUT} \sim V_{DD}/2$
- Delay time: $Td = \dfrac{CL \cdot V_{DD}}{(\beta/2) \cdot (V_{DD}-Vth)^2}$
- Standard logic block is composed of combinational logic and FFs.

What Circuit Designers must do



- Receive Requirement specification from customer;
  Design internal specification (for designers only);
- Design schematic topology and parameters;
  Optimize circuit's parameters for all corners;
- Check circuit behavior and performance;
  Compare to specification for optimization;
- Design Power and Ground supply lines;
  Place devices and route connections;
- Check design rules and connectivity;
- Extract parasitic;
- Check circuit behavior and performance;
  Check EM and IRDROP;
- Create blockage design libraries: LEF; Mikyway;
  Create characterization library: Timing library;

Thank you for your attention.