Topology-Based Interlocking of Electrical Substations

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TOPOLOGY-BASED INTERLOCKING OF ELECTRICAL SUBSTATIONS

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Abstract Conventional interlocking of substations is usually expressed by Boolean expressions and realized by electro-mechanical relays. Since these expressions are generated by applying verbally stated interlocking rules to a specific substation configuration, any change of the substation or of the operational philosophy affects them in such a complex way that the problem has to be tackled again in most cases from the very beginning. The proposed topology-based approach suited for microprocessors decouples knowledge-base and implementation, i.e. interlocking rules, and substation configuration. It results in interlocking rules that are independent of a single line diagram and can be applied to all known substation configurations. The rules are divided into mandatory and dependent on operational philosophy. The modularity allows for applying exactly those rules specified in the special project. Any new substation does not require new programming. The inherently fault-tolerant implementation in a 765 kV GIS is briefly described.

INTRODUCTION

Conventional interlocking schemes in electrical substations are generally formulated in terms of Boolean expressions (Fig.1). They are based on a set of operational switching sequences and are specific for the considered single line diagram. The sequences are tacitly assumed or are well-defined; they may be stated as allowed switching operations or as their complement, the forbidden switching operations.

For example, when energizing a feeder after maintenance, first the earthing switch (ES) is opened, then the neighbouring isolators (IS) are closed and as third step the circuit breaker (CB) is closed. The positive consequence is that no interlocking is required between CB and ES.

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On the other hand there are some situations where this technique has essential drawbacks:

- In case of a wrong status indication e.g. because of a fault in the secondary wiring the operator relies for CB closing on the previously determined, but no longer true release from the ES. This means that a consecutive fault can appear.
- Equipment fault or assembly mistake can bring the substation to a switching state which is not foreseen by the operational switching rules. In this case the Boolean expressions are no longer complete.
- Each new elaboration of logic expressions represents a potential error source. Since they cannot be worked out without knowledge of the single diagram, this shortcoming cannot be avoided.
- Substation extension or changes in the utility's operational philosophy after commissioning cannot be identified in all cases as simple "deltas" in the Boolean expressions. In general it is necessary to start again from scratch.

The principle of conventional interlocking is to generate release signals. So, in case of no or insufficient functioning of the interlocking chain the trip of a switching device (ES, IS, CB) is blocked. To-day most interlocking schemes are implemented by electromechanical relays which explains the application of this design rule. Electromechanical relays tend much more to no operation than to malfunction (action without applied control signal).

The availability of powerful microprocessors makes their application desirable for interlocking. In doing this the basic question which arises at the very beginning is whether conventional interlocking schemes shall be implemented on a 1:1 scale in a microprocessor or whether it might be more advantageous to make use of specific microprocessor features like processing capability. In doing this it has to be taken into account that microprocessors inherently tend to fail easier towards malfunction than towards no operation.

It is the subject of this paper to present an approach for microprocessors which can be applied to all known substation configurations. Its main feature is to decouple knowledge-base and implementation or in other words interlocking rules and substation configuration (Fig.1). The design along this line requires a reconsideration of interlocking from the very beginning.

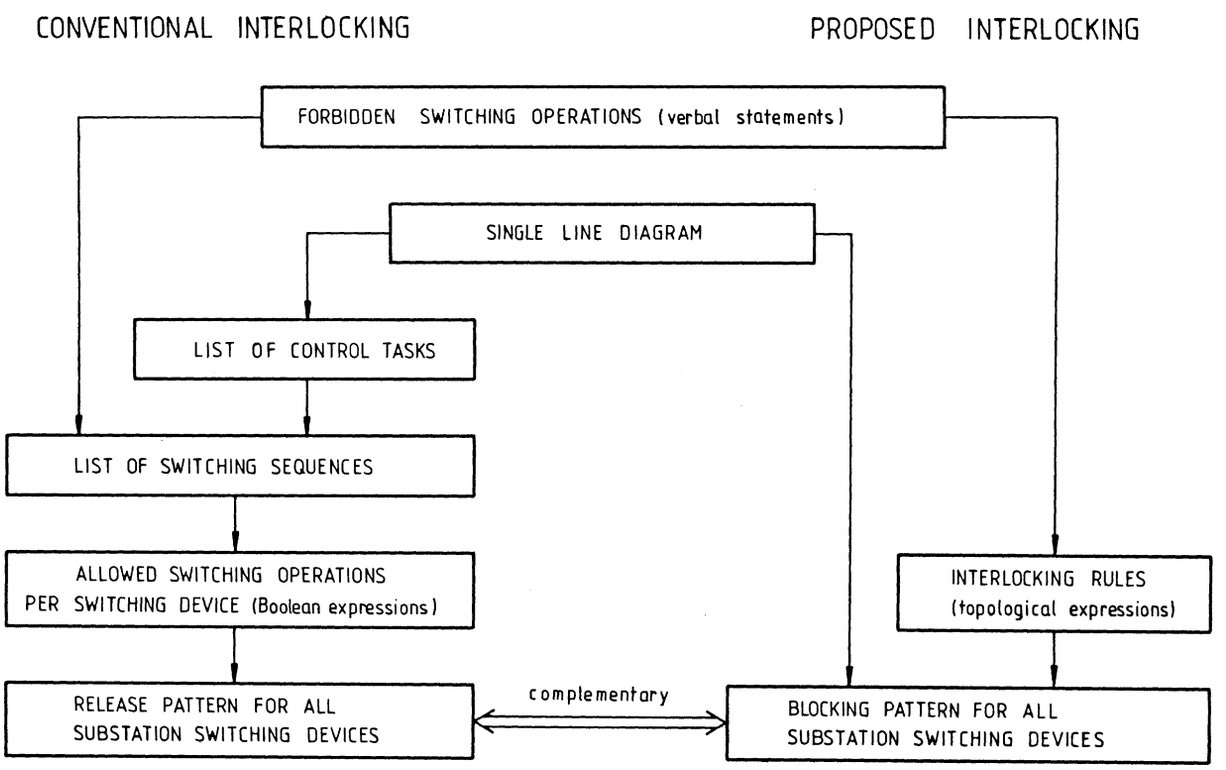


Fig.1 - Comparison of Boolean and topological interlocking approaches

CONSTRAINTS OF THE INTERLOCKING SYSTEM

The main constraints to be met by a new interlocking system are high security and high flexibility which means:
- Fault tolerant
- Self-checking with error location and indication
- Applicable to all known substation configurations
- Expandable for future extensions of an existing substation
- Adaptable to to-day's operational philosophy of the utility
- Expandable for future, changing operational philosophy
- No programming but only setting of parameters for an individual substation.

OBJECTIVES OF INTERLOCKING

All switching operations can be divided into allowed and forbidden operations (Fig.2). The latter are subdivided into the following groups. The notions are explained in Tab.3.

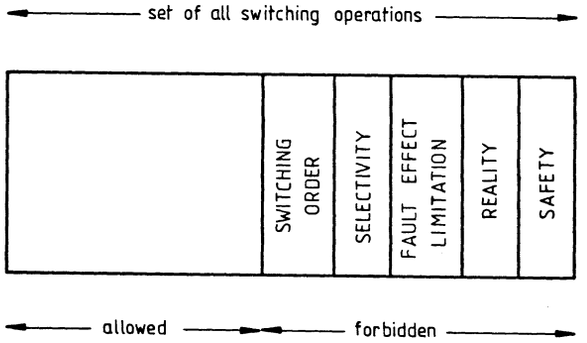


Fig.2 - Partition of all switching operations

Safety

Interlocking has to prevent any harm from equipment and personnel upon switching. This means:
- No earthing of a live substation section
- No power switching by an isolator

Reality

Each real switching device deviates from an ideal ON/OFF-device in two respects: Firstly, it has a specific non-negligible running time. Secondly, in very rare circumstances, its status signals may be unclear or contradictory which can be summarized as being unknown. The resulting interlocking statements are:
- No switching if any switching device is running
- No switching of unknown switching states

Fault Effect Limitation

This group refers to two situations:

A substation section may be identified from the status signals as being isolated whereas it is earthed in reality e.g. because of a forgotten mobile earthing equipment. Protective relays do not trip since no current is flowing. Upon energizing the section, a short-circuit appears.

A substation section may be earthed by transfer via a closed IS. In case of a long section or of unintended opening of the IS, capacitive coupling induces a voltage which may be dangerous to maintenance staff.

In order to limit the fault effects, interlocking in this context requires:
- No closing of an IS with one side at nominal voltage and the other side iso-

lated and consisting of more than one node
- No transfer of earth
- No isolation by a CB without surge withstand capacity
- Open all IS and CB with surge withstand capacity first, then earth the isolated points.

Selectivity

Protection zones are limited by closed/open CB and/or by open IS. Any switching shall not decrease the protective selectivity - if possible - nor shall it lead to a situation where deenergizing a feeder requires the opening of 2 CB instead of 1.
To assure this, we have to demand:
- No CB closing if the CB is allocated to more than one feeder and the feeders cannot be deenergized selectively
- No IS closing if it by-passed a CB, thus destroying the allocation of 1 CB per feeder
- No CB closing which generates a current loop with 2 CB
- Avoid opening of a current loop by CB.

The selectivity-oriented interlocking refers only to single, double and manyfold busbar arrangements with or without transfer busbar. In configurations where the feeder deenergization requires the opening of two CB as in the cases of 2 breaker, ring busbars and 1 1/2 breaker arrangements, the selectivity does not require a special consideration.

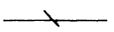
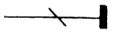
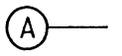
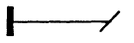
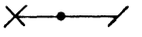
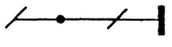
Switching order

The switching order within a sequence shall be straight-forward. In other words erratic switching has to be avoided to reduce both switching time and switching device duty. This goal is obtained by requiring:
- open first CB and then IS, close first IS and then CB.

General properties

The interlocking statements of the first two groups are mandatory in all cases. The last three groups could be neglected in principle; in many cases, however, they represent the operational switching philosophy of a utility that lies behind the Boolean expressions.

Two essential properties have to be added to complete the specification. They are generally valid:
- Interlocking provides the transition from one secure substation state to another one. An emergency state must not be included. For example, the transition from emergency to secure state is the objective of protection and is disregarded here.
- The substation has stable states. Under normal operation and during maintenance the substation is in a stable state. The continuous action of control or interlocking is not required. This situation is entirely different from e.g. a HVDC converter station where no power transmission is possible with inoperative closed-loop control.

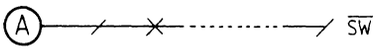
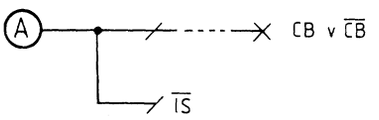
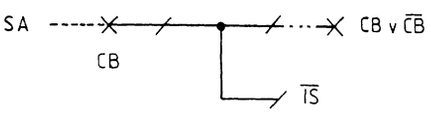
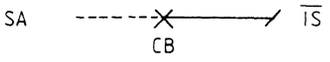
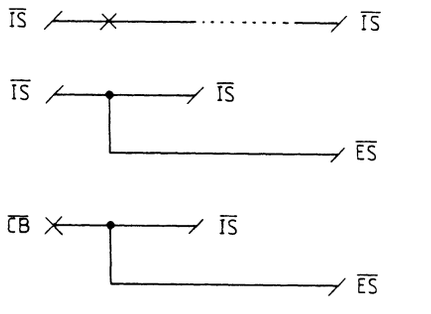
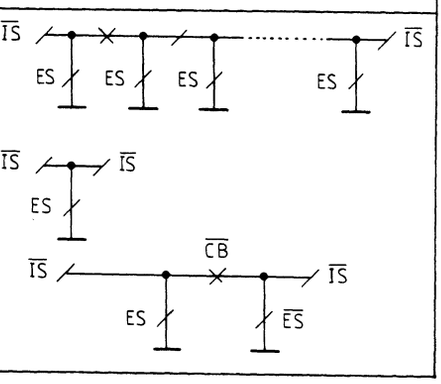
DESIGNATION	TOPOLOGICAL DESCRIPTION	SUBSTATION ELEMENT	GRAPHICAL REPRESENTATION
SW	Edge in the substation single line diagram	Switching device (CB, IS, ES)	- see below -
CB		Circuit breaker	
IS		Isolator	
ES		Earthing switch	
N	Node in the substation single line diagram	Inseparable electrical conductor	
BN	Boundary node	Open end of the single line diagram of the considered voltage level	- see below -
A	Active boundary node, i.e. node which may be energized independently of position of SW inside the substation	Power transformer, reactor, line	
E	Earthed boundary node	Earth point; can be connected to substation by ES	
C	Circuit breaker node	Node connected to 1 CB and to IS	
I	Isolator node	Node connected to IS and ES	

Tab.1 - Topological primitives

TOPOLOGY-BASED INTERLOCKING RULES

The above-mentioned objectives and specifications can be met by putting the interlocking problem on a topological base.

The basic idea is to find a set of topological elements which allow to describe interlocking by some rules which are independent of each other and independent of the single line diagram (Fig.1). Thus, additional or deviating customer-dependent interlocking

TOPOLOGICAL ELEMENTS DESIGNATION	DESCRIPTION	BOUNDARY SWITCHING DEVICE	BOUNDARY NODE	GRAPHICAL REPRESENTATION
S	Sequence of nodes and edges	$\overline{SW}$	A, E	- see below -
SA	Active sequence, i.e. live S with at least one active boundary node	$\overline{SW}$	A	
SAF	Active sequence of feeder type, i.e. part of SA starting from an active boundary node and ending at open isolators or at the first occurring CB (1), open or closed	$\overline{IS}$ CB v $\overline{CB}$	A	
SAB	Active sequence of busbar type, i.e. part of SA bounded by open isolators or the the first occurring CB (1); at least one CB has to be closed for activity transfer	$\overline{IS}$ CB v $\overline{CB}$ CB	-	
SAC	Active sequence of CB node type, i.e. SAB consisting of one node only	CB, $\overline{IS}$	-	
SP	Passive sequence, i.e. an S without active or earthed nodes	$\overline{SW}$	-	- see below -
SPM	SP of sequence type, i.e. consisting of more than one node	$\overline{SW}$	-	
SPI	SP consisting of one isolated isolator node (I) only	$\overline{IS}$, $\overline{ES}$	-	
SPC	SP consisting of one isolated circuit breaker node (C) only	$\overline{IS}$, $\overline{ES}$, $\overline{CB}$	-	
SE	Earthed sequence, i.e. S with least one earthed and without active node	$\overline{SW}$	E	- see below -
SEM	SE of sequence type, i.e. consisting of more than one node (exception see SEI); all ES closed	$\overline{IS}$	E	
SEI	SE of isolated node type, i.e. consisting of one node only	$\overline{CB}$, $\overline{IS}$	E	
SEC	Open, isolated CB earthed at one side only	$\overline{IS}$ $\overline{ES}$	E	

(1) Required, since only CB has power interruption capacity.

Tab.2 - Topological compound elements

GROUP OF RULES	NO.	DE-VICE	COM-MAND	TOPOLOGY CHANGE AND INDEX CONDITION	DESCRIPTION OF TOPOLOGY CHANGE	REASON FOR INTERLOCKING
1.SAFETY ======== Avoid damage of equipment and hazard for people	11	SW	Close	$SA + SE \longrightarrow$	Connection of live with earthed section	Earth fault yields damage
	12	IS	Close	$SA_i + SA_j \longrightarrow$ $i \neq j$	Connection of two different live sections by isolator	Avoid power switching by isolators because of damage
	13	IS	Open	$SA \longrightarrow SA_i + SA_j$ $i \neq j$	Splitting of live section by isolator	
2.REALITY ========= Behaviour in case of intermediate (temporary) and/or unknown states	21	SW	Operate	$R \longrightarrow$	No switching allowed if any switching device is running	Avoid interaction of two switching events
	22	SW	Close	$S + SU \longrightarrow$	Connection between any section and one with unknown state	Avoid switching in unknown states because of possible danger
	23	SW	Open	$SU \longrightarrow$	Opening of a switching device in a section of unknown state	
3. FAULT EFFECT LIMITATION ========== Minimize danger in case of undetected or unintentional potential changes	31	IS	Close	a) $SA + SPM \longrightarrow$ b) $SA + SPI \longrightarrow$	Connection of live and passive section which is no isolated CB node	Earth fault via IS with isolated section earthed in reality
	32	IS	Close	$SE + SP \longrightarrow$	Connection of earthed with isolated section	Avoid transfer of earth potential
	33	CB	Close			
	34	IS	Close	$S + SEC \longrightarrow$	Conn. of earthed section with incompletely earthed CB	Only for missing CB surge withstand capacity
	35	ES	Close	$SE + SPM \longrightarrow$	Conn. of earth point with isol. section which is larger than a single point	Only isolated points should be connected with earth
	36	ES	Open	$SEM \longrightarrow$		
4.SELECTIVITY ======== Retain always selective switching of feeder by 1 CB; i.e. there is only 1 CB at the end of a feeder protection zone	41	CB	Close	$SAF_i + SAF_j \longrightarrow$ $i \neq j$	Connection of two different feeder type sections by CB	Avoid 1 CB for more than one feeder
	42	IS	Close	$SAF_i + SAB_j[\overline{SAF}_i \vee SAF_k] \longrightarrow$ $i \neq k$	Connection of feeder type with busbar type section bounded by not or not only the same feeder type section	Retain 1 CB for each feeder
	43	CB	Close	$SAF_i + SAB_j[SAF_i] \longrightarrow$	Connection of feeder type with busbar type section allowed when bounded by the same feeder type section only	Avoid loops with two CB; i.e.one current path should be interrupted by 1 CB only
	44	CB	Open	$SAB_i \longrightarrow (SAB_i + SAB_i)$	Opening of a busbar type loop with only 1 CB by the CB	No loop opening by CB if current path with IS only is created
5.SWITCHING ORDER ========= Avoid erratic switching sequences	51	CB	Close	$S + SPC \longrightarrow$	Connection of any section with an isolated CB node by the circuit breaker	Retain switching order for opening : 1st CB, 2nd IS; for closing : 1st IS, 2nd CB.
	52	IS	Open	$SA \longrightarrow S + SAC$	Generation of a live CB node by IS opening	

Tab. 3 - Topological interlocking rules

specifications can easily be added. The difficulty is that electrical properties of the substation sections like current/no current or voltage/no voltage/earthed have to be expressed by the switching states of switching devices.

Topological Elements

The actual single line diagram is composed by topological elements. The elements are chosen such that all switching situations can be covered and all interlocking rules can be expressed by them. Therefore, the derived release pattern is secure even for switching which violates the operational switching sequences. Thus, the topological elements represent states with attributes that are relevant for interlocking, viz. same potential (connectivity), power flow (active, passive, earthed), and neighbourhood (relations between neighbouring switching devices or feeders). The topological elements can be divided into primitives and into compounds of them as listed in Tab.1 and Tab.2.

An open switching device can be characterized by two different topological elements on both ends (exception SEC see Tab.2). If the SW is part of a loop, both coincide. A closed switching device is always allocated to one topological element.

The boundaries of all primitives are fixed. The compound elements have either fixed length or their length changes upon switching. The former define local properties, i.e. neighbourhood relations (SPI, SPC, SEI, SEC) and the latter specify overall features.

Interlocking Rules

The interlocking statements of the previous section can now be put into formal rules by using the topological elements defined above (see Tab.3).The indices i, j refer to the elements on both sides of the operated switching device. The plus sign is identical to a union in terms of set theory. Rules 13 and 52 require look-ahead determination of the final state prior to the switching command release. A CB has either surge withstand capacity or not. As a consequence either rule 34 does apply or not.

By inspection it can be immediately seen that the topological interlocking formulation fulfils all objectives: it is independent of the configuration of a specific substation, its modularity allows to take into account the relevant utility-dependent rules and so on.

When the interlocking rules are applied to a single line diagram its boundaries require special consideration: Line, power transformer and reactor have to be modelled in the way shown in Fig.3.

Interlocking Example

In order to illustrate the topology-based approach the simple example of a feeder is considered (Fig.4) where the isolator Q9 is to be closed. The initial switching states which inhibit closing of Q9 according to the topological rules are given below in Tab.4.

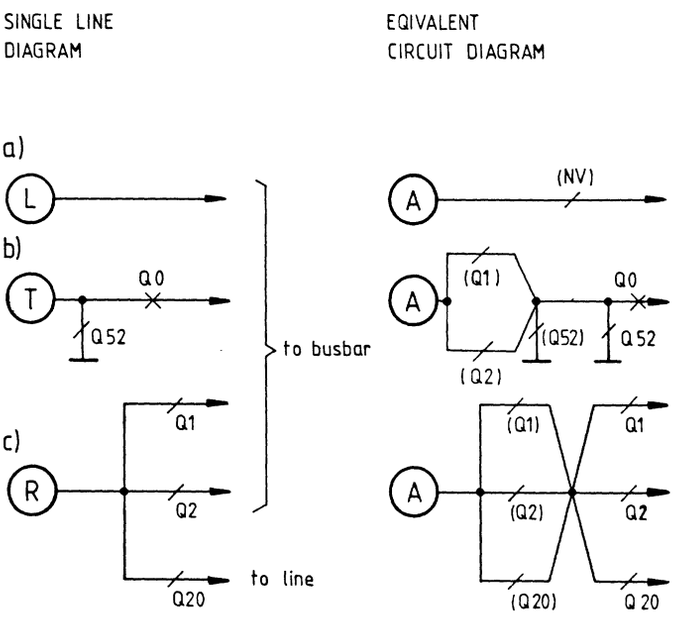


Fig.3 - Boundary elements L, T, R
(...) means non-interlocked indications
a) line (NV) = no voltage relay
b) transformer (Q1) = IS, (Q2) = IS, (Q52) = ES } at other voltage level

In the same table the corresponding Boolean release expression is found which says that Q9 operation is allowed when it is either isolated or earthed.

The Boolean release and the topological blocking expressions are complementary as can be easily checked by working out the Karnaugh plan. A more illustrative way is to mark all possible feeder states as allowed or forbidden. In order to make the reader familiar with the topological elements, one switching situation is marked with the relevant elements and rule numbers in Fig. 5.

For the simple example feeder the number of forbidden states exceeds those allowed. For real single line diagrams the opposite is true for busbar sections and complex feeders e.g. with by-pass isolators or transfer sections.

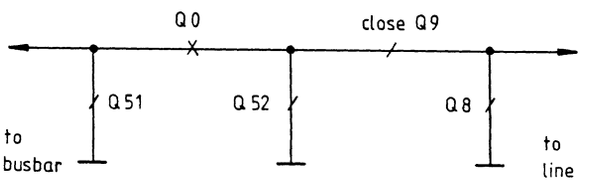


Fig.4 - Interlocking example: Close Q9

INTERLOCKED OPERATION	SWITCHING STATE EXPRESSION
Allowed by Boolean expression : Operate Q9	$\overline{0}.\overline{51}.\overline{52}.\overline{8}$ v 51.52.8
Forbidden by rule	
11 SA + SE $\xrightarrow{\text{SW cl}}$	51.52.$\overline{8}$ v $\overline{51}$.52.$\overline{8}$ v
	51.$\overline{52}$.$\overline{8}$ v 0.$\overline{51}$.$\overline{52}$.8
12 SA_i + SA_j $\xrightarrow{\text{IS cl}}$	0.$\overline{51}$.$\overline{52}$.$\overline{8}$
31 SA + SPM $\xrightarrow{\text{IS cl}}$	0.$\overline{51}$.$\overline{52}$.$\overline{8}$
32 SE + SP $\xrightarrow{\text{IS cl}}$	$\overline{51}$.$\overline{52}$.8
34 S + SEC $\xrightarrow{\text{IS cl}}$	$\overline{51}$.52.8 v 51.$\overline{52}$.8

Tab.4 - Interlocking of 'Q9 close' in Fig.4 by Boolean expressions and interlocking rules ('cl'= close ;'v'= logic OR ;'.'= logic AND)

STATES OF SWITCHING DEVICES Q				ALLOWED BY BOOLEAN EXPRESSIONS	FORBIDDEN BY TOPOLOGICAL RULE NO.
0	51	52	8	x	
0	51	52	$\overline{8}$		11
0	51	$\overline{52}$	8		34
0	51	$\overline{52}$	$\overline{8}$		11
0	$\overline{51}$	52	8		34
0	$\overline{51}$	52	$\overline{8}$		11
0	$\overline{51}$	$\overline{52}$	8		11, 32
0	$\overline{51}$	$\overline{52}$	$\overline{8}$		12
$\overline{0}$	51	52	8	x	
$\overline{0}$	51	52	$\overline{8}$		11
$\overline{0}$	51	$\overline{52}$	8		34
$\overline{0}$	51	$\overline{52}$	$\overline{8}$		11
$\overline{0}$	$\overline{51}$	52	8		34
$\overline{0}$	$\overline{51}$	52	$\overline{8}$		11
$\overline{0}$	$\overline{51}$	$\overline{52}$	8		32
$\overline{0}$	$\overline{51}$	$\overline{52}$	$\overline{8}$	x	

Tab. 5 - Comparison of allowed and forbidden states of Fig.4 and Tab.4

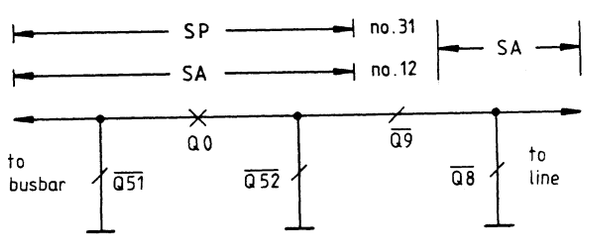


Fig.5 - Example from Fig.4 and Tab.4 for topological interlocking

INTERLOCKING SYSTEM DESIGN

The problem is divided into two subsequent parts. First, the actual substation switching state is determined (topology recognition). Second, the release or blocking state is calculated for each switching device (release pattern).

Topology Recognition Algorithm

All inseparable electric conductors or nodes of the single line diagram are decomposed into threefold nodes, i.e. nodes with three connectors. This decomposition simplifies the topology recognition. Each node is defined by static identification number, by actual sequence number and by actual electrical state attribute.

As an example for display on the host computer, the situation of Fig.5 is presented in Fig.6. The nodes are marked by sequence numbers (4,7,9,11,12) and state attribute (a = active, e = earthed). The letter O is allocated to switching devices released for opening. The missing C for release to close at the open switching devices Q8, Q9, Q51, Q52 means no release to close.

The actual connectivity pattern is determined by starting from one node and by progressing to the neighbouring node. The status of both nodes is compared with respect to power flow (active, passive, earthed node) and to neighbourhood (isolated point, same feeder) as well as to availability (running, unknown) of the connector in between. The procedure is continued until all nodes have been called once. In the second step all nodes are given their identifier.

```
          *
  a4--a4--XO--a4--/ --a7--a7
BUS   I    Q0 I    Q9 I    LINE
      I       I       I
      /       /       /
      IQ51    IQ52    IQ8
      I       I       I
      e12     e11     e9
```

Fig.6 - Display of Fig.5 on the host computer; closed devices marked by an asterix

Release Pattern Algorithms

The identified topological elements are now used to evaluate the above described interlocking rules. For each switching device a release or blocking status results. If a command is given to operate a switching device which is blocked because of one interlocking rule, the command will be blocked.

Inherent Fault Tolerance

Structure and algorithms have been developed such that inherent fault tolerance is obtained. It may be recalled that the main concern in interlocking is to obtain a high security. Fault detecting means are applied at each of the following levels.

1. Process :
- Check of invariants.
  Example: A sequence of nodes and edges (S) is by definition either active or passive or earthed ({ } ='set', ∩ ='intersection'):
  $\{SA\} \cap \{SE\} = \emptyset$
  $\{SA\} \cap \{SP\} = \emptyset$
  $\{SE\} \cap \{SP\} = \emptyset$

2. Software :
- Identifier calculation with two different starting points (e.g. left and right side of an open switching device)
- Check of permissive running time of a switching device
- Check of unallowed program states
- Error output with error identification

3. Hardware :
- Interlocking rather than release rules (as opposed to conventional electromechanical interlocking)
- Check sum
- Inverse data storage
- Watch-dog to supervise program running time

IMPLEMENTATION

The implementation covers three steps:

Host Computer

The topology-based interlocking system is implemented on a host computer. Topology recognition, release pattern, and man-machine communication programs are written in PASCAL.

Target Set-up

The on-site installation is in a feeder-oriented processor network which is connected to the substation. For instance, the high-speed bit-slice microprocessor described in [1] is applied.

1. EMI proof :
In substations electromagnetic perturbations are rather strong. In order to even meet the very hard requirements of a GIS (gas-insulated substation) at EHV, e.g. 765 kV, the following measures have been taken to obtain an acceptable degree of security:

- Real-time calculation of release pattern:
  When a switching command is given, the release pattern is updated. Only then the command is passed to the output relays of the processor. This feature avoids consecutive faults. Even from states which are not foreseen by the operational sequences secure switching is possible.

- Status information from two contacts:
  A normally open and a normally closed contact are used for each switching device status input (inverse logic). Thus, running time and DC supply failure can be monitored.

- Output relay supervision:
  A GO-contact is used in series to the output relay. Therefore, a periodic check of the processing system including the mechanical relay operation can be performed. The concept requires relays with pairs of mechanically coupled contacts.

2. Programming :
The host computer programs are down-loaded to the target processor.

Tests

The tests are structured. They are performed at different stages of design and implementation:

1. Software :
The software is entirely tested in the factory. The host software is checked for completeness of the interlocking rules, absence of contradictions and correctness of stored topology data. The test of the target processor software is done by checking each of the interlocking rules.

2. Hardware :
The hardware is tested per feeder and station cubicle. Thereafter the system consisting of microprocessors, connectors in between and process interface is tested. The tests include functional tests under different environmental conditions (temperature, moisture). Special attention is given to the EMI (electromagnetic interference) stress within the requirements of standard IEC 255-4.

3. System Test :
The total processing system is tested including electromechanical control cubicle, secondary wires with shielding, and earthing system connected to the substation. After installation it is tested by performing typical switching operations. To limit the number of switching device operations (switching device ageing!), the switching status of each device is once checked in the input mailbox of the corresponding feeder-level processor. Then a test unit with inputs and outputs is connected instead of the process interface. Correct wiring (static test) and operation of the total system (dynamic test) are then checked.

CONCLUSION

It has been shown that the use of digital processing systems for interlocking allows a topology-based approach which would be entirely unrealistic for electromechanical relays. However, it is feasible to solve interlocking along this line with powerful microprocessors of the latest technology. Their implementation in a 765 kV GIS has been outlined which fulfils both real-time and security requirements.

The most significant points of the presented method can be summarized as follows:

1. Problem decomposition into rules and configuration :
The consequent decoupling of interlocking rules and substation configuration allows to develop and to test programs which are independent of a single line diagram and which, therefore, can be reused for any known substation configuration. The actual single line diagram is entered as setting values or input data. Future substation extensions require nothing but adapting the setting values.

2. Structured rules :
The structuring of the interlocking rules into generally valid and utility-dependent groups makes it possible to tailor the interlocking system to the specific operational philosophy of a project by simply marking the relevant utility-dependent rules. Analogous arguments hold for the maintenance of switching devices.

3. Topological elements :
The interlocking rules are expressed by relations between topological elements which represent switching states of the substation. Since the switching states are dependent upon the performance of the switching devices, alternative properties like circuit breakers with/without surge withstand capacity or busbar isolators with/without busbar current carrying capacity can explicitly be considered.

OUTLOOK

The proposed interlocking approach includes the potential for future extension to switching sequences with objective function(s), e.g. to minimize the number of switching operations [2], to minimize the sum duty of all isolators upon on-load busbar transfer [3] and so on. For these tasks the actual sequences are the result of decision-making as opposed to automatic switching sequences. In artificial intelligence, this feature is referred to as an expert system.

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