6.101 Analog Electronics Final Project Report
Variable Power Supply

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Abstract

Our final project is an attempt to integrate two different charging ports (Standard USB 2.0, 3.0 and USB-C) into a shared switching power supply. An efficient and safe buck converter was built to charge devices. Our finished project is capable of providing up to 20 Volts DC to a device. Our goal was to provide three possible output voltages of 5, 12 and 20 Volts to power various devices and provide up to 3 Amps of current as well. Most importantly, the system would detect the voltage based on the device plugged in and provide the appropriate voltage to charge it. The system did not successfully act as an autonomous charger, in terms of detecting devices and switching the output voltage appropriately. There were various problems with noise, parasitics, and component issues that prevented us from fully integrating the various parts of the project. Our project ultimately accomplished a variable duty-cycle power supply capable of powering everyday devices.

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1. Introduction

With the release of the 2016 MacBook, Apple realized and implemented the concept of providing universal ports that handle not only power but as well as data using the USB-C standard for laptops. The new USB-C standard enables consumers to power devices ranging from smartphones to laptops up to 100 watts, using the same reversible cord.

For our final project, we attempted to design and construct a variable power supply brick that implements the USB power specifications. The finished prototype accommodates both the standard USB 2.0 and 3.0 as well as the USB-C variation by providing different ports such that the different USB standard cords can be used to power devices. Using design concepts from the class, we maximized power efficiency, minimized power losses, and provided device protection.

Eswar was responsible for buck converter design, step down transformer, bridge wave rectifier circuit, and testing of these modules. Lokhin was responsible for device detection, switching, and feedback.

2. Overview (Lokhin & Eswar)

This power electronics project attempted to accommodate both the ubiquitous USB 2.0, USB 3.0, and the USB-C standards. USB 2.0 and USB 3.0 have no distinguishable differences in the power provided; both protocols utilize a power supply of 5 volts at a maximum of 2 amperes.

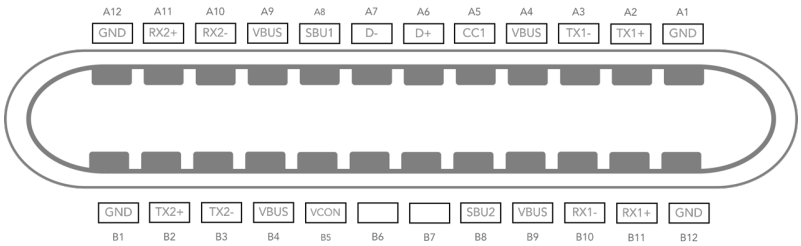

Figure 1. USB Type-C Connector Pin Diagram

However, the new USB-C implementation introduces a 24 pin, fully reversible plug connector that not only allows just transfer of energy but also data. Figure 1 refers to the pinout diagram of the USB-C 24 pin plug. USB-C uses a system of profiles, to identify each device, allowing the host to supply safe and appropriate voltage depending on the device.

In the USB-C power profile specification (Figure 2), five power configuration profiles exist to serve electronics with different power requirements. Due to power constraints and considerations to safety, we did not attempt to implement Profile 5, a 100 watt power supply.

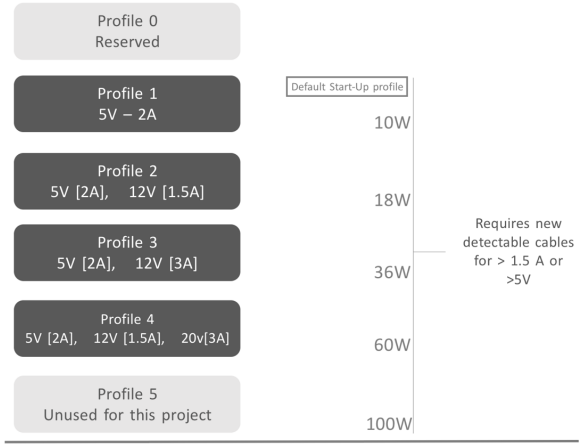

Figure 2. USB Type-C Power Profile Specifications

If a device with a drained battery is connected to a USB-C power supply, the circuit will first attempt to provide enough power to turn on the device using the safest and lowest power profile, 5 volts at 2 amperes, common among the USB 2.0, USB 3.0 and USB-C circuits. Once the device is powered, it can communicate to the circuit which profile is appropriate. This information is accessible via the Configuration Channel (CC) pins, in which current advertisements and power profiles can be deduced using an integrated chip solution.

3. Block Diagram

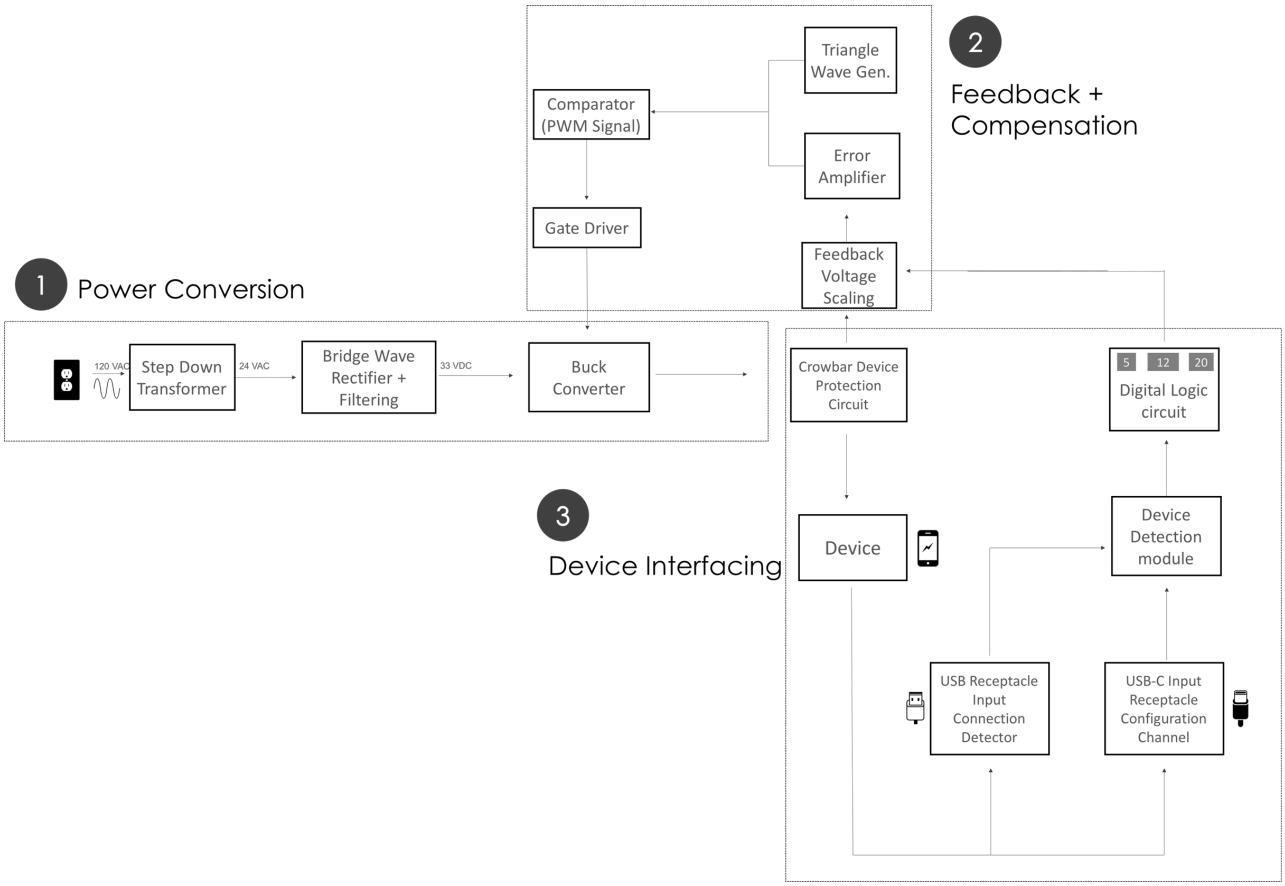

Figure 3: Block-Diagram of system

The block diagram can be broken up into three fundamental subsections. First is power conversion and the actual stepping down of the line voltage and conversion to DC. Second is the feedback loop and error compensation which creates the switching element of this switch mode power supply. The third component is device interfacing which involves device detection, device protection, and directly providing power to the device or load.

4. System Design[1]

From the 120 volts AC wall outlet, a transformer will be used to step down to safe 24 volts AC output. The project will use the 24 Volts to provide variable power and current based on the connected device. A buck converter will be used to provide variable voltage. Digital logic and an integrated chip will be used to signal a change in desired voltage to the circuit which will adjust voltage. The default circuit provides the safest profile of 5 v if no information is known. A crowbar circuit will be used to provide a layer of device and consumer protection, and the output voltage will be used to power the device. In any power electronic circuit,

[1] A full circuit view can be found in the Appendix

feedback is crucial to provide the appropriate voltage and current. A PWM (Pulse Width Modulation) circuit will be used to provide feedback control of the buck converter. A switching circuit will be driven by the the PWM to control the switch mode power supply.

4.1 Line Voltage to DC Rectification (Eswar)

The first stage in our power supply is to step down the line voltage (120V). Due to safety concerns, the line voltage was stepped down to 24VAC with a transformer. The second step rectifies the alternating current to convert the voltage to DC. This was done using a high powered bridge wave rectifier with a filtering capacitor. The filtering capacitor was chosen to eliminate as much ripple as possible on the DC output. The output of this first stage of is a 34 Volts DC supply.

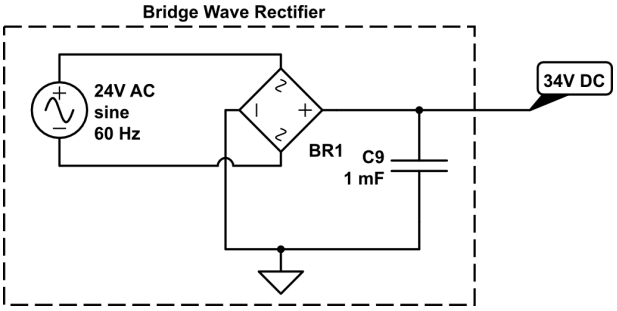

Figure 4. Filtered Bridge wave rectifier

4.2 Buck Converter (Eswar)

The 34 volts DC must be stepped down to appropriate voltages for the connected device. A buck converter was used to step down the voltage. Depending on the device, different voltages will be needed. We will be controlling the characteristics of the switching of the Buck converter to control the output voltage. Initially we planned on using a flyback converter, however various difficulties with that caused us to switch to a buck converter.

The primary problem with a flyback converter is winding a custom transformer. Much of the knowledge about winding custom transformers is difficult to find, and there are multiple ways to calculate the math behind the values. Despite vast numbers of application notes and guides online, almost none explain the reasoning behind the calculations causing much confusion. Numerous approximations and assumptions were made without explanation. A second complication with winding a transformer is inherent human error. Hand winding transformers can affect various parameters of the transformer usability and result in an unusable transformer. After we spent significant amounts of time designing and winding transformers, we decided to switch to a simpler buck converter. While it is not as complex as the flyback, the buck still has all the functionality that we wanted and is controllable in the same manner. There is no need for isolation, separate power supplies, and the difficult transformer. Removing this complexity and designing a well-known buck converter was the right choice to make.

The buck converter is a switching power supply design which is very similar to the flyback converter. The buck converter can step down input voltages and the output voltage is a function of PWM duty cycle.

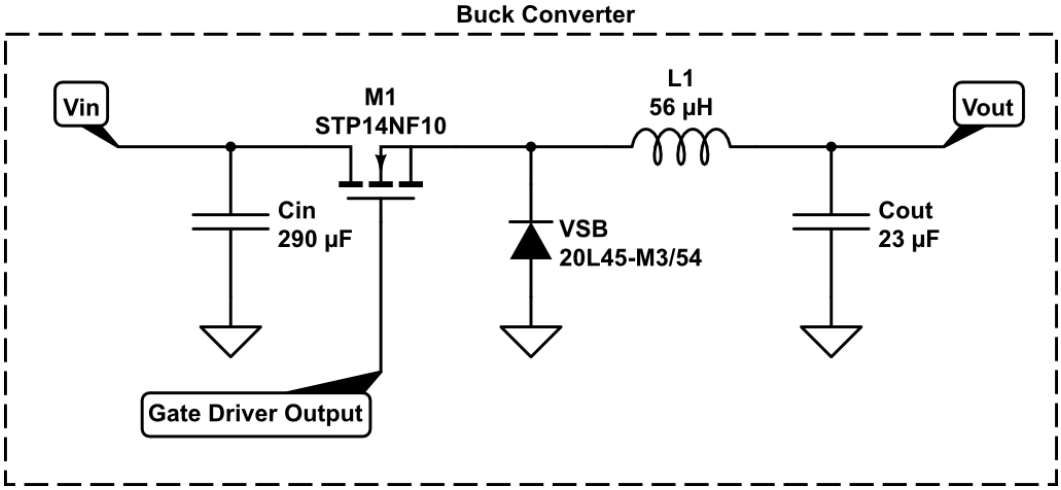

Figure 5: Buck Converter design

To design the actual buck converter, there are a few key components must be specified. The buck converter consists of an inductor, PWM switch, diode, and capacitors. To understand the operation of the buck converter, there are two modes of operation: the MOSFET switch is conducting or it is off. The diode will be reverse biased during the on state. During the off state, the diode will be conducting and preventing any back-EMF from the inductor. Additionally, the output seen by the load should be approximately a flat DC voltage. The output capacitor removes any ripple voltage and ensures that the output is a clean DC voltage.

The inductor is specified using predetermined input and output voltages, switching frequency, and current draw. Selecting the inductor is the first step in the design process. Next, a suitable PWM drive is needed. This is specified accordingly to the power rating needed and the switching frequency. A power MOSFET is needed because it is a high side switching element. The diode is specified according to the maximum reverse bias voltage required. The capacitors are sized with ESR(Equivalent Series Resistance) and ripple voltages in mind.

We made some assumptions before proceeding with the final design. These are the design parameters that were settled on for each output profile:

Profile	Duty Cycle	I_{ripple} In	V_{ripple}	I_{ripple} Out
5V, 2A	0.1515	1	0.05	0.6
12V, 3A	0.3636	1.5	0.12	0.9
20V, 3A	0.6061	1.5	0.2	0.9

Table 1. USB Design assumptions and parameters

The duty cycle is a direct function of the output and input voltages. The input ripple current was chosen as an estimate to be half of the load current. The ripple voltage was chosen to be 1% of the load voltage. The output ripple current was chosen to be 20% of the load current. Since the power supply required variable output the maximum of these values was chosen.

Based on the three voltage-current profiles we designed buck converters and bought three varying inductors. The table below shows the three possible designs.

$v_{in} = 34\,Volts$	$v_{in} = 34\,Volts$	$v_{in} = 34\,Volts$
$V_{out} = 5\,Volts, 12\,V, 20\,V$	$V_{out} = 5\,Volts, 12\,V, 20\,V$	$V_{out} = 5\,Volts, 12\,V, 20\,V$
$I_{load} = 3\,Amps\ at\ max$	$I_{load} = 3\,Amps\ at\ max$	$I_{load} = 3\,Amps\ at\ max$
$Fsw = 156kHz$	$Fsw = 550\,kHz$	$Fsw = 330kHz$
$Inductance: 56uH$	$Inductance: 17uH$	$Inductance: 27uH$
$C_{out}: 23uF$	$C_{out}: 8uF$	$C_{out}: 12uF$
$C_{in}: 300uF$	$C_{in}: 90uF$	$C_{in}: 140uF$

Table 2. Three possible designs

Since overall size was not an immediate concern for, we eliminated the factor in our decision making. The capacitances as well as switching frequency were important parameters. Since the specified switching frequencies are minimum values, we wanted to choose the lowest one to prevent switching losses and problems with MOSFET gate capacitances resulting from high switching frequencies. Secondly, we wanted the largest input and output ripple capacitors since the larger capacitors have lower ESR. Lower ESR is very desirable in converters since the resistance leads to efficiency losses. Thus based on these parameters the left most column with the largest inductor value of 56µh, was chosen.

4.3 Device Detection(Lokhin)

In a variable power supply, automated detection of the device is desired. Based on device connected to the receptacle, the power delivered will be appropriate for that device. The appropriate power is determined by the USB-C power profile communicated by the device to the final design circuit. This requires the design to accommodate detection of various USB-C devices and different power profiles. Once the USB-C device is plugged in and its power profile is determined, the circuit must be able to switch from one power profile to another to accommodate a new load. The device detection module contains three components

that work together to determine a USB-C power profile, to signal to the buck converter and PWM that a new output voltage is desired, and deliver that power to the device.

I. USB, USB-C Receptacles and Breakout Boards

In order to conveniently access the small pins that are located within the USB-C's and USB's port, breakout boards are needed. By using breakout boards, the small pins in the ports are now accessible on the breadboard, enabling easier access to the receptacles. The boards that were purchased for this project included a male USB-C breakout board and a female USB breakout board, with the USB receptacle mounted on the top of the board.

The breakout board and the USB receptacle are responsible for two roles within the final design. The first role involves device detection. Once a device is plugged into the USB-C port, its power profile can be revealed by its CC1 and CC2 pins. A chip purchased from Texas Instruments is used to determine the power profile, which will be described in the next section. No device detection is required for the USB port because the chip automatically defaults to the lowest USB-C power profile, which is coincidentally the power that a USB 3.0 requires.

The second role the receptacles play in the final design is to charge the device. The USB breakout board and receptacle can handle up to 5V 2A, defined in the USB specifications. The USB-C breakboard theoretically can handle up to 100 watts of power as determined by the USB-C specifications. However, 100 watts was not tested in practice for this final design.

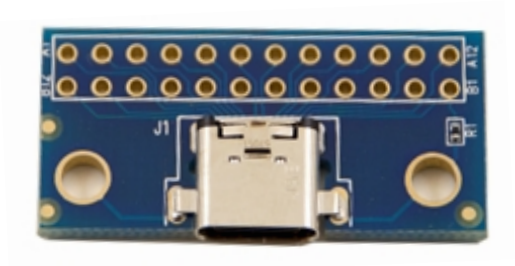

Figure 6: USB-C breakout board receptacle

II. TUSB321 Chip

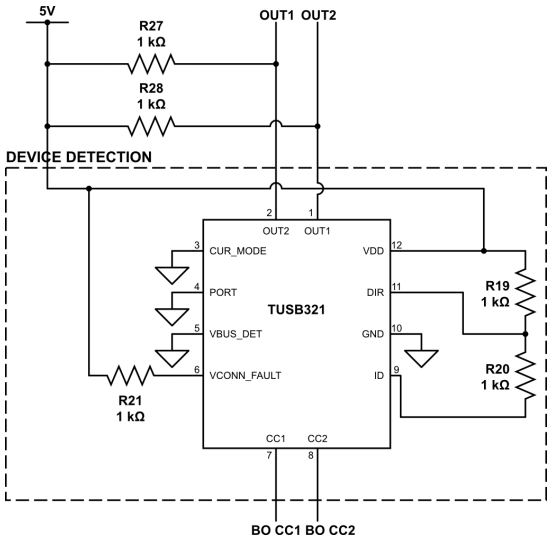

Figure 7. TUSB321 Device detection chip

Once the USB-C device connects to the breakout board, pins A5 and B5 can be accessed to determine its power profile. These two pins are known as the Configuration Channel pins, which are used by the device to communicate what power profile is appropriate for the device. However, the information at the CC1 and CC2 pins are difficult to decipher without the use of an integrated chip. Conveniently, the TUSB321 chip was purchased so the CC1 and CC2 pins can be deciphered into logic.

The TUSB321 chip can be configured as a upward facing port (UFP) or a downward facing port (DFP), which corresponds to a sink or a source. When the device is first plugged in, the desired state is DFP, because the power profile information from the device is needed. However, after the power profile of the device is determined, the desired state is UFP (source) to provide power to the device. Consequently, the TUSB321 chip enables switching between the UFP and DFP states.

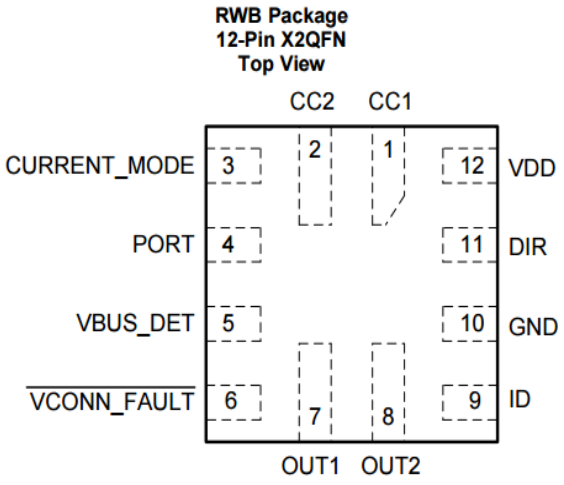

Figure 7: TUSB321 Package

The inputs to the TUSB321 chip are V_{DD}, which is 5V, the CC_1 and CC_2 obtained from the device via the USB-C breakout board. The primary outputs used in the final design from

the chip is OUT_1 and OUT_2. The OUT_1 and OUT_2 pins will either be high (approximately V_{DD}) or low (0.4 V), depending on which power profile the device advertises to the chip. The logic possibilities are described in table 3. Since these outputs are open drain, a pull up resistor to V_{DD} is required to receive the correct outputs. OUT_1 and OUT_2 are then put through logic gates, which will be described in the next section, to determine what output voltage the buck converter will operate at for the device.

Unfortunately, this chip was not implemented in the final design. Several reasons contribute to the omission of the TUSB321 chip. Due to the obscured package of the chip (X2QFN) and its extremely small size, no premade breakout boards were available. We designed our own PCB breakout board in Eagle CAD. However, we hit a roadblock when the traces were far too small for a CNC mill to etch. Then, we considered chemical etching by painting a sheet of copper and etching a negative trace using a laser cutter. Unfortunately, the extremely thin traces required for the chip still were problematic and was not possible to chemical etch properly. Finally, we had the board professionally fabricated. For our project, the actual power supply was a more significant component than the device detection. As such, we focused our attention primarily on creating a variable power supply first, and were unable to integrate the chip/device detection in the end.

Type-C CURRENT		UFP of DRP acting as UFP Current Detection
Default:	500mA – USB 2.0 900 mA - USB 3.1	OUT1 = High, OUT2 = Low
Medium – 1.5 A		OUT1 = Low OUT2 = High
High – 3A		OUT1 = Low OUT2 = Low

Table3 . TUSB321 configuration channels

III. Digital Logic Gates and Feedback Resistor Network

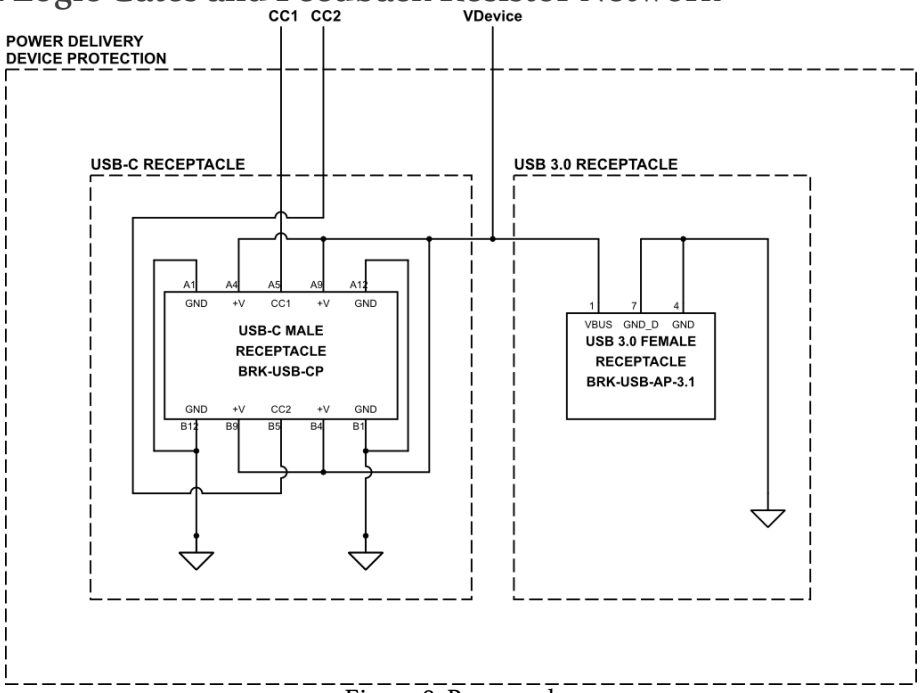

Figure 8. Receptacles

Now that the OUT_1 and OUT_2 are accessible from the device via the TUSB321 chip, digital logic circuits are needed to process the information at OUT_1 and OUT_2 to map the permutations of high or low logic to different output voltages. Since OUT_1 and OUT_2 only provides current information, the mapping between current to voltage is needed to go from the current advertisement of the CC pin goes to determine the output voltage to the device. Coincidentally, each level of current corresponds to each level of voltage. Consequently, each logic circuit was created for a high voltage (20V), a medium voltage (12V), and a low voltage (5V). The following logic tables for the three different voltage levels are described below.

HIGH VOLTAGE (20V)			MEDIUM VOLTAGE (12V)			LOW VOLTAGE (5V)		
OUT_1	OUT_2	OUTPUT	OUT_1	OUT_2	OUTPUT	OUT_1	OUT_2	OUTPUT
0	0	1	0	0	0	0	0	0
0	1	0	0	1	1	0	1	0
1	0	0	1	0	0	1	0	1
1	1	0	1	1	0	1	1	1

Figure 2. USB Type-C Power Profile Specifications

In the final design, 7400 series gates are used because such chips were available in lab. Furthermore, the V_{OH} is greater than 4.0 V, which satisfies the V_{GS} of the MOSFETs used to create a resistor network that is fed to the input of the PWM. The resistor divider network formed by power MOSFETS will be described in the next section, under Pulse Width Modulation.

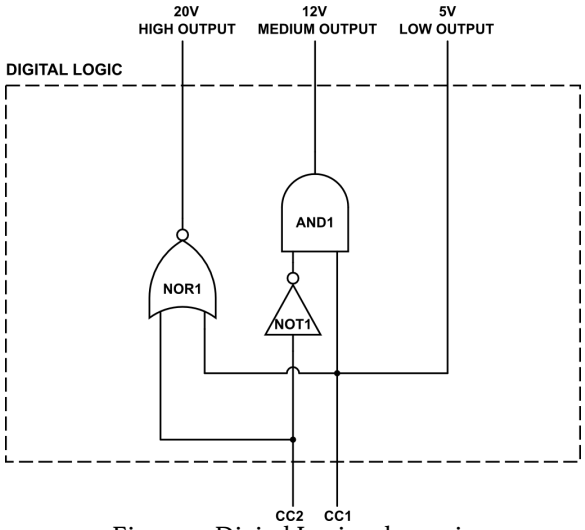

Figure 9. Digital Logic schematic

4.4. Feedback & Switching (Lokhin)

In any power electronics project, feedback is paramount to ensure that the circuit is providing the correct power to avoid damaging the device by overloading it with excessive power. Furthermore, the final design's output power is restricted in terms of voltage and current as specified by the USB-C and USB specifications. Due to the switching mode characteristics of the buck converter, the duration of the on states, referred to as the positive duty cycle, of the MOSFET dictates the output voltage. The feedback loop and compensation adjusts the output voltage when the load is switched to a different profile. Since the output voltage of a buck converter is a function of its positive duty cycle, a switch to a higher power profile requires a greater positive duty cycle. Conversely, a drop to a lower power profile requires a lower duty cycle. Consequently, feedback is not only crucial for device protection but also plays an important role in switching from one power profile to another. In the final design, feedback is modularized into multiple components which work collectively to ensure the correct power is at the output at any time. The entire feedback module consists of a feedback resistor network, error amplification, pulse width modulation, and a gate driver.

i. Feedback Resistor Network

Since the final design is a variable power supply, the feedback module must be able to correctly rectify any disturbances on the output of the circuit, regardless of whether the output voltage is 5V, 12V, or 20V. Traditionally, a comparator is used to determine whether an input voltage is higher or lower than the reference voltage. However, for variable power supply, a more complex network is needed to bring voltages from 5V, 12V, and 20V to compare against a single reference voltage.

The reference voltage was determined to be approximately 2.5V, typically half of the minimum output voltage, which is approximately 5V at the lowest USB-C power profile. To achieve the reference voltage of 2.5V, a shunt regulator powered from the 34V DC rail was used. This reference voltage will only be used in the feedback module. Since the reference voltage was chosen to be 2.5V, the variable output voltages must be divided down to approximately 2.5V to compare output voltages against the reference. The following resistor values were chosen to achieve a ratio of approximately 2.5.

The feedback resistors will vary, dependent on which power profile the circuit is operating in. Consequently, the logic that determines the USB-C power profile in which a device requires is used to drive n-channel MOSFETs. When the MOSFET is turned on, a resistor is connected to ground, creating a voltage divider the brings the output voltage to roughly 2.5V, called scaled V_{OUT}. This scaled V_{OUT} is used to compare against the 2.5V from the shunt regulator.

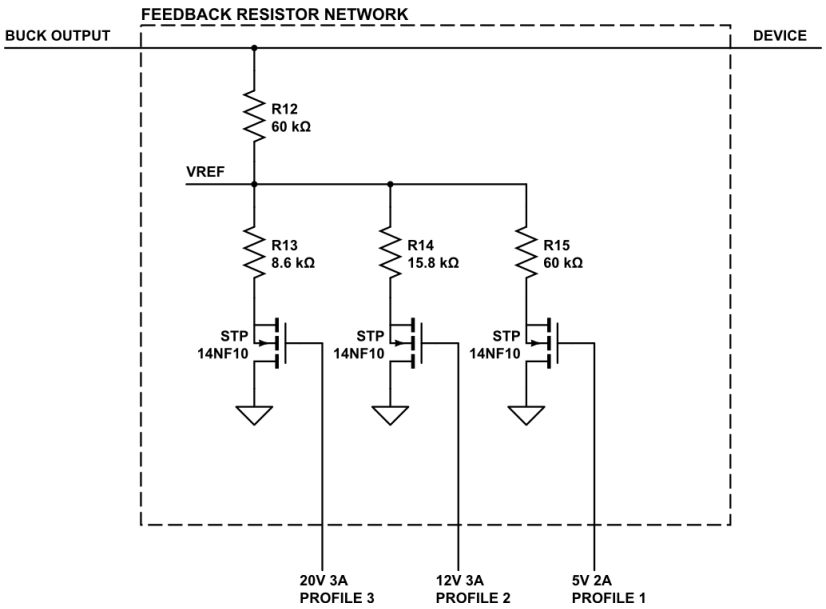

Figure 10. Feedback resistor network

Due to the resistor divider network, the power through the MOSFETs at the feedback resistor stage is relatively low. Consequently, the resistors and MOSFETs specifications do not need to meet high power standards. Power MOSFETs to be safe even though high power should never occur across the feedback resistor network.

Some potential issues arise due to the configuration of MOSFETs. Although the configuration channel logic prevents multiple MOSFETs to turn on in steady state operation, it is possible for multiple MOSFETs to turn on when the load is switched. Once a load is switched, the configuration channel logic driving the gates changes. It is possible that in the process of switching from one MOSFET to another MOSFET, propagation delays results in two MOSFETs in the on state for a small amount of time. In the worst-case scenario, the parallel combination resulting from two resistors being connected to ground via two on MOSFETs

results in an incorrect scaled V_{OUT} for the output voltage. However, it is assumed that the propagation delay is negligible and the device protection circuitry will be able to rectify any spikes of voltage that results from two MOSFETs being turned on.

ii. Error Amplifier

The most common method to regulate voltage in power electronics is the use of Pulse Width Modulation (PWM). An error signal is generated from a comparison of the desired voltage and the actual voltage. This error signal is amplified and is then compared to a waveform in which its output is used to adjust the duty cycle of the switching MOSFET and thus, adjusts the output voltage. Consequently, three main circuit components constitute the Pulse Width Modulation module - the error amplifier, the triangle wave generator, and the comparator.

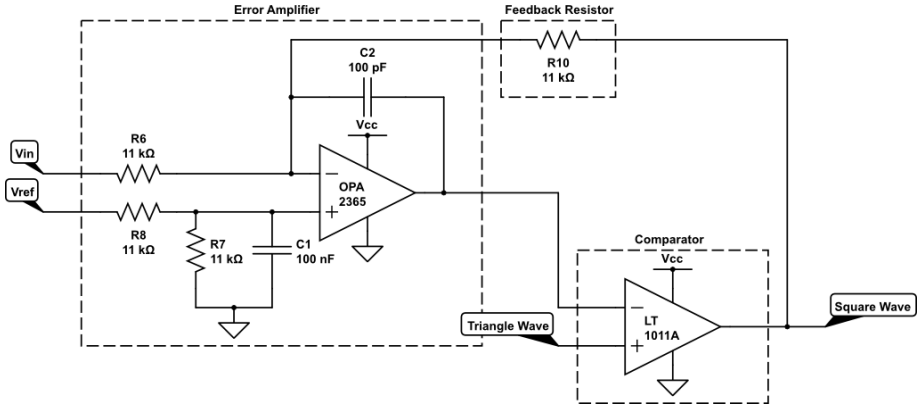

Figure 11. Error Amplifier Schematic

The error amplifier, through the 10k ohm feedback resistor from the output of the comparator, corrects any errors in the voltages that the comparator outputs. By selecting resistors R_6, R_7, R_8, R_{10}, the gain of the error amplifier is chosen to be one. Unity gain is desirable because any gain in the error amplifier would misrepresent the actual error present in the scaled V_{OUT}. Consequently, a 2.5V DC offset is added to the output voltage because the triangle wave used as comparison in the next section is also has an offset of 2.5V. Since there are no negative rail supply voltages in our circuit, an offset was required. Therefore, a 2.5V DC offsets enables all the operational amplifiers in the PWM to be powered with 0V and 5V rails. As a result, the final output from the comparator is a rail-to-rail square wave going from 0V to 5V.

iii. Triangle Wave Generator and Low Pass Filter

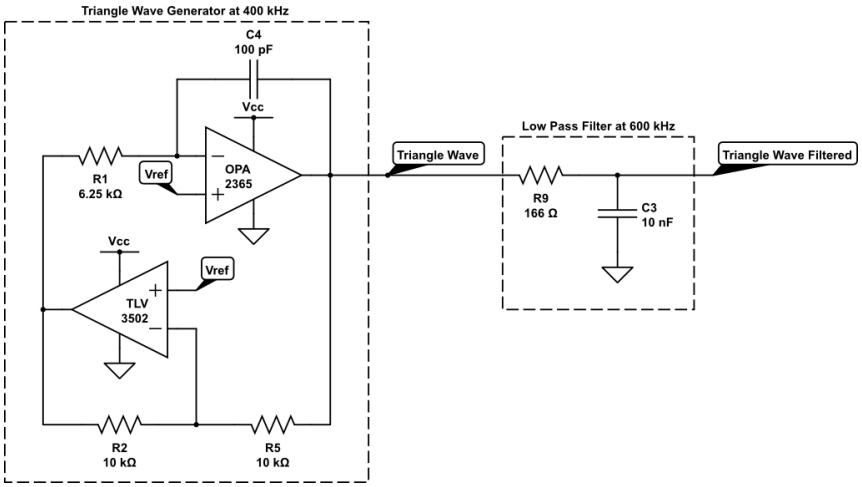

Figure 12. Triangle Wave generator

Typical applications of pulse width modulation use a triangle wave as comparison against the error signal. Consequently, a triangle wave must be generated for the PWM to function. Most triangle waves are generated by the constant charging and discharging of a capacitor. In the final design, one operational amplifier and one comparator (OPA2365 and TLV3502) are used to generate a triangle wave. The operational amplifier in the circuit is used as an integrator. When the comparator output is low, the output of the operational amplifier increases linearly. When the comparator output is high, the output of the operational amplifier decrease linearly. As the output of the operational amplifier crosses the point of the reference voltage, 2.5V, the comparator output voltage changes. This circuit configuration results in a triangle wave as an integrated square wave. As the reference voltage is passed by the output of the operational amplifier, the slope of the triangle changes from positive to negative, generating a triangle wave. Again, since the circuit is designed to be powered from a single 5V supply rather than a bipolar supply, an offset of 2.5V was added to the triangle wave, consistent with all other components in the PWM module.

The frequency in which the triangle wave is generated can be modified by changing the resistor values R_1, and C_4. Since the buck converter is operating a switching frequency of around 400 kHz, the triangle wave generator must also produce a 400kHz triangle wave.

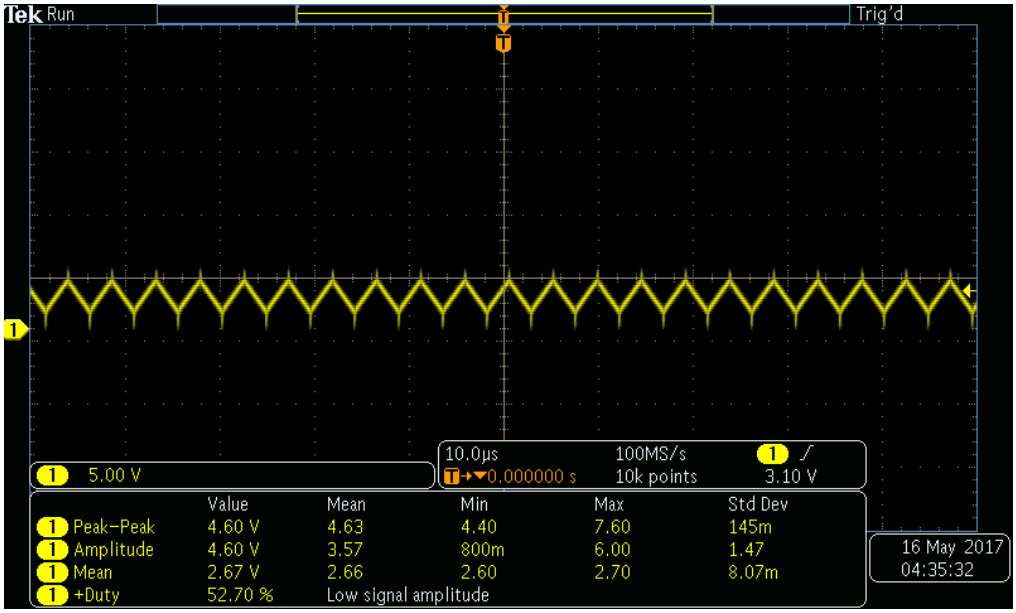

Figure 13. Triangle Wave Scope Shot

In theory, the triangle wave generated from the circuit should be adequate as a comparison against the error signal. However, in practice, the triangle wave seemed to be distorted at the peaks and contained distorted slopes. Consequently, the non-ideal triangle wave resulted in non-ideal output of the comparator. It was determined that a low pass filter should be used to filter noises and imperfections from the triangle wave. A low pass passive filter was used since an active filter will not only consume more power but would also require a bipolar power supply.

iv. PWM Comparator

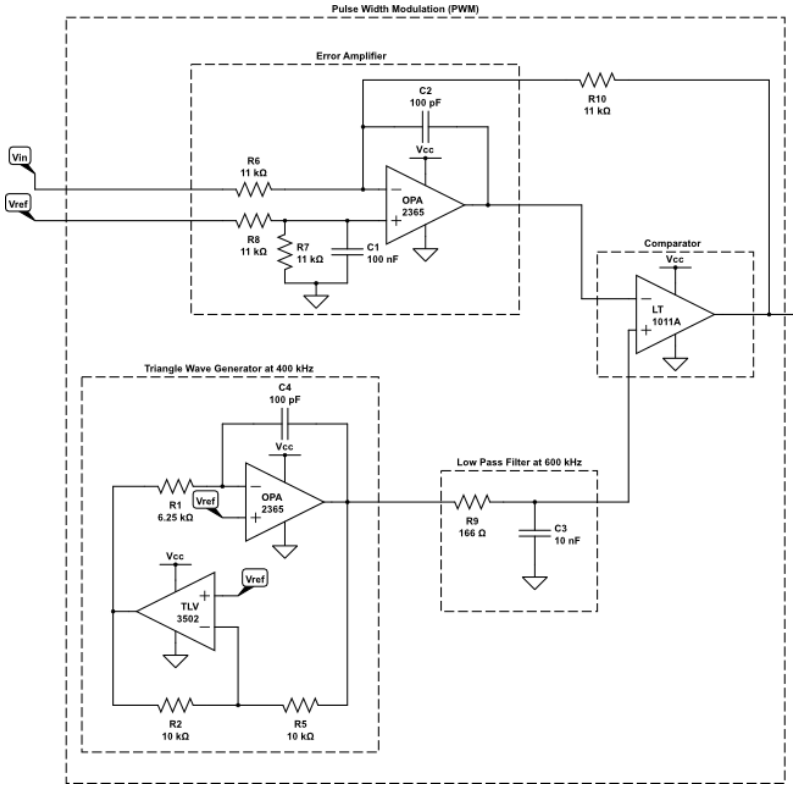

Figure 14. PWM Module

The final component of the Pulse Width Modulation module is the comparator. The comparator compares the error signal against the reference or expected voltage, and produces a rail-to-rail output square wave. The triangle wave is tied to the inverting (-) input of the comparator, while the error signal is tied to the non-inverting input. If the triangle wave voltage is greater than the input voltage, the comparator will output low. Conversely, when the triangle wave voltage is less than the input voltage, the comparator will output high. Since every signal in the PWM module includes a 2.5V offset, the comparator does not need a bipolar power supply to operate.

This simple comparator produces a square wave with varying duty cycle that changes depending on the input voltage. At a certain power profile, if the output voltage drifts higher than its reference voltage, the comparator output square wave will decrease in positive duty cycle, bringing the output voltage back down to the desired voltage. Consequently, if the output voltage drifts lower than its reference voltage, an increased duty positive duty cycle will restore the output voltage back up to the desired voltage.

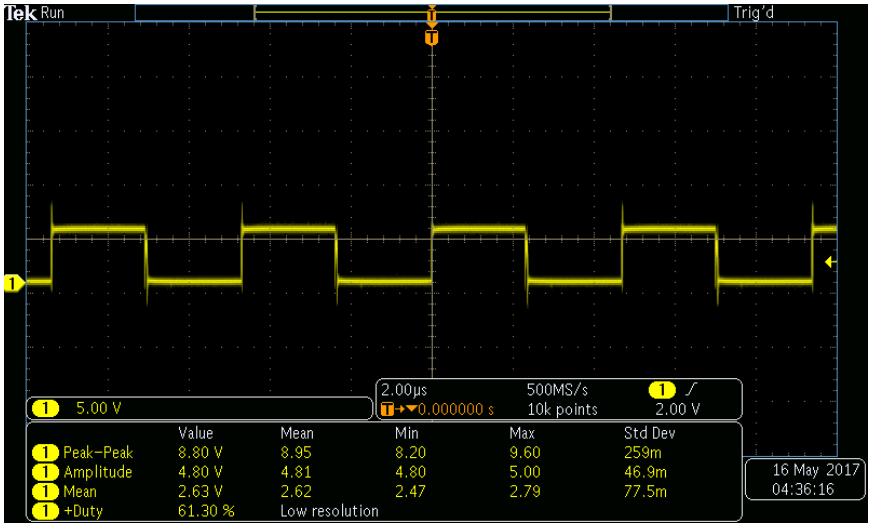

Figure 15. PWM Module Output

V. Component Selection

The components used in the error amplification component and triangle component of the Pulse Width Modulation module were required to meet crucial design parameters. Consequently, a typical operational amplifier such as the LM741 could not be used.

The comparator used in the triangle wave generator needs to have rapid switching, which is usually in a push-pull topology because it does not require a pull up resistor. Open drain topologies require a pull up resistor slowing them down. This allows the output voltage to rapidly pull down to ground, but slowly pull up to V_{DD} via the pull up resistor. Furthermore, the propagation delay of the comparator must be much less than the PWM waveform period to minimize the phase delay introduced by the comparator. Consequently, the TLV3502 comparator with a propagation delay of 4.5 nanoseconds in a push-pull output topology was implemented in the final design.

The amplifier used in both the error amplification and triangle wave generator also needs to meet specific design parameters. The slew rate and the gain bandwidth product of the operational amplifier must be considered in its configuration within the triangle wave generator. The slew rate, specified at an operating frequency of 400 kHz, must be greater than 3.4 volts/microsecond. The gain bandwidth product must be approximately 7.6 MHz, if the summation of 10 harmonics is sufficient to produce a triangle wave. At the 10th harmonic, the frequency is approximately 19 times the fundamental. The OPA2365 amplifier, with a bandwidth of 50 MHz and a slew rate of 25V/microsecond, was chosen.

The comparator used to compare the triangle wave and the amplified error is specified as an LT1011A. Initially the TLV3502 was used, but it was observed that output square wave of varying duty cycle from the PWM was extremely noisy. It was determined that the TLV3502 propagation delay of 4.5 nanoseconds was too quick, introducing noise into the output of the PWM. In order to reduce noise at the output, another comparator, LT1011A, with a slower propagation of 200 nanoseconds was chosen.

VI. Gate Driver (Eswar)

One concern with driving MOSFETS as switches at high frequencies is the MOSFET internal capacitances that exists between its gate and source, which lead to undesirable behavior. A high-side gate driver is used to drive the MOSFET gate with large currents to overcome the intrinsic capacitances.

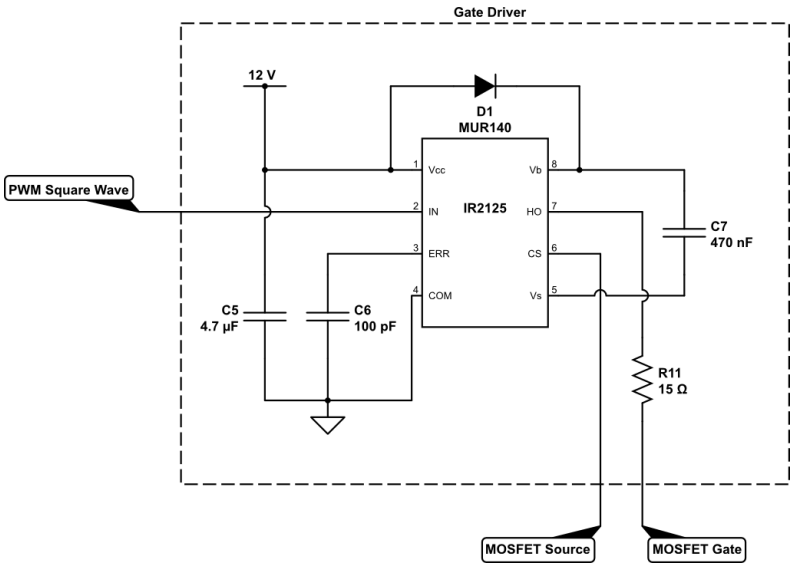

Figure 16. Gate Driver

A second challenge is the actual gate to source voltage needed to turn on the MOSFET. Referring to the buck converter topology, the gate voltage will need to go to a voltage higher than the source voltage, which is the 34V DC rail. By the definition of the threshold voltage, the voltage in which an inversion layer forms in the MOSFET to produce current, the voltage between the gate and source must be around 4V. Consequently, the gate, with reference to ground, voltage must be greater than 37V in order to turn the N-channel power MOSFET on. Since 34V DC is the highest voltage present in the power supply, it is difficult to provide a voltage higher than what is available to drive the N-channel MOSFET. A P-Channel MOSFET would be simpler to drive, but the efficiency losses are greater. Additionally, due to difficulty of finding a suitable high-side P-channel gate driver, the N-channel MOSFET was chosen with acknowledgement of greater difficulty.

To overcome the issue of a higher than rails gate voltage, a boot-strapping configuration is used. Bootstrapping is, in its simplest form, using a capacitor's charge storage characteristics to charge the voltage at the gate beyond the rail voltage. This provides enough voltage at the gate to turn the MOSFET on. In Figure 16 C_7 is the bootstrap capacitor. The bootstrap components were designed using three methods. First, bootstrap elements were designed for the steady state operation of the gate driver based on various assumed and required parameters. Second, the idle state operation is used to calculate bootstrap component values. Lastly, the calculations are completed for the maximum on-state operation. Based on all three of these calculations, the maximum capacitor and component values are chosen.

Several gate drivers were purchased but the gate driver that worked the best was the IR2125, which was already available in 6.101 laboratory. Furthermore, the IR2125 was through-hole and much simpler than other surface mounted integrated chips that were purchased.

A quick overview of the key components of the gate driver circuit shown in figure 16:

- ⇒ C5 is a bypass capacitor
- ⇒ D1 is a fast switching Diode
- ⇒ C7 is the bootstrap capacitor
- ⇒ R11 is a low value gate resistor over voltage protection for the gate driver

Designing and utilizing the gate driver was one of the trickiest parts of this project. There are various configurations and many parts are enigmatic and application specific. After scouring many application notes and documents, designing the gate driver circuitry was still experimental and difficult. Given more time, we would try to design a discrete gate driver, level shifter, and bootstrapping all-in-one circuit to avoid IC difficulties with the gate drivers.

Figure 17. Output of Gate Driver

5 Testing (Both)

Testing the circuit modules individually was straightforward and simple. Integration testing became much more difficult due to noise and distortion caused by one module feeding into the other. The first module to test was the input rectification and conversion. The transformer's $24V_{AC}$ output was bridge rectified and converted to $34V_{DC}$. This was easily tested by verifying the voltage at the output of the rectifier stage and also scoping the node to verify the expected waveform, with a fairly flat DC output.

To test the pulse width modulation (PWM) module, the triangle wave generator was first tested individually. A relatively clean triangle wave without much noise distortion at the switching frequency was desired. Scoping the output of the waveform, it was evident that there were blips at the switching points of the triangle wave. This can be attributed to the breadboards, non-ideal conditions, and parasitic capacitance. On a PCB, without the opportunities to introduce noise, a cleaner triangle wave is expected. As mentioned earlier, the passive low pass filter rounds out the 'blips' seen on the triangle wave to eliminate any invalid switching.

Next, the output of the entire PWM module was tested at the output of the LTIOIIA comparator. The desired waveform would be a square waveform with varying duty cycle and pulse width. A sine wave was used as the error signal to exaggerate the possible error resulted in a square wave with rapidly changing pulse width. A flat DC signal naturally produces a constant duty cycle in the square wave output.

The clean square wave output, when connected to an functional gate driver, becomes distorted. The output of the gate driver is also distorted, but was clean enough drive the MOSFET off and on.

Testing the buck converter individually, a perfect square wave was applied to the gate driver with its output driving the switching power MOSFET. Sweeping from low to high voltages, an output voltage matching the expected voltage based off the duty cycle of the input square wave was observed. A key insight was that using the gate driver and buck converter heavily distorted the square wave. Filtering and isolation would likely prevent this from affecting the circuit. However, the noise did not interfere with the operation and efficacy of the buck converter. Consequently, a design decision was made to focus on other aspects of the final design.

Integrating the PWM, feedback, and buck converter modules resulted in multiple problems. The designed feedback loop could not be stabilized and failed to obtain a clean signal to drive the switching power MOSFET. The noise accumulation and time delays posed a crucial problem that can only be rectified by redesigning the feedback loop itself.

After debugging and liberal use of bypass capacitors, we were able to obtain a constant and stable DC output voltage but were not able to do so with the completed feedback loop.

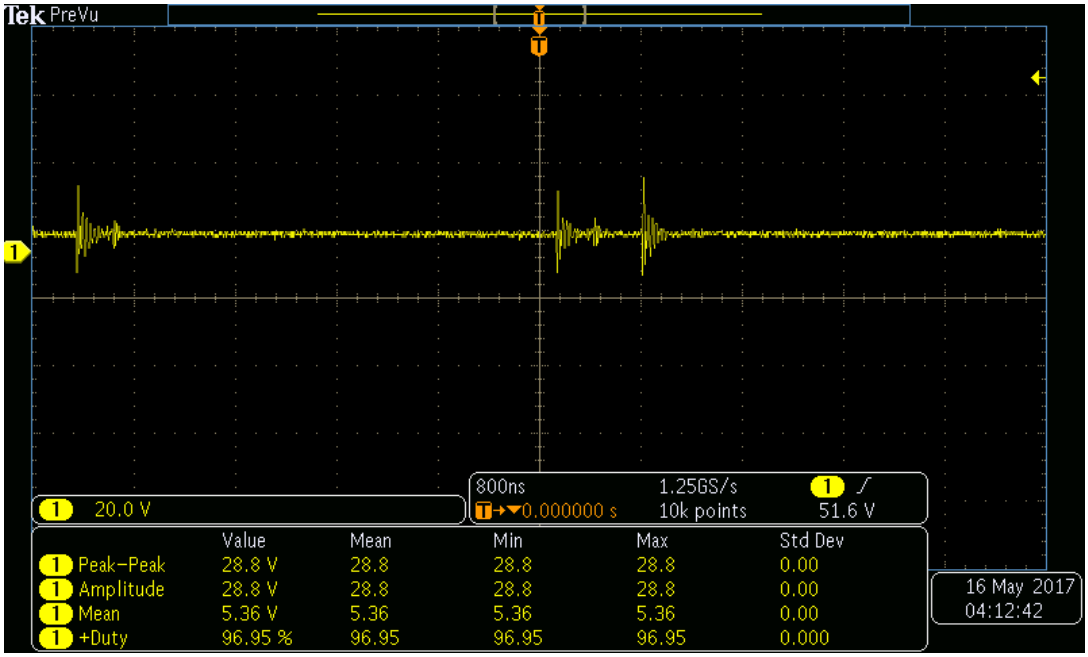

Figure 18. DC voltage output with minimal ripple

6 Conclusion (both)

In the end our project was able to power the lowest level devices and produced variable output. What we didn't accomplish was the autonomous switching and smart detection of devices. Secondly, we did not have the time to design and implement device protection. Despite not fully accomplishing all of our goals, we met many of them and designed a working variable power supply. There were some key challenges in this project. The first and foremost challenge was the need to buy high power rated devices for most of the components in our project. This inhibited our prototyping speed and caused delays in our project for specifying parts, ordering, and shipping. The second problem was the effect of parasitics and layout concerns which are inherent with power supplies. Power supplies are difficult to build on breadboards and there is no workaround to remedying this problem. The biggest issue and learning experience was to simplify the project as early as possible. Our initial design was a flyback converter and the inherent challenges and difficulties of that lost us valuable time. Switching to a simpler buck converter led to much better progress.

Given more time, we would fix our feedback loop stability such that we can use our device detection and autonomously switch output voltages based on connected device. We would implement more sophisticated device protection and PCB or solder all of the components for better reliability, performance, and efficiency.

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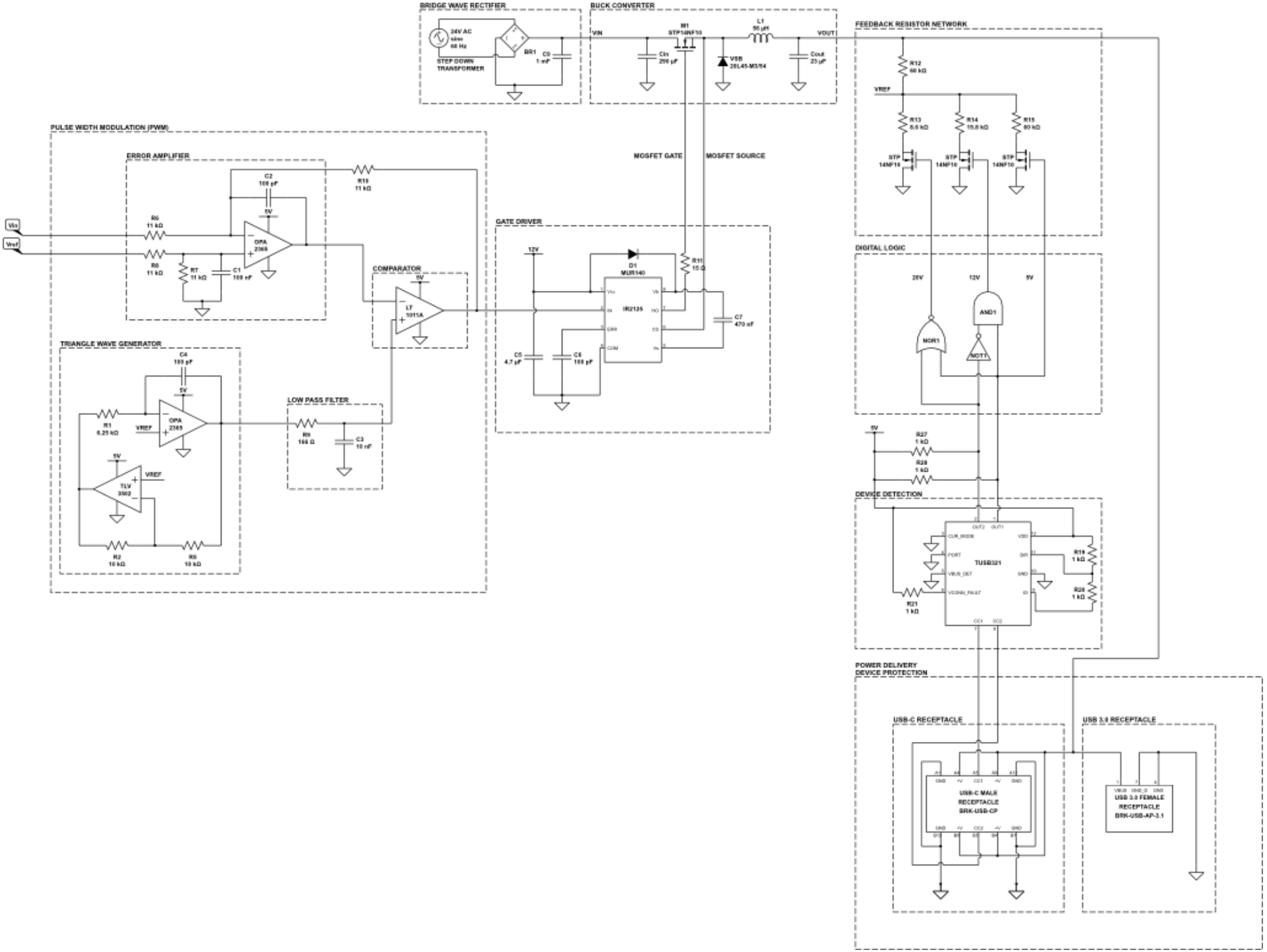
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ERROR AMPLIFIER
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100 pF
5V
R10
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IR2125
C7
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C5
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C6
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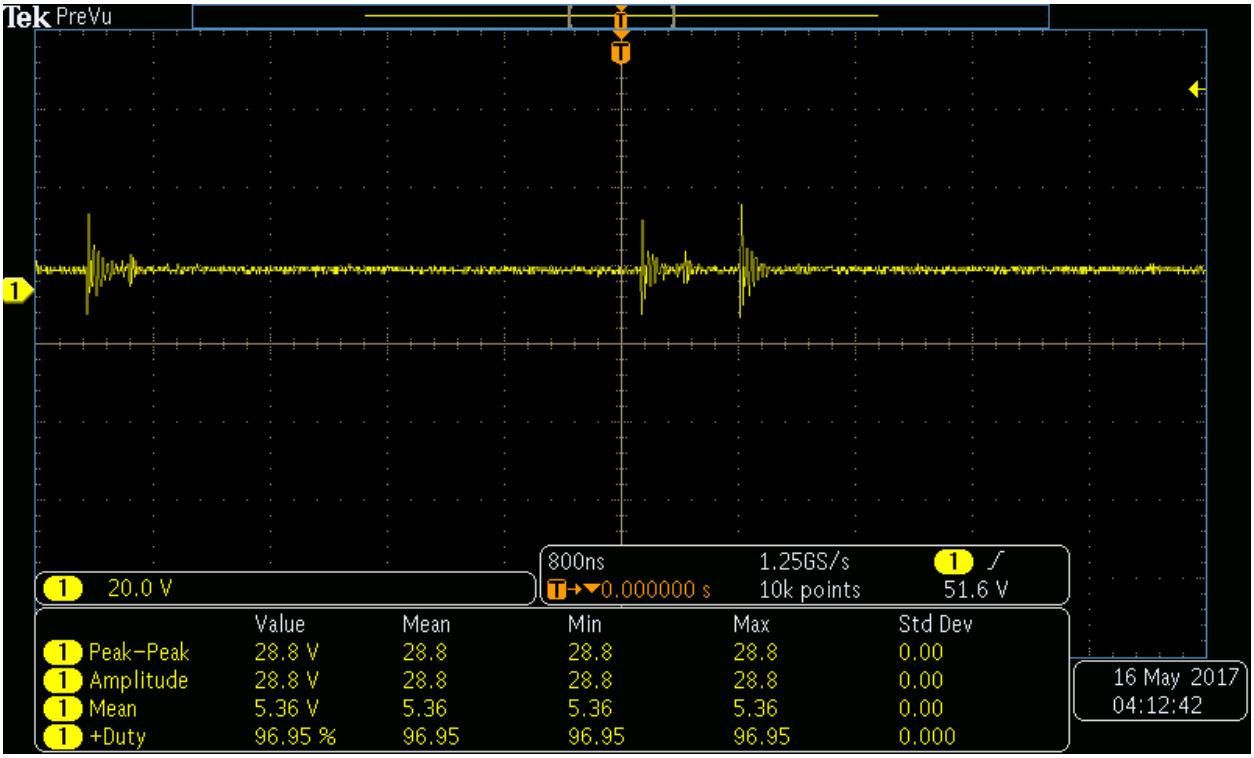
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