

# Hybrid Inverter System Design

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**Abstract:** The report hereby presents the design of a DC to AC hybrid inverter system. The inverter topology proposed is a five-level active NPC based inverter. The design as its a hybrid model aims to be implemented in both grid-tied and off-grid operating modes. At grid-tied instance the system synchronises the inverter AC output to the actual grid voltage such that they are in phase. At off-grid the system provides AC output for a specified AC load demand. The topology uses PWM switching states to drive the H-bridge MOSFET switches and establish a sinusoidal AC output power. A 1 kW hybrid inverter design procedure is presented with DC input of 400  $V_{DC}$  and a sinusoidal AC output of 230  $V_{rms}$  at 50 Hz frequency.

**Keywords:** SPWM,

## 1 INTRODUCTION

The application of multilevel inverter systems in power networks is extensive in commercial and industrial electrical power systems to convert DC power to AC power or vice versa. They have triggered increasing demand with the increase in electric vehicles and renewable energy technology as they are efficient in the conversion process. They are also used in uninterruptible to control and protect the flow of power in electrical networks and for active power filtering [1]. Therefore, it is important to develop high efficiency and quality inverter systems that can maintain power flow at the interface between DC and AC electrical networks with minimal losses and distortion in the desired sinusoidal AC output. Many multilevel topologies have been developed such as the neutral pointer clamper (NPC) topology that is presented.

In this design a 5L-ANPC topology with flying capacitors topology cascaded to an H-Bridge is chosen for the design. Multilevel inverters have revolutionised inverter design topology in medium voltage networks. The design aims to convert a steady 1 kW DC power at 400  $V_{DC}$  input from an external power supply to a AC output which is either grid-tied or off-grid. In grid-tied systems inverter are designed such that the AC output power generated is integrated and feed into an active grid with other active power supplies and

loads. In off-grid systems the inverter provides AC output power for a specified load demand with limited losses and noise. Therefore for an effective design it entail designing an hybrid inverter system that can operate in grid-tie and off-grid systems.

The report is structure as follows: section 2 discusses project background. Section 3 is literature review of content considered in the design. Section 4 discusses the design methodology and system modules. Section 5 discusses the inverter system model. Section 6 concludes the design discussion.

## 2 BACKGROUND

The project aims to design a hybrid inverter system that can produce sinusoidal AC output shape and characterise its performance at different specified operating instances. The general structure of the Inverter system is shown In block diagram shown in figure 1 bellow.

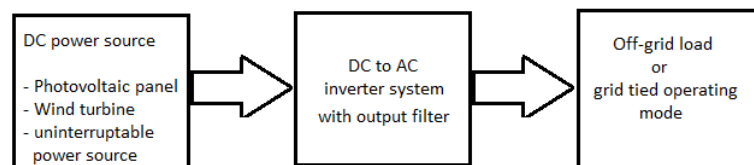


Figure. 1. Designed system structure showed in block diagram form with the main sub-systems.

### 2.1 Project Requirements

- This design project requires a 1 kW inverter design and supervisory control system that will be able to switch between the two modes of operation depending on conditions.
- Either the system is off-grid, therefore the inverter needs to act as a voltage source and a generate a stable supply to a specified output load (thus grid forming).
- The system is grid-tied into an active grid, therefore the inverter needs to operate as a current source injecting any PV power into the grid (grid tie).
- The designed inverter is to convert a steady 400 Vdc input at 1 kW maximum power from an optimised external Photovoltaic system.

- A 220/240 V sinusoidal shape AC output is desired at a frequency of 50 Hz, as this is standard voltages and frequency for domestic distributed electricity by Eskom in South Africa. The output power maximum is 1 kVA, as its dependent on the system input power supply and the type of output load.
- The System could operate in one of two modes. Where either the system is off-grid, therefore the inverter needs to act as a voltage source to a specified output load and to generate a stable supply (thus grid forming),
- The system is grid-tied into an active grid, therefore the inverter needs to operate as a current source injecting any PV power into the grid (grid tie).
- These two modes of operation require quite different characteristics in the control and operation of the inverters.
- The input over-voltage and under-voltage protection is to be implemented.
- The output under-voltage and over-current protections is to be implemented.
- A high efficiency design is expected with minimal losses and noise on the system output.

## 2.2 Assumptions

The supply to the inverter can be considered constant and the MPPT of the PV system need not be incorporated.

## 3 LITERATURE REVIEW

There is a wealth of knowledge and research pertaining to the development and optimization of inverter design. Reference [1] presents and compares the different design topologies of inverter system. The literature suggests that a five-level active neutral point clamper (5L-ANPC) multilevel inverter topology is more efficient. Therefore the 5L-ANPC topology is chosen for the design. Reference [2] discusses the design of an 5L-ANPC inverter type operated to give voltage level output that is optimised by cascading a flying capacitor and is controlled by switching states of power switches in the network. Reference [3] presents a grid tied inverter design and development procedure using a microcontroller based controller unit of the system. The system switching state are through SPWM signals that optimize ac average voltage level by varying SPWM active high duty-cycle. In Reference [4] the paper proposes a five-level hybrid topology combining features of neutral point clamped and flying capacitor Multilevel inverter. Though the system is to supply to a induction motor this is a viable load in the design presented here as the system is a medium to high power drive inverter.

## 4 DESIGN METHODOLOGY AND SYSTEM MODULES

A modular design topology is used where different modules of the overall design are investigated separately and merged for a fully functional system. Figure 2 shows the inverter system model which illustrate the different sub-modules in the system. The modules are each discussed in detail in the following sub-sections.

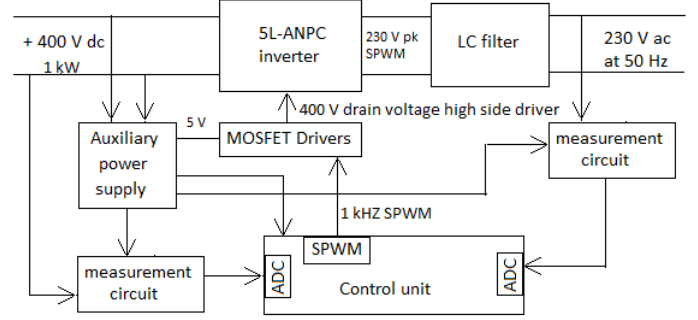


Figure. 2. Inverter system model is presented, which shows the sub-modules integrated to define the overall inverter.

### 4.1 DC to AC inverter

The module is comprised by the DC to AC converter. A 5L-ANPC topology with flying capacitors is chosen for the design. The model is an integration of Flying capacitor topology and NPC configuration [2]. The prototype inverter circuit diagram is shown in figure 3. The inverter is in full-bridge configuration with flying capacitors and an output LC filters. The operational principle of the inverter is achieved through switching cross corresponding H-bridge switches periodically to generate an alternating output at a controlled frequency, amplitude and shape (sinusoidal in this instance).

The proposed topology, as discussed in [2], has a parallel flying capacitor (FC) connected to the input dc bus voltage  $V_{DC}$ . A capacitor-fed H-bridge is cascaded to the FC. The voltage across the H-bridge capacitor has to be maintained at  $\frac{V_{DC}}{4}$ . The combination of switching states can produce voltage levels of  $0, \frac{V_{DC}}{4}, \frac{V_{DC}}{2}, 3\frac{V_{DC}}{4}, V_{DC}, -\frac{V_{DC}}{4}, 5\frac{V_{DC}}{4}$  at the output. However  $-\frac{V_{DC}}{4}, 5\frac{V_{DC}}{4}$  levels are not used as output is out of the required range. The capacitors are charged and discharged in any direction of the current for the voltages. The useful switching states of voltage levels are given in table 1 bellow. The corresponding switch pairs (S1 and S11), (S2 and S22), (S3 and S33), and (S4 and S44) are operated in complementary manner, where if S1 is on the switch S11 is off. The output voltage is based on the switching states that decide the path of the current flow.

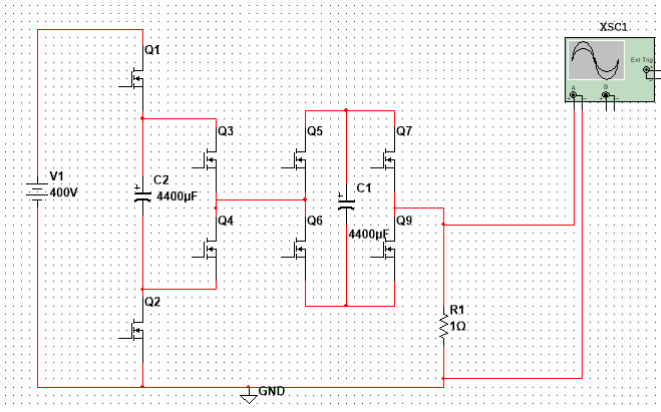


Figure. 3. 5L-ANPC inverter topology.

TABLE 1  
INVERTER SWITCHING STATES AND STEP VOLTAGE LEVELS

State no.:	Switches states (S1, S2, S3, S4)	Output
1	(0,0,0,0)	0
2	(0,0,1,1)	0
3	(0,0,0,1)	$\frac{V_{DC}}{4}$
4	(0,1,1,0)	$\frac{V_{DC}}{4}$
5	(1,0,1,0)	$\frac{V_{DC}}{4}$
6	(1,0,0,0)	$\frac{V_{DC}}{2}$
7	(0,1,0,0)	$\frac{V_{DC}}{2}$
8	(0,1,1,1)	$\frac{V_{DC}}{2}$
9	(1,0,1,1)	$\frac{V_{DC}}{2}$
10	(0,1,0,1)	$3\frac{V_{DC}}{4}$
11	(1,0,0,1)	$3\frac{V_{DC}}{4}$
12	(1,1,1,0)	$3\frac{V_{DC}}{4}$

The H-bridge topology is initially simulated in the build up to the 5L-ANPC topology. The H-bridge design principle using MOSFETs as switches are applied. IRF 440 mosfets are selected as they are high voltage mosfets with a 500 V maximum drain-voltage and high drain current characteristics. The tested circuitry is shown in figure 8 of the appendix. The test results are shown in figure 9. The SPWM generator circuit used for switching the mosfets is discussed bellow.

#### 4.2 Mosfet Driver

Mosfet driver circuitry is used in the design to gate-drive high-side and low-side mosfets to turn on and off. These are needed as they provide the required gate voltage. Different H-bridge high-side and low-side MOSFET driver ICs are available. The IR2110 is currently selected. The driver circuitry is still in design as only the low side drive output operates. However currently in designing the H-bridge, selecting switching mosfets and specifying the drive voltages, voltage controlled voltage sources where used

#### 4.3 controller module

The module represents the inverter control unit, as shown in figure 2. It is the core optimization controller and driver of the inverter switching

operations. It measures the operating state of the inverter (input and output voltages and currents) to control the inverter system modules. This is done according to the control algorithm required for switching control to produce the required PWM drive signal. This is implemented using a PWM control circuit. The subcircuit block is labled PWM-GENERATOR as shown in figure 4 in the appendix. The block is designed to provide the required PWM signals for switching operations of the inverter H-bridge that emulate AC sinusoidal output. The PWM-GENERATOR internal logic circuit diagram is shown in figure 5, that is shows the logic control circuit used to produce the PWM control signal per switch pair (S1, S2, S3, S4) of the 5L-ANPC inverter. The output PWM signals are shown in figure 6.

The pulses are produced periodically from switching state 1-12 shown in table 1 emulating half cycle of the sinusoidal output as the step voltage changes for  $0 - 3\frac{V_{DC}}{4}$ . The second half cycle is produced by switching state from 12-1 in reverse such that the step voltages changes from  $3\frac{V_{DC}}{4} - 0$ . The periodic pulse changes are controlled by an up/down counter block designed. The counter internal circuit diagram is shown in figure 7.

#### 4.4 Filter

The output filter is fitted to **convert** high frequency noise of the modulated AC output to a sinusoidal shape AC output at fundamental frequency of 50 Hz. Therefore the filter cut-off frequency is of the filter is chosen to be higher at  $\pm 500$  Hz. This also surves as an electromagnetic field interference filter to improve output shape and reduce ringing.

#### 4.5 Protection circuit

The external protection circuit of the system consists of input relay trip switches for over-current and over-voltage fault protection that protects the inverter. It is triggered by the controlling unit which sense these fault conditions. The output side of the inverter is protected by the controller unit which drives the inverter circuit off by switching the MOSFETs H-bridge to an open circuit state when a fault is detected.

#### 4.6 Auxiliary power supply

The auxiliary power supply works independently of the inverter input power supply to source system module components such as the micro-controller, operational amplifiers, MOSFET driver ICs. The Auxiliary power supply unit is shown in figure 3 with the corresponding connection to the sourced components sourced by the auxiliary power supply. The power supply is essentially a DC to DC

converter that can step down input  $400 V_{DC}$  to the desired low voltage of  $12 V_{DC}$ . The  $12 V_{DC}$  output is regulated to supply the required  $V_{ss}$  of the system modules.

## 5 MODELLING THE SYSTEM

The designed system is to convert  $400 V_{DC}$  1 kW power from an external power source to a power network line level sinusoidal AC voltage of 230 V at frequency of 50 Hz. The inverter topology chosen must meet system requirements.

The controller unit executes the control algorithm. The control process establishes the optimised AC output under a DC input. Initially the sampling circuit is expected to read output to characterize inverter mode of operation, off-grid or grid-tied. The controller unit then synchronises the inverter to grid specification, where in grid-tied mode the inverter output must produce AC voltage and current that is in phase with the active grid and maintain a grid specified line voltage (230 V). When the inverter is switched and a  $400 V_{DC}$  input is realised, the PWM signal is generated to drive the MOSFET switching operations. The isolated auxiliary power supply for the MOSFET driver micro-controller based circuitry, that drive the low-side and high-side H-Bridge MOSFETS, and a linear analogue isolation amplifier for amplification of feedback signal to the control unit ADC that measure system output and input for control and protection of the inverter system.

The PWM signals produced by the control module are input to the high-side and low-side drivers mosfet driver that are to be designed. These are to produce PWM signal that control the switching instants of the inverter MOSFETS. Figure 6 shows the PWM technique for single phase PWM inverter. The PWM technique is used to derive the voltage steps signals that emulate sinusoidal AC inverter output. Output voltage waveforms generated by the inverter go through the output filter then through to the live - neutral load connectors (where the system is either grid connected or off-grid). The PWM Generator circuit is thus far simulated on multisim and produce the required PWM signals that are expected to drive the inverter switching operations.

For the current H-bridge design Both high-side and low-side driver are to produce SPWM signal that control the switching instants of the inverter IRF 440 MOSFETS. Through SPWM pulse the H-bridge system sinusoidal output can be emulated more accurately. Figure 9 shows the SPWM technique for single phase

PWM inverter. The SPWM technique is used to derive the SPWM signal that emulate sinusoidal inverter output. The technique is applied by using two types of waveforms: The desired reference waveform, which is the sinusoidal waveform with fundamental frequency, and the carrier waveform which is triangular waveform with higher frequency than the fundamental for modulation. The frequency of the carrier waveform is to decide the sampling switching frequency of the inverter SPWM driven H-bridge, whilst the reference waveform determines the inverter output frequency of 50 Hz. The AC output is generated as the compared output of carrier waveform and the desired reference waveform create an SPWM signal.

## 6 RESULTS

Thus far the design was loaded under a small resistive  $10 \mu$ . The overall simulated circuit diagram is shown in figure 9. operated at half bridge the SPWM signal is generated using a LM741A comparator with the reference and carrier signal connected. where the comparator is designed produce a SPWM of 5 V pulse high when the reference signal is high than the triangular carrier wave thus producing the desired SPWM. Channel 4 signal (the green in figure 9) shows the output voltage over the  $100 \mu$  load. The signal thus far shows a sinusoidal variation in pulse peaks, however the signal is pulsed and does not form the desired sinusoidal analogue AC output. An LC filter is currently being designed to filter and delay the fall down time during switch off to allow to step increases that emulate a sinusoidal AC output rather than pulses of increasing amplitude as seen on figure 9.

## 7 CONCLUSION

The hybrid inverter model is presented that convert the 400 V DC signal input to a 230 V ac at 50 Hz. The model component quantification and simulation is currently being tested and will be presented in the follow-up report. The report hereby has discussed design methodology that is applied in designing the inverter. The design aims to quantify the efficiency of the system topology and the distortion error of the desired sinusoidal AC output.

## REFERENCES

- [1] S. Iturriaga-Medina, C. A. Limones-Pozos, P. R. Martinez-Rodriguez, G. Escobar, J. M. Sosa, A. A. Valdez-Fernandez, and J. F. Martinez-Garcia, "A comparative analysis of grid-tied single-phase transformerless five-level npc-based inverters for photovoltaic applications," in *2016 13th International Conference on Power Electronics (CIEP)*, June 2016, pp. 323–328.
- [2] P. Roshankumar, P. P. Rajeevan, K. Mathew, K. Gopakumar, J. I. Leon, and L. G. Franquelo, "A five-level inverter topology with single-dc supply by cascading a flying capacitor inverter

- and an h-bridge,” *IEEE Transactions on Power Electronics*, vol. 27, no. 8, pp. 3505–3512, Aug 2012.
- [3] N. Hossain, T. Routh, A. H. Yousuf, M. Asaduzzaman, M. Hossain, and U. Husnaeen, “Design and development of a grid tied solar inverter,” 05 2012, pp. 1054–1058.
- [4] Manga.R and Srinivas.V, “Analysis and design of hybrid active multi-level inverter topology fed induction motor drive manga,” 2016.



## APPENDIX

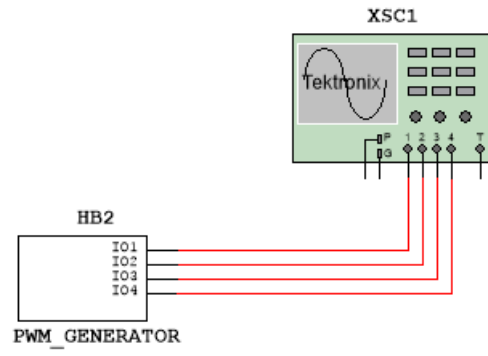


Figure. 4. PWM-GENERATOR Block.

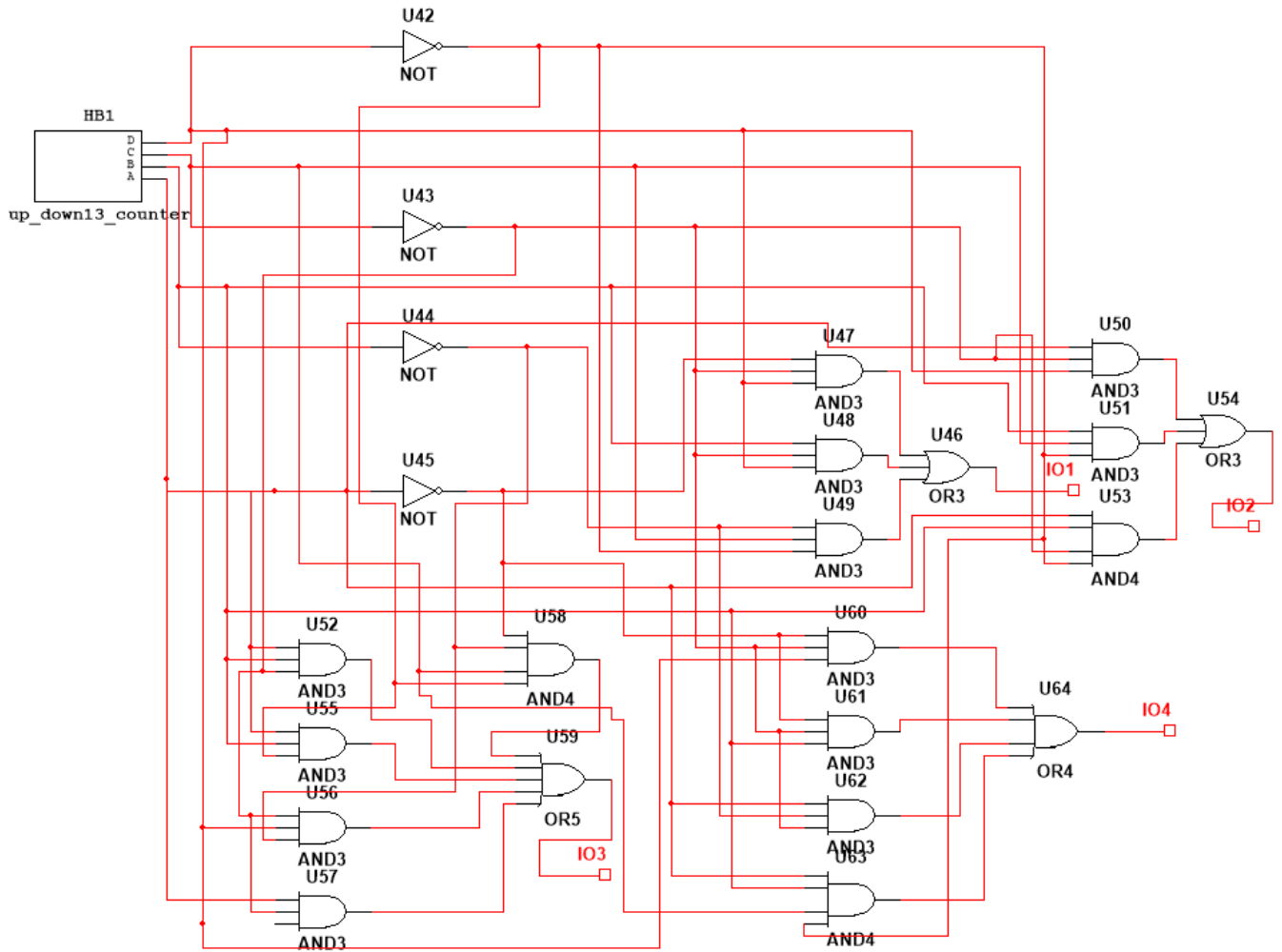


Figure. 5. PWM-GENERATOR internal logic circuit diagram.



