DESIGN OF A SIMPLE HYBRID SOLAR INVERTER - THIRD DRAFT

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Abstract: This document outlines the design of a simple hybrid solar inverter which is capable of operating either in standalone or grid-tie mode. The design assumes a 1 kW solar array and corresponding charge controller are present which are capable of acting as a 400 V supply for standalone operation and a current source for grid-tie operation. The design makes use of an oscillator circuit to generate a reference 50 Hz sinusoid, for standalone operation, which is converted into a pulse width modulated signal through analogue conditioning. Pulse width modulation is used in conjunction with an n-channel mosfet H-bridge and low-pass filtering to yield a relatively pure, high voltage sine wave output. For grid-tie operation, the reference sinusoid is replaced by a scaled version of mains voltage and hysteresis current control is utilised to ensure synchronous power delivery to a fixed-voltage grid. Manual switching between operating modes is presented and simple feedback control is incorporated.

1. INTRODUCTION

The ever decreasing supply of conventional fossil-fuel-based energy sources and ever increasing interest in solar power has warranted the design of a hybrid DC-AC inverter which can operate in standalone or grid-tie mode. This report presents the design methodology and simulation results of the proposed hybrid inverter. Section 2 provides context to the project as well as all design specifications and assumptions. An overview of the main system blocks is presented in Section 3 and is followed by a detailed description of the design for standalone operation in Section 4. Section 5 presents the design for grid-tie operation and is followed by Section 6, which proposes a method of switching between modes of operation. Section 7 proposes security measures to protect the inverter from extreme temperature and power consumption conditions. Section 8 presents testing results for the final integrated hybrid inverter and is followed by an evaluation and future recommendations in Section 9. Section 10 discusses some of the social implications of the proposed design and the report is concluded in Section 11.

2. BACKGROUND

The benefits of utilising renewable energy as an alternative to conventional fossil fuel sources has been explored extensively. Renewable energy, particularly solar energy, has been identified as a solution to the world energy crisis as well as the issue of climate change as a result of carbon emissions [1]. This has warranted particular emphasis being placed on the improvement of photovoltaic (PV) technology, which has become increasingly more refined and cost-effective. Utilisation of PV technology has its challenges, however, particularly in the conversion of low voltage direct current (LVDC) from a solar panel to high voltage alternating current (HVAC) for use in home appliances or the formation of micro-grids [2]. In order to address these challenges, a hybrid DC-AC inverter design which is capable of operating in standalone and grid-tie mode is proposed. Emphasis has been placed on device robustness and utilisation of as few components as possible to achieve an acceptably clean output.

In order for the proposed design to be acceptable, it must adhere to the following specifications:

- The inverter is single phase and must be capable of operating in two modes, either standalone (grid-forming) or grid-tie (connected to mains supply).
- The design needs to cater to a general household load, but does not need to consider load profiling or time of day. Provision should be made for the possibility that power output from the PV array may reduce below the stipulated 1 kW and that users may attempt to draw more than the maximum power than the array can provide.
- The system must be simple and robust. No microcontroller will be utilised in this design.
- The design must be transformerless as a high voltage DC input will be provided by a fixed charge controller.
- A cost analysis of the device is not required, but the trade-off of design complexity and efficiency must be considered.

The following assumptions have been made:

- A PV array and charge controller / maximum power point tracker (MPPT) have been provided and cannot be changed.
- The charge controller is capable of supplying the inverter with a floating 400 V source and a maximum power of 1 kW.
- It is assumed that the charge controller is also capable of supplying the inverter with a 12 V DC input for powering low-voltage circuitry without the need for an additional buck-converter (the PV array is naturally low voltage).
- It is assumed that a 1 Vpk pure sinusoidal reference oscillator has been supplied for standalone inverter operation, removing the need for an oscillator design.
- It is assumed that the grid may be modelled as a low impedance voltage source for grid-tie operation.
- System earthing need not be considered in this design.

3. SYSTEM OVERVIEW

An overview of the required system functionality is illustrated in Figure 1. The basic design was established by consulting several articles for standalone and grid-tie inverter operation [3], [4], [5]. In both modes, a reference 50 Hz sinusoid must be provided which the inverter output can be synchronised to. In the case of standalone operation, a low voltage sinusoid generated from an oscillator circuit is used as the AC reference. In grid-tie mode, the mains supply is stepped down to low voltage and used as the AC reference.

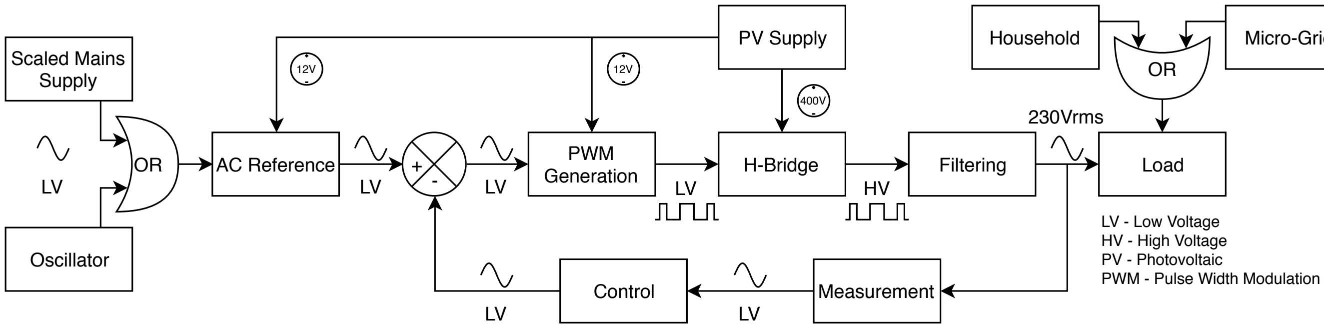

Figure 1 : Overview of complete system functionality.

In standalone operation, the AC reference sinusoid is compared with a high frequency carrier signal to generate a pulse width modulated (PWM) output which rapidly steps between 0 and 5 V [3]. The PWM signal is passed to an n-channel mosfet H-bridge (with mosfet drivers included), which uses the 400 V PV supply to convert the low voltage PWM signal into a high voltage PWM signal. By passing the high voltage PWM signal to a passive low-pass filter with a high frequency cutoff and suitable attenuation, a smooth, 50 Hz, high voltage output waveform can be generated. This voltage is suitable for powering household appliances, but cannot be used to supply a micro-grid. In grid-tie operation the inverter cannot act as a voltage source because of the grid's fixed voltage of 230 Vrms 50 Hz (in South Africa). As such the inverter must act as a current source, injecting power into the grid. The scaled mains voltage reference is used to calculate a reference current waveform, which is compared to the current output of the inverter. The error between reference current and inverter output current in grid-tie mode is used to generate a different PWM signal for H-Bridge switching. This is known as hysteresis current control and requires the use of inductive filtering at the output of the H-Bridge [5].

The 'OR' gates in Figure 1 indicate switching between the modes of inverter operation, which will most likely take the form of a manual switch-over with mechanical lockout to prevent the oscillator feeding asynchronous power into the grid. In both modes of operation some form of negative feedback control is required. In the case of standalone operation, a simple proportional control scheme will be implemented to control the amplitude of the output voltage waveform. In grid-tie mode, hysteresis current control will ensure that the inverter output current remains within a certain error margin of the reference current waveform. Control circuits will be implemented at the low voltage level and, as such, measurement circuitry will be required to scale output voltage/current down to suitable levels.

In order to simplify the design of the complete inverter system, it has been split into four main components, as shown below.

1. Standalone design.
2. Grid-tie design.
3. Switch mechanism for alternating between modes of operation.
4. Protection against over-voltage, under-voltage, over-current and over-temperature conditions.

The design and testing of each component will be discussed in detail in the following report sections.

4. STANDALONE DESIGN

The basic model of the standalone DC-AC inverter follows that of a bi-level, sinusoidal pulse width modulated, n-channel mosfet H-bridge. It has been designed to produce an output of 230 Vrms at 50 Hz, as is the standard in South Africa. All components of the standalone system are discussed in the following subsections.

4.1 H-Bridge

Many inverter designs utilise the H-Bridge circuit as a means of producing AC from a DC source. This design utilises four high power, n-channel switching mosfets in the H-Bridge configuration to convert the 400 V DC supply from the charge controller to an AC signal which may be passed to a filtering circuit.

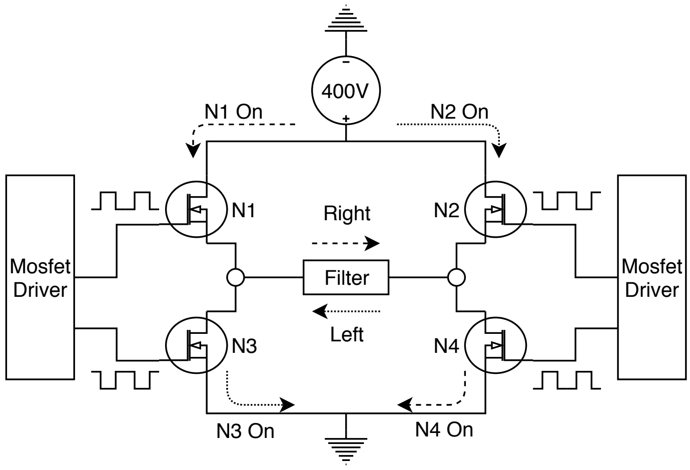

Figure 2 : Circuit diagram of n-channel mosfet H-Bridge with current flows indicated.

Figure 2 illustrates this configuration and the current flow through the circuit when each of the mosfet pairs (N1-N4 and N2-N3) are switched on in alternating fashion. A PWM signal is sent to the gate of each mosfet in order to time the switching so that the output pulsed waveform can be filtered to produce a smooth 50 Hz sinusoid. This concept is illustrated in Figure 3.

It is important to note that because n-channel enhancement mosfets have been selected (for their use in high voltage applications) the switches are active-high and the gate-source voltage must be a positive 8-12 V for activation. This implies that a high voltage mosfet driver circuit must be utilised to allow the high and low side mosfets to be switched with a 5 V PWM signal.

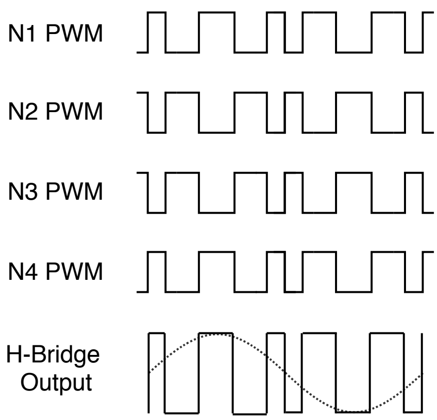

Figure 3 : Simplified 5 V PWM signals sent to each H-Bridge switch and 400 Vpk output signal shape.

4.2 PWM Generation

The inverter has been designed to produce a pure sine wave output as opposed to a modified sine wave output as it may be required to power sensitive electronics. As such, the 1 Vpk 50 Hz sinusoidal reference has been compared with a 1 Vpk triangular carrier wave of frequency 20 kHz. This produces a PWM signal which embeds the sinusoid within it, as explained by Doucet, Eggleston and Shaw [3]. This is known as a sinusoidal pulse width modulated (SPWM) signal. Bi-level SPWM has been chosen for this design for simplicity, but multi-level SPWM can be adopted for better results [3]. The complete circuit diagram for generation of all PWM signals in standalone operation is shown in Figure 4.

Two 5 V SPWM signals which are 180 ° apart in phase are generated using two comparators. This allows mosfets N1 and N4 to be driven with one SPWM signal and N2 and N3 to be driven with the other such that there is no instance when the 400 V supply is shorted to neutral. While this design is simple, all four mosfets are switching at 20 kHz, which will result in additional heat loss. A potential solution to this is to generate a low frequency square wave for switching half of the mosfets at 50 Hz (the other half still switched at 20 kHz).

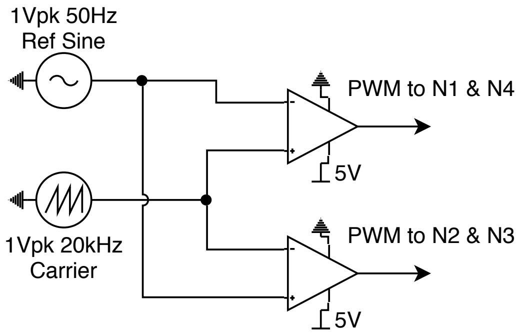

Figure 4 : Circuit used to generate required PWM signals.

By combining the H-Bridge in Figure 2 and the PWM generation circuit in Figure 4, the 1 kHz high voltage oscillating output shown in Figure 5 was generated using Multisim. This figure is purely for illustrative purposes and all future results were generated using a switching frequency of 20 kHz. Embedded within the pulsed waveform is an 800 Vp-p sinusoid with a fundamental frequency of 50 Hz. In order to extract the 50 Hz sinusoid, however, the high frequency carrier must be filtered away using passive (high voltage) filtering components.

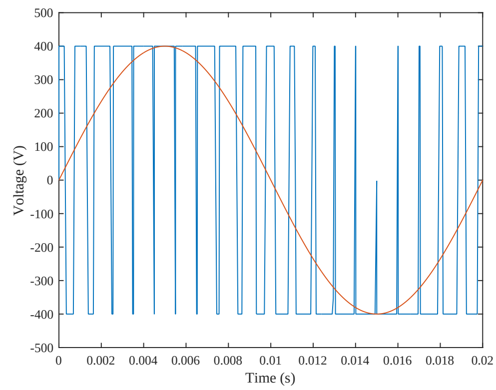

Figure 5 : Bridge voltage output for 1kHz switching frequency.

4.3 Filtering

Low frequency filtering is often limited by the physical size of the passive components required to achieve a suitably smooth 50 Hz output signal. As such, it is more practical to filter out the high frequency carrier signal from the H-Bridge SPWM output. It is for this reason that a passive LC filter has been designed with a cutoff frequency of 1 kHz (the geometric mean between the 50 Hz fundamental and 20 kHz carrier). The basic form of the filter is illustrated in Figure 6.

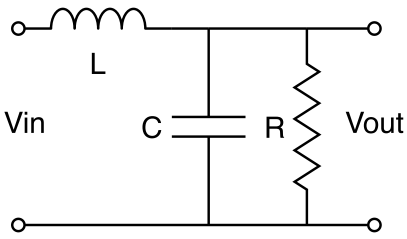

Figure 6 : Basic LC filter with purely resistive load.

Is is assumed that the load is purely resistive, but in practice household appliances may contain inductive elements. The following two equations can be extracted from the filter's transfer function:

$$f_c = \frac{1}{2\pi\sqrt{LC}} \tag{1}$$

$$\xi = \frac{\sqrt{L}}{2R\sqrt{C}} \tag{2}$$

Here, ξ is the damping ratio of the second order system and f_c is the filter cutoff frequency in Hz. Knowing that the maximum power from the PV array is 1 kW and that the output voltage must be 230 Vrms, the following equation is used to calculate the full load resistance.

$$R = \frac{V^2}{P} = \frac{230^2}{1000} = 52.9\ \Omega \tag{3}$$

By rounding the full load resistance to 53 Ω, selecting f_c to be 1 kHz and selecting ξ to be 1.1 (overdamped) at this load, using equations 1 and 2 the values of L and C were calculated to be 18.5 mH and 1.4 μF, respectively. It is important to note that the filter damping reduces with increasing resistance (reduced load). This is illustrated in Figure 7 which shows the filter output under various resistive loads when connected to the H-Bridge circuit. The half load condition was tested by increasing the load resistance to 106 Ω and the 10 % load condition was tested by increasing the load resistance to 530 Ω. Under all load conditions, it can be seen that the output waveform is a 50 Hz sinusoid with a peak magnitude slightly greater than required. The issues of increased amplitude and undamped oscillation may be rectified with the use of feedback control.

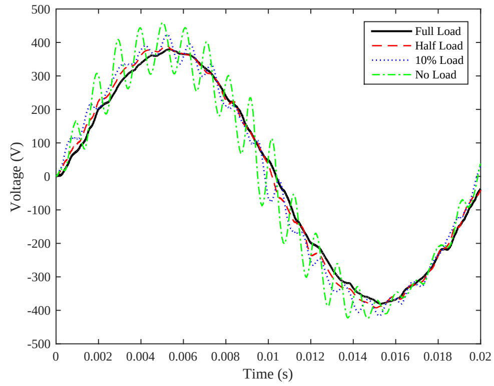

Figure 7 : Open loop filter output for different resistive loads.

4.4 Control

As the output of the filter does not need to be synchronised to any grid in standalone operation, phase control of the output sinusoid is not a concern. Output amplitude, however, does need to be controlled to remain close to 230 Vrms (325 Vpk). As the inverter ideally converts the 1 Vpk sinusoidal reference into a 400 Vpk output sinusoid, the open loop system can be modeled as an ideal gain of 400, as illustrated in Figure 8. Knowing this, the simple closed loop control scheme illustrated in Figure 9 can be adopted to ensure that the output magnitude remains within a suitable range. This is done through the use of proportional control, with a gain block of magnitude K being included in the control loop.

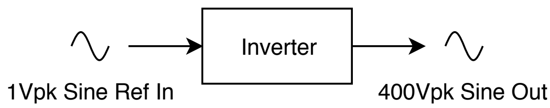

Figure 8 : Open loop control model of inverter system.

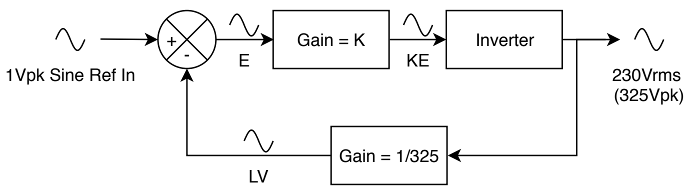

Figure 9 : Closed loop control method of inverter system.

The greater the magnitude of K the lower the output error will be. Proportional control was chosen as it is the simplest form of feedback control for steady state error compensation. If transient effects needed to be compensated for, more comprehensive control schemes would be required. Figure 10 illustrates the change in full load inverter output with unity gain (K=1) feedback incorporated. It can be seen that the amplitude of the controlled output is considerably closer to the ideal 230 Vrms output. Figure 11 illustrates that closed loop control also improves the output magnitude of the system under other loads. That said, the no-load output still possesses undamped oscillations.

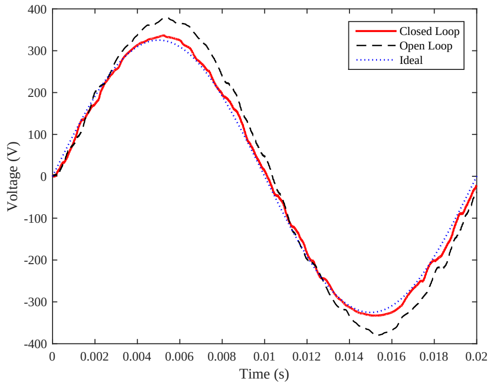

Figure 10 : Full load open loop output vs full load closed loop output.

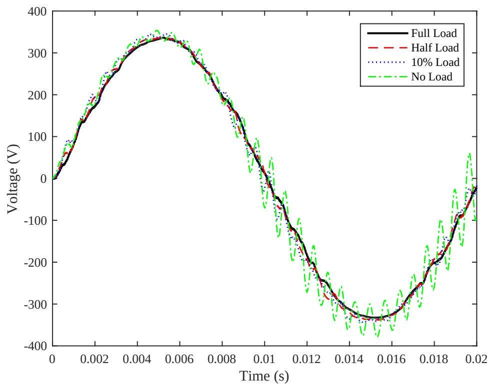

Figure 11 : Closed loop filter output for different resistive loads.

5. GRID-TIE DESIGN

The design of a grid-tie inverter presented in this report is largely based on that proposed by Rahim and Selvaraj [5]. The basic premise of the device is to measure the grid voltage using a low power transformer and convert it into an ideal current waveform (measured as a voltage) which will allow the inverter to supply its maximum power to the grid. Knowing that the inveter is to supply a 230 Vrms grid with 1 kW of power, the following equation is used to calculate the desired peak current output.

$$I = \frac{P}{V} = \frac{1000}{230} \approx 4\ Arms = 5.66\ Apk \tag{4}$$

Preliminary results of tests conducted on the proposed circuit is illustrated in Figure 12. More details on the grid-tie inverter implementation will follow in the next report iteration.

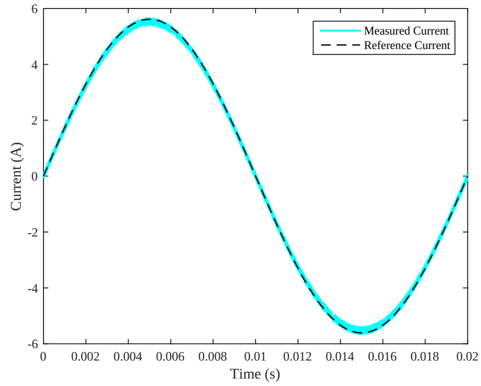

Figure 12 : Hysteresis controlled output current.

6. MODE SWITCHING

This section will be addressed once the previous subsection has been completed.

7. CIRCUIT PROTECTION

This section will be addressed once the previous subsection has been completed.

8. INTEGRATED TESTING

This section will provide results for tests conducted on the complete integrated inverter system upon completion of the individual parts discussed in the previous sections.

9. EVALUATION AND FUTURE RECOMMENDATIONS

Based on the evaluation of results obtained in the previous section, recommendations for future improvements and design trade-offs will be discussed.

10. SOCIAL IMPACT

As with any design aimed at affordably providing electricity, there are social implications that need to be considered. This section will discuss the proposed design's place within the market and how people may make use of it. More details on the social impact of the design may be found in Appendix A.

11. CONCLUSION

A block diagram illustrating the high-level functionality of the proposed hybrid solar inverter has been presented and discussed. A design for standalone inverter operation has been presented and shown to produce an uncontrolled 800 Vp-p 50 Hz output waveform post filtering with varying degrees of ripple depending on the load connected. The output magnitude has been shown to improve with the addition of simple proportional feedback control. More details on the implementation of grid-tie inverter operation will be presented in the next report iteration.

12. REFERENCES

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