Dual-Mode Double-Carrier-Based Sinusoidal Pulse Width Modulation Inverter With Adaptive Smooth Transition Control Between Modes

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***Abstract*—Three dual-mode boost–buck-derived inverters with smooth transition between modes have been proposed: 1) boost-full bridge inverter; 2) boost-H5 inverter; 3) boost-dual buck inverter. For the same topologies, in conventional control method, the first stage is needed to boost input voltage to a constant high voltage, and the second stage is for sinusoidal inverting. However, in the proposed three inverters, either buck or boost mode works at a single time, thus, only one switch works at a high switching frequency. In this way, a lot switching loss can be reduced, and moreover, since the voltage across the middle capacitor is smaller than the conventional constant high voltage, the further switching loss mitigation is possible. In order to achieve smooth transition between the two modes, a double-carrier-based sinusoidal pulse width modulation (SPWM) is proposed. Other than this, three advanced modulation methods are proposed: 1) double-carrier with different frequencies; 2) double-carrier with different magnitudes; and 3) double-carrier with different frequencies and magnitudes. Following that, the loss distribution in every component is provided and the California Energy Commission efficiency of these inverters under different input voltage conditions is compared. Finally, the experimental results show the dual-mode double-carrier-based SPWM inverter can improve the efficiency by 2% than the traditional constant dc bus voltage solutions.**

***Index Terms*—Dual mode, inverter, multi-carrier, sinusoidal pulse width modulation (SPWM), smooth transition.**

I. Introduction

RENEWABLE energy power supplied to the utility grid is gaining more and more attention, particularly photovoltaic (PV) system [1]–[7]. For residential PV power generation systems, single-phase utility interactive inverters less than 5 kW are of particular interest [8]–[14]. For this power level, the input voltage of a residential PV inverter can vary in a wide range because of the I–V characteristics of PV panels [13], such as from 200 V to 500 V. Hence, the PV power conditioning system (PCS) should feature both the step-up and step-down functions to supply more power generated from the PV panels to the grid. In the state-of-the-art, the most popular solution is to use a dc-dc converter with dc link voltage of a constant voltage in conjunction with a dc-ac inverter arrangement as shown in Fig. 1 [12]–[18]. In this structure, the dc bus voltage can be easily regulated, and the dc-ac stage can be a voltage source type high-frequency pulse width modulation (PWM) inverter. However, this kind of configuration is usually difficult to be highly efficient, because both the dc-dc converter and the dc-ac inverter operate in the high-frequency switching mode so that the huge switching loss in the two stage cannot be avoided. In order to mitigate the switching loss and improve the power conversion efficiency, the dual-mode boost–buck converter-based PV inverter has been proposed in [19], [20] as shown in Fig. 2. In this topology, the interleaved boost–buck type dc-dc converter, which is composed of L_1, L_2, S_1, S_2, S_3, D_1, D_2, D_3, and C_L, is employed as the first stage, and the full-bridge unfolding circuit which consists of S_a, S_b, S_c, and S_d is utilized as the second stage. Here, the first stage regulates the output inductor current to be rectified sinusoidal under high-frequency switching operation, while the second stage switches the polarity of the output current which is synchronized to the line frequency such as 50 or 60 Hz. Since the circuit runs either in boost or buck mode, its first stage can be very efficient even if it operates under high-frequency switching. For the second stage, the switching loss can be practically eliminated, because the unfolding circuit only operates at the zero crossing point (ZCP) of the line voltage, and it switches at zero voltage and zero current conditions.

In this paper, the dual-mode boost–buck converter is adapted with three different inverter topologies such as unipolar

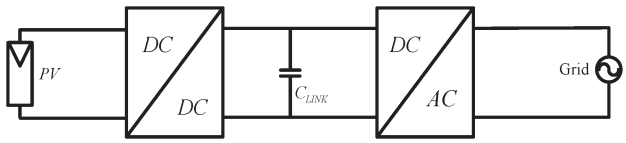

Fig. 1. Conventional two-stage PV inverter.

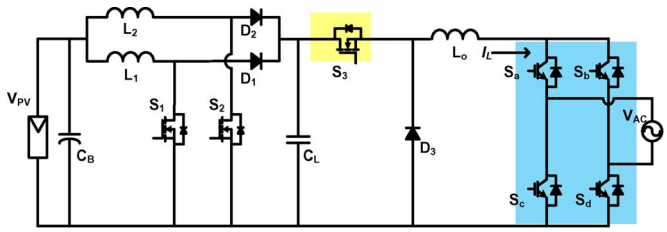

Fig. 2. Boost–buck-unfolding inverter in [19], [20].

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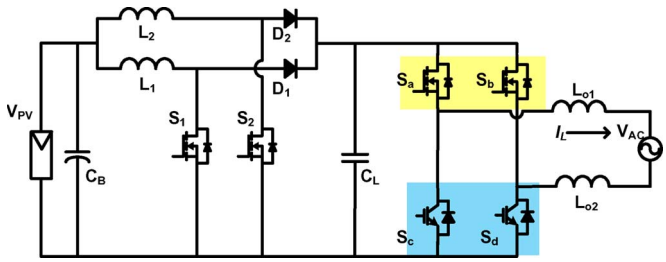

Fig. 3. Boost-full bridge inverter.

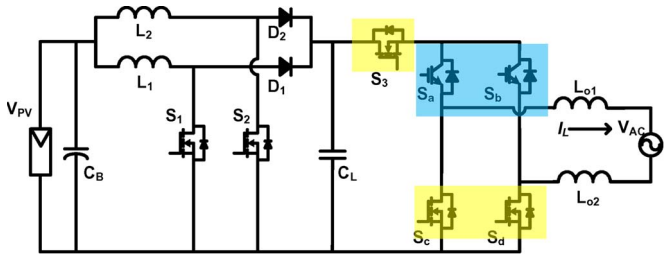

Fig. 4. Boost-H5 inverter.

modulated full bridge (FB) inverter, H5 inverter [21], and dual buck (DB) type inverter to improve the efficiency of the PCS or to reduce the number of the components. In the proposed topologies, the buck stage is totally removed, and the adapted inverter topologies take the role of the buck stage and the unfolding circuit in the dual-mode boost–buck converter shown in Fig. 2. The operation of the three proposed topologies is analyzed in detail. In addition to this, the double-carrier-based sinusoidal PWM (SPWM) is proposed to obtain smooth mode transition between the boost mode in the first stage and the inverting mode in the second stage. Because of this double-carrier-based SPWM, smooth transition between two operation modes can be realized and avoid comparing the input and output voltage. Furthermore, the variations of the fundamental double-carrier-based SPWM method are also proposed to improve the efficiency or the control characteristics. The efficiencies of these inverters are compared later. Finally, both simulation and experiment results are provided. The results show the dual-mode double-carrier-based SPWM inverter can improve the efficiency by 2% than the traditional constant dc bus voltage solutions.

II. Proposed Inverters and Operation Modes

The proposed three types of inverters are shown in Figs. 3–5. In these figures, the IGBTs in the blue boxes are operating in line frequency for selecting grid polarity as the same function of $S_a - S_d$ in unfolding circuit in Fig. 2, while the MOSFETs in the yellow boxes are operating as the same function of S_3 in Fig. 2. In the proposed circuits, the output inductor L_o in Fig. 2 locates between the converter and the grid.

If the input voltage from the PV panel is lower than the rectified instantaneous grid voltage, the switches in the interleaved boost part S_1 and S_2 are under switching operation, and the MOSFETs in the inverter stage are always on or off depend on the polarity of the grid. "Boost mode" is named for this condition.

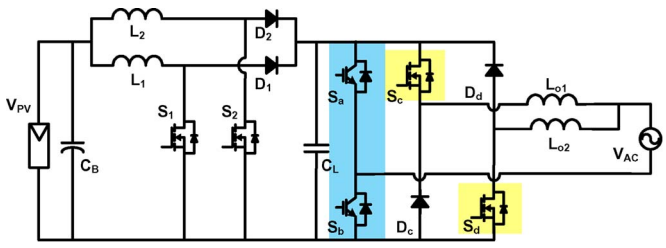

Fig. 5. Boost-dual buck inverter.

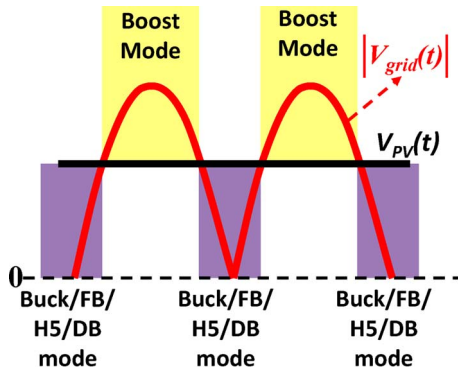

Fig. 6. Operation mode.

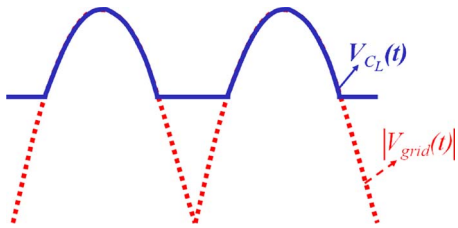

Fig. 7. Voltage across the middle capacitor C_L.

If the input voltage is higher than the rectified instantaneous grid voltage, the switches in the interleaved boost part S_1 and S_2 are off, and the MOSFETs in the inverter stage operates under switching mode. "Buck/FB/H5/DB mode" is named for this condition based on the dual-mode topologies. Fig. 6 shows the operating mode of the converter according to the magnitude of the rectified instantaneous grid voltage.

Under these operation modes, the voltage of the middle capacitor C_L is no longer constant as in conventional boost converters. In boost mode, the capacitor voltage will follow the rectified grid voltage. On the other hand, it will be equal to the input voltage in buck/FB/H5/DB modes. This relationship is shown in Fig. 7.

In [20], four switches are used in unfolding circuit for selecting the polarity of the grid. However, in the proposed topologies, only two switches are used for polarity selection, and the conduction loss is cut by the half compared to the traditional circuit. For the boost-FB inverter in Fig. 3, the number of the components is reduced so that the implementation cost is reduced. For the boost-H5 inverter as shown in Fig. 4, one diode is saved, and the diodes in the same package with IGBTs are also utilized. Moreover, it can reduce the voltage stress for each component, its switching loss is greatly reduced, and thus it still can achieve high efficiency. For boost-DB inverter, it

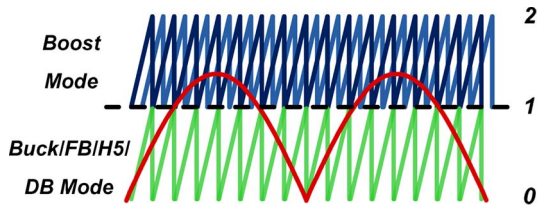

Fig. 8. Double-carrier-based SPWM.

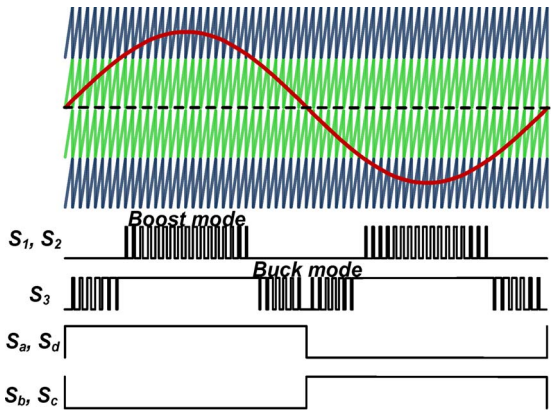

Fig. 9. PWM generation of boost with buck.

keeps the same component number, but no reverse recovery loss SiC diode can be used, thus it can reach further high efficiency. Detailed efficiency comparison will be shown in Section V.

III. Double-Carrier-Based SPWM for Smooth Transition Between Modes

In order to achieve smooth mode transition between different operating modes, the double-carrier-based SPWM method is proposed as similar in multilevel inverter applications [22]–[26]. As illustrated in Fig. 8, two interleaved carriers with the unit offset are employed for the boost mode, and single carrier without any offset is utilized for the buck/FB/H5/DB mode.

In this way, the rectified sinusoidal waveform would only introduce high-frequency switching in either boost mode or buck/FB/H5/DB mode. In this method, the MOSFETs for the buck/FB/H5/DB mode are always on during the boost mode whereas the MOSFETs for the boost mode are always off during buck/FB/H5/DB mode as expected.

Fig. 9–12 show how to generate the PWM signal for these four inverters. It is slightly different as Fig. 8. Based on the polarity of the grid, an offset of the sawtooth/triangular ramp right on the top of the buck/FB/H5/DB mode carrier needs to be applied to boost mode during positive cycle, and on the bottom of the buck/FB/H5/DB mode, PWM modulator needs to be applied to boost mode during negative cycle. From these figures, it is clear to observe that only one mode is operating at a single period.

Fig. 13 shows the control diagram of the proposed inverters. The MPPT loop provides the magnitude of the current reference I_{mag}, and the phase locked loop tracks the phase angle of the grid voltage. By multiplying the two components, the current reference i_{ref} is generated. The signal after the compensator i_{err} is sinusoidal signal, which provides SPWM with the double-carriers. It is necessary to point out that, there is no need to compare the input voltage and the output voltage, because the current will be adaptively controlled by using this double-carrier SPWM method.

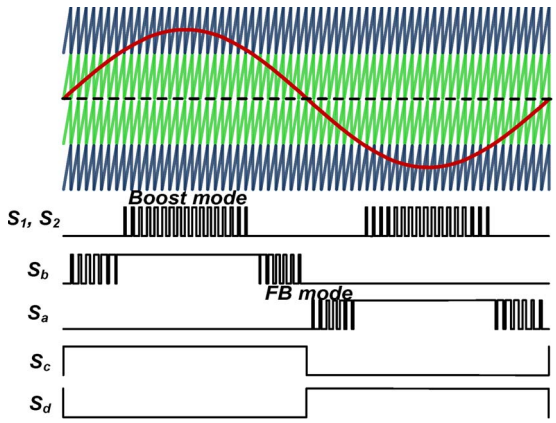

Fig. 10. PWM generation of boost with full bridge.

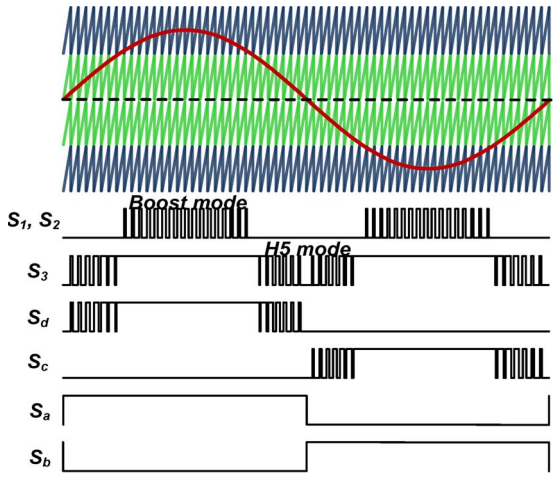

Fig. 11. PWM generation of boost with H5.

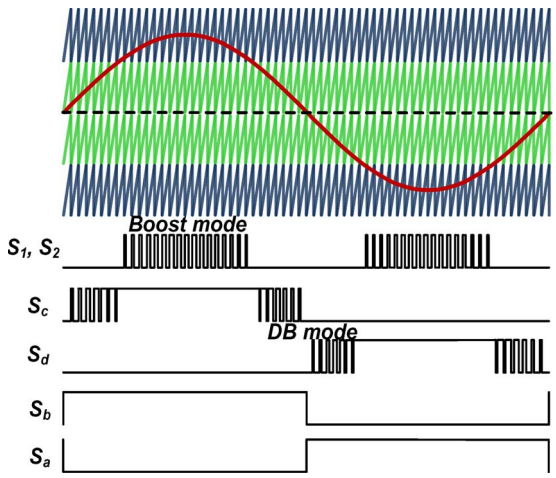

Fig. 12. PWM generation of boost with dual buck.

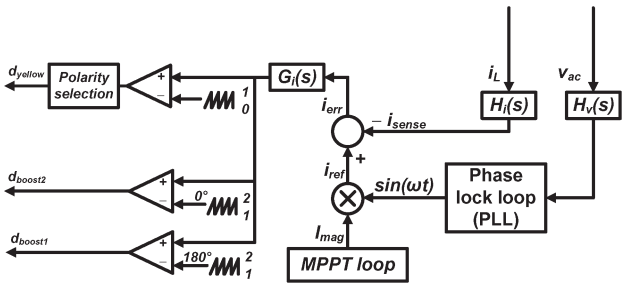

Fig. 13. Control diagram of the proposed inverters.

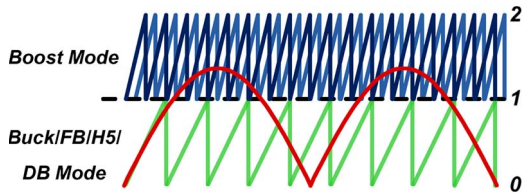

Fig. 14. Double-carrier with different frequency.

IV. Three Advanced Double-Carrier-Based SPWM Control

A. Double-Carrier With Different Frequency

As known from [20], small boost inductance L_1 and L_2 and large buck inductance L_o make the compensator design easy. In order to keep the same current ripples, it is good to increase the carrier frequency for boost mode, which leads to small inductance and reduce the carrier frequency for buck/FB/H5/DB mode, which leads to large inductance as shown in Fig. 14. If only the frequency of carrier for the buck/FB/H5/DB mode is reduced while the carrier frequency for the boost mode is kept the same, switching loss can be further saved. However, since the inductance L_o needs to be increased, the copper loss introduced by this inductor may increase as well. As a result, the frequency should be selected by compromising between switching loss, core loss, and copper loss.

B. Double-Carrier With Different Magnitude

In the dual-mode converter operation, the compensator designed should be based on the boost mode operation rather than the buck mode operation [20]. This gives the possibility of implementing a universal controller for the boost mode and the buck/FB/H5/DB mode. Hence, only one compensator can be applied to both of the operating modes. However, for the rectified sinusoidal waveform, it is very difficult to avoid current distortion near the ZCPs unless the controller has very wide control loop bandwidth. In order to handle this situation, an advanced double-carrier-based SPWM with different magnitudes between the carriers in each mode is proposed as shown in Fig. 15. The distortion of the reference sinusoidal waveform is due to the different magnitude of these two modes. In order to guarantee the correct effective duty cycle, the duty reference signal is adaptively changing according to the magnitude of the carriers. The implementation scheme of this method is shown in Fig. 16. Unlike the magnitude of the boost mode carrier is "1" in Fig. 8, it becomes "k" in Fig. 16.

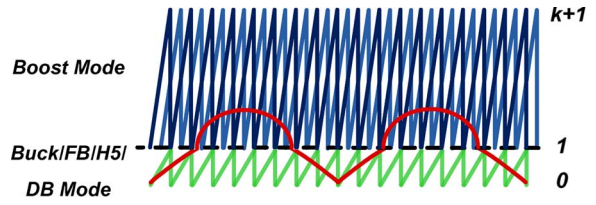

Fig. 15. Double-carrier with different magnitude.

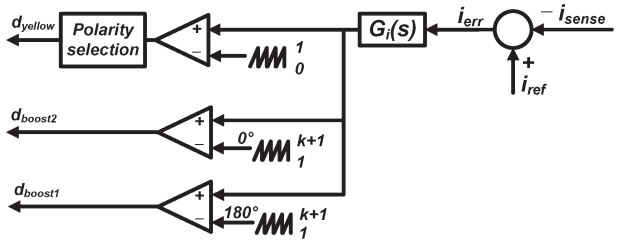

Fig. 16. Control diagram of double-carrier with different magnitude.

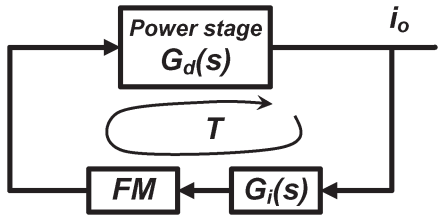

Fig. 17. Control diagram of loop gain.

In Fig. 17, $G_i(s)$, FM, and $G_d(s)$ represent the compensator gain, the PWM modulation gain, and the control-to-output transfer function, respectively. Here, the loop gain of the entire control system is written as

$$T = G_d \cdot FM \cdot G_i \tag{1}$$

where $FM = 1/V_m$ where V_m is the magnitude of the carrier.

Thus, for boost mode, its loop gain is

$$T_{\text{boost}} = G_d \cdot G_i \cdot \frac{1}{k} \tag{2}$$

and for buck/FB/H5/DB mode, its loop gain is

$$T_{\text{buck}} = G_d \cdot G_i \cdot 1. \tag{3}$$

$$\text{Thus, } T_{\text{buck}} = T_{\text{boost}} \cdot k. \tag{4}$$

Thus, with different carrier magnitudes, the buck/FB/H5/DB mode can obtain larger loop gain than the boost mode. In this method, buck/FB/H5/DB mode does not need to be constrained by the boost mode, and it can have wider bandwidth and higher gain. Fig. 18 shows the loop gain of buck/FB/H5/DB mode with the same carrier magnitude as boost mode. Its bandwidth is 2 kHz, and its gain at 60 Hz is 60 dB. Fig. 19 shows the loop gain of buck/FB/H5/DB mode with the three times smaller carrier magnitude than boost mode. Its bandwidth is 4 kHz, and its gain at 60 Hz is 75 dB. Table I shows a comparisons.

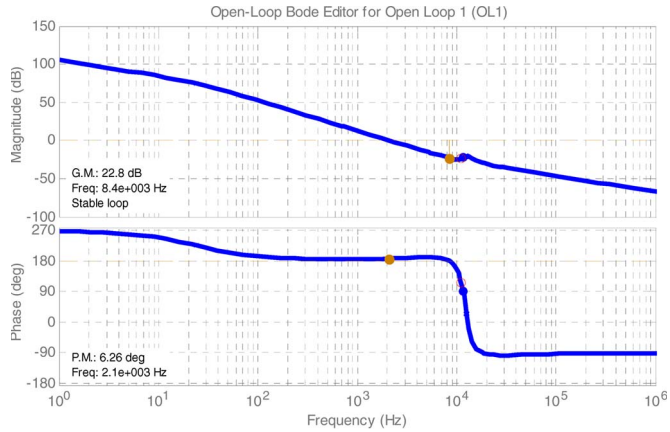

Fig. 18. Loop gain of buck/FB/H5/DB mode with the same carrier magnitude as boost mode.

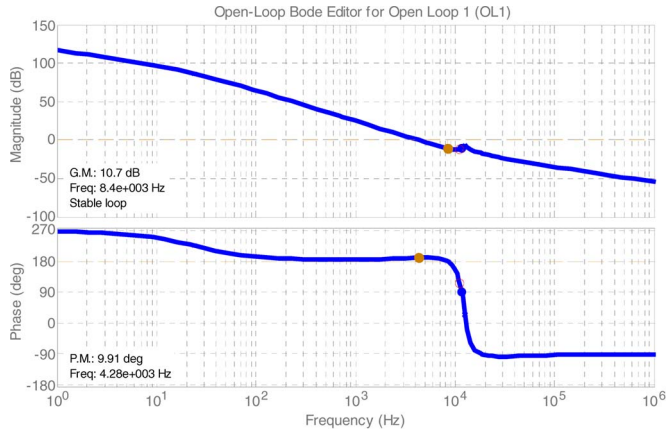

Fig. 19. Loop gain of buck/FB/H5/DB mode with three times smaller carrier magnitude than boost mode.

TABLE I
PARAMETERS OF ALL THE INVERTERS

	Same carrier magnitude as boost mode	Three times smaller carrier magnitude than boost mode
Bandwidth	*2 kHz*	*4 kHz*
Gain @ 60 Hz	*60 dB*	*75dB*

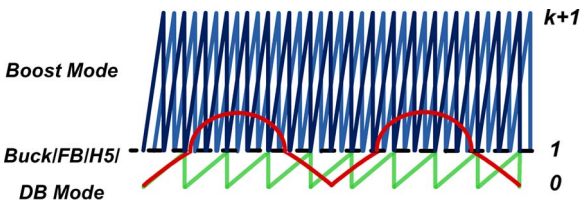

Fig. 20. Double-carrier with different frequency and magnitude.

C. Double-Carrier With Different Frequency and Magnitude

Based on the previous two modulation methods, it is straightforward to combine these two modulation methods and take the advantages of both. Fig. 20 illustrates this modulation method. The carrier for the boost mode is still on the top of the carrier for the buck/FB/H5/DB mode. And the carrier for buck/FB/H5/DB mode has a different frequency and magnitude than that for the boost mode. As a result, the switching loss in the buck/FB/H5/DB mode can be reduced, and the buck/FB/H5/DB mode obtains wide bandwidth and high gain.

V. Loss Distribution and Efficiency Comparison

The two different operating modes and the non-constant middle link capacitor voltage as shown in Fig. 6 and 7 give the complication of calculating the loss in this type of inverters. Some details about calculations of loss are provided below.

If the input voltage range is set from 200 V to 500 V, under different input voltage condition, the angle and the voltage across the middle link capacitor can be found in (5) and (6), respectively.

$$\theta = \begin{cases} a\sin\left(\frac{V_{\text{in}}}{V_{\text{opk}}}\right), & \text{if } 200 \le V_{\text{in}} < 340 \\ \frac{\pi}{2}, & \text{if } 340 \le V_{\text{in}} \le 500 \end{cases} \tag{5}$$

$$V_{CL}(\omega t) = \begin{cases} V_{\text{opk}}\sin(\omega t), & \text{if } 200 \le V_{\text{in}} < 340 \\ V_{\text{in}}, & \text{if } 340 \le 1V_{\text{in}} \le 500. \end{cases} \tag{6}$$

For example, in the boost FB inverter, based on Fig. 10, the entire loss in this inverter includes the loss in the boost part, the FB part as shown in

$$\begin{aligned}(P_{\text{Loss}} = {} & (P_{S1con} + P_{S1sw}) \cdot 2 + (P_{D1con} + P_{D1rr}) \\ & \cdot 2 + (P_{Sccon} + P_{Scsw}) \cdot 2 + (P_{Dacon} + P_{Darr}) \cdot 2 \\ & + (P_{Sacon} + P_{Sasw}) \cdot 2 + P_{Lin} + P_{Lo}).\end{aligned} \tag{7}$$

The loss in the boost part can be calculated by (8)–(12)

$$\begin{aligned}P_{\text{con\_boostmos}} = {} & \frac{1}{\pi} \cdot \left[\int_0^{\theta} 0 \, d\,\omega t + \int_{\theta}^{\pi-\theta} \frac{\frac{2P_o}{V_{\text{in}}}\sin^2(\omega t)}{2} \cdot R_{dson} \frac{\frac{2P_o}{V_{\text{in}}}\sin^2(\omega t)}{2} \right. \\ & \left. \times \left(1 - \frac{V_{\text{in}}}{V_{\text{opk}}\,|\sin(\omega t)|}\right) d\omega t \right]\end{aligned} \tag{8}$$

$$\begin{aligned}P_{\text{sw\_booston}} = {} & \left[t_r \cdot \frac{1}{\pi} \cdot \int_{\theta}^{\pi-\theta} \frac{\frac{2P_o}{V_{\text{in}}}\sin^2(\omega t)}{2} \cdot \frac{V_{CL}(\omega t)}{2} \, d\omega t + \frac{2}{3} \cdot C_{oss} \right. \\ & \left. \cdot V_{\text{in}}^2 \cdot \left(1 - \frac{2\theta}{\pi}\right) \right] \cdot f_{\text{swboost}}\end{aligned} \tag{9}$$

$$P_{\text{sw\_boostoff}} = \left[t_f \cdot \frac{1}{\pi} \cdot \int_{\theta}^{\pi-\theta} \frac{\frac{2P_o}{V_{\text{in}}}\sin^2(\omega t)}{2} \cdot \frac{V_{CL}(\omega t)}{2} \, d\,\omega t \right] \cdot f_{\text{swboost}} \tag{10}$$

$$\begin{aligned}P_{\text{con\_boostD}} = {} & \frac{1}{\pi} \cdot \left[2 \cdot \int_0^{\theta} \frac{\frac{2P_o}{V_{\text{in}}} \cdot \sin^2(\omega t)}{2} \cdot \left[R_{ak} \cdot \frac{\frac{2P_o}{V_{\text{in}}} \cdot \sin^2(\omega t)}{2} + V_f \right] d\,\omega t \right. \\ & + \int_{\theta}^{\pi-\theta} \frac{\frac{2P_o}{V_{\text{in}}} \cdot \sin^2(\omega t)}{2} \cdot \left[R_{ak} \cdot \frac{\frac{2P_o}{V_{\text{in}}} \cdot \sin^2(\omega t)}{2} + V_f \right] \\ & \left. \times \frac{V_{\text{in}}}{V_{\text{opk}} \cdot |\sin(\omega t)|} \, d\,\omega t \right]\end{aligned} \tag{11}$$

$$P_{\text{Lin}} = 2\cdot\frac{1}{\pi}\cdot\int_0^{\pi}\left(\frac{\frac{2P_o}{V_{\text{in}}}\cdot\sin^2(\omega t)}{2}\right)^2\cdot R_{L1}\,d\,\omega t. \tag{12}$$

The loss in FB part can be calculated by (13)–(17).

$$P_{\text{Con\_buckmos}} = \frac{1}{\pi}\left[2\cdot\int_0^{\theta}\frac{P_o}{V_{\text{orms}}}\cdot\sqrt{2}\sin(\omega t)\cdot R_{\text{dson}}\cdot\left(\frac{P_o}{V_{\text{orms}}}\cdot\sqrt{2}\sin(\omega t)\right)\cdot M\sin(\omega t)\,d\omega t + \int_{\theta}^{\pi-\theta}\frac{P_o}{V_{\text{orms}}}\cdot\sqrt{2}\sin(\omega t)\cdot R_{\text{dson}}\cdot\left(\frac{P_o}{V_{\text{orms}}}\cdot\sqrt{2}\sin(\omega t)\right)d\,\omega t\right] \tag{13}$$

$$P_{\text{sw\_buckon}} = \left(t_r\cdot\frac{V_{\text{in}}}{2}\frac{1}{\pi}2\cdot\int_0^{\theta}\frac{P_o}{V_{\text{orms}}}\cdot\sqrt{2}\sin(\omega t)\,d\,\omega t + \frac{2}{3}\cdot C_{oss}\cdot V_{\text{in}}^2\cdot\frac{2\theta}{\pi}\right)\cdot f_{\text{swbuck}} \tag{14}$$

$$P_{\text{sw\_buckoff}} = t_f\cdot\frac{V_{\text{in}}}{2}\frac{1}{\pi}2\cdot\int_0^{\theta}\frac{P_o}{V_{\text{orms}}}\cdot\sqrt{2}\sin(\omega t)\,d\omega t\cdot f_{\text{swbuck}} \tag{15}$$

$$P_{\text{con\_buckD}} = \frac{2}{\pi}\cdot\int_0^{\theta}\frac{\frac{P_o}{V_{\text{orms}}}\cdot\sqrt{2}\sin(\omega t)}{2}\cdot\left[R_{ak}\cdot\frac{\frac{P_o}{V_{\text{orms}}}\cdot\sqrt{2}\sin(\omega t)}{2}+V_f\right]\cdot[1-M\,|\sin(\omega t)|]\,d\,\omega t \tag{16}$$

$$P_{Lo} = \frac{1}{\pi}\cdot\int_0^{\pi}\left[\frac{P_o}{V_{\text{orms}}}\sqrt{2}\sin^2(\omega t)\right]^2\cdot R_{Lo}\,d\,\omega t. \tag{17}$$

IGBTs S_c and S_d operate at line frequency, so this part only includes conduction loss.

$$P_{\text{con\_IGBT}} = \frac{1}{2\pi}\int_0^{\pi}\frac{P_o}{V_{\text{orms}}}\cdot\sqrt{2}\sin(\omega t)\times\left[R_{ce}\left(\frac{P_o}{V_{\text{orms}}}\cdot\sqrt{2}\sin(\omega t)\right)+V_t\right]d\,\omega t. \tag{18}$$

Then, the efficiency can be calculated as:

$$\eta = \frac{P_o}{P_o + P_{\text{Loss}}}. \tag{19}$$

The parameters of these inverters are listed in Table II. All the MOSFETs are selected as Infineon CoolMos SPW47N60C3, and diodes are selected as Cree SiC diode C3D20060D, and Fairchiled FGH30N60LSD are selected for IGBTs. Figs. 21 and 22 show the loss distribution at the rated power 2.5 kW under different input voltage conditions, where diode loss includes its conduction loss and the reverse recovery loss.

TABLE II
PARAMETERS OF ALL THE INVERTERS

Rated Power	Grid Voltage	Grid Frequency	Input Voltage	Switching Frequency
2.5 kW	*240 V_{ac}*	*60 Hz*	*200 – 500 V*	*50 kHz*

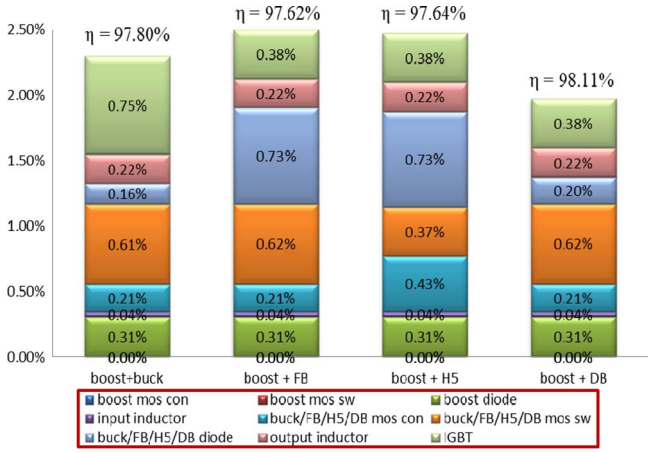

Fig. 21. Loss distribution in three inverters when $V_{\text{in}} = 400$ V.

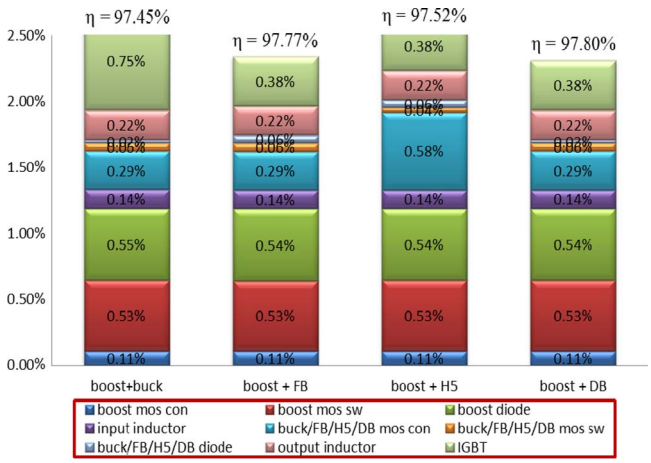

Fig. 22. Loss distribution in three inverters when $V_{\text{in}} = 200$ V.

When $V_{\text{in}} = 400$ V, only the buck/FB/H5/DB mode operates, thus all the boost-related losses are close to zero. In the FB and the H5 inverters, the diode reverse recovery is dominant because of the anti-paralleled diodes with IGBTs. Since the MOSFETs in H5 have lower voltage stress than which in buck and FB, its switching loss of MOSFETs is smaller than the other two. However, its conduction loss is larger because there are two MOSFETs in series. The loss due to IGBTs in buck type is higher than the other two, because there are always two IGBTs operating together. This can give the idea that if buck type inverter can change the IGBTs in unfolding circuit to MOSFETs, the efficiency in that type would be even higher.

When $V_{\text{in}} = 200$ V, both buck mode and boost mode operate. Because of the uniformity, all the boost-related losses are the same. Due to high input current, the boost diode's conduction loss is high. Different with high input voltage case, the

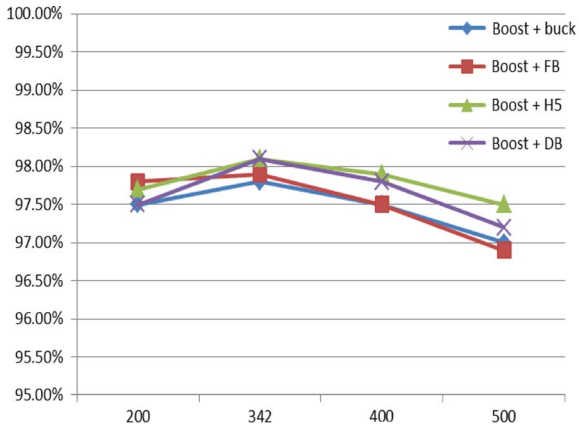

Fig. 23. CEC efficiency of four inverters under different input voltage condition.

switching loss in buck/FB/H5/DB becomes less on account of lower voltage stress.

It can be observed that the switching loss in the buck/FB/H5/DB mode is dominant if the input voltage is larger than the peak of the grid voltage because of the high voltage stress when the switches are off. In this case, modulation method A, reducing the carrier frequency for buck/FB/H5/DB mode, will help improve the efficiency. However, the switching loss in in buck/FB/H5/DB mode becomes not dominant if the input voltage is smaller than the peak of the grid voltage because of the small voltage stress when the switches are off. In this case, modulation method A, reducing the carrier frequency for buck/FB/H5/DB mode, will not help improve the efficiency significantly. Thus, a more complicated modulation method, changing the carrier's frequency based on the input voltage, can be proposed. That will be discussed in the future papers. Currently, modulation method B, reducing the carrier magnitude for buck/FB/H5/DB mode but keeping the same frequency, is implemented.

Fig. 23 shows the calculated California Energy Commission (CEC) efficiency, which is a weighted efficiency under different power levels calculated as (20), of these four inverters

$$\eta_{\mathrm{CEC}} = 0.04\eta_{10\%} + 0.05\eta_{20\%} + 0.12\eta_{30\%} + 0.21\eta_{50\%} + 0.53\eta_{75\%} + 0.05\eta_{100\%}. \quad (20)$$

It is easy to observe that boost with H5 type inverter gives the highest CEC efficiency in most of the conditions, because H5 type will give the advantages of lower switching loss as explained before. In particular, in light load condition, the conduction loss is no longer dominant, and H5's superiority gives higher efficiency.

VI. Simulation and Experimental Results

Fig. 24–27 show the simulation results of the proposed three different topologies with one advanced SPWM method B, reducing the carrier magnitude for buck/FB/H5/DB mode but keeping the same frequency. I_{grid} is the current sent to the grid. V_{boost}, V_{buck}, S_3, S_a, S_b, S_c, and S_d represent the PWM signals for the corresponding switches. V_{boostc}, V_{buckc}, and $\mathrm{ABS}(V_{\mathrm{m}})$

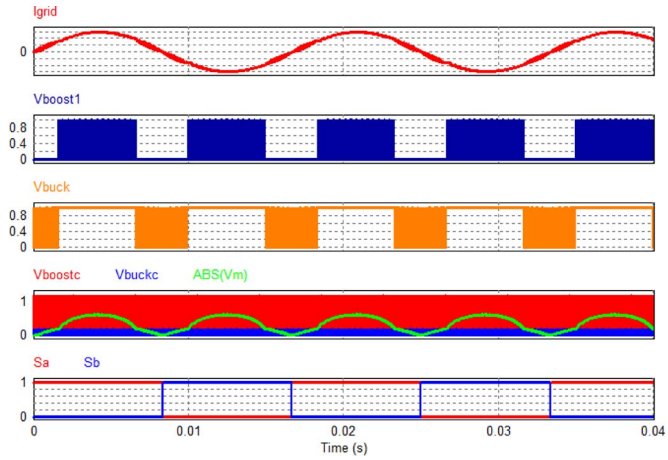

Fig. 24. Simulation results of boost with buck.

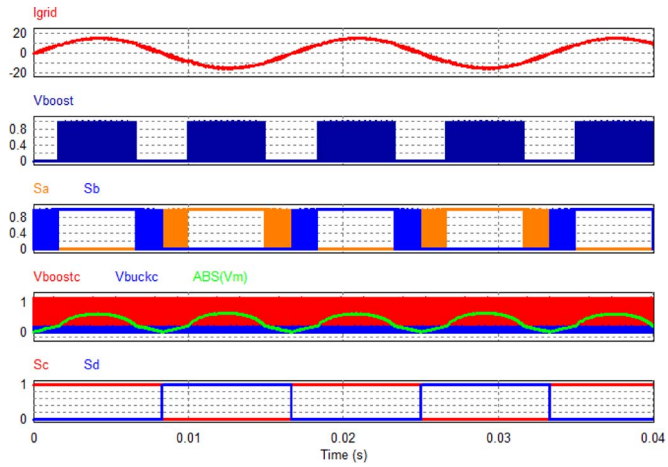

Fig. 25. Simulation results of boost with full bridge.

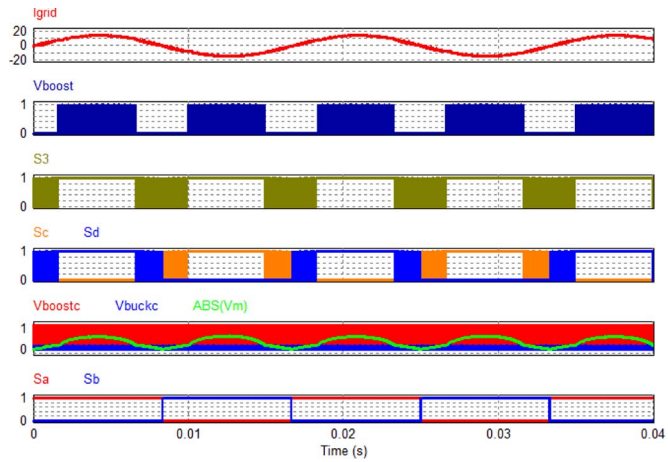

Fig. 26. Simulation results of boost with H5.

represent boost carrier, buck carrier, and the compensated signal, respectively. The switches operating modes are clearly illustrated, which match the analysis shown in Fig. 9–12. The boost mode and the buck/FB/H5/DB mode never operate simultaneously. And the advanced SPWM method B, reducing the carrier magnitude for buck/FB/H5/DB mode, is also well illustrated, which match the analysis shown in Fig. 15.

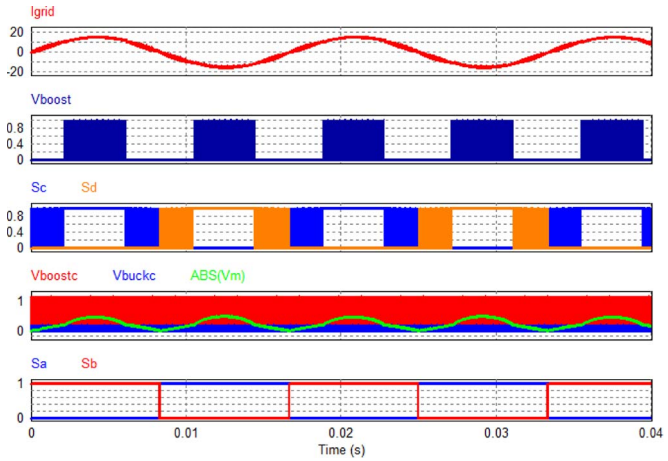

Fig. 27. Simulation results of boost with dual buck.

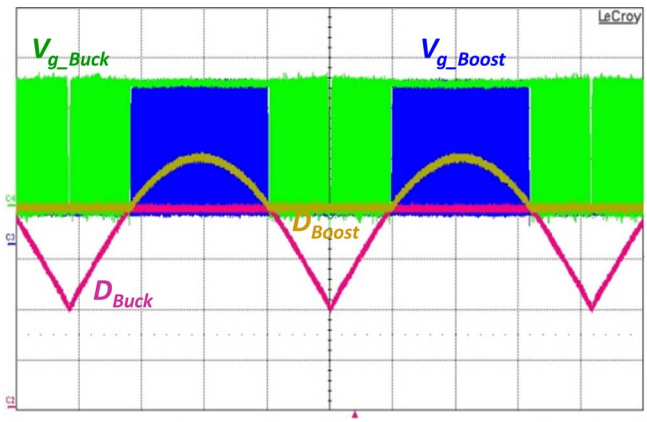

Fig. 28. Experimental results of gate signal and duty cycle.

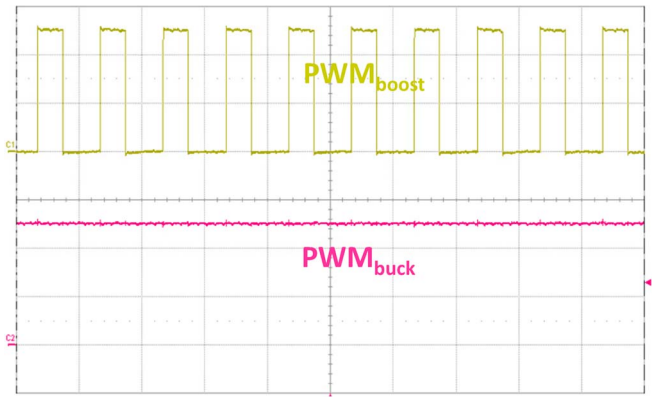

Fig. 29. PWM signals of advanced double-carrier with different frequency in boost mode.

From Fig. 28–33, the experimental results are shown. For the controller implementation, Texas Instruments' 32 bit floating point digital signal processor (DSP) TMS320F28335-based custom made digital control board was used. Fig. 28 shows the duty cycle and the modulated PWM signals for both of the operating modes. It is easy to observe that the buck switch is always on if the boost switch is operating on and off, and the boost switch is always off if the buck switch is operating on and off. Figs. 29 and 30 represent the PWM signals with advanced double-carrier with different frequency in boost mode and

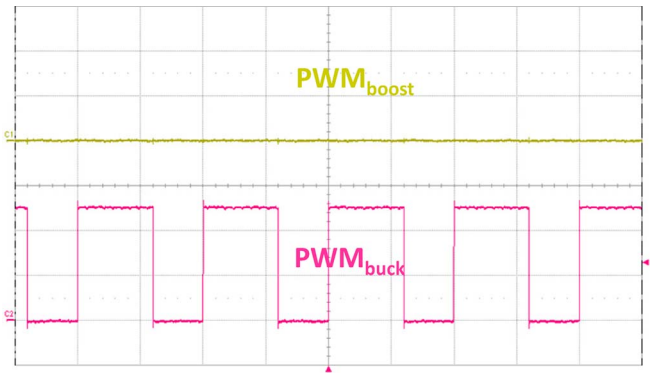

Fig. 30. PWM signals of advanced double-carrier with different frequency buck/FB/H5/DB mode.

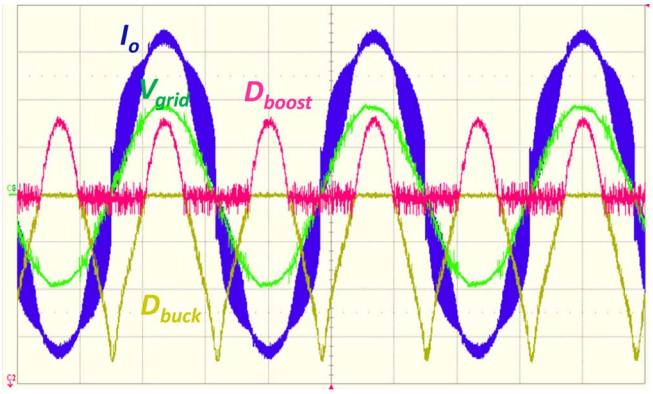

Fig. 31. Experimental results of voltage, current, and duty cycle with small input voltage.

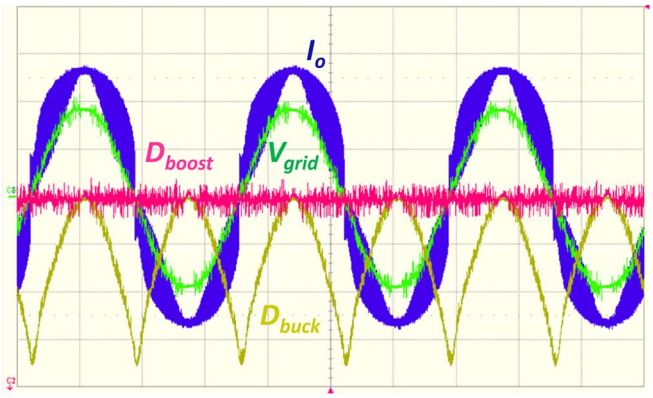

Fig. 32. Experimental results of voltage, current and duty cycle with middle input voltage.

buck/FB/H5/DB mode, respectively. Since there is no way to show the carrier waveform which is implemented using internal counters in the DSP via an oscilloscope, these two figures still represent the validity of the modulation method A. However, for modulation method B and C, there is no straightforward waveform to show their validity, but they can be implemented in DSP easily.

Fig. 31–33 show the experimental results with different input voltage condition of boost with FB inverter implemented by double-carrier with the same frequency and magnitude. Each topology in this paper would have the same experimental results since they are all boost part plus buck type inverters. It can be

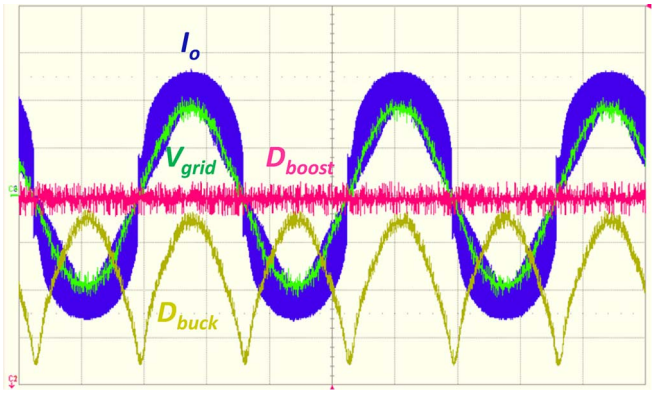

Fig. 33. Experimental results of voltage, current and duty cycle with large input voltage.

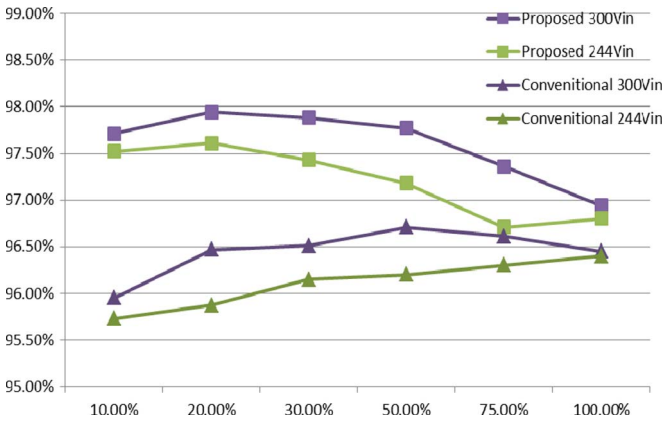

Fig. 34. Efficiency comparisons of the proposed inverter and the traditional inverter under different input and load condition.

observed clearly that if the inverter runs in boost mode, the duty cycle of buck switch is always one, and if the inverter runs in buck mode, the duty cycle of buck switch is always zero.

Testing with the traditional boost and the FB combination using conventional control methods with constant voltages on C_L has also been conducted. Fig. 34 shows efficiency comparisons of the proposed and the traditional control methods under different input and load conditions. The results demonstrate the proposed inverter improves the efficiency by 2% particularly at light power condition, because the switching losses become dominant in this case. During heavy power condition, the current becomes large and the conduction losses become dominant, and the proposed inverter still performs better than the conventional one. Nearly 1% efficiency could be improved in heavy power conditions.

VII. Summary

Three dual-mode double-carrier-based SPWM inverters have been proposed. With both step-up and step-down functions, this type of inverter can achieve high efficiency in a wide range because only one switch operates at the PWM frequency at a time. Along with that, three advanced double-carrier modulation methods are proposed. One of them can help improve the efficiency, and one of them can help increase the bandwidth and gain, and the last one takes the advantage of both. The efficiencies and the detailed loss distribution of these inverters with one of the advanced modulation method are compared. Based on the comparison, boost mode with H5 PV inverter gives highest CEC efficiency in most cases, because it has lowest switching loss. Finally, both simulation and experiment results validate the three topologies and the three advanced modulation methods. And the experimental results show that the proposed dual-mode double-carrier-based SPWM inverter can improve the efficiency by 2% than the traditional constant dc bus voltage solutions.

References

[1] J. P. Benner and L. Kazmerski, "Photovoltaics gaining greater visibility," *IEEE Spectr.*, vol. 36, no. 9, pp. 34–42, Sep. 1999.

[2] G. Velasco-Quesada, F. Guinjoan-Gispert, R. Pique-Lopez, M. Roman-Lumbreras, and A. Conesa-Roca, "Electrical PV array reconfiguration strategy for energy extraction improvement in grid-connected PV syst," *IEEE Trans. Ind. Electron.*, vol. 56, no. 11, pp. 4319–4331, Nov. 2009.

[3] J. T. Bialasiewicz, "Renewable energy systems with photovoltaic power generators: Operation and modeling," *IEEE Trans. Ind. Electron.*, vol. 55, no. 7, pp. 2752–2758, Jul. 2008.

[4] X. Guan, Z. Xu, and Q. S. Jia, "Energy-efficient buildings facilitated by microgrid," *IEEE Trans. Smart Grid*, vol. 1, no. 3, pp. 243–252, Dec. 2010.

[5] H. Kanchev, D. Lu, F. Colas, V. Lazarov, and B. Francois, "Energy management and operational planning of a microgrid with a PV-based active generator for smart grid applications," *IEEE Trans. Ind. Electron.*, vol. 58, no. 10, pp. 4583–4592, Oct. 2011.

[6] H. Patel and V. Agarwal, "Maximum power point tracking scheme for PV systems operating under partially shaded conditions," *IEEE Trans. Ind. Electron.*, vol. 55, no. 4, pp. 1689–1698, Apr. 2008.

[7] H. Beltran, E. Bilbao, E. Belenguer, I. Etxeberria-Otadui, and P. Rodriguez, "Evaluation of storage energy requirements for constant production in PV power plants," *IEEE Trans. Ind. Electron.*, vol. 60, no. 3, pp. 1225–1234, Mar. 2013.

[8] D. Casadei, G. Grandi, and C. Rossi, "Single-phase single-stage photovoltaic generation system based on a ripple correlation control maximum power point tracking," *IEEE Trans. Energy Convers.*, vol. 21, no. 2, pp. 562–568, Jun. 2006.

[9] Y. Huang, M. Shen, F. Z. Peng, and J. Wang, "Z-source inverter for residential photovoltaic systems," *IEEE Trans. Power Electron.*, vol. 21, no. 6, pp. 1776–1782, Nov. 2006.

[10] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1292–1306, Sep.–Oct. 2005.

[11] T. Kerekes, R. Teodorescu, P. Rodríguez, G. Vázquez, and E. Aldabas, "A new high-efficiency single-phase transformerless PV inverter topology," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 184–191, Jan. 2011.

[12] F. Tian, H. Al-Atrash, R. Kersten, C. Scholl, K. Siri, and I. Batarseh, "A single-staged PV array-based high-frequency link inverter design with grid connection," in *Proc. Appl. Power Electron. Conf. Expo.*, Mar. 2006, pp. 19–23.

[13] J.-M. Kwon, K.-H. Nam, and B.-H. Kwon, "Photovoltaic power conditioning system with line connection," *IEEE Trans. Ind. Electron.*, vol. 53, no. 4, pp. 1048–1054, Aug. 2006.

[14] E. Koutroulis and F. Blaabjerg, "Design optimization of transformerless grid-connected PV inverters including reliability," *IEEE Trans. Ind. Electron.*, vol. 28, no. 1, pp. 325–335, Jan. 2013.

[15] C. Meza, D. Biel, J. Negroni, and F. Guinjoan, "Boost-buck inverter variable structure control for grid-connected photovoltaic systems with sensorless MPPT," in *Proc. IEEE Int. Symp. Ind. Electron.*, 2005, pp. 657–662.

[16] M. Calais, J. Myrzik, T. Spooner, and V. G. Agelidis, "Inverter for single-phase grid connected photovoltaic systems—An overview," in *Proc. IEEE Power Electron. Spec. Conf.*, Feb. 2002, vol. 4, pp. 1995–2000.

[17] D. Biel, G. Guinjoan, E. Fossas, and J. Chavarria, "Sliding-mode control design of a boost-buck switching converter for AC signal generation," *IEEE Trans. Circuits Syst.*, vol. 51, no. 8, pp. 1539–1551, Aug. 2004.

[18] B. Yang, W. Li, Y. Zhao, and X. He, "Design and analysis of a grid-connected photovoltaic power system," *IEEE Trans. Power Electron.*, vol. 25, no. 4, pp. 992–1000, Apr. 2010.

[19] Z. Zhao, M. Xu, Q. Chen, J. Lai, and Y. Cho, "Derivation, analysis, implementation of a boost-buck converter based high-efficiency PV inverter," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1304–1313, Mar. 2012.
[20] Z. Zhao, M. Xu, Q. Chen, J. Lai, and Y. Cho, "Derivation, analysis and implementation of boost-buck converter based high-efficiency PV inverter," *IEEE Tran. Power Electron.*, vol. 27, pp. 1304–1313, Mar. 2012.
[21] German Patent H5-Topology: DE 10 2004 030 912 B3, Jan. 19, 2006.
[22] G. Carrara, S. Gardella, M. Marchesoni, R. Salutari, and G. Sciutto, "A new multilevel PWM method: A theoretical analysis," *IEEE Trans. Power Electron.*, vol. 7, no. 3, pp. 497–505, Jul. 1992.
[23] D. Floricau, E. Floricau, and G. Gateau, "New multilevel converters with coupled inductors: Properties and control," *IEEE Trans. Ind. Electron.*, vol. 58, no. 12, pp. 5344–5351, Dec. 2011.
[24] Y. Ounejjar, K. Al-Haddad, and L.-A. Grégoire, "Packed U cells multilevel converter topology: Theoretical study and experimental validation," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1294–1306, Apr. 2011.
[25] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, and M. A. rez Pé, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010.
[26] G. Buticchi, E. Lorenzani, and G. Franceschini, "A five-level single-phase grid-connected converter for renewable distributed systems," *IEEE Trans. Ind. Electron.*, vol. 60, no. 3, pp. 906–918, Mar. 2013.

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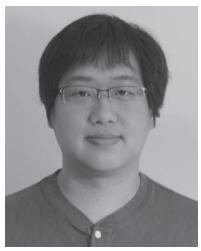

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