Lab 1

Name: Mihir Malikali Mithani.

Enrollment No: 92301733025

CO1: Develop fundamentals in fabrication of MOSFETs and MOS transistor

CO2: Analyze MOS inverters with its static and switching characteristics

CO3: Analyze Combinational and Sequential MOS logic circuit

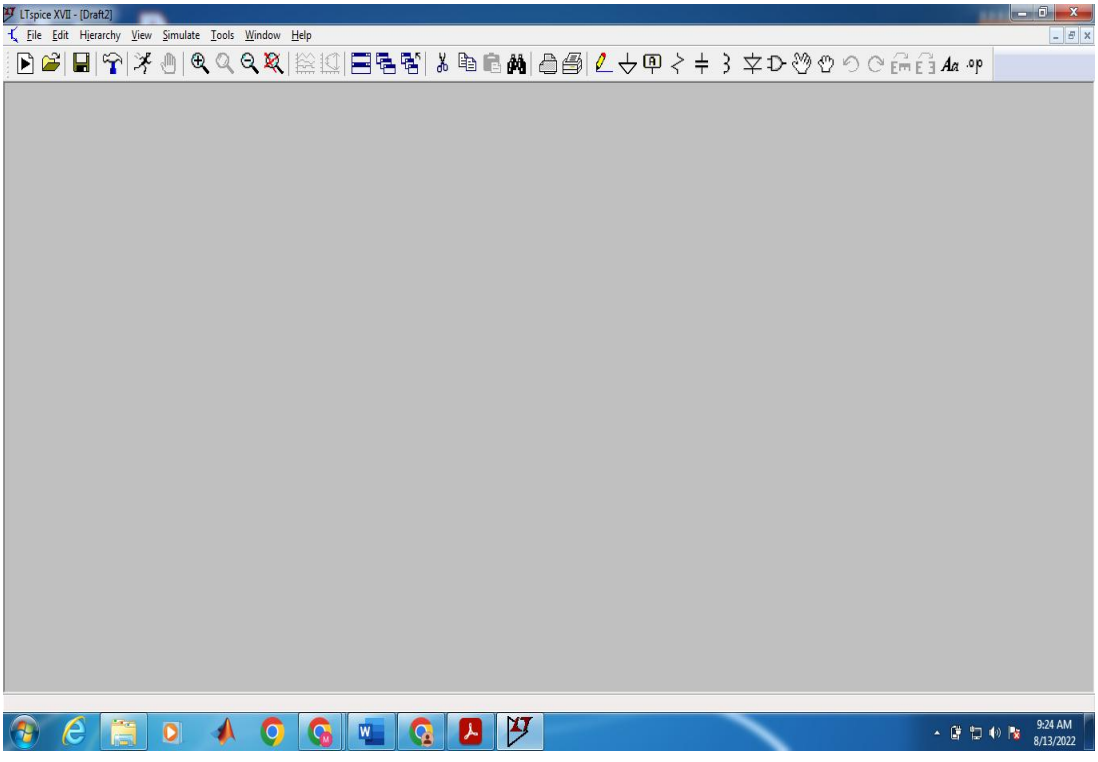
Experiment 1: Introduction to LTSPICE Tool & Microwind Tool

Basic Circuit Simulation with LTspice

A flexible, precise, and cost-free circuit simulator for Windows and Mac is called LTSpice. It introduces AC and DC simulation and details the analysis of digital circuits' output signals.

Getting Started

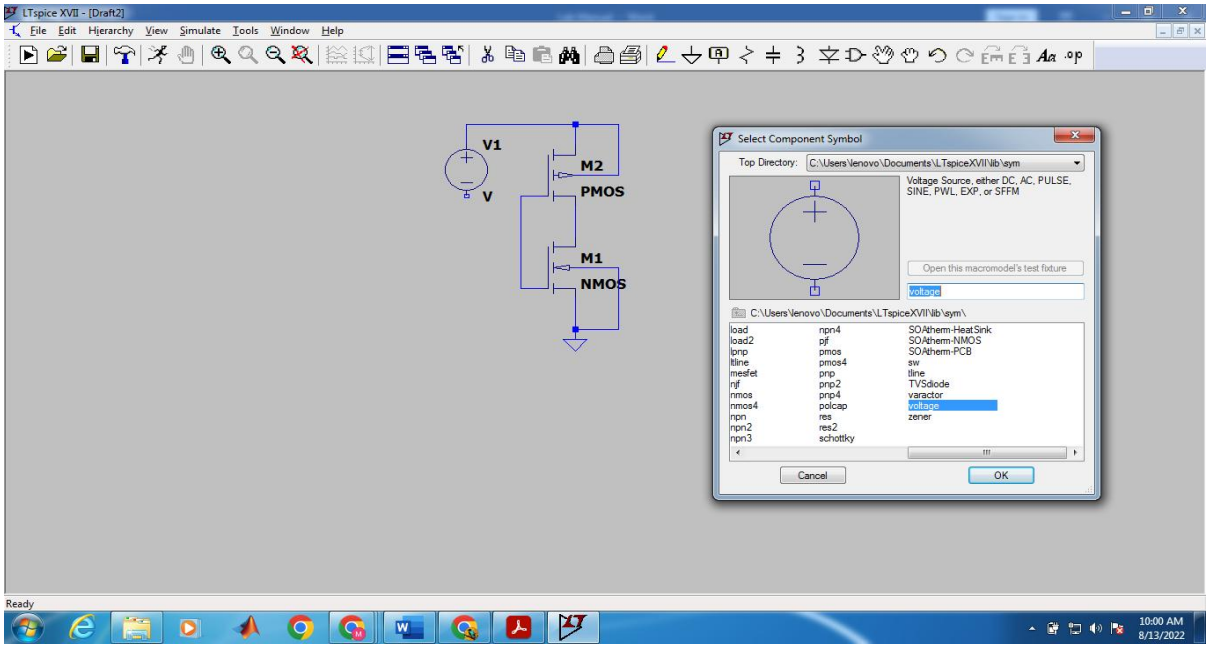
Visit the Linear Technology design tools website (www.analog.com) to download a copy of the LTSpice executable. When the software is installed and running, you will see a screen similar to the one below. You must first make a new draught by clicking the tiny red "LT" icon next to the file option in order to start creating a schematic:



You may begin adding and altering components from here, but let's first go through some keyboard shortcuts. The majority of these are located on the toolbar above the circuit window or, if you prefer, in the "Edit" and "View" menus. There is a significant collection of resources, including further usage examples, in the Help menu if you ever run into trouble using LTSpice. Some hotkeys for building your schematic are listed below:

R: Place Resistor	**F2:** Component Menu	**F7:** Move without Wires
C: Place Capacitor	**F3:** Draw Wire	**F8:** Drag/Move with wires
L: Place Inductor	**F4:** Label Net	**F9:** Undo (Shift + F9)
D: Place Diode	**F5:** Delete	**CTRL+R:** Rotate
G: Place Ground	**F6:** Copy	**CTRL+E:** Mirror

CTRL+Z and CTRL+B are used to zoom in and out, respectively; CTRL+Z does not undo. By pressing the spacebar, you may "zoom to fit," which elegantly adjusts the viewing area. Launch a new schematic editor and begin the circuit simulation using LTSpice. Click the new schematic under File. A CMOS inverter must have the following components: NMOS, PMOS, a voltage source, wire, capacitor, and ground. Place the NMOS and PMOS in the schematic now. When you click on the component symbol, a list of component symbols will appear for you to choose from. Choose NMOS and PMOS.



On the schematic, put it anywhere. The following step is to access the component menu once more and select a different voltage source from the component menu's top level (you can save time by using the copy hotkey after placing the first).

DC Characteristics of CMOS Inverter

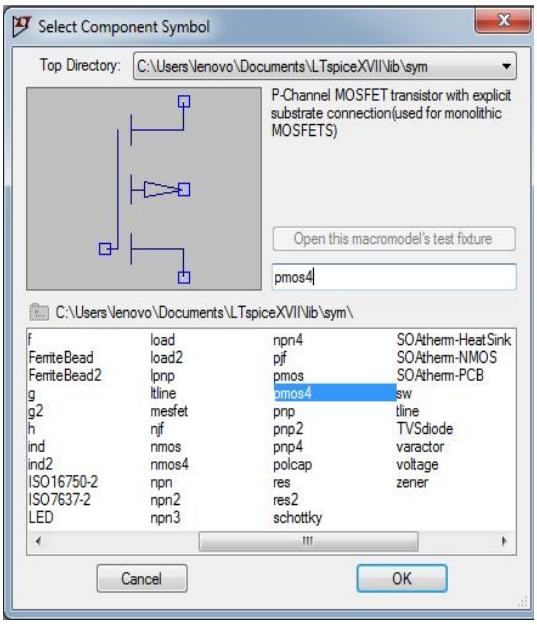
With the help of the LTSpice circuit modeling tool, we will simulate the CMOS inverter. In order to simulate the CMOS inverter circuit, we will use the BSIM4 Spice model.

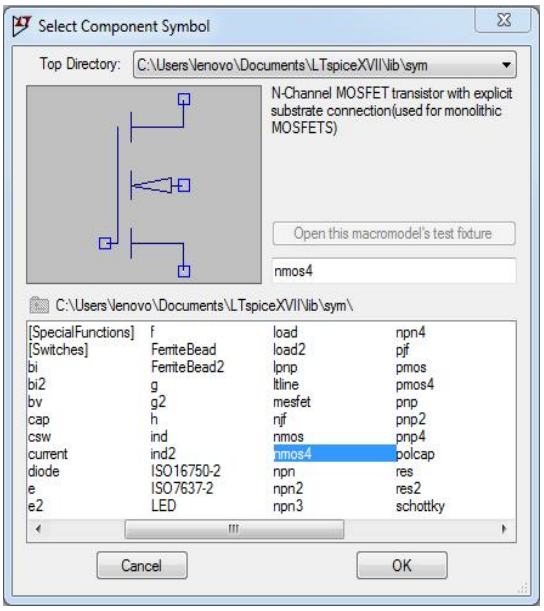
What is BSIM4?

BSIM, also known as the Berkeley short-channel IGFET model, first gained popularity in 1987. The following steps are involved in modeling any device.

- Processing or fabrication technique.
- Device simulation emphasizes device physics.
- Characterization of the device.
- Transform into software programming.

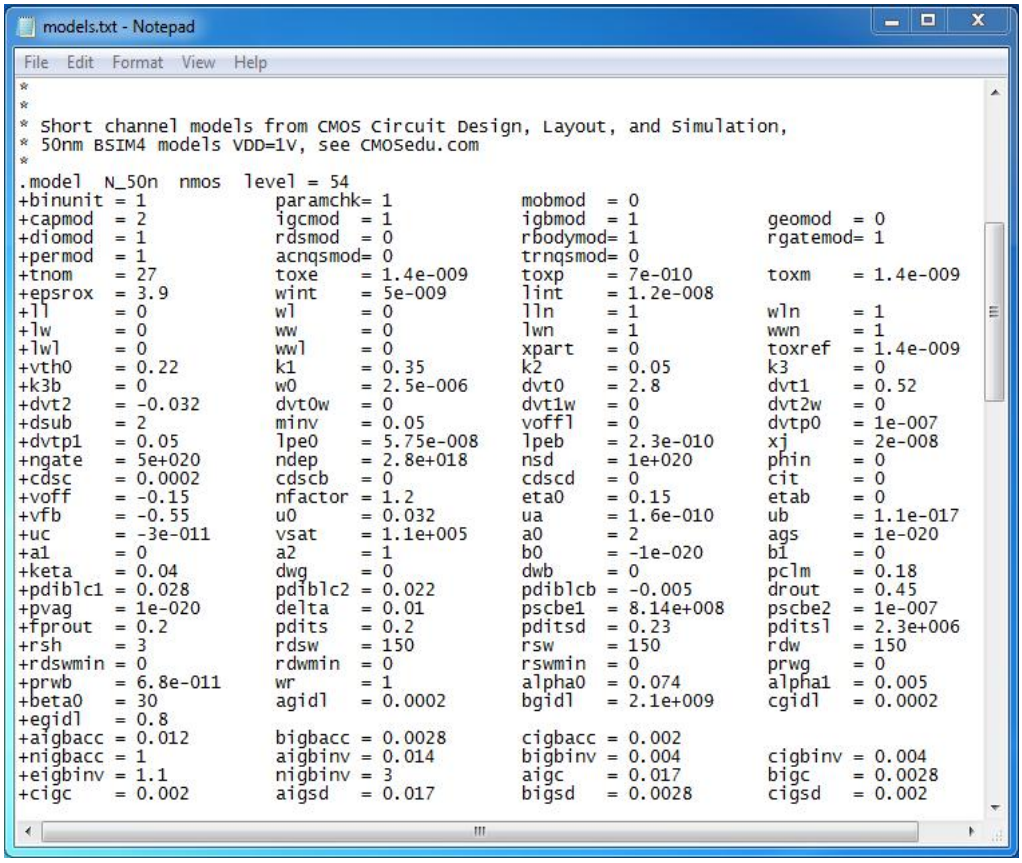
The first industrially accepted MOSFET model, BSIM, is also the first CMC standard model in TM12, allowing for effective macro modeling. The BSIM model's success can be attributed to Professor Don Peterson giving the industry free use of the Spice model. 90% of integrated circuits are made using CMOS technology, and CMOS inverters are the fundamental component of every digital circuit. Use the 4 terminal NMOS and PMOS device, which uses the symbol to indicate the substrate is p-type to n channel, to place the PMOS and NMOS on the schematic with the MOSFET terminal source connected to the bulk. Set the PMOS and NMOS sizes by selecting the MOSFET from the context menu, as seen in the image below. According to the BSIM model file used in our experiment, give the model the names P1 and N1.

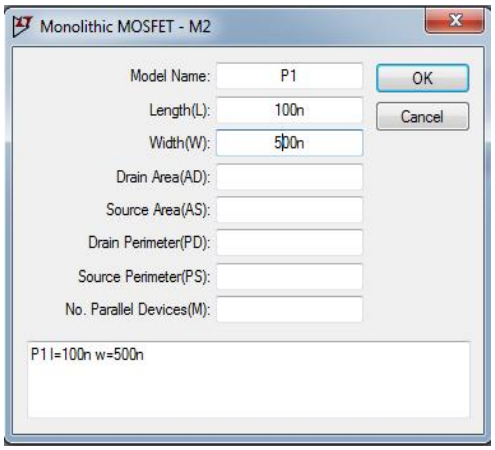


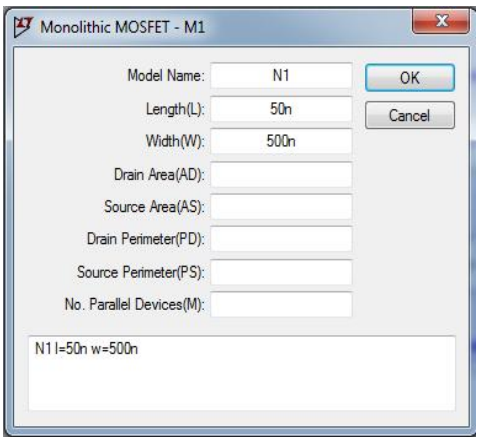


The logical operation of CMOS inverter

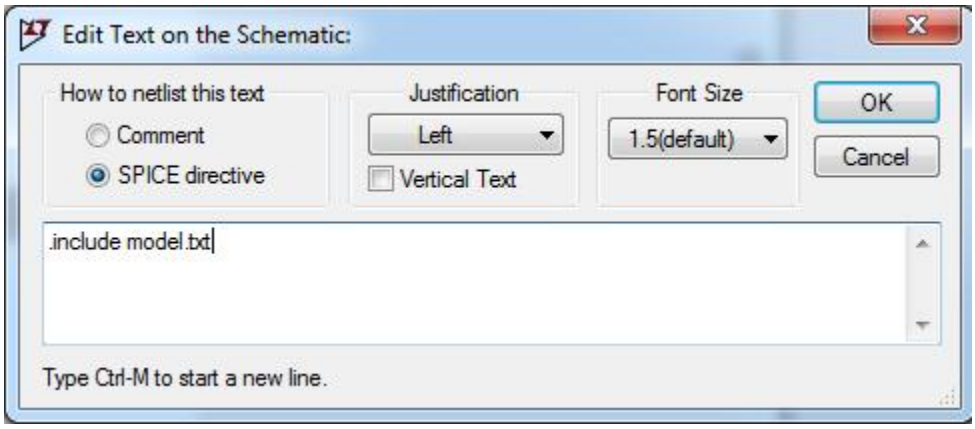
Input	Output
Low	High
High	Low





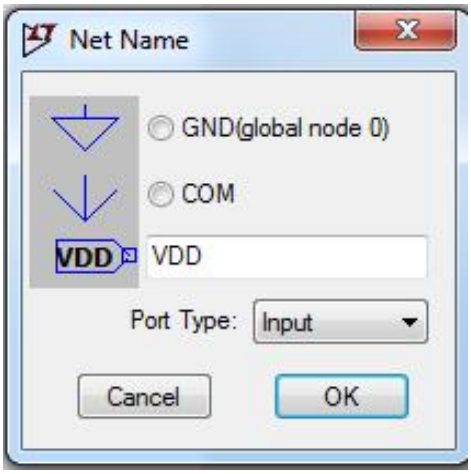


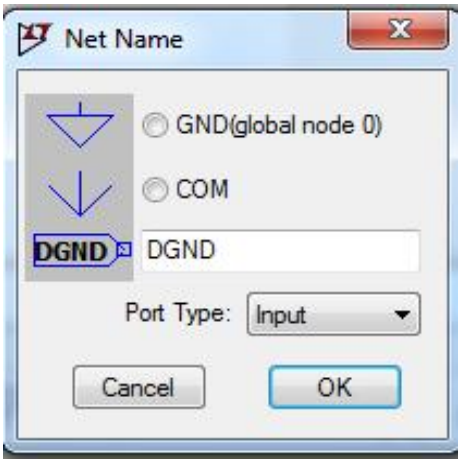
To include the BSIM model file, Go to edit and select SPICE Directive'S' and then type .include model.txt.

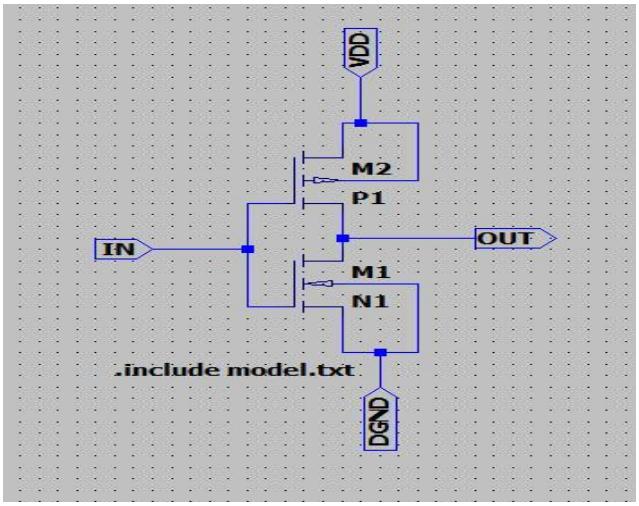


The VDD and digital ground must be defined as input pins in this work, as illustrated in the fig below. Give an input or output port type definition.

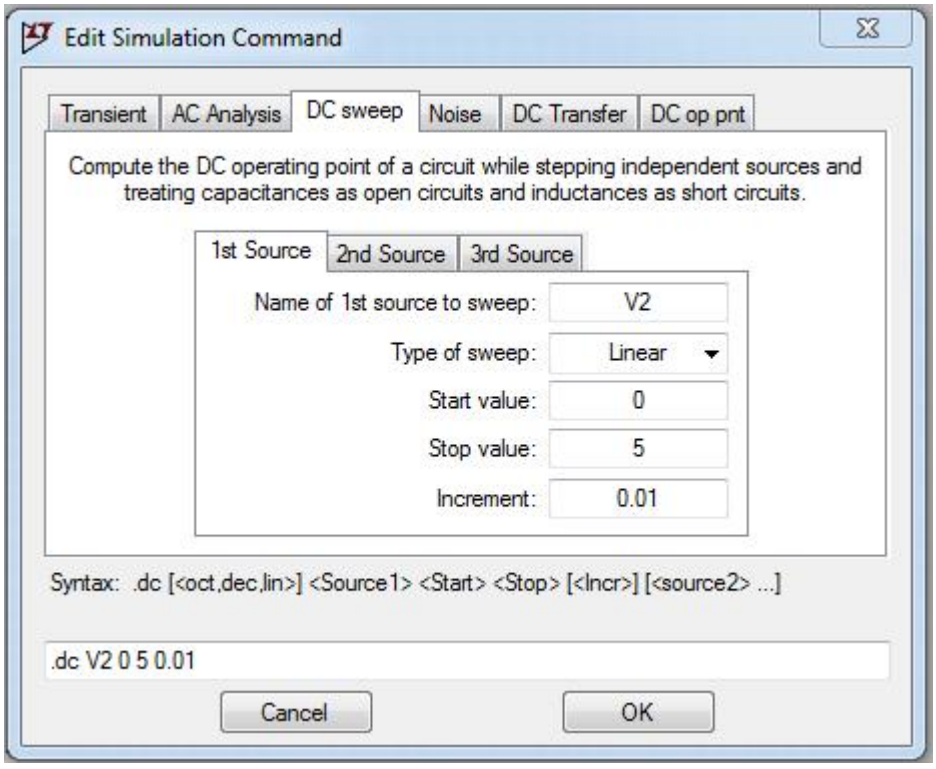
Label the output as OUT and the input as IN. When the CMOS inverter input is linked to ground, the output is pushed through the ground by the NMOS device and is pulled to VDD by the PMOS device when the input is connected to VDD.



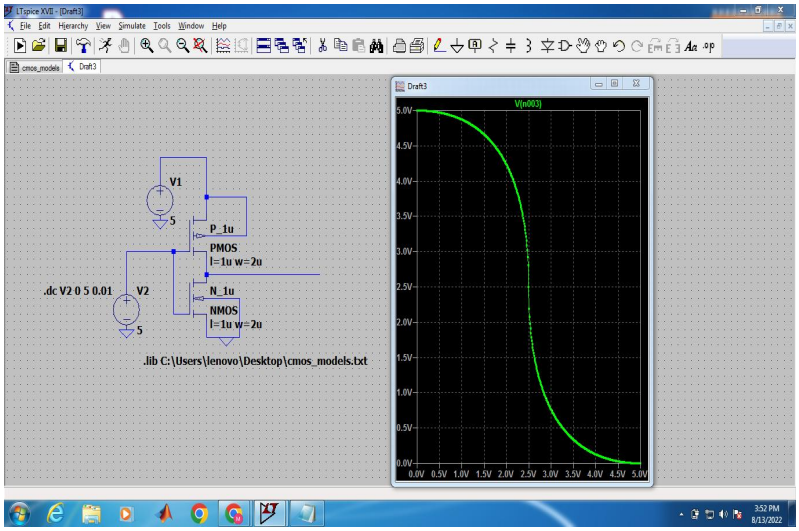




The first source of sweep will be V2, the start value to be 0, and stop value as 5 with 0.01 increment.



Let us place the SPICE analysis on the schematic and run the simulation. Region 1 of the DC characteristics, the input voltage is low, the NMOS is OFF, and PMOS is ON. As the input voltage increases, both the NMOS and PMOS turn ON. When the input voltage increased further, PMOS turns OFF, and NMOS fully turns ON.

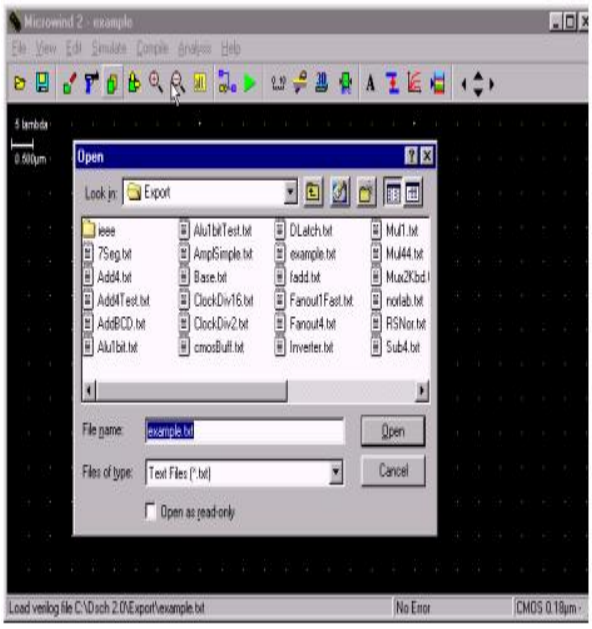


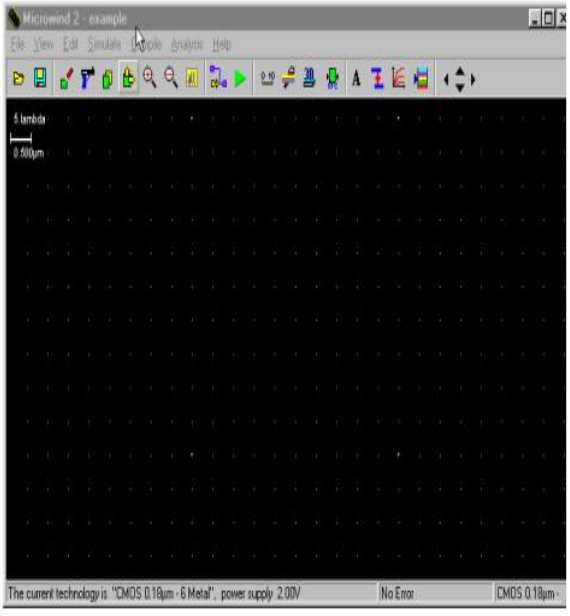
Microwind Tool:

The MICROWIND2 program allows the student to design and simulate an integrated circuit at physical description level. The package contains a library of common logic and analog ICs to view and simulate. MICROWIND2 includes all the commands for a mask editor as well as original tools never gathered before in a single module (2D and 3D process view, VERILOG compiler, tutorial on MOS devices). You can gain access to Circuit Simulation by pressing one single key. The electric extraction of your circuit is automatically performed and the analog simulator produces voltage and current curves immediately.

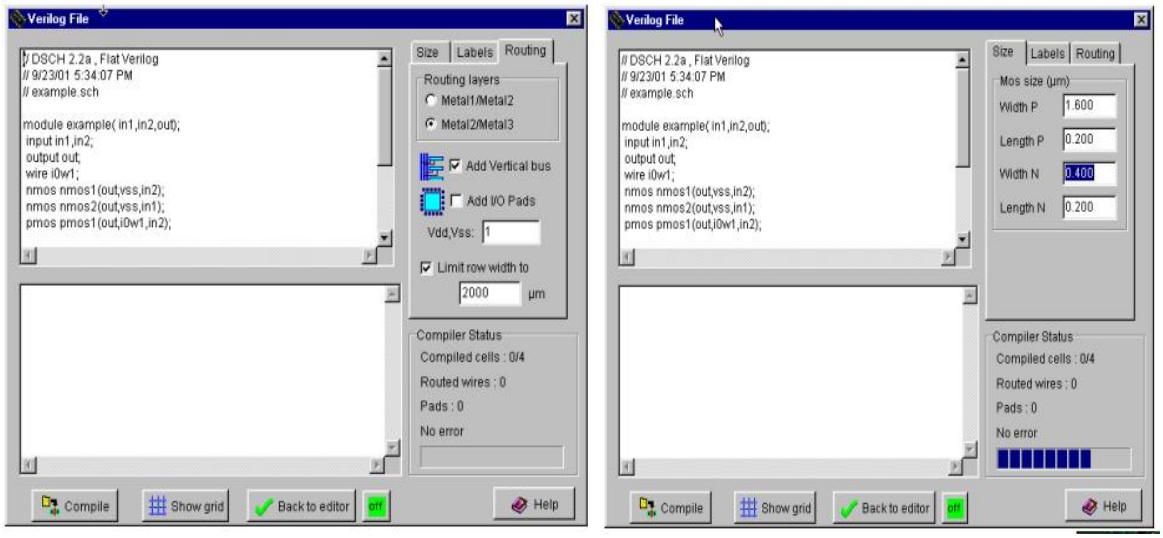
Open the layout editor window in Microwind. Click File -> Select Foundry and select X.rul. This sets your layout designs in X technology.

Click on Compile -> Compile Verilog File. An Open Window appears. Select the .txt verilog file saved before and open it.



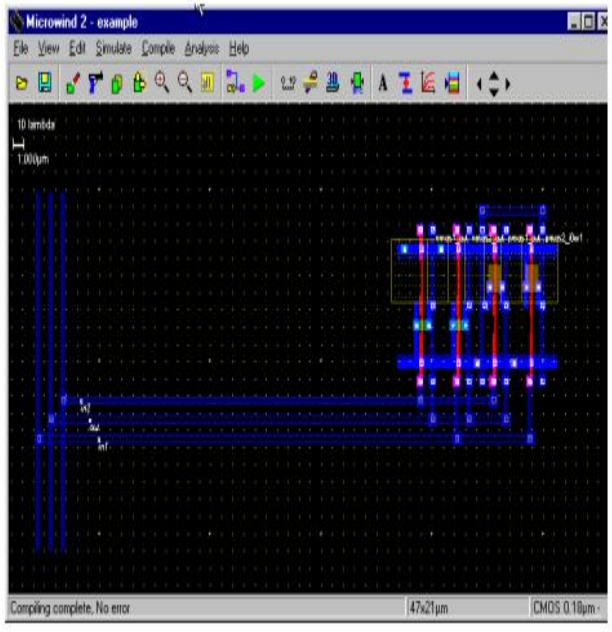


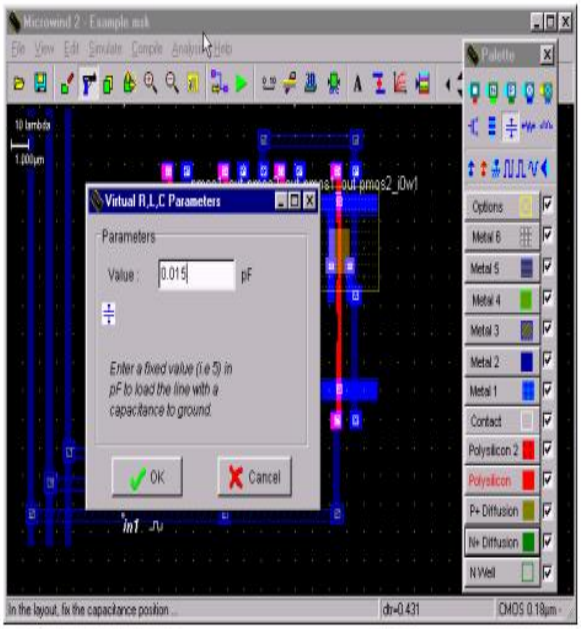
After selecting the .txt file, a new window appears called Verilog file. Click on Size on the right top menus. This shows up the NMOS and PMOS sizes. Set the sizes according to choose.



Click Compile and then Back to editor in the Verilog File Window. This creates a layout in layout editor window using automatic layout generation procedure.

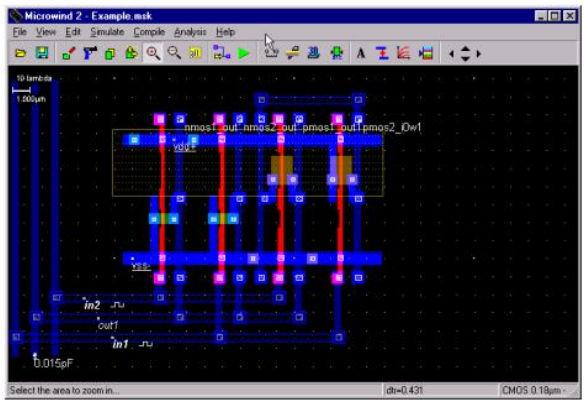
Add a capacitance to the output of the design. The value of the capacitance depends on your choice.

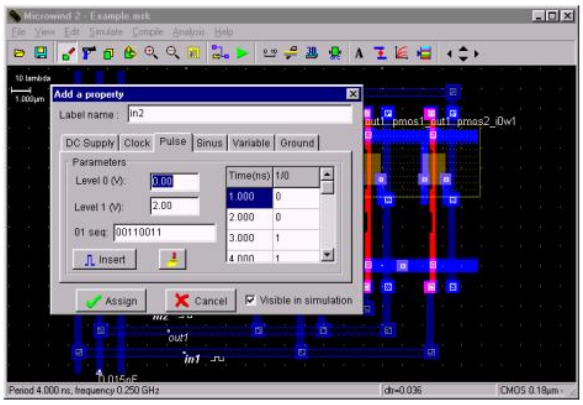




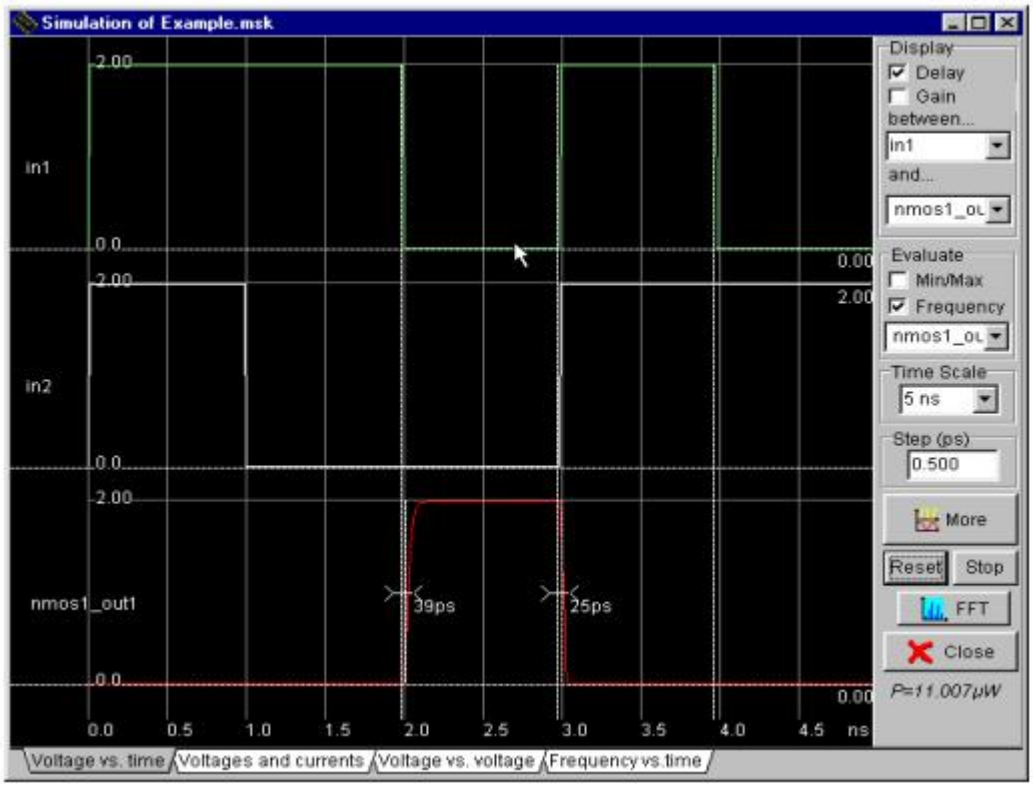
Click on OK. The capacitance is shown on the left bottom corner with a value of 0.015fF.

Click on the label marked In1. A window appears. Click on the Pulse option in the window. Insert a 01 sequence for that specific input and click on Insert. Then click on Assign. Perform this assignment on the other inputs.





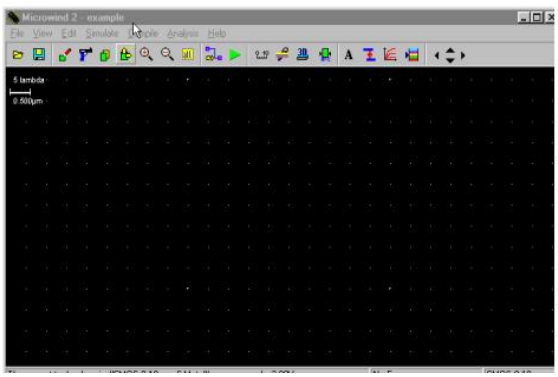
Click Simulate -> Run simulation. A simulation window appears with inputs and output, shows the tphl, tplh and tp of the circuit. The power consumption is also shown on the right bottom portion of the window. • If you are unable to meet the specifications of the circuit change the transistor sizes. Generate the layout again and run the simulations till you achieve your target delays.

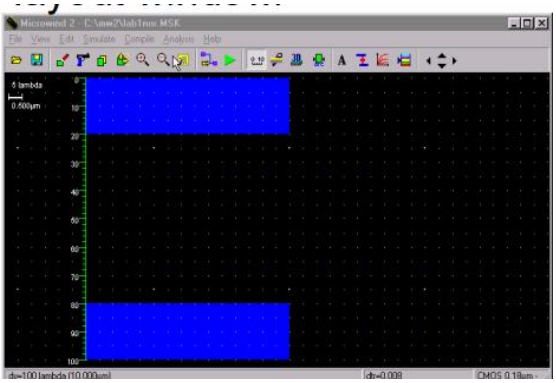


Design the layout manually

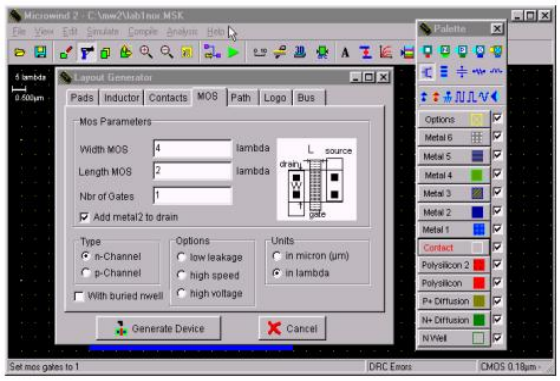
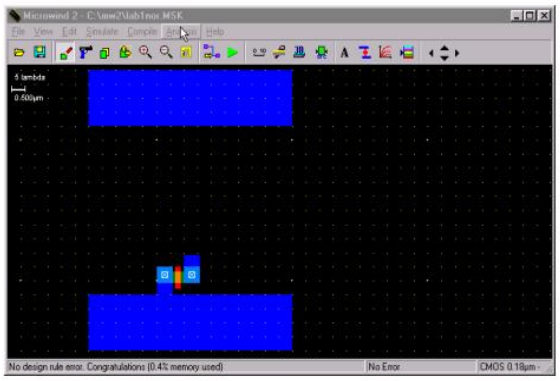
Open the layout editor window in Microwind. Click File -> Select Foundry and select X.rul

Vdd and GND rails are of Metal1. The top rail is used as Vdd and the bottom one as GND. Click on Metal 1 in the palette and then create the required rectangle in the layout window



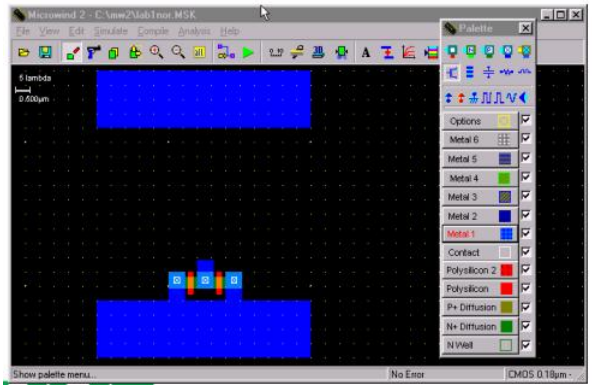
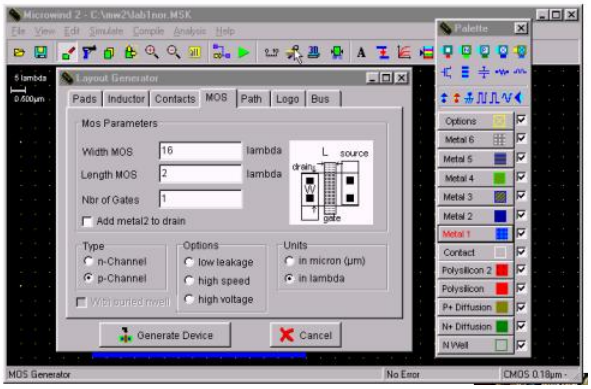


The next step is to build the NMOS transistors. Click on the transistor symbol in the palette. Set the W, L of the transistor. Then click on Generate device. The source of the transistor is connected to the GND rail

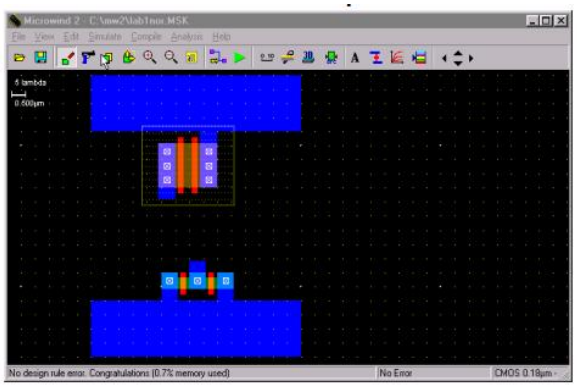
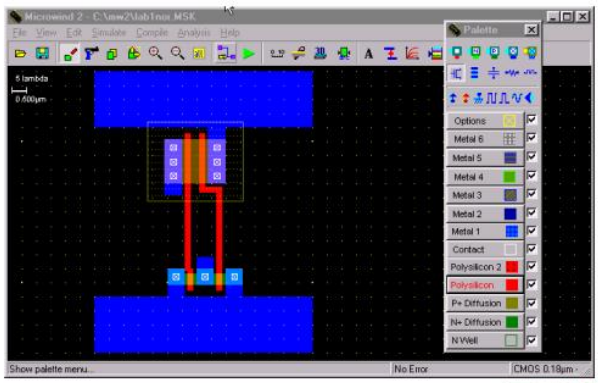
Create another NMOS and place it in parallel to the first NMOS device. We share the two devices' drain diffusions. A DRC check can be run by clicking on Analysis -> Design Rule Checker.

The next step is to place two PMOS transistors in series

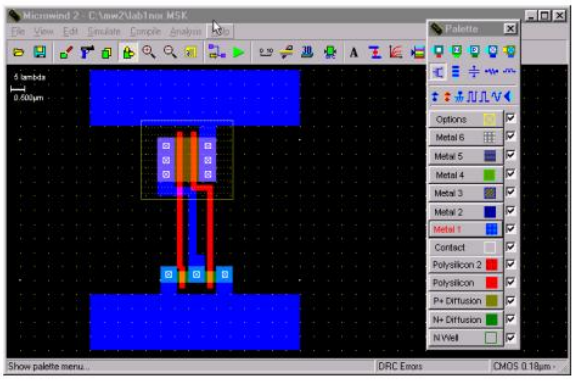



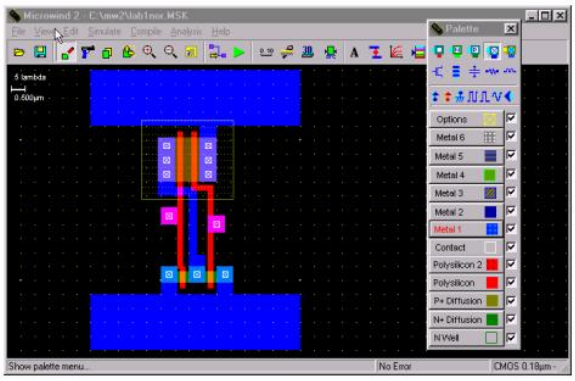
Place the PMOs transistor on layout close to the Vdd rail on the top. To construct two PMOS transistors in series, diffusions are shifted to a side and another poly line is added as second transistor. The diffusion is shared to save area and reduce capacitance.

The next step is to connect the inputs and the output of the two transistors.

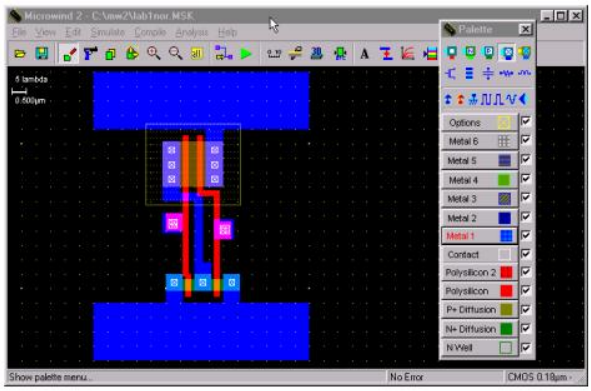



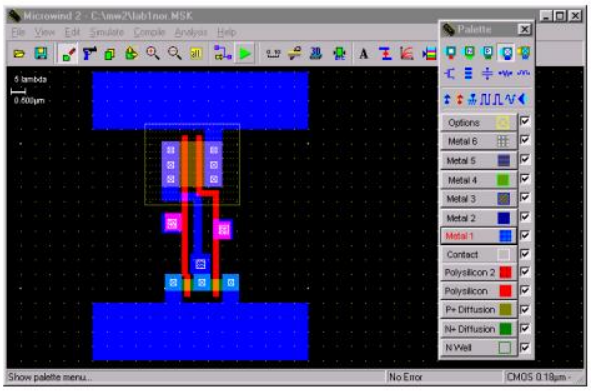
Poly inputs are connected. Metal output is connected. The next step is to connect the poly to metal1 and then to metal2. The first symbol in the first row of the palette is the poly to metal1 contact.



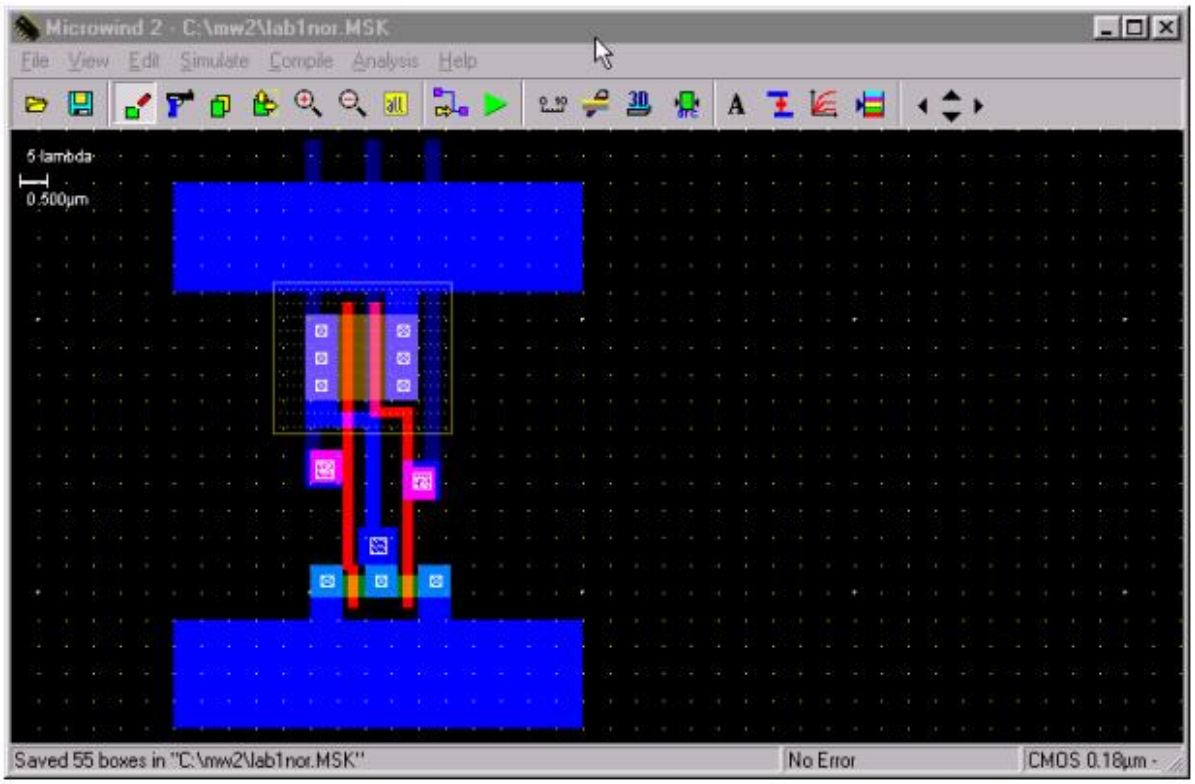


Then we connect the metal1 to metal2 contact to the previous contact. This is the 4th contact on the first row. The next step is to connect the output Metal1 to Metal2. Once again use the 4th contact in the first row.

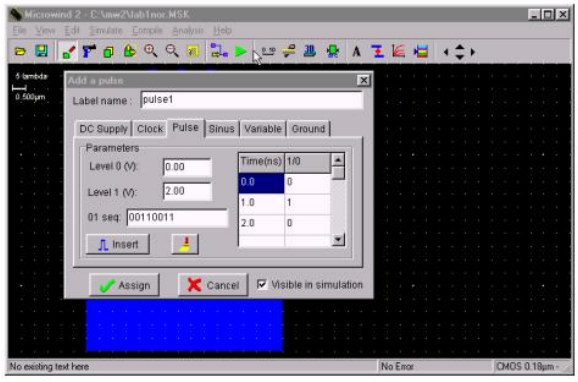


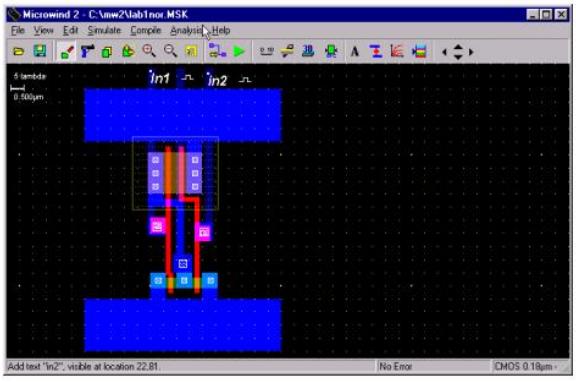


Now we connect metal2 to the two inputs and one output and bring them to the top to go out of the cell. Observe the two inputs (left & right) and an output (middle) above the Vdd rail in dark blue color.

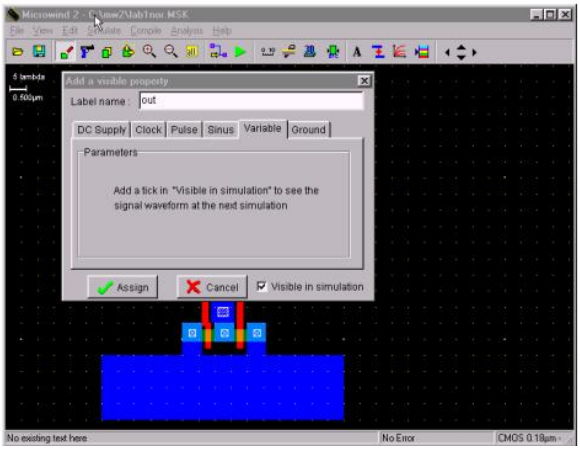


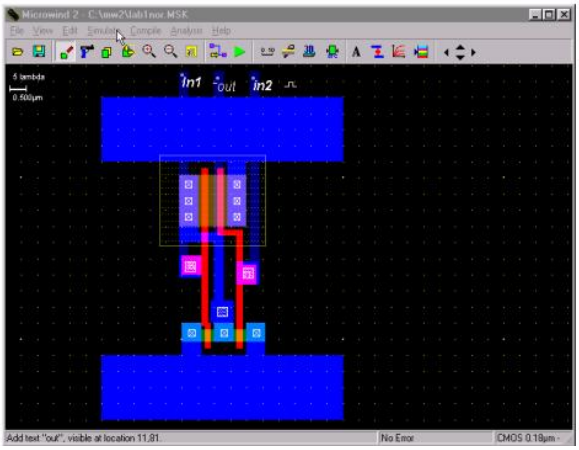
Now we label the inputs and output as In1, In2 and out. Click on Add a Pulse Symbol in the palette (5th from the right in the 3rd row). Then click on the metal2 of one of the inputs. A window appears. Change the name of the input signal. Insert 01 sequences and click on Insert. The click on Assign. Similarly assign the 2nd input a pulse.





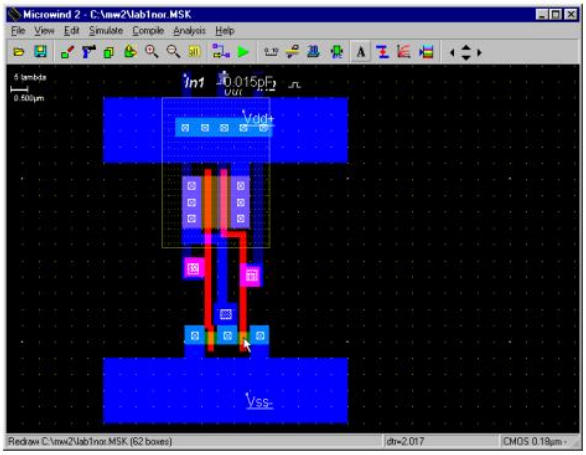
Now select the Visible Node symbol from the palette (7th in the third row). Select it and click on the output. The 'Add a Visible Property' window appears. Change the label name to out. Select Visible in Simulation. Click on Assign. Now the output is also labeled.

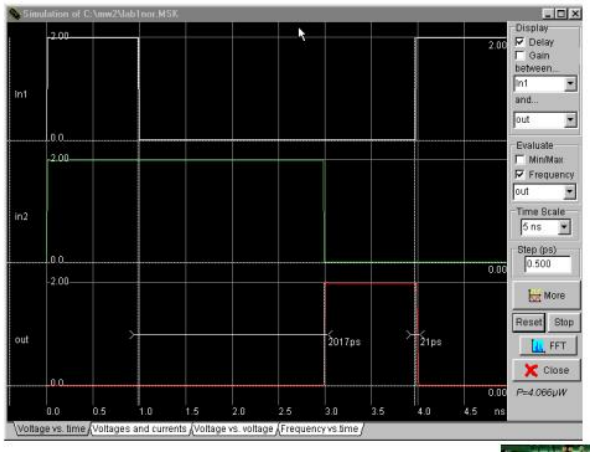




Select Vdd Supply and GND from the palette (third row). Also click on the capacitor (3rd in 2nd row) symbol and add it to the output. Also, extend the pwell into the Vdd Rail. The click on Edit -> Generate -> Contacts. Select PATH and then in Metal choose Metal1 and N+ polarization.

To run the Simulation of your circuit, click on Simulate -> Start Simulation. Depending on the input sequences assigned at the input the output is observed in the simulation. The power value is also given





Conclusion:

This lab introduced LTSpice and Microwind tools for CMOS inverter design and analysis. Using LTSpice, we simulated the inverter's DC characteristics with the BSIM4 model. In Microwind, we created both automatic and manual layouts, performed DRC checks, and analyzed delays and power. The lab provided hands-on experience in both circuit simulation and physical layout design in VLSI.