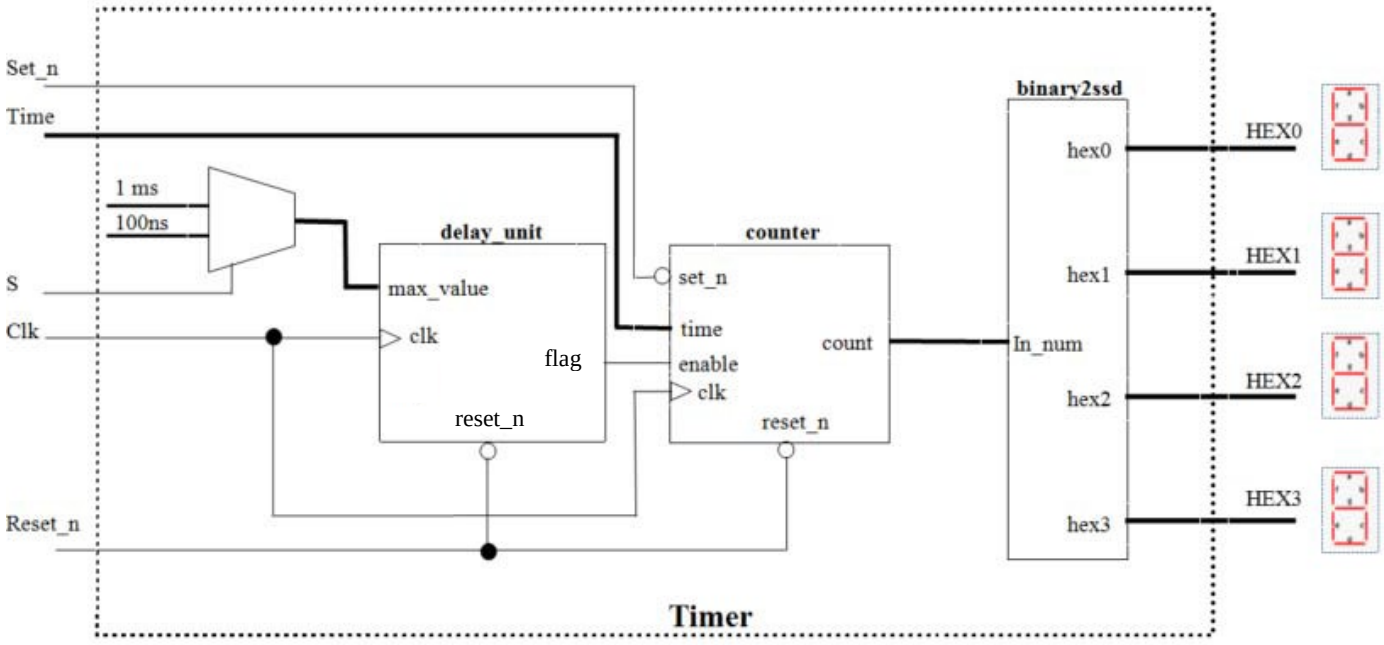
Technical Objective:
In this lab, the concept of designing mechanism to keep track of time will be investigated. In a digital design, there are many applications that require a mechanism that is capable of tracking time. A timer and/or counter is useful for a variety of tasks where a delay is required.

The technical objective of this lab will be met through the design and implementation of a presettable millisecond timer in VHDL.

Pre-Laboratory: (30%)
The block diagram below represents the timer system.

- The mux chooses the constant that will be used by the delay unit. The 1ms constant is used for the hardware implementation of the timer, the 100ns constant is used for simulation.
- The delay unit creates a 1 clock cycle pulse at the interval defined by its delay input (every 1ms or every 100ns).
- The counter is a 10 bit binary counter that counts to 999 and then rolls over. It only increments when its enable input is 1. The timer can be preset to any value between 000 and 999 by putting the preset value on the 10-bit **time** input and activating the **set_n** input
- The binary2ssd component converts a 10 bit binary number into the seven segment display constants.



1. Using VHDL, and targeting the Altera DE0-CV board, create a VHDL circuit for the timer system.

2. Your VHDL MUST adhere to the following guidelines:
    a. No integers types
    b. No latch warnings
    c. Hierarchical design and components for the delay unit, counter and display drivers
3. Submit your VHDL code to the dropbox before your lab section.

Procedure: (70%)

1. Synthesize your design using Altera Quartus Prime.
2. Using the testbench provided on MyCourses, simulate your design in Modelsim. Note that it would take forever to test the timer operating at 1 ms, so the 100 ns option will be used. Make print outs of several locations where the timer loads and rolls over.
3. Connect reset_n to KEY0, clk to CLOCK_50, time to SW9-SW0, S to KEY1, set_n to KEY2 and HEX0, HEX1, HEX2 and HEX3 to the seven segment displays. Compile and download to the DE0 board.
4. Verify proper operation of your timer and obtain a signoff.

Documentation: There is no lab report for this lab. Save all of your signoffs, Modelsim waveforms and oscilloscope outputs to be included in the report for lab 9.

Signoffs and Grade:

Please submit with Lab 9 Report

Name:_____

Component	Signoff	Date	Time
Functional Simulation (30 pts)			
Working Board (30 pts)			

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Component	Received	Possible
Prelab		30
Signoff		70
Penalties • after the first 15 minutes of lab session 9: -10 • after the first 15 minutes of lab session 10: -25 • no signoffs after the first 15 minutes of lab session 11:	-	
Total		100