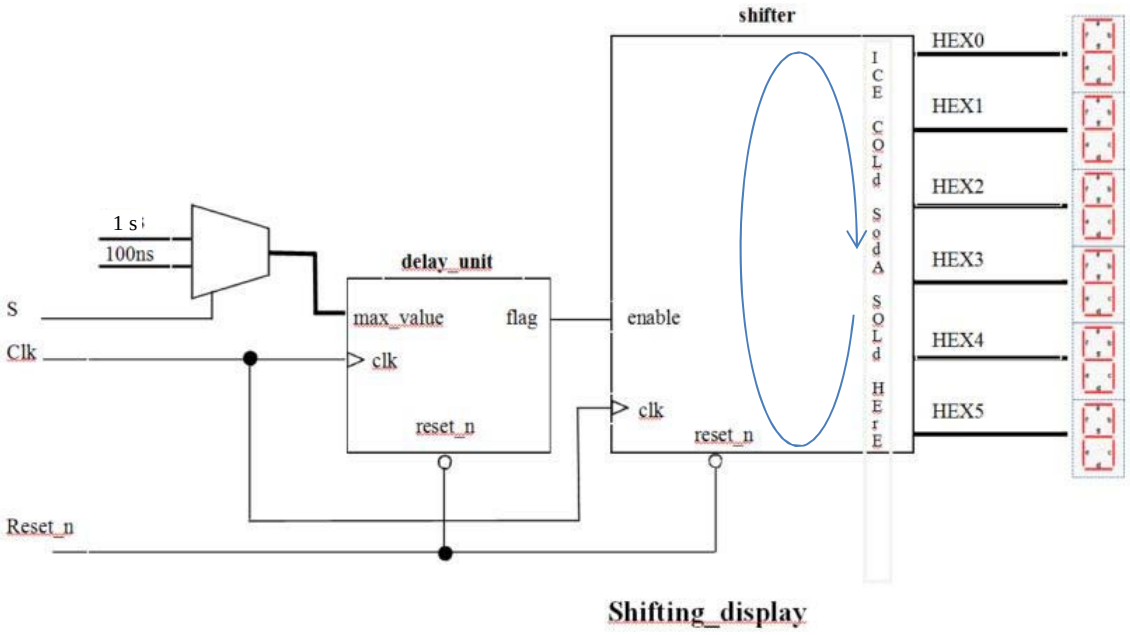
Technical Objective:

In this lab, the concept of synchronous digital systems will be further investigated. In a digital design there are many applications that require timekeeping and shifting of data. A timer and/or counter is useful for tasks where a delay is required and a shift register is used to move data in a serial manner.

The technical objective of this lab will be met through the design and implementation of a scrolling display system for a soda machine with six seven segment displays. The message that is to be displayed on the soda machine is “ICE COLd SOdA SOLd HErE” with the letters appearing for 1 second and then shifting one position to the left. Note: you can change the message, but it needs to be at least 20 characters long.

The system is shown in the block diagram below:

- The mux chooses between the constants for a 1 second delay (s = 1) or a 100ns delay for test mode.
- The delay_unit creates a pulse that is 1 clk period wide at the rate determined by the input mux.
- The shifter is a circular shift register that circulates a two-dimensional array of display constants. Six elements of the constants array are passed out to the six seven-segment displays on the DE0-CV board.



Pre-Laboratory: (20%)

1. Using VHDL, and targeting the Altera DE0 Board, create a VHDL circuit for the soda display system. You are free to change the message to say anything you want as long as it is at least 20 characters in length.

2. Your VHDL MUST adhere to the following guidelines:
    a. No integers types
    b. No latch warnings
    c. Use of a shift register in the shifter component
    d. Hierarchical design and components for the mus, delay unit and shifter

3. Submit your VHDL code to the dropbox before your lab section.

Procedure: (60%)

1. Synthesize your design using Altera Quartus Prime.
2. Using the testbench provided on MyCourses, simulate your design in Modelsim. Note that this IS NOT a self-checking testbench. You should edit the wave.do file to match your constants so that you can check your waveform for correct operation. For a signoff, demonstrate to the instructor or TA the correct message will be displayed.
3. Connect reset_n to KEY0, S to a switch, clk to CLOCK_50, HEX0, HEX1, HEX2, HEX3, HEX4 and HEX5 to the seven segment displays. Compile and download to the DE0 board. Verify that your display works as expected. Obtain a signoff.

Documentation: Documentation: (20%)
This is a formal lab report and should discuss labs 8 and 9. Be sure to include and discuss simulation waveforms (annotate comments on them), and fully documented VHDL code and any other documentation useful in explaining what was done in the lab.

Signoffs and Grade:

Please submit with Lab 9 Report

Name:_____

Component	Signoff	Date	Time
Functional Simulation (30 pts)			
Working Board (30 pts)			

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Component	Received	Possible
Prelab		20
Signoff		60
Report		20
Penalties • after the first 15 minutes of lab session 10: -10 • after the first 15 minutes of lab session 11: -25	-	
Total		100