

## **MSP430FG461x Device Erratasheet**

### **1 Current Version**

See [Appendix A](#) for prior silicon revisions.

✓ The checkmark indicates that the issue is present in the specified revision.

Devices	Rev:	ADC18	ADC25	CPU8	CPU16	CPU19	DMA3	DMA4	FLL3	FLL6	LCDA5	RTC1	TA12	TA16	TA18	TAB22	TB2	TB16	TB18	USCI19	USCI20	USCI21
MSP430FG4616	G	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430FG4617	G	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430FG4618	G	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430FG4619	G	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Devices	Rev:	USCI22	USCI23	USCI24	USCI25	USCI26	USCI27	USCI30	WDG2	XOSC5	XOSC8	XOSC9
MSP430FG4616	G	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430FG4617	G	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430FG4618	G	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430FG4619	G	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

## 2 Package Markings

### PZ100

#### **LQFP (PZ) 100 Pin**



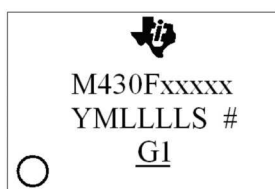
YM = Year and Month Date Code  
 LLLL = LOT Trace Code  
 S = Assembly Site Code  
 # = DIE Revision  
 o = PIN 1



YM = Year and Month Date Code  
 LLLL = LOT Trace Code  
 S = Assembly Site Code  
 # = DIE Revision  
 o = PIN 1

### ZQW113

#### **BGA (ZQW), 113 Pin**



YM = Year and Month Date Code  
 LLLL = LOT Trace Code  
 S = Assembly Site Code  
 # = DIE Revision  
 o = PIN 1

### 3 Detailed Bug Description

<b>ADC18</b>	<b>ADC12 Module</b>
<b>Function</b>	Incorrect conversion result in extended sample mode
<b>Description</b>	<p>The ADC12 conversion result can be incorrect if the extended sample mode is selected (SHP = 0), the conversion clock is not the internal ADC12 oscillator (ADC12SSEL &gt; 0), and one of the following two conditions is true:</p> <ul style="list-style-type: none"> <li>• The extended sample input signal SHI is asynchronous to the clock source used for ADC12CLK and the undivided ADC12 input clock frequency exceeds 3.15 MHz.</li> <li>or</li> <li>• The extended sample input signal SHI is synchronous to the clock source used for ADC12CLK and the undivided ADC12 input clock frequency exceeds 6.3 MHz.</li> </ul>
<b>Workaround</b>	<ul style="list-style-type: none"> <li>• Use the pulse sample mode (SHP = 1).</li> <li>or</li> <li>• Use the ADC12 internal oscillator as the ADC12 clock source.</li> <li>or</li> <li>• Limit the undivided ADC12 input clock frequency to 3.15 MHz.</li> <li>or</li> <li>• Use the same clock source (such as ACLK or SMCLK) to derive both SHI and ADC12CLK, to achieve synchronous operation, and also limit the undivided ADC12 input clock frequency to 6.3 MHz.</li> </ul>
<b>ADC25</b>	<b>ADC12 Module</b>
<b>Function</b>	Write to ADC12CTL0 triggers ADC12 when CONSEQ = 00
<b>Description</b>	<p>If ADC conversions are triggered by the Timer_B module and the ADC12 is in single-channel single-conversion mode (CONSEQ = 00), ADC sampling is enabled by write access to any bit(s) in the ADC12CTL0 register. This is contrary to the expected behavior that only the ADC12 enable conversion bit (ADC12ENC) triggers a new ADC12 sample.</p>
<b>Workaround</b>	<p>When operating the ADC12 in CONSEQ = 00 and a Timer_B output is selected as the sample and hold source, temporarily clear the ADC12ENC bit before writing to other bits in the ADC12CTL0 register. The following capture trigger can then be re-enabled by setting ADC12ENC = 1.</p>
<b>CPU8</b>	<b>CPU Module</b>
<b>Function</b>	Using odd values in the SP register
<b>Description</b>	<p>The SP can be written with odd values. In the original CPU, an odd SP value could be combined with an odd offset (for example, <code>mov. #value, 5(SP)</code>). In the new CPU, the SP can be written with an odd value, but the first time the SP is used, the LSB is forced to 0.</p>
<b>Workaround</b>	Do not use odd values with the SP.

<b>CPU16</b>	<b><i>CPU Module</i></b>
<b>Function</b>	Indexed addressing with instructions <code>calla</code> , <code>mova</code> , and <code>bra</code>
<b>Description</b>	<p>With indexed addressing mode and instructions <code>calla</code>, <code>mova</code>, and <code>bra</code>, it is not possible to reach memory above 64k if the register content is &lt; 64k.</p> <p>Example: Assume R5 = FFFEh. The instruction <code>calla 0004h(R5)</code> results in a 20-bit call of address 0002h instead of 10002h.</p>
<b>Workaround</b>	<ul style="list-style-type: none"> <li>• Use different addressing mode to reach memory above 64k.</li> <li>• First use <code>adda [index], [Rx]</code> to calculate address in upper memory and then use <code>calla [Rx]</code>.</li> </ul>
<b>CPU19</b>	<b><i>CPU Module</i></b>
<b>Function</b>	CPUOFF can change register values
<b>Description</b>	<p>If a CPUOFF command is followed by an instruction with an indirect addressed operand (for example, <code>mov @R8, R9</code>, and <code>RET</code>), an unintentional register-read operation can occur during the wakeup of the CPU. If the unintentional read occurs to a read-sensitive register (for example, UCB0RXBUF or TAIV), which changes its value or the value of other registers (IFGs), the bug leads to lost interrupts or wrong register read values.</p>
<b>Workaround</b>	Insert a NOP instruction after each CPUOFF instruction.
<b>DMA3</b>	<b><i>DMA Module</i></b>
<b>Function</b>	Read-modify-write instructions may corrupt DMA address registers
<b>Description</b>	<p>When a 16-bit-wide read-modify-write instruction (such as <code>add.w</code> and <code>sub.w</code>) is directly used on a DMA address register (DMAxSA or DMAxDA), the register contents are corrupted.</p>
<b>Workaround</b>	<ul style="list-style-type: none"> <li>• Do not use 16-bit-wide read-modify-write instructions on DMA address registers. Instead, if address calculations are necessary, do the calculations first, and then assign the result to the DMA address registers. or</li> <li>• Use 20-bit-wide read-modify-write instructions (such as <code>addx.a</code>, <code>subx.a</code>) on the DMA address registers, if needed.</li> </ul>

<b>DMA4</b>	<b><i>DMA Module</i></b>
<b>Function</b>	Corrupted write access to 20-bit DMA registers
<b>Description</b>	When a 20-bit wide write to a DMA address register (DMAxSA or DMAxDA) is interrupted by a DMA transfer, the register contents may be unpredictable.
<b>Workaround</b>	<ul style="list-style-type: none"> <li>Design the application to ensure that no DMA access interrupts 20-bit wide accesses to the DMA address registers.</li> <li>or</li> <li>When accessing the DMA address registers, enable the Read Modify Write disable bit (DMARMWDIS = 1), or temporarily disable all active DMA channels (DMAEN = 0).</li> <li>or</li> <li>Use word access for accessing the DMA address registers. Note that this limits the values that can be written to the address registers to 16-bit values (lower 64K of flash).</li> </ul>
<b>FLL3</b>	<b><i>FLL+ Module</i></b>
<b>Function</b>	FLLDx = 11 for /8 may generate an unstable MCLK frequency
<b>Description</b>	When setting the FLL to higher frequencies using FLLDx = 11 (/8), the output frequency of the FLL may have a larger frequency variation (for example, averaged over 2 seconds) and a lower average output frequency than expected when compared to the other FLLDx bit settings.
<b>Workaround</b>	None
<b>FLL6</b>	<b><i>FLL+ Module</i></b>
<b>Function</b>	LFXT1DIG readout is wrong
<b>Description</b>	The LFXT1DIG bit is always read as 0, even when the bit has been programmed as 1. The clock bypass implementation is functional, but the bit is always read as 0.
<b>Workaround</b>	None
<b>LCDA5</b>	<b><i>LCD_A Module</i></b>
<b>Function</b>	Wrong cycle time for first cycle of COMx/Sx signals
<b>Description</b>	The time of the first cycle of COMx/Sx signals after enabling the LCD_A module is only half of the selected value. All following cycles are correct.
<b>Workaround</b>	Not required, because it does not influence the LCD function.

## RTC1

### RTC Module

#### Function

Incorrect RTCDAY count in BCD mode

#### Description

When using the RTC in BCD mode, RTCDAY counts from 0x29 to 0x31 instead of counting to 0x30 in the month of December (RTCMON = 0x12). Furthermore, due to a malfunction in the leap year detection logic, RTCMON/RTCDAY may incorrectly count from 0x02/0x28 to 0x03/0x01 instead of 0x02/0x29, or it may incorrectly count from 0x02/0x28 to 0x02/0x29 instead of 0x03/0x01.

#### Workaround

Do not operate the RTC module in BCD mode. Use the RTC in hexadecimal format mode (RTCB CD = 0) instead. Convert RTC registers to BCD on demand using software.

**NOTE:** The CPU instruction DADD.B/.W can be used to efficiently implement a hex to BCD conversion. An Assembly language example of such an optimized 8-bit conversion is shown below:

```

mov.b    #8,R14    // Loop counter, process 8 bits
clr.b    R12       // Result will get assembled in R12
loop    rlc.b    R13    // Get MSB from input variable in R13
        dadd.b   R12,R12
        dec.b    R14
        jnz     loop

```

## TA12

### Timer\_A Module

#### Function

Interrupt is lost (slow ACLK)

#### Description

Timer\_A counter is running with slow clock (external TACLK or ACLK) compared to MCLK. The compare mode is selected for the capture/compare channel and the CCRx register is incremented by one with the occurring compare interrupt (if TAR = CCRx).

Due to the fast MCLK, the CCRx register increment (CCRx = CCRx + 1) happens before the Timer\_A counter has incremented again. Therefore, the next compare interrupt should happen at once with the next Timer\_A counter increment (if TAR = CCRx + 1). This interrupt is lost.

#### Workaround

Switch capture/compare mode to capture mode before the CCRx register increment. Switch back to compare mode afterward.

## TA16

### Timer\_A Module

#### Function

First increment of TAR erroneous when IDx > 00

#### Description

The first increment of TAR after any timer clear event (POR/TACLK) happens immediately following the first positive edge of the selected clock source (INCLK, SMCLK, ACLK, or TACLK). This is independent of the clock input divider settings (ID0, ID1). All following TAR increments are performed correctly with the selected IDx settings.

#### Workaround

None

<b>TA18</b>	<b><i>Timer_A Module</i></b>
<b>Function</b>	MOV to TACTL may clear TAR
<b>Description</b>	When TACTL is modified with a MOV instruction, the contents of TAR may be cleared, even when TACLR is not set.
<b>Workaround</b>	Use BIS or BIC instructions to modify TACTL.
	<hr/> <p><b>NOTE:</b> A DMA transfer must not occur while these BIS and BIC instructions execute. This can be prevented by disabling the DMA prior to these instructions, or by using the DMAONFETCH bit to align DMA transfers to instruction fetch boundaries.</p> <hr/>
<b>TAB22</b>	<b><i>Timer_A/Timer_B Module</i></b>
<b>Function</b>	Timer_A/B register modification after Watchdog Timer PUC
<b>Description</b>	Unwanted modification of the Timer_A/B registers TACTL and TAIV can occur when a PUC is generated by the Watchdog Timer (WDT) in watchdog mode and any Timer_A/B counter register TACCRx/TBCCRx is incremented/decremented (Timer_A/B does not need to be running).
<b>Workaround</b>	<p>Initialize TACTL/TBCTL register after the reset occurs using a MOV instruction (BIS/BIC may not fully initialize the register). TAIV/TBIV is automatically cleared following this initialization.</p> <p><b>Example code:</b></p> <pre>MOV.W #VAL, &amp;TACTL</pre> <p>or</p> <pre>MOV.W #VAL, &amp;TBCTL</pre> <p>Where, VAL = 0, if Timer is not used in application; otherwise, user defined per desired function.</p>
<b>TB2</b>	<b><i>Timer_B Module</i></b>
<b>Function</b>	Interrupt is lost (slow ACLK)
<b>Description</b>	<p>Timer_B counter is running with slow clock (external TBCLK or ACLK) compared to MCLK. The compare mode is selected for the capture/compare channel and the CCRx register is incremented by 1 with the occurring compare interrupt (if TBR = CCRx).</p> <p>Due to the fast MCLK, the CCRx register increment (CCRx = CCRx + 1) happens before the Timer_B counter has incremented again. Therefore, the next compare interrupt should happen at once with the next Timer_B counter increment (if TBR = CCRx + 1). This interrupt is lost.</p>
<b>Workaround</b>	Switch capture/compare mode to capture mode before the CCRx register increment. Switch back to compare mode afterward.

<b>TB16</b>	<b><i>Timer_B Module</i></b>
<b>Function</b>	First increment of TBR erroneous when IDx > 00
<b>Description</b>	The first increment of TBR after any timer clear event (POR/TBCLR) happens immediately following the first positive edge of the selected clock source (INCLK, SMCLK, ACLK, or TBCLK). This is independent of the clock input divider settings (ID0, ID1). All following TBR increments are performed correctly with the selected IDx settings.
<b>Workaround</b>	None
<b>TB18</b>	<b><i>Timer_B Module</i></b>
<b>Function</b>	MOV to TBCTL may clear TBR
<b>Description</b>	When TBCTL is modified with a MOV instruction, the contents of TBR may be cleared, even when TBCLR is not set.
<b>Workaround</b>	Use BIS or BIC instructions to modify TBCTL.
	<hr/> <p><b>NOTE:</b> A DMA transfer must not occur while these BIS and BIC instructions execute. This can be prevented by disabling the DMA prior to these instructions or by using the DMAONFETCH bit to align DMA transfers to instruction fetch boundaries.</p> <hr/>
<b>USCI19</b>	<b><i>USCI Module</i></b>
<b>Function</b>	LPM4 may affect USCI operation
<b>Description</b>	When SMCLK is used as the USCI clock source, and SMCLK is deactivated due to a LPM4 entry, ongoing SPI master, I <sup>2</sup> C master, and UART transmit transaction are interrupted. Also, while in LPM4, UART receive operation is nonfunctional.
<b>Workaround</b>	Do not enter LPM4 while SPI master, I <sup>2</sup> C master, or UART transmit operations are active. Wait for the operation to be completed prior entering LPM4, or enter a different low-power mode. Also, do not use LPM4 during UART receive operation. Instead, use a different low-power mode.



**USCI20**
**USCI Module**
**Function**

I<sup>2</sup>C mode multi-master transmitter issue

**Description**

When configured for I<sup>2</sup>C master-transmitter mode and used in a multi-master environment, the USCI module can cause unpredictable bus behavior if all of the following conditions are true:

1. Two masters are generating SCL.  
and
2. The slave is stretching the SCL low phase of an ACK period while outputting NACK on SDA.  
and
3. The slave drives ACK on SDA after the USCI has already released SCL, and then the SCL bus line is released.  
and
4. The transmit buffer has not been loaded before the other master continues communication by driving SCL low.

The USCI remains in the SCL high phase until the transmit buffer is written. After the transmit buffer has been written, the USCI interferes with the current bus activity and may cause unpredictable bus behavior.

**Workaround**

- Ensure that slave does not stretch the SCL low phase of an ACK period.  
or
- Ensure that the transmit buffer is loaded in time.  
or
- Do not use the multi-master transmitter mode.

**USCI21**
**USCI Module**
**Function**

UART IrDA receiver filter

**Description**

The IrDA receive filter can be used to filter pulses with length UCAIRRXFL configured in UCAXIRRCTL register. If UCIRRXFE is set the IrDA receive decoder may filter out pulses longer than the configured filter length depending on frequency of BRCLK. This results in framing errors or corrupted data on the receiver side.

**Workaround**

Depending on the used baud rate and the configured filter length, a maximum frequency for BRCLK needs to be set to avoid this issue:

$$\text{Max BRCLK} = \frac{\text{Filter Length} + 64}{2} \times \frac{\text{Baud Rate} \times 16}{3 \times 10^6}$$

Baud Rate	Filter Length UCIRRXFL (dec)	Max BRCLK (MHz)
9600	64	3.28
	32	2.46
	16	2.05
	8	1.84
	4	1.74
	2	1.69
	1	1.66
	0	1.64
19200	64	6.55
	32	4.92
	16	4.1
	8	3.69
	4	3.48
	2	3.38
	1	3.33
	0	3.28
38400	64	13.11
	32	9.83
	16	8.19
	8	7.37
	4	6.96
	2	6.76
	1	6.66
	0	6.55
56000	64	19.11
	32	14.34
	16	11.95
	8	10.75
	4	10.15
	2	9.86
	1	9.71
	0	9.56

<b>USCI22</b>	<b><i>USCI Module</i></b>
<b>Function</b>	I <sup>2</sup> C master receiver with 10-bit slave addressing
<b>Description</b>	<p>Unexpected behavior of the USCI_B can occur when configured in I<sup>2</sup>C master receive mode with 10-bit slave addressing under the following conditions:</p> <ol style="list-style-type: none"> <li>1. The USCI sends first byte of slave address, the slave sends an ACK and when second address byte is sent, the slave sends a NACK.</li> <li>2. Master sends a repeat start condition (if UCTXSTT = 1).</li> <li>3. The first address byte following the repeated start is acknowledged.</li> </ol> <p>However, the second address byte is not sent; instead, the master incorrectly starts to receive data and sets UCBxRXIFG = 1.</p>
<b>Workaround</b>	Do not use a repeated start condition; instead, set the stop condition UCTXSTP = 1 in the NACK ISR prior to the following start condition (USTXSTT = 1).
<b>USCI23</b>	<b><i>USCI Module</i></b>
<b>Function</b>	UART transmit mode with automatic baud rate detection
<b>Description</b>	Erroneous behavior of the USCI_A can occur when configured in UART transmit mode with automatic baud rate detection. During transmission if a "Transmit break" is initiated (UCTXBRK = 1), the USCI_A does not deliver a stop bit of logic high; instead, it sends a logic low during the subsequent synch period.
<b>Workaround</b>	<ul style="list-style-type: none"> <li>• Follow user's guide instructions for transmitting a break/synch field following UCSWRST = 1.</li> <li>or</li> <li>• Set UCTXBRK = 1 before an active transmission; that is, check for bit UCBUSY = 0 and then set UCTXBRK = 1.</li> </ul>
<b>USCI24</b>	<b><i>USCI Module</i></b>
<b>Function</b>	Incorrect baud rate information during UART automatic baud rate detection mode
<b>Description</b>	Erroneous behavior of the USCI_A can occur when configured in UART mode with automatic baud rate detection. After automatic baud rate measurement is complete, the UART updates UCAxBR0 and UCAxBR1. Under oversampling mode (UCOS16 = 1), for baud rates that should result in UCAxBRx = 0x0002, the UART incorrectly reports it as UCAxBRx = 0x5555.
<b>Workaround</b>	When break/synch is detected following the automatic baud rate detection, the flag UCBRK flag is set to 1. Check if UCAxBRx = 0x5555 and correct it to 0x0002.
<b>USCI25</b>	<b><i>USCI Module</i></b>
<b>Function</b>	TXIFG is not reset when NACK is received in I <sup>2</sup> C mode
<b>Description</b>	When the USCI_B module is configured as an I <sup>2</sup> C master transmitter, the TXIFG is not reset after a NACK is received if the master is configured to send a restart (UCTXSTT = 1 and UCTXSTP = 0).
<b>Workaround</b>	Reset TXIFG in software within the NACKIFG interrupt service routine.

**USCI26**
**USCI Module**
**Function**
 $t_{buf}$  parameter violation in I<sup>2</sup>C multi-master mode

**Description**

In multi-master I<sup>2</sup>C systems, the timing parameter  $t_{buf}$  (bus free time between a stop condition and the following start) is not ensured to match the I<sup>2</sup>C specification of 4.7  $\mu$ s in standard mode and 1.3  $\mu$ s in fast mode. If the UCTXSTT bit is set during a running I<sup>2</sup>C transaction, the USCI module waits and issues the start condition on bus release, causing the violation to occur.

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**NOTE:** It is recommended to check if UCBBUSY bit is cleared before setting UCTXSTT = 1.

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**Workaround**

None

**USCI27**
**USCI Module**
**Function**

Timing of USCI I<sup>2</sup>C interrupts may cause device reset due to automatic clear of an IFG.

**Description**

When certain USCI I<sup>2</sup>C interrupt flags (IFG) are set and an automatic flag-clearing event on the I<sup>2</sup>C bus occurs, the program counter may become corrupted. This happens only when the IFG is cleared within a critical time window (~6 CPU clock cycles) after a USCI interrupt request occurs and before the interrupt servicing is initiated. The affected interrupts are UCBxTXIFG, UCSTPIFG, UCSTTIFG and UCNACKIFG.

The automatic flag-clearing scenarios are described in the following situations:

- A pending UCBxTXIFG interrupt request is cleared on the falling SCL clock edge following a NACK.
- A pending UCSTPIFG, UCSTTIFG, or UCNACKIFG interrupt request is cleared by a following Start condition.

**Workaround**

- Polling the affected flags instead of enabling the interrupts  
or
- Ensuring the above mentioned flag-clearing events occur after a time delay of 6 CPU clock cycles has elapsed since the interrupt request occurred and was accepted.

**USCI30**
**USCI Module**
**Function**

I2C mode master receiver / slave receiver

**Description**

The USCI I2C module, when configured as a receiver (master or slave), performs a double-buffered receive operation. For example, in a transaction of two bytes, after the first byte is moved from the receive shift register to the receive buffer, the byte is acknowledged and the state machine allows the reception of the next byte.

If the receive buffer has not been cleared of its contents by reading the UCBxRXBUF register by the time the seventh bit of the following data byte is received, an error condition may occur on the I2C bus. Depending on the USCI configuration, the following may occur:

- If the USCI is configured as an I2C master receiver, an unintentional repeated start condition can be triggered or the master can switch into an idle state (I2C communication aborted). The reception of the current data byte is not successful in this case.
- If the USCI is configured as I2C slave receiver, the slave can switch to an idle state, stalling I2C communication. The reception of the current data byte is not successful in this case. The USCI I2C state machine notifies the master of the aborted reception with a NACK.

Note that the error condition described above occurs only within a limited window of the seventh bit of the current byte being received. If the receive buffer is read outside of this window (before or after), then the error condition does not occur.

**Workaround**

The error condition can be avoided by servicing the UCBxRXIFG in a timely manner. This can be done by (a) servicing the interrupt and ensuring UCBxRXBUF is read promptly or (b) using the DMA to automatically read bytes from receive buffer upon UCBxRXIFG being set.

OR

If the receive buffer cannot be read out in time, test the I2C clock line before the UCBxRXBUF is read out to ensure that the critical window has elapsed. This is done by checking if the clock line low status indicator bit UCSCLOW is set for at least three USCI bit clock cycles; that is,  $3 \times t_{\text{BitClock}}$ .

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**NOTE:** The last byte of the transaction must be read directly from UCBxRXBUF. For all other bytes, follow the workaround.

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Code flow for workaround:

1. Enter RX ISR for reading receiving bytes
2. Check if UCSCLOW.UCBxSTAT == 1
3. If no, repeat step 2 until set.
4. If yes, repeat step 2 for a time period  $> 3 \times t_{\text{BitClock}}$ , where  $t_{\text{BitClock}} = 1/f_{\text{BitClock}}$
5. If window of  $3 \times t_{\text{BitClock}}$  cycles has elapsed, it is safe to read UCBxRXBUF.

<b>WDG2</b>	<b><i>Watchdog Module</i></b>
<b>Function</b>	Incorrectly accessing a flash control register
<b>Description</b>	If a key violation is caused by incorrectly accessing a flash control register, the watchdog interrupt flag is set in addition to a correctly generated PUC.
<b>Workaround</b>	None
<b>XOSC5</b>	<b><i>LFXT1 Module</i></b>
<b>Function</b>	LF crystal failures may not be properly detected by the oscillator fault circuitry
<b>Description</b>	The oscillator fault error detection of the LFXT1 oscillator in low-frequency mode (XTS = 0) may not work reliably, causing a failing crystal to go undetected by the CPU; that is, OFIFG is not set.
<b>Workaround</b>	None
<b>XOSC8</b>	<b><i>LFXT1 Module</i></b>
<b>Function</b>	ACLK failure when crystal ESR is below 40 kΩ
<b>Description</b>	When ACLK is sourced by a low-frequency crystal with an ESR below 40 kΩ, the duty cycle of ACLK may fall below the specification; the OFIFG may become set or, in some instances, ACLK may stop completely.
<b>Workaround</b>	See the application report <i>XOSC8 Guidance</i> ( <a href="#">SLAA423</a> ) for information regarding working with this erratum.
<b>XOSC9</b>	<b><i>LFXT1 Module</i></b>
<b>Function</b>	XT1 oscillator may not function as expected in high-frequency (HF) mode
<b>Description</b>	XT1 oscillator does not work correctly in high-frequency mode at supply voltages below 2 V with crystal frequency > 4 MHz.
<b>Workaround</b>	None. When XT1 oscillator is used in HF mode with crystal frequency > 4 MHz, ensure a supply voltage > 2.2 V.

## Appendix A Prior Revisions

✓ The checkmark indicates that the issue is present in the specified revision.

Devices	Rev:	ADC18	ADC25	CPU8	CPU16	CPU19	DMA3	DMA4	FLL3	FLL6	LCDA5	RTC1	TA12	TA16	TA18	TAB22	TB2	TB16	TB18	USCI16	USCI19	USCI20
MSP430FG4616	G	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓
	F	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓
	E	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430FG4617	G	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓
	F	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓
	E	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430FG4618	G	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓
	F	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓
	E	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430FG4619	G	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓
	F	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓
	E	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Devices	Rev:	USCI21	USCI22	USCI23	USCI24	USCI25	USCI26	USCI27	USCI30	WDG2	XOSC5	XOSC8	XOSC9
MSP430FG4616	G	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	F	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	E	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430FG4617	G	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	F	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	E	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430FG4618	G	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	F	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	E	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430FG4619	G	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	F	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	E	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

## **A.1 Detailed Bug Description**

<b>USCI16</b>	<b>USCI Module</b>
<b>Function</b>	UART/IrDA mode lost characters
<b>Description</b>	<p>When configured for UART/IrDA mode, the USCI baud rate generator may halt operation under the following conditions:</p> <ul style="list-style-type: none"> <li>• IrDA mode: Repeated invalid start bits on the receive line or</li> <li>• UART/IrDA modes: Positive pulse on the receive line during break character reception inside the stop-bit time slot (the second stop-bit time slot if UCSPB = 1) with a pulse width that passes the deglitch filter but is shorter than one-half of a bit time.</li> </ul> <p>After halting, additional characters are ignored. Transmit functionality is not affected.</p>
<b>Workaround</b>	<p>Check the UCBUSY flag status periodically in software. If the flag is set and no character has been received in the expected time, reset the USCI module in software. To reset the USCI module, toggle UCSWRST and reenale the USCI interrupts.</p>



## Revision History

Changes from I Revision (January 2010) to J Revision	Page
• Updated USCI21 description .....	<a href="#">10</a>
• Added USCI30 .....	<a href="#">13</a>

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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