Techo Chao (趙至勛)

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Professional Summary

Engineering Manager with 7+ years of experience in IC design and processor architecture. Currently leading a 15+ member team to develop high-performance computing engines. Proven track record of delivering 10+ successful product releases and defining product roadmaps. Experienced in working directly with Tier-1 US clients (Meta, Company G) to define custom silicon specifications. Skilled in aligning engineering goals with business needs to deliver complex chips on schedule.

Core Competencies

Engineering Leadership: Cross-functional Team Management, Agile Development.
Product Strategy: Roadmap Planning, Requirement Definition.
Key Account Management: Technical Consulting for Meta & Company G.
Technical Expertise: RISC-V SoC, Accelerator Design, UVM Verification.

Professional Experience

Andes Technology Corporation – *Manager*

📅 Apr 2023 – Present | Hsinchu, Taiwan

Strategic Planning & Product Release

- Collaborated with Product Managers (PDM) to define future product features and roadmaps for ACE-Scalar and ACE-RVV accelerators.
- Successfully managed the full development cycle of 10+ product releases in collaboration with Project Manager (PJM), ensuring high quality and on-time delivery.
- Balanced resource allocation between new feature development and customer support to meet tight schedules.

Tier-1 Client Engagement (Meta & Company G)

- Participated in face-to-face technical meetings with Meta: Discussed and defined specifications for their future customized orders, focusing on AI and computing requirements.
- Collaborated with Company G's North America FAE team: Clarified complex customer requirements to ensure our design met their data center needs.
- Acted as the primary technical window to translate client needs into engineering specifications.

Deputy Manager

📅 Oct 2021 – Apr 2023

- Led the Hardware–ACE group, managing 3 Architects and 7 Verification Engineers.
- Established UVM block-level verification flows, which significantly reduced bug rates.
- Oversaw processor design and UVM block-level verification activities.

Advanced Engineer

📅 Apr 2019 – Oct 2021

- Developed RISC-V instruction extension tool **Andes Custom Extension COPILOT**, including ACE pipeline design and UVM block-level verification.
- Supported CPU customization by enabling designers to implement their own CPU instructions.

Realtek Semiconductor Corporation – *IC Design Engineer*

📅 Dec 2017 – Mar 2019 | Hsinchu, Taiwan

- Designed SSD flash controllers focusing on LDPC-based error correction coding.
- Implemented encoder for NAND flash memory.
- Performed IP-level design verification for storage solutions.

Education

National Sun Yat-sen University – *Master's Degree, Electrical Engineering*
📅 2015 – 2017

National Sun Yat-sen University – *Bachelor's Degree, Electrical and Electronics Engineering*
📅 2011 – 2015

Certifications & Training

- Dale Carnegie Cource - Highest Award For Achievement
- Doulos UVM Adopter Class
- Logic Synthesis with Design Compiler at National Applied Research Laboratories

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Languages

- Mandarin Chinese (Native)
- English (Fluent)