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B.E. V Semester Examination

BE - V/12(A)

233894

COMP. ENGG.

Course No .COM - 503

(Microprocess or 8085)

Time Allowed- 3Hours *Maximum Marks-100*

Note: Attempt any **Five** questions selecting atleast **Two** from each section.

SECTION - A

1. Draw and explain the architecture and pin description of 8085 in detail. **(20)**

2. a) Write a program in 8085 assembly language to find square of an 8- bit number. **(10)**

   b) Categorize the instruction set of 8085 microprocessor. Support your answer with relevant example in each case. **(10)**

3. a) Explain how information is exchanged between the program counter and the stack. Identify the contents of the stack pointer register, when a subroutine is called. **(10)**

   b) Write an 8085 assembly language program to generate all Fibonacci numbers which can be represented using 8-bits, and store them in successive memory locations starting from XX50H on wards. **(10)**

4. a) What do you understand by vectored interrupts? **(5)**

b) Explain the hardware implementation of RST5 . **(5)**

c) Write an 8085 assembly language program which takes the data from memory location X and multiplies this byte by 10 and stores the result at memory location Y. **(10)**

SECTION - B

5. What is the difference between 8253 and 8254 ? With the help of block diagram explain 8253 and its modes of operation in detail. **(20)**

6. a) Explain the mode 1 input configuration of 8255 using its control word, control signals, timing diagram and status word. **(10)**

b) Explain and illustrate the ICW formats of 8259. **(10)**

7. a) Design a seven segment LED output port with device address F5H. It is a common anode segment LED. Generate IOW control signal. Write instructions to display digit5. **(10)**

b) Design a fully decoded scheme to address 16K x 8 of memory using chips of 2K x 8. Derive memory addresses for each chip. **(10)**

8. a) Illustrate the mode set register format and status word register format of 8237. **(10)**

b) What is 8279 chip meant for ? Draw its functional block diagram **(10)**