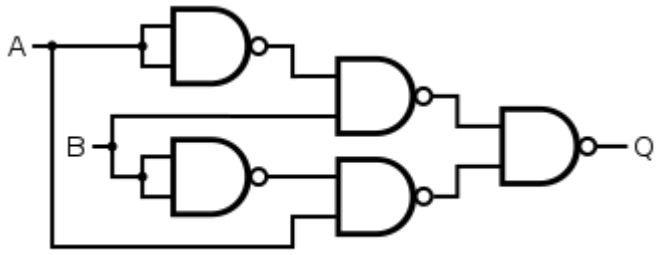
COA Lab Evaluation I - Set I

1. For the circuit given below, draw the full truth table (two inputs, 5 outputs) and full logic equation in a sheet of paper and conclude which logic gate the circuit resembles. Design the *data flow Verilog HDL* for the full circuit in your system. [10 marks]



2. For the logic equation given below, draw the full truth table and circuit diagram in a sheet of paper and conclude which logic gate the circuit resembles. Design the *data flow Verilog HDL* for the full circuit in your system.

{ [**A** NOR (**A** NOR **B**)] NOR [**B** NOR (**A** NOR **B**)] } NOR { [**A** NOR (**A** NOR **B**)] NOR [**B** NOR (**A** NOR **B**)] }

COA Lab Evaluation I - Set II

1. For the logic equation given below, draw the full truth table and circuit diagram in a sheet of paper and conclude which logic gate the circuit resembles. Design the *data flow Verilog HDL* for the full circuit in your system. [10 marks]

{ [**A** NAND (**A** NAND **B**)] NAND [**B** NAND (**A** NAND **B**)] } NAND { [**A** NAND (**A** NAND **B**)] NAND [**B** NAND (**A** NAND **B**)] }

2. For the circuit given below, draw the full truth table (two inputs, 5 outputs) and full logic equation in a sheet of paper and conclude which logic gate the circuit resembles. Design the *data flow Verilog HDL* for the full circuit in your system. [10 marks]