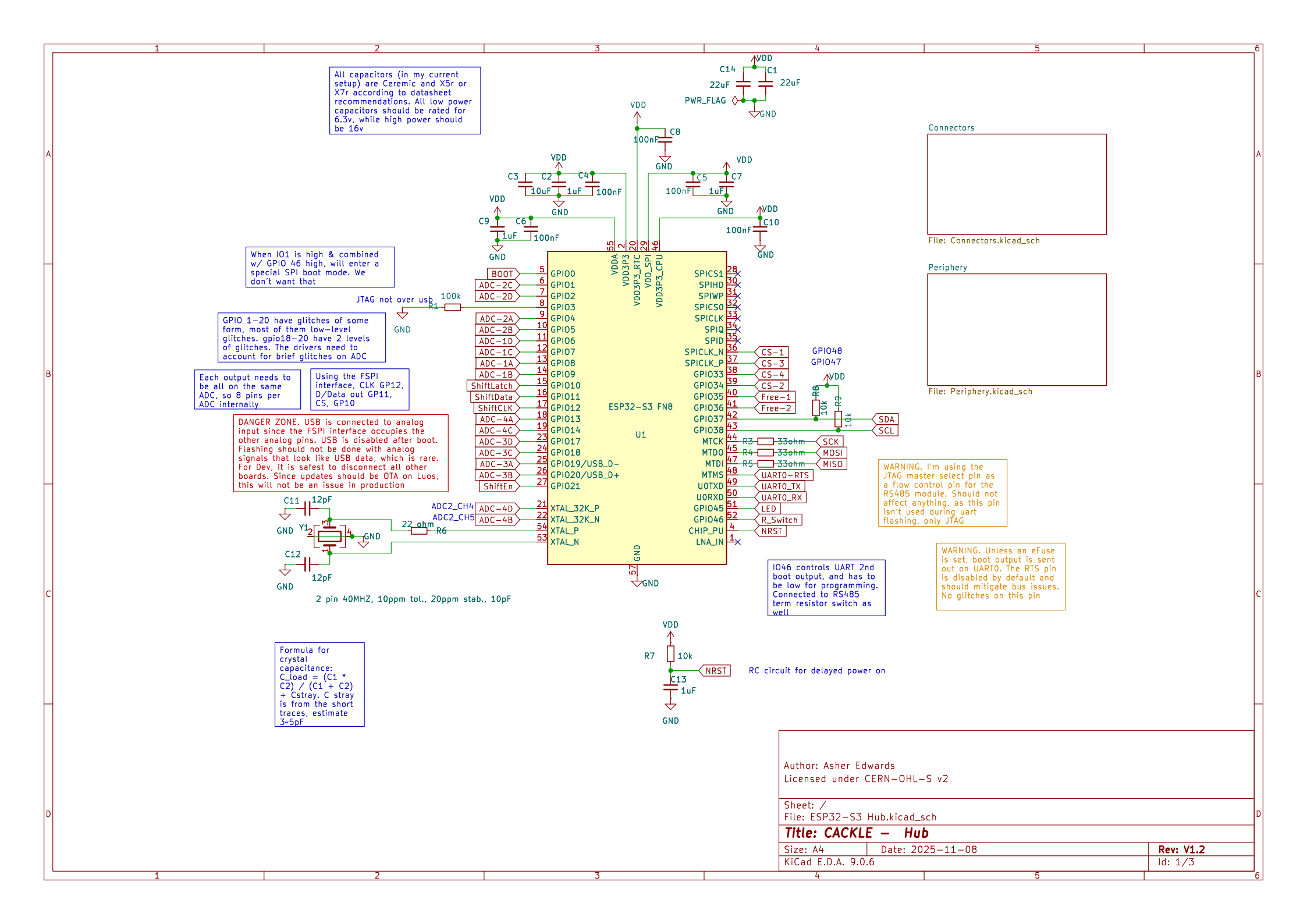

All capacitors (in my current setup) are Ceremic and X5r or X7r according to datasheet recommendations. All low power capacitors should be rated for 6.3v, while high power should be 16v
When IO1 is high & combined w/ GPIO 46 high, will enter a special SPI boot mode. We don't want that
GPIO 1-20 have glitches of some form, most of them low-level glitches. gpio18-20 have 2 levels of glitches. The drivers need to account for brief glitches on ADC
Each output needs to be all on the same ADC, so 8 pins per ADC internally
Using the FSPI interface, CLK GP12, D/Data out GP11, CS, GP10
DANGER ZONE. USB is connected to analog input since the FSPI interface occupies the other analog pins. USB is disabled after boot. Flashing should not be done with analog signals that look like USB data, which is rare. For Dev, it is safest to disconnect all other boards. Since updates should be OTA on Luos, this will not be an issue in production
Formula for crystal capacitance: C_load = (C1 * C2) / (C1 + C2) + Cstray. C stray is from the short traces, estimate 3-5pF
2 pin 40MHZ, 10ppm tol., 20ppm stab., 10pF
IO46 controls UART 2nd boot output, and has to be low for programming. Connected to RS485 term resistor switch as well
WARNING. I'm using the JTAG master select pin as a flow control pin for the RS485 module. Should not affect anything, as this pin isn't used during uart flashing, only JTAG
WARNING. Unless an eFuse is set, boot output is sent out on UART0. The RTS pin is disabled by default and should mitigate bus issues. No glitches on this pin
RC circuit for delayed power on
Connectors
File: Connectors.kicad_sch
Periphery
File: Periphery.kicad_sch
ESP32-S3 FN8
U1
JTAG not over usb
100k
R1
22 ohm
R6
Y1
C11 12pF
C12 12pF
C1 22uF
C14 22uF
PWR_FLAG
C2 10uF
C3
C4 1uF
100nF
C5 100nF
C6 100nF
C7 1uF
C8 100nF
C9 1uF
C10 100nF
R3 33ohm
R4 33ohm
R5 33ohm
R7 10k
R8 10k
R9 10k
C13 1uF
BOOT
ADC-2C
ADC-2D
ADC-2A
ADC-2B
ADC-1D
ADC-1C
ADC-1A
ADC-1B
ShiftLatch
ShiftData
ShiftCLK
ADC-4A
ADC-4C
ADC-3D
ADC-3C
ADC-3A
ADC-3B
ShiftEn
ADC-4D
ADC-4B
ADC2_CH4
ADC2_CH5
CS-1
CS-3
CS-4
CS-2
Free-1
Free-2
SDA
SCL
SCK
MOSI
MISO
UART0-RTS
UART0_TX
UART0_RX
LED
R_Switch
NRST
GPIO48
GPIO47
VDD
GND
Author: Asher Edwards
Licensed under CERN-OHL-S v2
Sheet: /
File: ESP32-S3 Hub.kicad_sch
Title: CACKLE - Hub
Size: A4
Date: 2025-11-08
Rev: V1.2
KiCad E.D.A. 9.0.6
Id: 1/3

DEBUG pins

UART0-RTS — TP20 RTS
UART0_RX — TP2 RX
UART0_TX — TP3 TX

Female. The male connector is 852-10-004-20-001101 or 852-80-004-20-001101

J15
Precidip 853-87-004-20-001101
PWM-1A, PWM-1C, PWM-1B, PWM-1D

J1
Precidip 853-87-004-20-001101
ADC-1A, ADC-1C, ADC-1B, ADC-1D

J2
Precidip 853-87-004-20-001101
PWM-2A, PWM-2C, PWM-2B, PWM-2D

J4
Precidip 853-87-004-20-001101
ADC-2A, ADC-2C, ADC-2B, ADC-2D

J6
Precidip 853-87-004-20-001101
PWM-3A, PWM-3C, PWM-3B, PWM-3D

J7
Precidip 853-87-004-20-001101
ADC-3A, ADC-3C, ADC-3B, ADC-3D

J9
Precidip 853-87-004-20-001101
PWM-4A, PWM-4C, PWM-4B, PWM-4D

J10
Precidip 853-87-004-20-001101
ADC-4A, ADC-4C, ADC-4B, ADC-4D

CS pullup helps during device startup and decreases randomness

VDD — 10k — R2 — CS-1
GND
SCK, MISO, MOSI → J3 FPC 0.3mm Aces 51688-0070M

VDD — 10k — R18 — CS-2
GND
SCK, MISO, MOSI → J5 FPC 0.3mm Aces 51688-0070M

VDD — 10k — R19 — CS-3
GND
SCK, MISO, MOSI → J8 FPC 0.3mm Aces 51688-0070M

VDD — 10k — R20 — CS-4
GND
SCK, MISO, MOSI → J11 FPC 0.3mm Aces 51688-0070M

Maybe buffer the clock net and MOSI. Won't screw up edges depending offboard stuff. SN74LVC2G17

Can't populate due to parts not being available from China. Will have to manually populate

Motor Drivers

Communication/Chaining/Stacking Connectors

Reverse orientation top side receptacles, all pins are the same on both sides. This hub can hold two sensors

J13
TE 3-2363961-0 receptacle

J16
TE 3-2363961-0 receptacle

VDD, GND, Free-1, Free-2, NRST, UART0_TX, UART0_RX, SCK, MOSI, MISO, SDA, SCL, MP

All connectors need: SPI, I2C, programming, and 1 multipurpose pin. Beyond that, nothing is gaurunteed (what do the free pins do, are they different on each side, etc...)

VBUS - Hotswap controller power input. Chained together, so VDD is up top

Female
RS485+, RS485-, VDD, GND
Precidip 853-87-004-20-001101
J12

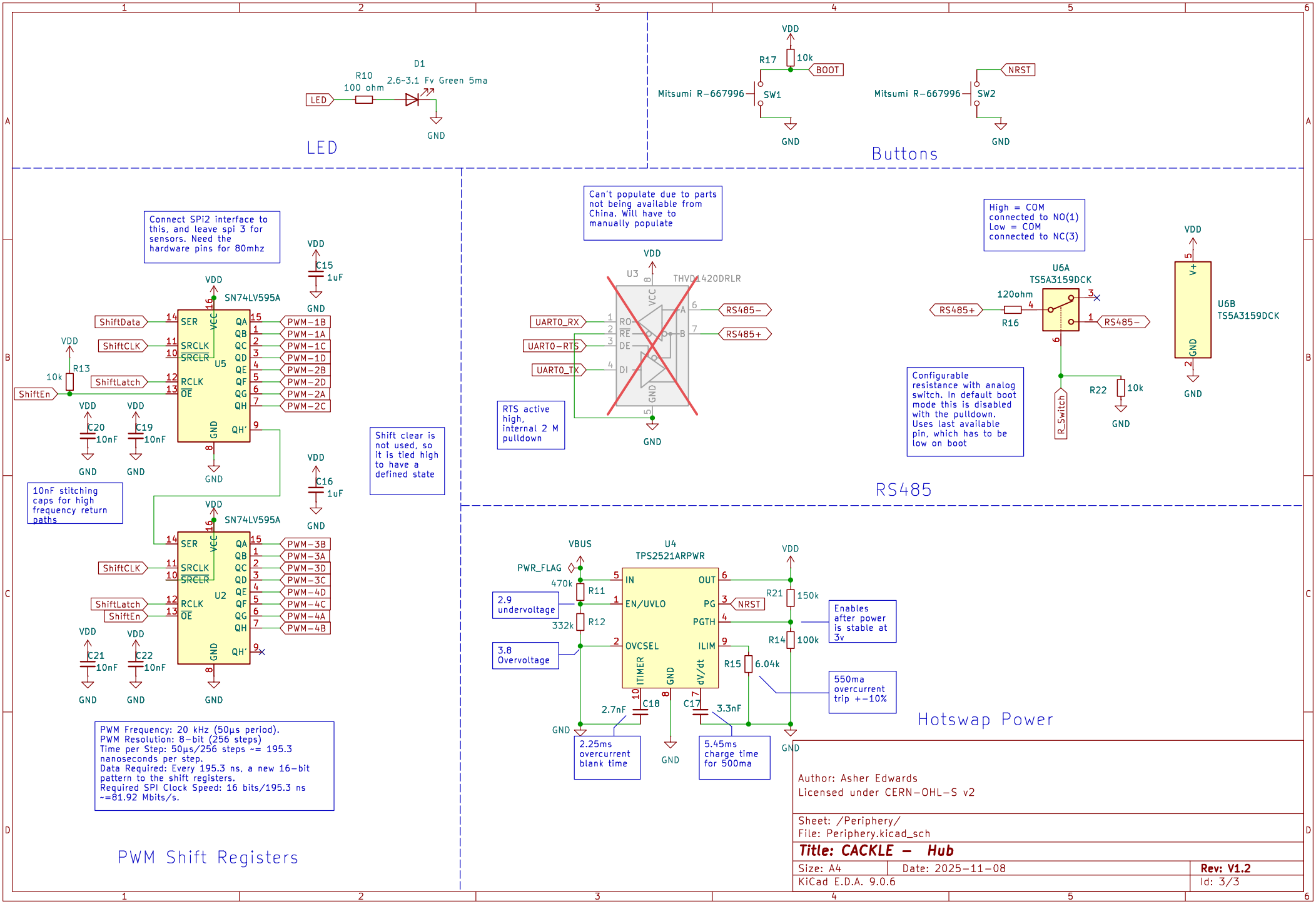
Male
J18
Precidip 852-10-004-20-001101
RS485+, RS485-, VBUS, GND

Author: Asher Edwards
Licensed under CERN-OHL-S v2

Sheet: /Connectors/
File: Connectors.kicad_sch

Title: CACKLE - Hub

Size: A4 | Date: 2025-11-08 | **Rev: V1.2**
KiCad E.D.A. 9.0.6 | Id: 3/3


LED
R10
100 ohm
D1
2.6-3.1 Fv Green 5ma
LED
GND
Buttons
VDD
R17
10k
BOOT
Mitsumi R-667996
SW1
GND
NRST
Mitsumi R-667996
SW2
GND
Connect SPi2 interface to this, and leave spi 3 for sensors. Need the hardware pins for 80mhz
SN74LV595A
U5
SER
SRCLK
SRCLR
RCLK
OE
QA
QB
QC
QD
QE
QF
QG
QH
QH'
VCC
GND
ShiftData
ShiftCLK
ShiftLatch
ShiftEn
PWM-1B
PWM-1A
PWM-1C
PWM-1D
PWM-2B
PWM-2D
PWM-2A
PWM-2C
R13
10k
C15
1uF
C20
10nF
C19
10nF
C16
1uF
Shift clear is not used, so it is tied high to have a defined state
10nF stitching caps for high frequency return paths
U2
PWM-3B
PWM-3A
PWM-3D
PWM-3C
PWM-4D
PWM-4C
PWM-4A
PWM-4B
C21
10nF
C22
10nF
PWM Frequency: 20 kHz (50µs period).
PWM Resolution: 8-bit (256 steps)
Time per Step: 50µs/256 steps ~= 195.3 nanoseconds per step.
Data Required: Every 195.3 ns, a new 16-bit pattern to the shift registers.
Required SPI Clock Speed: 16 bits/195.3 ns ~=81.92 Mbits/s.
PWM Shift Registers
Can't populate due to parts not being available from China. Will have to manually populate
U3
THVD1420DRLR
VCC
RO
RE
DE
DI
A
B
GND
UART0_RX
UART0_RTS
UART0_TX
RS485-
RS485+
RTS active high, internal 2 M pulldown
High = COM connected to NO(1)
Low = COM connected to NC(3)
U6A
TS5A3159DCK
120ohm
R16
R_Switch
R22
10k
U6B
TS5A3159DCK
V+
Configurable resistance with analog switch. In default boot mode this is disabled with the pulldown. Uses last available pin, which has to be low on boot
RS485
U4
TPS2521ARPWR
VBUS
PWR_FLAG
IN
EN/UVLO
OVCSEL
ITIMER
GND
dV/dt
ILIM
PGTH
PG
OUT
470k
R11
332k
R12
2.9 undervoltage
3.8 Overvoltage
R21
150k
R14
100k
R15
6.04k
Enables after power is stable at 3v
550ma overcurrent trip +-10%
2.7nF
C18
3.3nF
C17
2.25ms overcurrent blank time
5.45ms charge time for 500ma
Hotswap Power
Author: Asher Edwards
Licensed under CERN-OHL-S v2
Sheet: /Periphery/
File: Periphery.kicad_sch
Title: CACKLE - Hub
Size: A4
Date: 2025-11-08
Rev: V1.2
KiCad E.D.A. 9.0.6
Id: 3/3