AX88180 Gigabit Ethernet Controller Application Design Note

Revision 1.01
Sep. 9th, 2008

Revision History

Revision	Date	Description
1.00	2008/08/15	Initial Release
1.01	2008/09/09	1. Update the reference circuits in Section 2, 3, 4 and 10.

Content

Figures

1. Introduction

ASIX Electronics provides some cost-effective and highly integrated embedded Ethernet controllers that support generic processor interface (local bus interface or Non-PCI) or SRAM-like interface that are commonly used in embedded system applications. The following URL provides detailed online resource of ASIX Electronics single port embedded Ethernet solutions: (Refer to http://www.asix.com.tw/products.php?op=ProductList&PLine=65.)

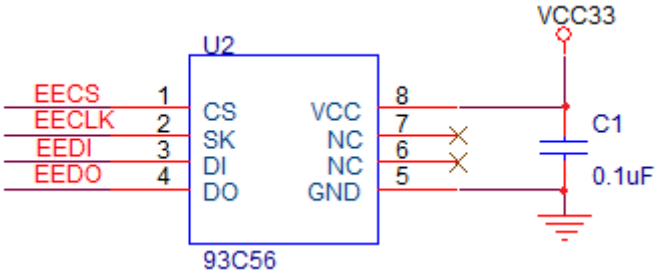
This Application Design Note applies specifically to the following Gigabit Ethernet controller, namely, AX88180.

AX88180 -- High-Performance Non-PCI 32-bit 10/100/1000M Gigabit Ethernet Controller

This Application Design Note provides important information about external component selection, schematic design and PCB design/layout for designing with ASIX Electronics' embedded Gigabit Ethernet controller. ASIX Electronics highly recommends that user read through this Design Note before starting hardware design on schematic capture and PCB layout.

2. EEPROM Selection Considerations

The following is the EEPROM reference circuit of AX88180 Non-PCI 32-bit 10/100/1000M Gigabit Ethernet application.



Note:

1. The AX88180 supports 16-bit data access serial EEPROM device such as 93C56 EEPROM. The 93C56 EEPROM is optional if the MAC address can be stored on the Flash memory of your embedded system. The other EEPROM setting can also be configured by AX88180 registers setting.

3. Crystal Selection Considerations

The 125MHz clock sources can be generated from an Oscillator or Gigabit PHY in RGMII mode. Connect to a 125MHz free-running clock source when in RGMII mode. Please refer to the datasheet at the section 5.2 for details about the CLK125 clock, RGMII timing, and related information when implementing this section.

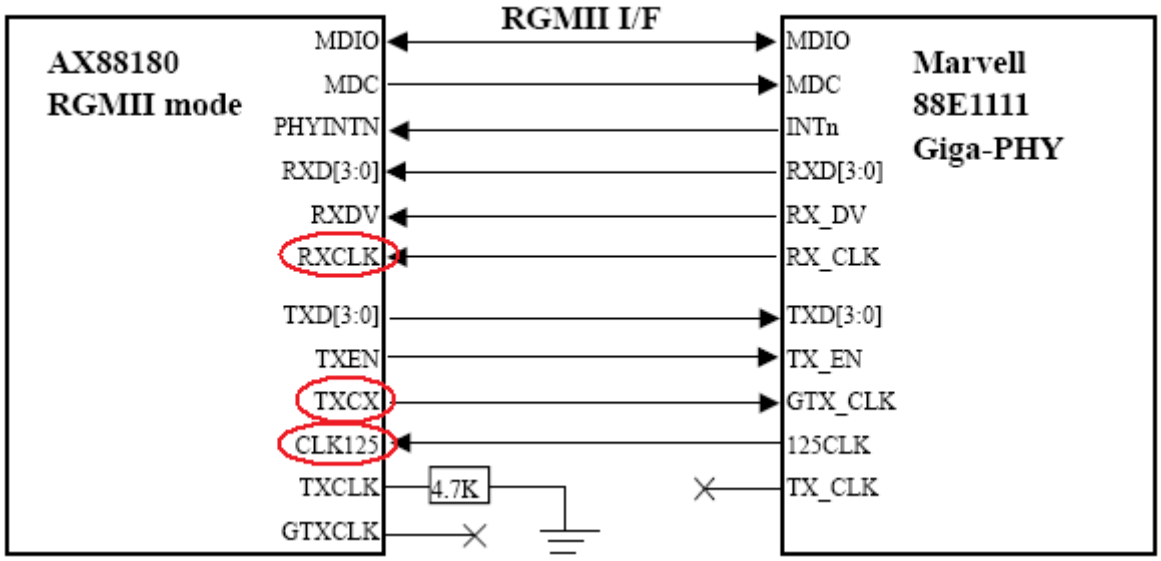


Figure 1. Clock Source from Gigabit PHY RGMII Interface Reference Connection

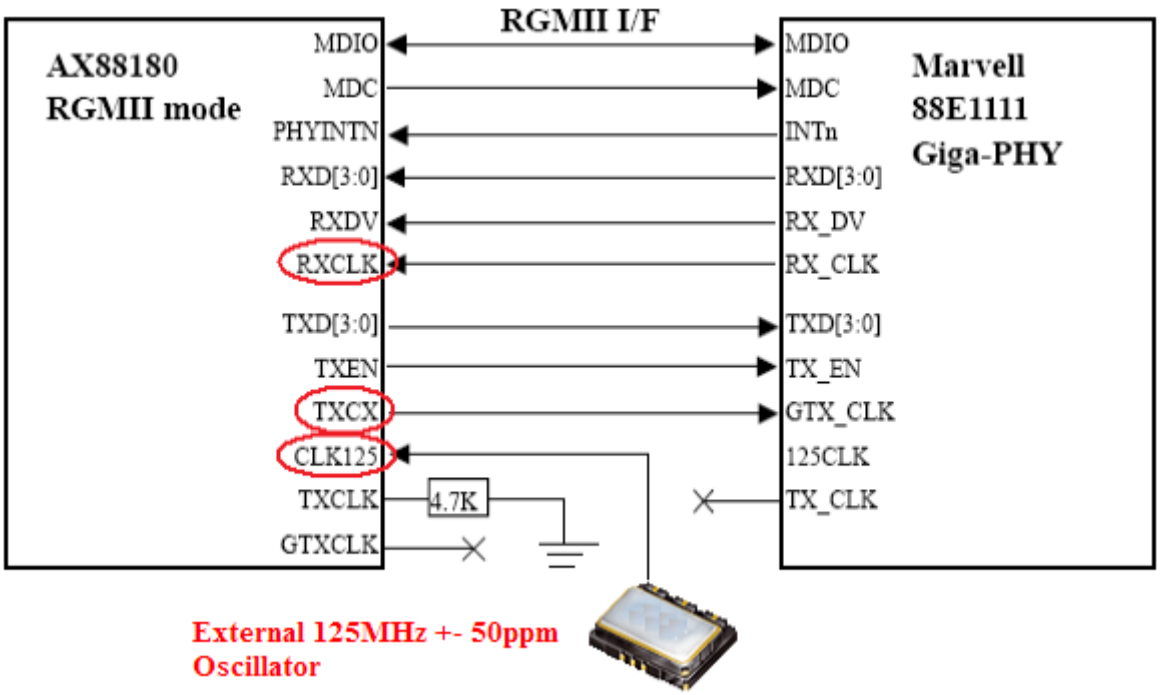
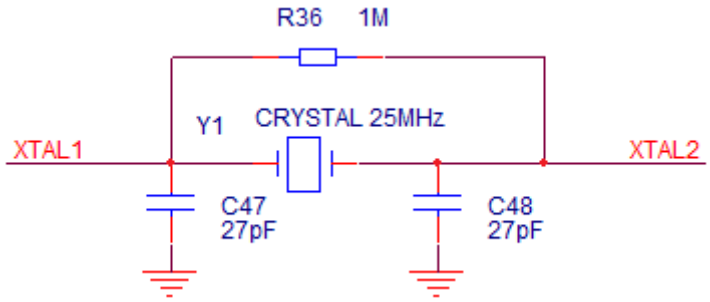


Figure 2. Clock Source from Oscillator RGMII Interface Reference Connection

The following is the reference 25MHz crystal specification (NSK HC-49/U 25Mhz crystal, with CL 20pF and ESR maximum 40 Ohm) of Marvell 88E1111 Gigabit PHY on the AX88180 + Marvell 88E1111 Gigabit PHY demo board.

Parameter	Symbol	Typical Value
Nominal Frequency	Fo	25.000000MHz
Oscillation Mode		Fundamental
Frequency Tolerance (@25℃)		±30ppm
Equivalent Series Resistance	ESR	40 Ohm max.
Load Capacitance	CL	20pF
Operation Temperature Range		0℃ ~ +70℃
Aging		±3ppm/year

The following is a sample 25MHz crystal clock circuit of external Gigabit PHY.

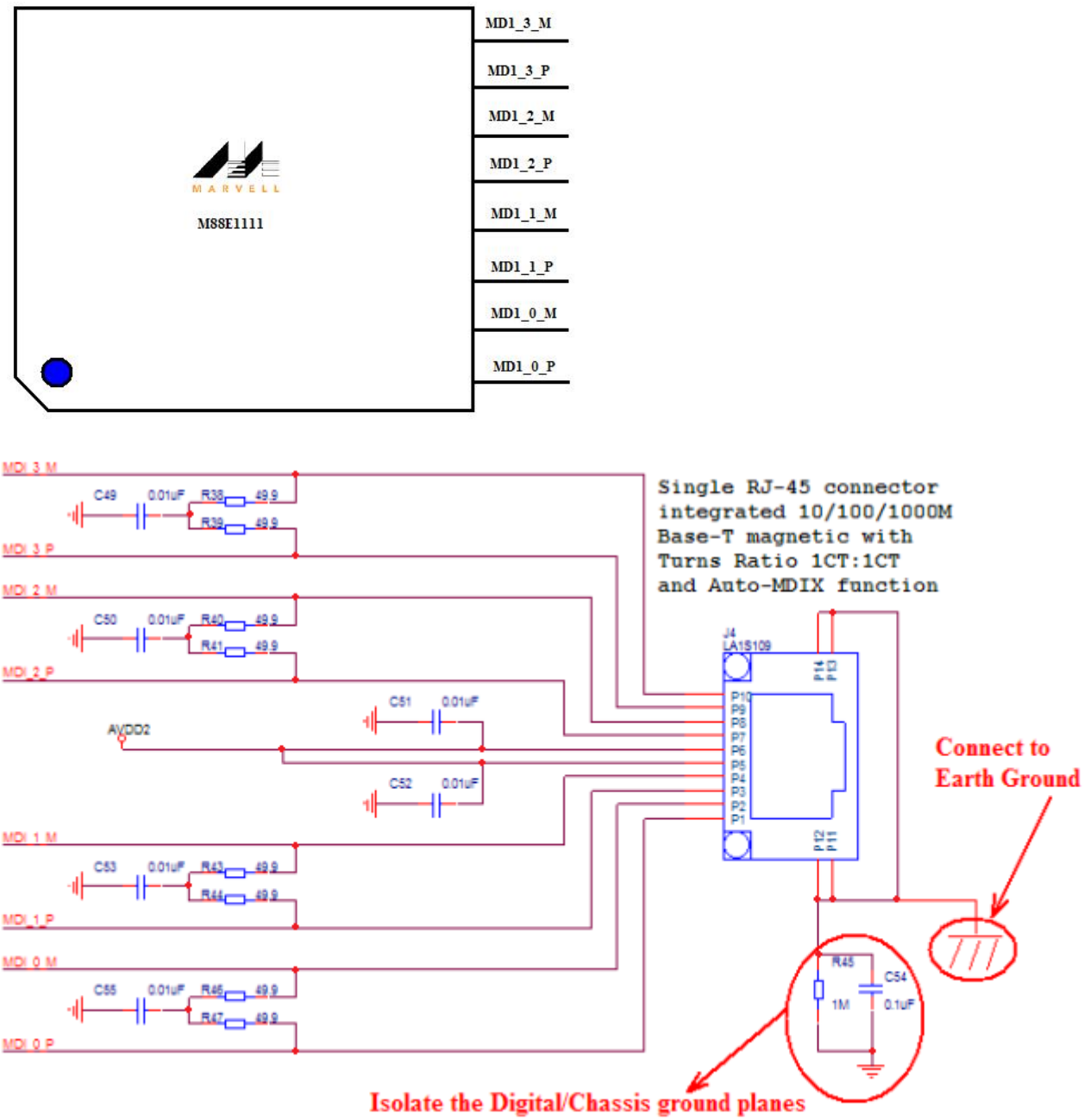


Note: Please make sure the XTAL2 25MHz clock output signals are within 25MHz +- 50ppm. If the XTAL2 25Mhz clock output signals are out of the specification, please fine-tune the load capacitors (C47, C48) to meet the specification. The 25MHz clock circuit is dependent on the external PHY. Please refer to the external PHY's datasheet and reference schematic for the detailed specification requirement of the 25MHz crystal.

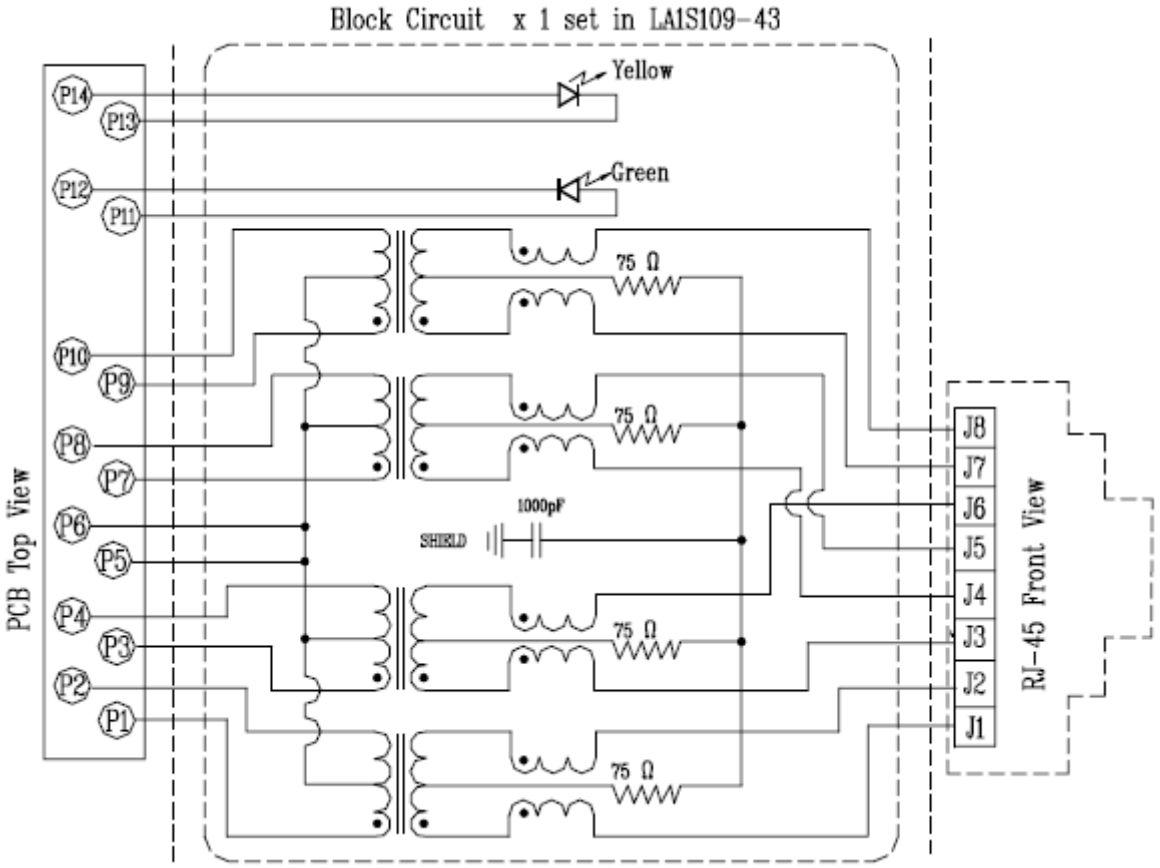
4. Ethernet Magnetic Selection Considerations

The Ethernet magnetic is dependent on the external PHY. Please refer to the external PHY's datasheet and reference schematic for the detailed requirement of the Ethernet magnetic.

The following is the reference Ethernet magnetic circuit (single RJ-45 connector integrated 10/100/1000M Base-T magnetic with Turns Ratio 1CT:1CT and Auto-MDIX function) of Marvell 88E1111 Gigabit PHY on the AX88180 + Marvell 88E1111 Gigabit PHY demo board.



The following is an example (Bothhand LA1S109) of single RJ-45 connector (with integrated 10/100/1000M Base-T magnetic).



5. 4-Layer PCB Design

We strongly suggest customers to design ASIX Electronics' embedded Gigabit Ethernet controller on the printed circuit board (PCB) with at least 4 layers. The 4-layer PCB design can help reduce some potential EMI, thermal and signal integrity issues, etc.

The following is an example 4-Layer PCB design for an embedded system application that uses ASIX Electronics' embedded Gigabit Ethernet controller.

Layer 1	Component (Top)	Magnetic and major signals
Layer 2	Ground	Digital/analog ground planes
Layer 3	Power	Digital/analog power planes
Layer 4	Component (Bottom)	Magnetic and other signals

Figure 3. An Example of 4-Layer PCB Design

6. Power and Ground Planes Considerations

6-1. The RJ-45 chassis ground and the digital ground should be isolated through a 1M Ohm resistor and a 0.1uF decoupling capacitor. And the gap between the chassis ground and digital ground must be wider than 60 mils.

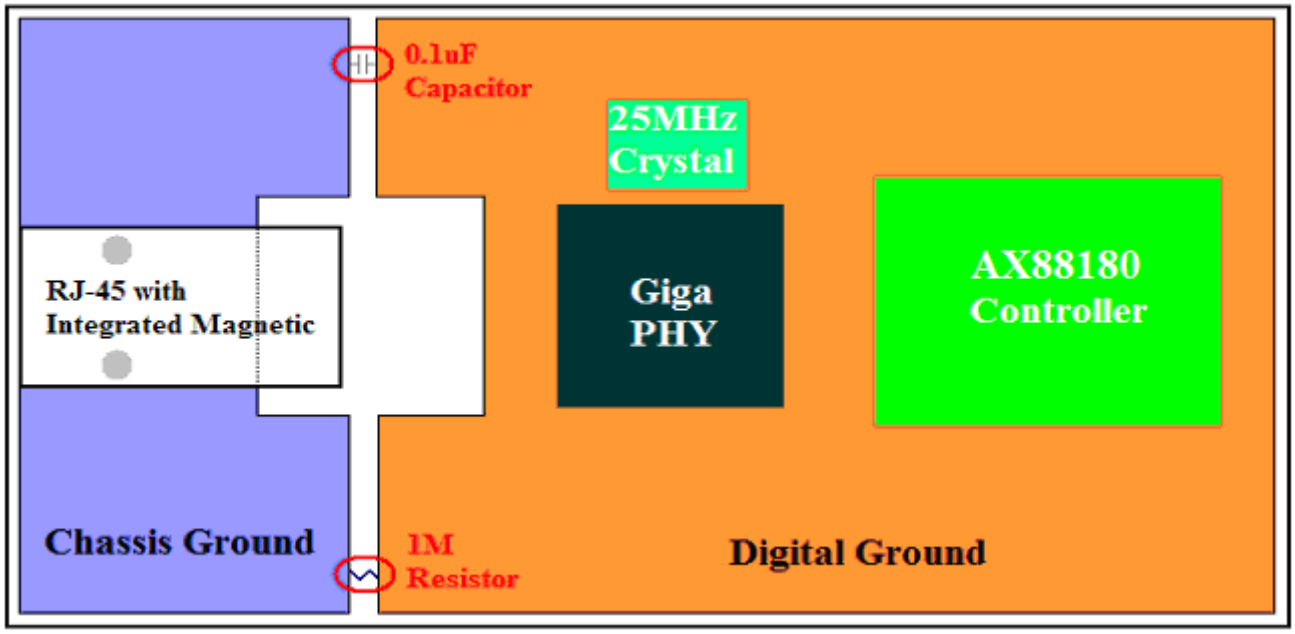


Figure 4. Typical Chassis/Digital Ground Planes for Single RJ-45 with Integrated Magnetic

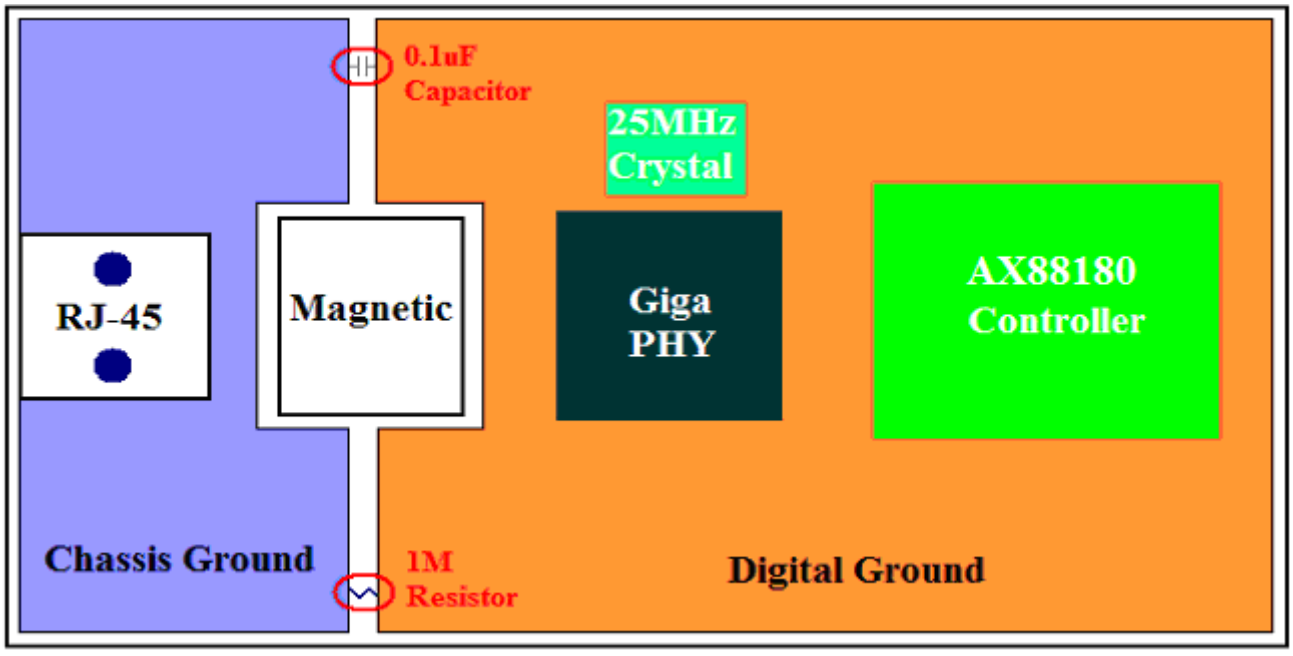


Figure 5. Typical Chassis/Digital Ground Planes for Separated RJ-45 and Magnetic

6-2. All the digital and analog power planes for different voltage supplies should be isolated.

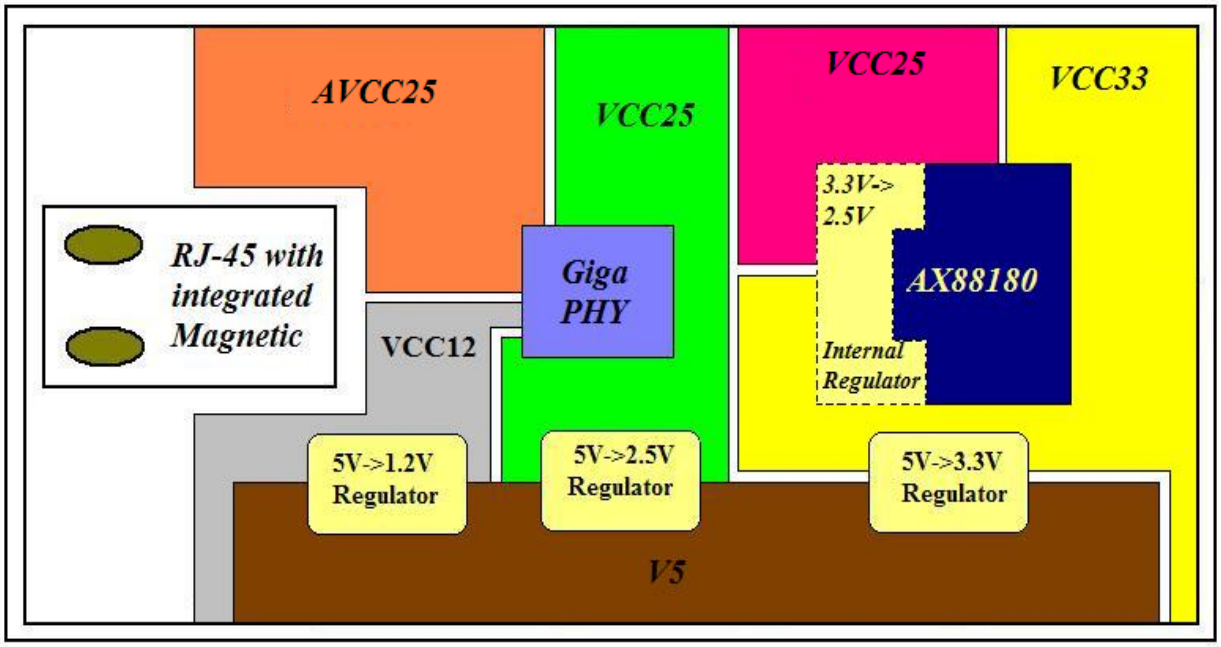


Figure 6. Typical Digital/Analog Power Planes for Single RJ-45 with Integrated Magnetic

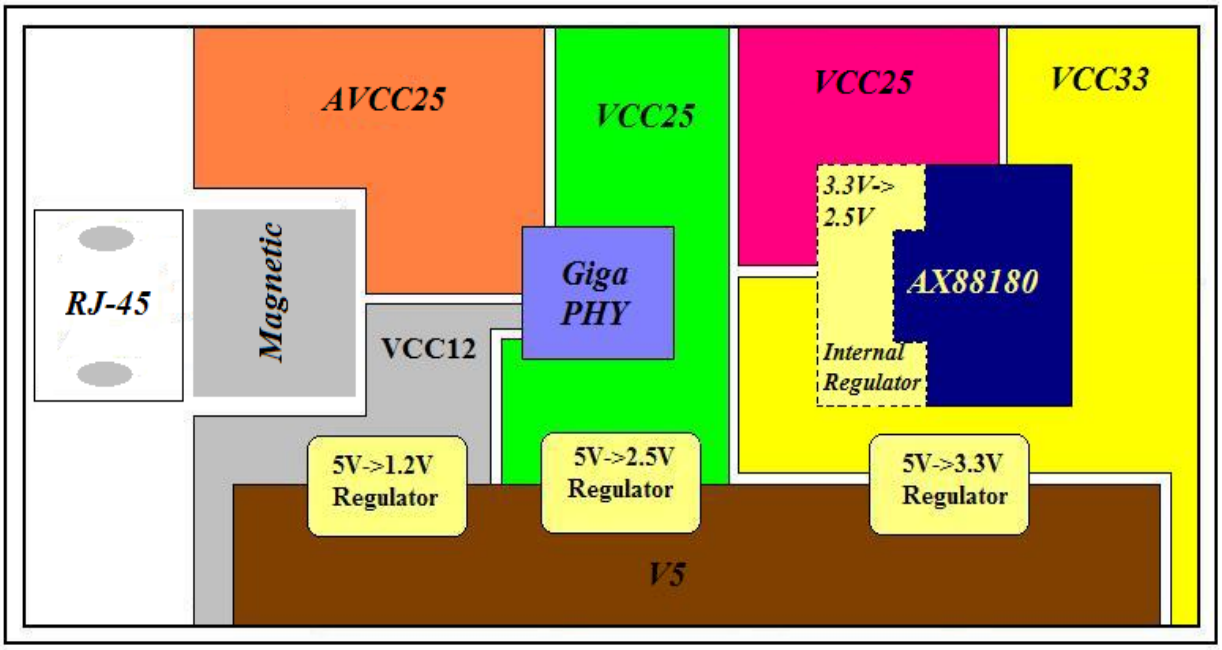
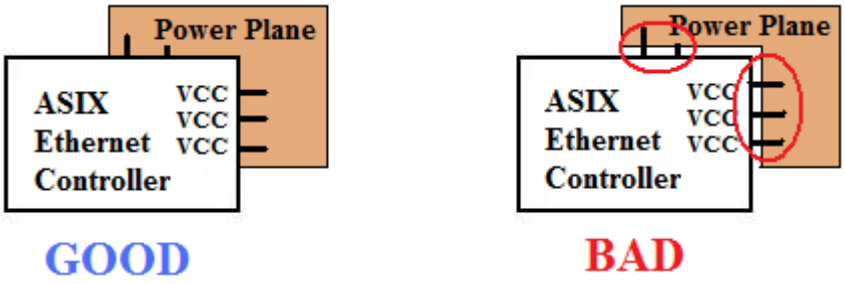


Figure 7. Typical Digital/Analog Power Planes for Separate RJ-45 and Magnetic

Note: The above figures are the Digital Power (VCCxx) and Analog Power (AVCCxx) planes diagram of an illustrative LAN board design. For exact layout pattern, ASIX Electronics provides some demo boards and the layout PCB files and Gerber files for customer reference.

6-2-1. Provide a power plane right underneath the ASIX Ethernet controller such that the VCC pins can be contacted to the power plane without going through thin traces.



6-2-2. All power pins should be implemented with a decoupling capacitor, and the decoupling capacitor should be as close to the respective power pin of ASIX Ethernet controller as possible.

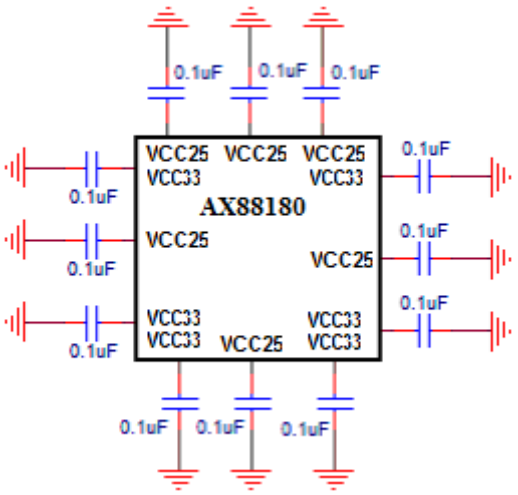


Figure 8. An Example of AX88180 Power Pins and Decoupling Capacitors Circuits

7. Ethernet Magnetic Layout Considerations

The Ethernet magnetic layout considerations are dependent on the external PHY. Please refer to the preferred external PHY Ethernet magnetic layout guide for the detailed requirements.

The following are some general Gigabit Ethernet layout considerations for the differential signals of the Gigabit Ethernet PHY, the Ethernet magnetic and the RJ-45 connector. All trace routes from 10/100/1000M magnetic, RJ-45, and Gigabit Ethernet PHY should be as short as possible. It is an appropriate policy to have the same length for all differential pair signal traces. General speaking, reducing signal crosstalk, providing a solid ground plane, and decreasing parallel route should be considered.

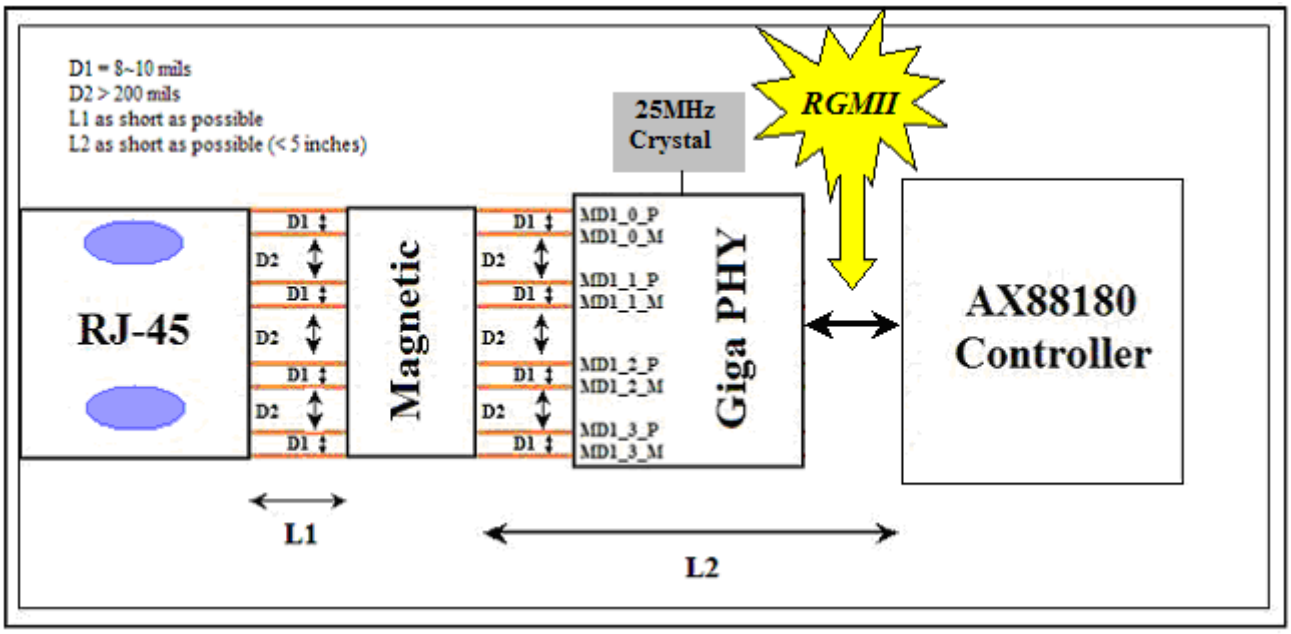
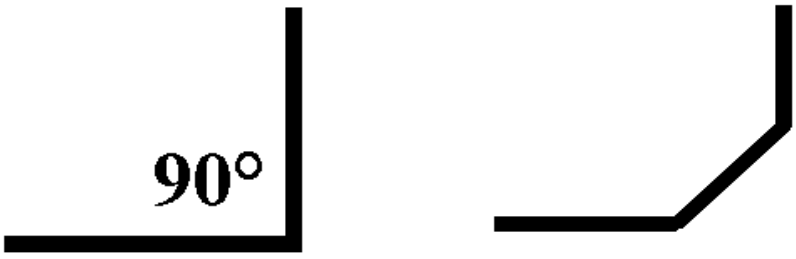


Figure 9. Gigabit Ethernet MDI0±, MDI1±, MDI2±, and MDI3± Differential Pairs Layout

1. The crystal/oscillator clock source and the switching noises from digital signals should be kept away from the MDI0±, MDI1±, MDI2±, and MDI3± differential pairs. Moreover, the crystal/oscillator may be sensitive to wander capacitances and noise from other signals; it is better to deploy the crystal far away from I/O ports, high frequency signal traces, magnetic, board edges, and so on.
2. The Ethernet magnetic should be placed as close to the RJ-45 connector as possible.
3. The Gigabit Ethernet PHY should be placed as close as possible to the magnetic. If there are some limitations on the PCB layout, the trace length from the Gigabit Ethernet PHY to the magnetic should not be longer than 5 inches.
4. The MDI0±, MDI1±, MDI2±, and MDI3± differential pairs should be routed as close as possible. The trace spacing D1 between MDI0+ and MDI0- (or between MDI1+ and MDI1-, MDI2+ and MDI2-, MDI3+ and MDI3-) pair should be in 8 ~ 10 mils. The trace width should be adjusted accordingly to yield the required trace impedance.

5. The spacing D2 should be larger than 200 mils. If the PCB layout is really difficult to meet this requirement, the D2 spacing should be as larger as possible.
6. Route the MDI0±, MDI1±, MDI2±, and MDI3± differential pairs as straight as possible and keep them in parallel for differential pairs.
7. Keep the trace length difference between MDI0+ and MDI0- (or between MDI1+ and MDI1-, MDI2+ and MDI2-, MDI3+ and MDI3-) pair within 700 mils.
8. The termination resistors 49.9Ω and capacitors of the MDI0±, MDI1±, MDI2± and MDI3± differential pairs should be placed as close to the magnetic as possible and the trace should be shorter than 400 mils.
9. Route the MDI0±, MDI1±, MDI2±, and MDI3± differential pairs running symmetric, equal length and close whenever possible.
10. Avoid using vias on the traces of the MDI0±, MDI1±, MDI2±, and MDI3± differential pairs. If the PCB layout really needs to use vias on the differential pairs, please match the vias to keep the differential pairs balanced.
11. The power plane and digital ground plane should not be placed under the magnetic and RJ-45 connector.
12. Avoid routing the signal trace with right angle, instead, the signal trace should be routed with multiple 45° angles.



Worst Better

8. Thermal Considerations

This section describes some information about how to reduce the operating temperature on the embedded Ethernet applications.

8-1. Improve the Cooling Plane

There are some major heat sources on the embedded Ethernet applications included the AX88180 Gigabit Ethernet controller, the external PHY and the external voltage regulators.

You can connect the VCC/GND pins of the AX88180 Gigabit Ethernet controller and the external PHY with wide traces to the respective power/ground planes to increase the cooling effect and reduce the operating temperatures of the AX88180 Gigabit Ethernet controller and external PHY.

You can also add cooling planes on the external voltage regulators to reduce the operating temperature of the external voltage regulators.

8-2. Improve the Air Convection

If the AX88180 Gigabit Ethernet controller and external PHY are implemented on the embedded system, you can place the AX88180 Gigabit Ethernet controller and external PHY at the location with good air convection and stay away from the high-operating-temperature IC such as voltage regulators or MCU to reduce the operating temperature of the AX88180 Gigabit Ethernet controller and external PHY.

8-3. Disable the on-chip regulator

Disabling the on-chip regulator of the AX88180 Gigabit Ethernet controller is an alternative solution to reduce the operating temperature of the AX88180 Gigabit Ethernet controller itself. However, this solution may or may not improve the operating temperature of your overall Gigabit Ethernet applications, depending on how the actual 2.5V power supply is generated.

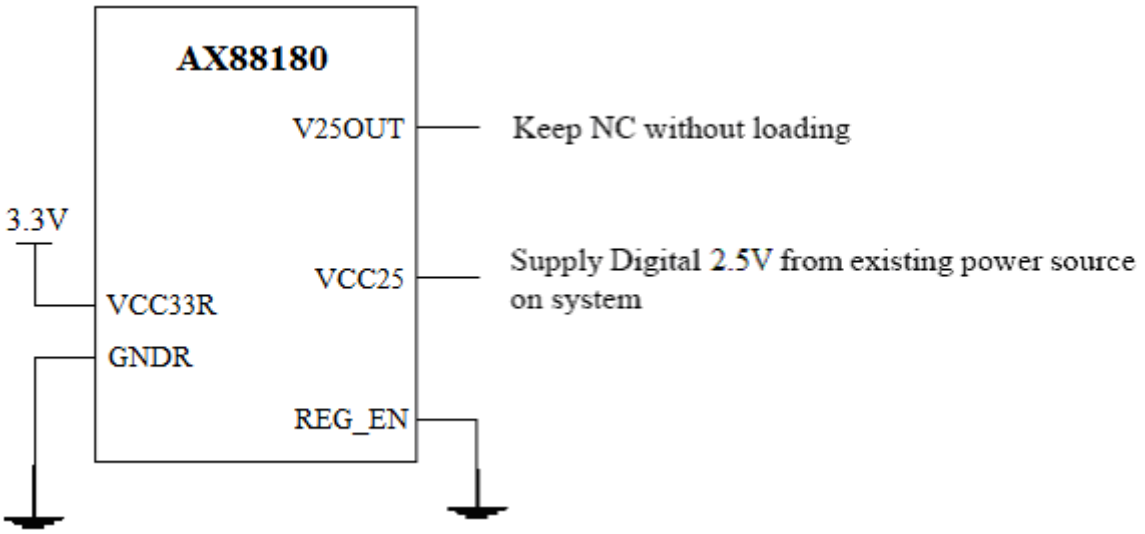


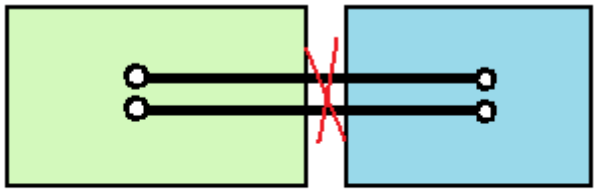
Figure 10. AX88180 On-Chip Regulator Disabled Reference Circuit

9. EMI Considerations

9-1. The chosen connector must be shielded so that EMI integrity of the design is not compromised. The shield must be electrically connected to chassis ground to extend the chassis barrier for high frequency emissions. If an unshielded connector were used, the EMI would pass through the nylon material of the connector. The shield will also prevent less external EMI from entering the chassis.

9-2. To reduce electromagnetic emissions and susceptibility, it is imperative that traces from the transceiver to the magnetic sand from the magnetic to the RJ-45 be routed as differential pairs. The objective is to close the loop area formed by the two conductors. The radiated field from the loop or the voltage picked up by the loop by external fields is governed by the field strength and the area formed by the two conductors. Reasonable board design uses 5~10 mils trace widths separated by 10 mils. Transmit differential pairs should be routed adjacent to a VDDO power plane.

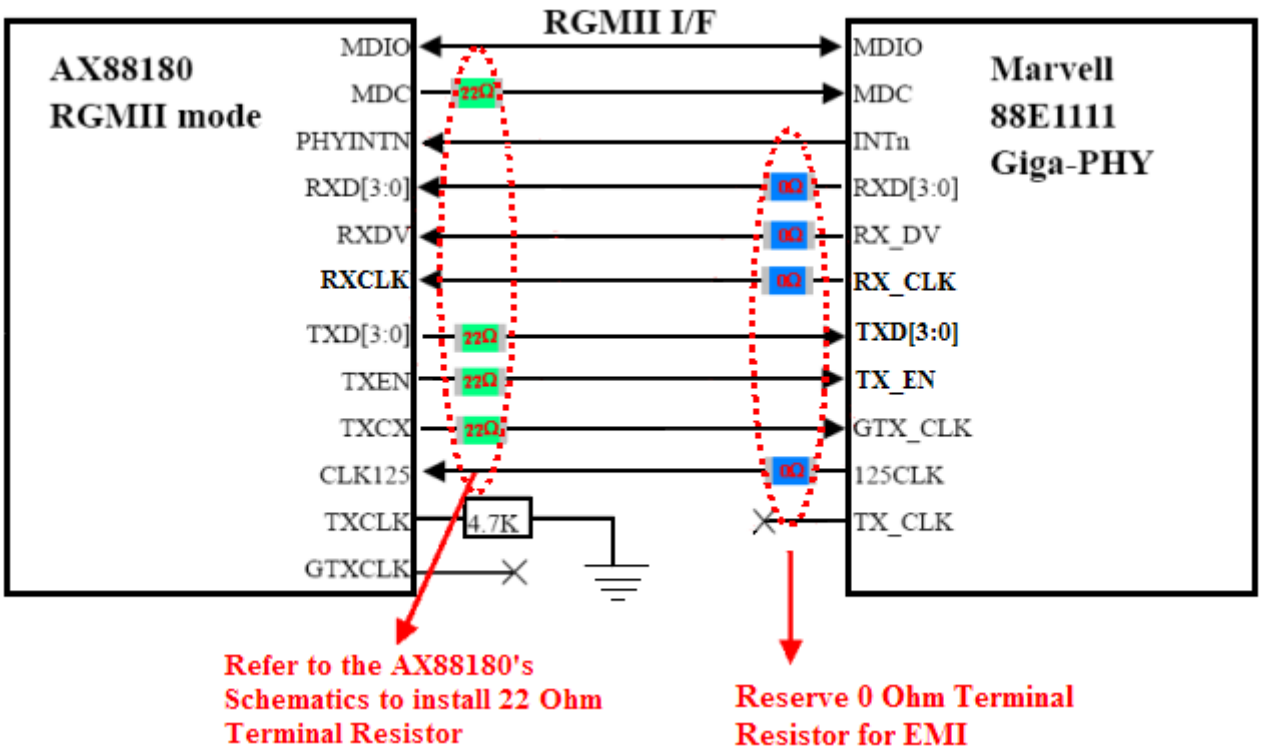
9-3. DON'T CROSS ANY SIGNAL TRACES OVER ANY REFERENCE PLANE CUTS. This might cause some unpredictable EMI problems.



Don't cross any signal traces over any reference plane cuts!!

9-4. A clock circuit or high-speed data access may cause an amount of electromagnetic interference. To minimize noise, EMI, and Jitter, make sure you have installed the termination resistors on the transmitter side (i.e. 22Ω for the MDC, TXD[3:0], TXEN, and TXCX of AX88180). And these resistors must be as close as possible to the AX88180 Gigabit Ethernet controller.

To prevent improper PCB trace delays or some external PHYs that may not contain an internal delay element, please reserve 0Ω terminal resistor in the external PHY side for calibrating the impedance to meet the timing between the MAC and PHY interface. Those reserved 0Ω terminal resistors should be also as close as possible to PHY. Theoretically, that could fine-tune and suppress EMI and Jitter if necessary without revising your circuit by doing so.



10. ESD Considerations

This section describes some information about the ESD design guideline. Users can refer to the following circuit to avoid the ESD issue.

It is necessary to install 1M Ohm and 0.1uf capacitor (2kV or 3kV) to isolate the chassis ground and digital ground as below figure and give the gap with a proper distance (at least 60 mils) for better ESD protection. If possible, directly connect the RJ-45 Connector with fully shielded and choose a RJ-45 Connector that provides a low impedance path to ground for improved noise immunity performance.

Note: The following figure is just an example of the magnetic circuit for the ESD considerations. Please refer to the reference schematic of the preferred external PHY for the detailed Ethernet magnetic circuit.

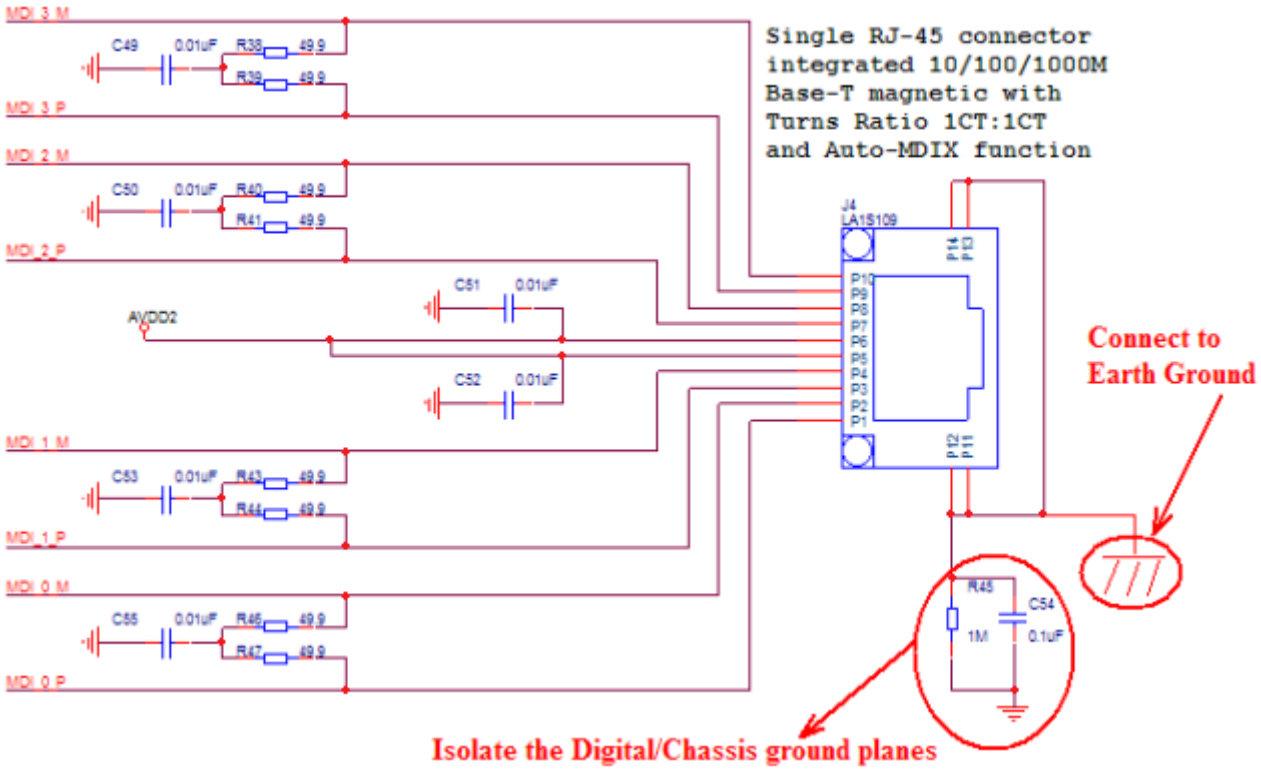


Figure 11. An Example of Single RJ-45 Connector Magnetic Circuit for ESD Considerations

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