GENERAL DESCRIPTION

The SPCA501B provides a single chip solution to the PC camera application. It includes all the control, image processing, image compression and data transaction units needed by a PC camera. The compressed data is transferred to the PC side via the USB bus. The embedded USB controller is a hard-wired state machine. There is no need to use external microprocessors.

FEATURES

- 10 bits CCD raw data input.
- Support RGB mosaic progressive type CCD image sensor with built-in timing generator, such as Sony ICX098AK, Sharp LZ24BP, Panasonic MN3777PT
- Support RGB mosaic CMOS image sensor I/F using flexible external timing.
- Provide window image's white balance measurement and gain parameter control.
- Provide window image's exposure and sharpness measurement.
- 3.3 Volt power supply.
- USB Suspend mode available.
- Support YUV422, YUV420, Raw Data 8 bit and Raw data 10 bit format when using 1Mx16 DRAM , Support YUV420 and Raw Data 8 bit format when using 256Kx16 DRAM.
- Adjustable compression rate.
- Synchronous Serial Interfaces for CDS/AGC or CMOS sensor setting
- USB Vendor ID, Product ID, BCD number and the string descriptor index and data selectable via serial EEPROM.
- 100 pins QFP packages.

BLOCK DIAGRAM

Figure 1. Shows the block diagram of the SPCA501B and its external connection.

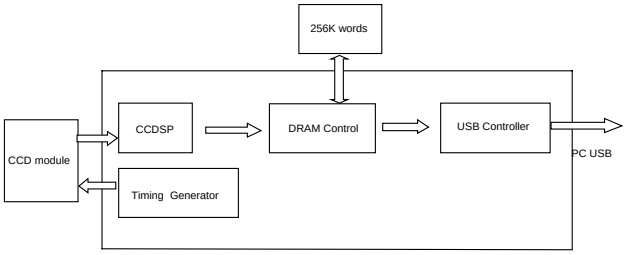


Figure 1. Block diagram of SPCA501B

The first block of the SPCA501B is the CCDSP block. It receives image data from the CCD module. The CCDSP handles a series of image processing operations such as color interpolation, gamma correction and edge enhancement. The image data is then and stored in the 256K or 1 Mega words DRAM. The data is then read back from the DRAM and transmit to the USB bus via the USB controller. The timing generator generates all the clocks needed by the CCD sensor and the clocks needed inside the SPCA501B. The detailed function of each block is described in the following subsection.

■ TIMING GENERATOR DESCRIPTION

The embedded timing generator for CCD sensor and CDS/AGC/ADC can be controlled by USB interface. The programming model is exactly the same as others described in this document. Each programming value will take effect at the next frame. The supported CCD sensors are: Sharp LZ24BP, Sony ICX098AK and Panasonic MN3116/7. CDS/AGC/ADC supported are: Sharp IR3Y38M, Sony CXA2006Q, Hitachi HD49322BF, ADI AD9801/2/3, EXAR XRD98(L)53, … etc. The next section describes all programmable registers and their default values when the chip is reset.

■ DSP

The CCDSP performs optical black compensation, color separation, color correction, edge enhancement, gamma correction, white balance measurement and exposure measurement. The functional block is shown.

There are many parameters could be customized by users. Each parameters is 8-bit which are described in section 6.2. All of the customized parameter value are updated at the beginning of one frame.

The parameter of the white balance gain denotes the unsigned representation, the integer part 3-bit and the decimal fraction part 6-bit (ref. Addr 51 to Addr 55).

The parameter of the color correction and rgb-to-yuv transformation denotes the 2's compliment representation, the sign bit, the integer part 1-bit and the decimal fraction part 6-bit (ref. Addr 8 to Addr 10). The operation range is from 1.984375 to -2. The color correction and rgb-to-yuv transformation performs the following matrix operation :

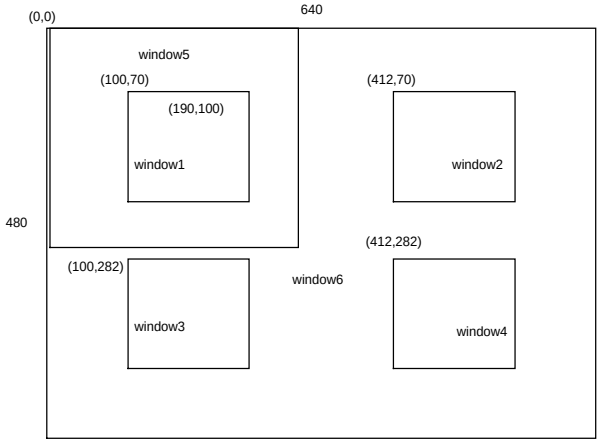
Y = A11 * Rin + A12 * Gin + A13 * Bin

CR = A21 * Rin + A22 * Gin + A23 * Bin

CB = A31 * Rin + A32 * Gin + A33 * Bin

The parameter of the white balance offset denotes the 2's compliment representation, the integer part 7-bit and no the decimal fraction part(ref. Addr 11 to Addr 14).

There are six windows for exposure measurement and five windows for white balance measurement. The window start point (X,Y) is at the most upper left corner. The X is the horizontal axis and equals to 2 times the parameter value. The Y is the vertical axis and equals to 2 times the parameter value except window 5. The Y of the window 5 is same as the parameter value. The window 1 to the window 4 are the 128x128 pixels. The window 5 and the window 6 are the 256x256 pixels. All of the window's position is programmable except the window 6. The average luminance windows and the average (R-G)/(B-G) windows are located on the same position. The window's default position is shown.



The average luminance denotes with dynamic range [0~255] (ref. Addr 21 to Addr 26).
The average (R-G)/(B-G) means the average value of (R-G)/(B-G) in the specified window that the luminance value is greater than the low luminance threshold(Addr 16) and less than the high luminance threshold(Addr 15). It denotes with dynamic range [-128~+127]. However, the actual average (R-G)/(B-G) value in the CCDSP module is 2 times the parameter value (ref. Addr 27 to Addr 30).

The spot count value means the total pixel number in the specified window that the luminance value is greater than the luminance threshold and less than the high luminance threshold . It is a reference value for auto white balance (ref. Addr 33 and Addr 3c).

The look-up table is an optional function for ccd gamma correction. There are 3 combinations of the CCD gamma ROM and CCD look-up table. The first one is the ccd gamma ROM used only. The second is the look-up table used only. The third is both used.(ref. Addr 40 to Addr 50)

The USB burst-read can be performed by reading Addr. 7D, Addr 7E and Addr. 7F.

■ COMPRESSION UNIT

● Input/Output Image Formats

Input image: Compression Unit may accept RGB(up to 10 bit) or YUV 4:2:2 input image format.

Output image: It may generate various output image formats as list in the following table :

Image Size	Mode	Image Type
VGA	640x480	YUV 4:2:0 (compression supported)
CIF	320x240	YUV 4:2:0 (compression supported)
QCIF	160x120	YUV 4:2:0 (compression supported)
VGA	640x480	RGB 10 bits
VGA	640x480	RGB 8 bits
VGA	640x480	YUV 4:2:2

YUV 4:2:0 type images may be either compressed or non-compressed; while other type images will always be non-compressed.

● Compression

Compression is mainly implemented by a two-stage scheme: Filtering & Encoding. First, the image data is processed by filtering and thus creating an intermediate filtered image. Second, the intermediate filtered image is encoded to get a compressed image. Please refer to the VideoComp field of the Control Port 6, 7 in the Register Definition Table for setting the compression approach.

● **Snap Control**

– **Initiate the Snap function**

A snap picture may be obtained either by pressing the hardware snap button on the camera or by writing the software-emulated snap button register.

– **Snap-control operation mode**

Two operation modes for snap-control (Control/status register: address 1, bit 6) are implemented for snapping a picture: one is normal mode; the other is toggle mode.

Normal mode:

When normal mode is selected, 7 image types are defined. User may select one of the 7 image types to display a motion picture. When the snap button is pressed, either by pressing the hardware snap button or writing software-emulated snap button register, the camera will keeps displaying motion pictures according to the image type selected. Meanwhile, the snap bit in the property byte associated with the image frame right after the snap button is pressed will be set to 1. Thus, the application software may detect such change and save an image frame.

Toggle mode:

When toggle mode is selected, 3 image types are classified as video image type and the other 4 image types are classified as snap image type. User may select one of the 3 video image types for video mode and one of the 4 snap image types for snap mode respectively. Video mode and snap mode may toggle dynamically during playing. The camera is default in video mode and displaying motion pictures. When the snap button is pressed, either by pressing the hardware snap button or writing software-emulated snap button register, the camera will change to snap mode right after the current video mode image frame is finished. Then one image frame with the format set for the snap mode will be output. Meanwhile, the snap bit in the property bytes associated with this image frame will also be set as 1. After this snap mode image frame is finished, the camera will immediately resume to video mode and display motion pictures.

– **Related registers & property bytes**

The **hardware snap button status bit** (Control/Status register: address 5, bit 8) will be set to 1 whenever the hardware snap button is pressed and cleared to 0 whenever the host read this register bit. This bit won't be set to 1 by writing the software-emulated snap button register.

The **software-emulated snap button register** (Control/Status register: address 2) may trigger the chip to emulate the behavior of pressing the hardware snap button on the camera to get a snap image when it is written. While, hardware snap button status bit won't be set by this emulation.

The **snap bit in the property bytes** (Property byte 2, bit 7) associated with the image frame right after the snap button is pressed, either by pressing the hardware snap button or writing software-emulated snap button register, will be set to 1. The snap bit associated with the next image frame will resume to 0.

■ DRAM CONTROLLER

The 256K x 16bit DRAM is used as the temporary buffer for the compression controller and as the ISO packet FIFO for the USB controller. The DRAM controller must schedule all the requests to satisfy the bandwidth and latency time requirements for various image operations in order to get better performance. The contents of the DRAM can also be accessed with the USB vendor commands. The procedure is described below.

1. set the starting row address
2. set the starting column address
3. set the return row address
4. set the return column address
5. set the prefetEn bit in the control port 1 register if the operation is read
6. access the DRAM data port

The row and column addresses for the DRAM are internal generated by the chip.

■ USB CONTROLLER

There are two USB pipes built-in the chip: the first one is the default pipe which is used to handle the standard and vendor commands. The other one is the ISO-IN pipe that is used to transmit the image data.

- **Pipe 0**

  The maximum packet size is 8 bytes for pipe 0. All standard commands except SET_DESCRIPTOR and SYNCH_FRAME are supported. All the USB descriptors, except vendor ID and product ID, are hardwired. The values of vendor ID and product ID could be hard-wired or loaded from an external serial EEPROM(AT93C66). The selection is done by an IO-trap pin, refer to IO-pin section for further details. If the EEPROM is selected, the SPCA501B automatically loads the values of the vendor ID and product ID from the EEPROM after power-on reset. The vendor ID is stored in the address 0 of the EEPROM and the products ID is in address 1.

Vendor commands are used to access the internal registers that are categorized to five groups that are selected by the bRequest byte in the setup packet.

	bmRequestType	bRequest	wValue	wIndex	wLength
Timing Generator	0x41/0xc1 (*)	0	data	Register index	0x00/0x01(**)
CCDSP	0x41/0xc1	1	data	register index	0x00/0x01 or 0x08
Control/Status	0x41/0xc1	2	data	register index	0x00/0x02
EPROM	0x41/0xc1	3	data	register index	0x00/0x02
DRAM	0x41/0xc1	4	data	register index	0x00/0x02
Synchronous Serial Interface	0x41/0xc1	5	data	register index	0x00/0x01

* : 0x41 for write , 0xc1 for read.

** : **wLength** specifies the data size in the DATA phase of an USB setup transfer. When writing to a register, the data is stored in the **wValue**. So the value of **wLength** is always 0x00. When reading a register, there are one, two or eight bytes data returned in the data phase.

● **ISO-IN pipe**

For the ISO-IN pipe, the host may issue standard commands to change its maximum packet size. To achieve the optimal system performance, the user must adjust the alternative interface setting based on the image size and compression rate. The following table shows the maximum packet sizes for the available alternative interface settings.

Alternative Interface Setting	Maximum Packet Size for ISO IN Pipe (bytes)
0	0
1	256
2	384
3	512
4	640
5	768
6	896
7	1023

● **ISO Packet Property byte:**

Each image frame stream consists of a set of USB ISO packets. In the first USB ISO packet for an image frame stream, several bytes are defined as property bytes to record the image type, compression scheme, and snap approach for the image frame stream. Thus, software may identify each incoming image frame stream.

There are eight property bytes for the start of frame packet . They are sequence byte, property byte 1, property byte 2, …, property byte 6 and property byte 7. The other packets contains only the sequence byte. The value of the sequence byte in the first packet of an image stream is 0X00, followed by sequence byte 0X01,0X02,0X03 …,etc. The last value of the property byte is 0XFE. The value will wrap around to 0X00 when it reach 0XFE. 0XFF is a special value for the property byte which marks a drop packet, i.e. no image data is in this packet.

The following is the property byte definition:

Property Byte 1:

Bit	Field	Att	Description
7:0	GPIO	r	The general purpose I/O

Property Byte 2:

Bit	Field	Att	Description
3:0	ImageType	r	Image type Two definitions are determined by the snap control bit Snap control = 0 (normal mode) : (Software control) bit [3]: reserved bit bits [2:0] 000: 640x480 YUV 4:2:0 001: 320x240 YUV 4:2:0 010: 160x120 YUV 4:2:0 011: reserved 100: 640x480 RGB 10 bits 101: 640x480 YUV 4:2:2 110: 640x480 RGB 8 bits 111: 640x480 YUV 4:2:0 Snap control = 1 (toggle mode) : (Hardware control) bits [1:0] 00: 640x480 YUV 4:2:0 01: 320x240 YUV 4:2:0 10: 160x120 YUV 4:2:0 11: reserved bits [3:2] 00: 640x480 RGB 10 bits

Bit	Field	Att	Description
			01: 640x480 YUV 4:2:2 10: 640x480 RGB 8 bits 11: 640x480 YUV 4:2:0
4	SnapControl	r	Snap control 0: normal mode 1: toggle mode
6:5	Reserved		
7	Snap	r	Prepare to start to snap an image 0: disable 1: enable

Property Byte 3:

Bit	Field	Att	Description
5:0	Reserved		
7:6	TurnPoint3A	r	Filtering 3A band turn point 00: 0 01: 32 10: 64 11: 96

Property Byte 4:

This is the sequence count for the video frame from the CMOS module.

Property Byte 5:

Bit	Field	Att	Description
7:0	VideoComp	r	VideoComp filed (total 22 bits) consists of Property Byte 5, Property Byte 6 and Property Byte 7 (bit 5~0): Property Byte 5 = VideoComp[7:0] Property Byte 6 = VideoComp[15:8] Property Byte 7 = VideoComp[21:16] Definition of VideoComp[21:0] VideoComp[0]: image compression enable 0: without compression 1: with compression

Bit	Field	Att	Description
			VideoComp[3:1]: threshold for 1D band VideoComp[6:4]: threshold for 2D band VideoComp[9:7]: threshold for 3D band 000: threshold = 0; 001: threshold = 2; 010: threshold = 4; 011: threshold = 8; 100: threshold = 16; 101: threshold = 32; else: threshold = 0; VideoComp[12:10]: quantization factor for 1D band VideoComp[15:13]: quantization factor for 2D band VideoComp[18:16]: quantization factor for 3D band VideoComp[21:19]: quantization factor for 3A band 000: quantization factor = 1 001: quantization factor =2 010: quantization factor = 4 011: quantization factor = 8 100: quantization factor = 16 else: quantization factor = 1

Property Byte 6:

Bit	Field	Att	Description
7:0	VideoComp	r	Please refer to Property Byte 5 (VideoComp[15:8]).

Property Byte 7:

Bit	Field	Att	Description
5:0	VideoComp	r	Please refer to Property Byte 5 (VideoComp[21:16]).
6	EdgeMode	r	Edge enhancement: 0: disable 1: enable
7	GammaEn	r	Gamma correction enable 0: disable 1: enable

● **USB Power Control**

According to the USB specification 1.0, no USB device may require more than 100 mA when first attached, a configured bus-powered USB device attached to a self-powered hub may use up to 500 mA and all USB devices must support a suspended mode that requires less than 500 uA. For the USB power budgeting, there are three states designed in the chip: unconfigured, full-speed and suspend. The chip behavior in the three states are described as follows:

Unconfigured : all output pins, except connecting to the USB transceiver and serial EEPROM pins, are not driven and all bi-directional pins, except the GPIO pins, are pulled-down to 0.

Full-speed : all pins are normally operated.

Suspend : all output pins, except connecting to the USB transceiver pins, are not driven and the serial EEPROM output pins and all bi-directional pins are pulled-down to 0. The internal clocks are gated and unchanged and the clock driver pin is disabled.

There is a newly adding bit at the bit 15 in the control port 0 to enable the DRAM control and TG output buffer. The default value of this bit is zero that means the DRAM control and TG output buffer is disabled. So the power for the DRAM and CCD module must be turned off before this bit is enabled.

■ **SERIAL EEPROM CONTENT**

There is an interface to access the 256x16 serial EEPROM (93c66) that can be used to store some data about the device. The first 6 words have been used by the chip and their purposes are described as follows:

Address	Purpose
0	Vendor ID
1	Product ID
2	BCD Number
3	the starting address of String Descriptor Index 0 and 1
4	the starting address of String Descriptor Index 2 and 3
5	the starting address of String Descriptor Index 4 and 5

If the staring address of these string descriptors is zero, it indicates the string descriptor index is not supported; otherwise it indicates the starting address in the serial EEPROM to store the string descriptor. The string descriptor must be continuously store in the serial EEPROM and its format must follow the USB spec. The purpose of these string descriptor indices is in the following table:

Index	Purpose
0	Language supported by the device
1	The string descriptor describing manufacturer
2	The string descriptor describing product
3	The string descriptor describing the device's serial number
4	The string descriptor describing the device configuration
5	Reserved

■ SYNCHRONOUS SERIAL INTERFACE

The synchronous serial interface is used to program CMOS sensor. The write sequence:

S	Slave Address + wb	ACKs	Sub Address	ACKs	Data	ACKs	P

The read sequence:

S	Slave Address + wb	ACKs	Sub Address	ACKs	
Sr	Slave Address + r	ACKs	Data	ACKm	P

Or

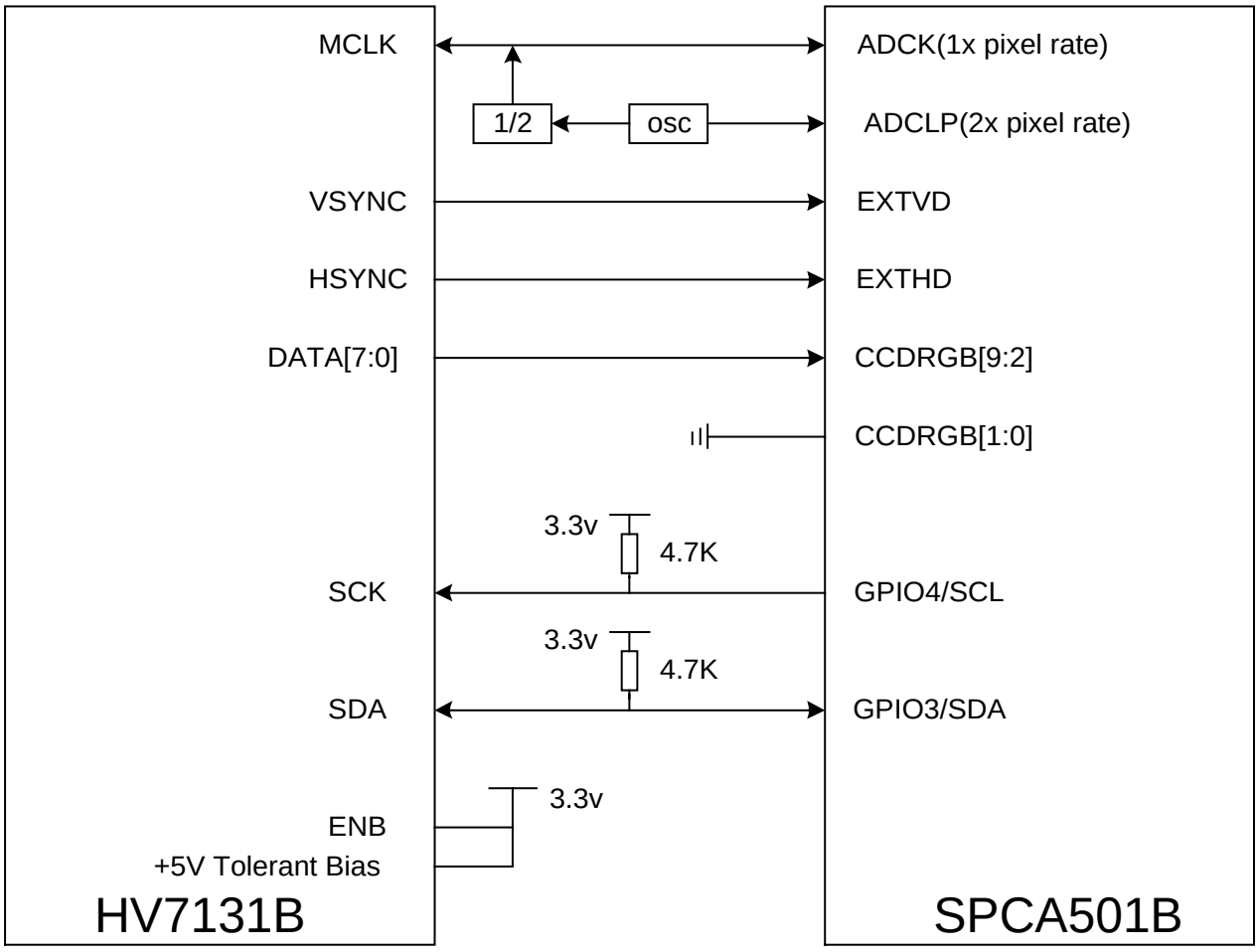
S	Slave Address + wb	ACKs	Sub Address	ACKs	P
S	Slave Address + r	ACKs	Data	ACKm	P

Where S is start condition, ACKs is acknowledge from slave, P is stop, Sr is repeat start condition, and ACKm is acknowledge from master.

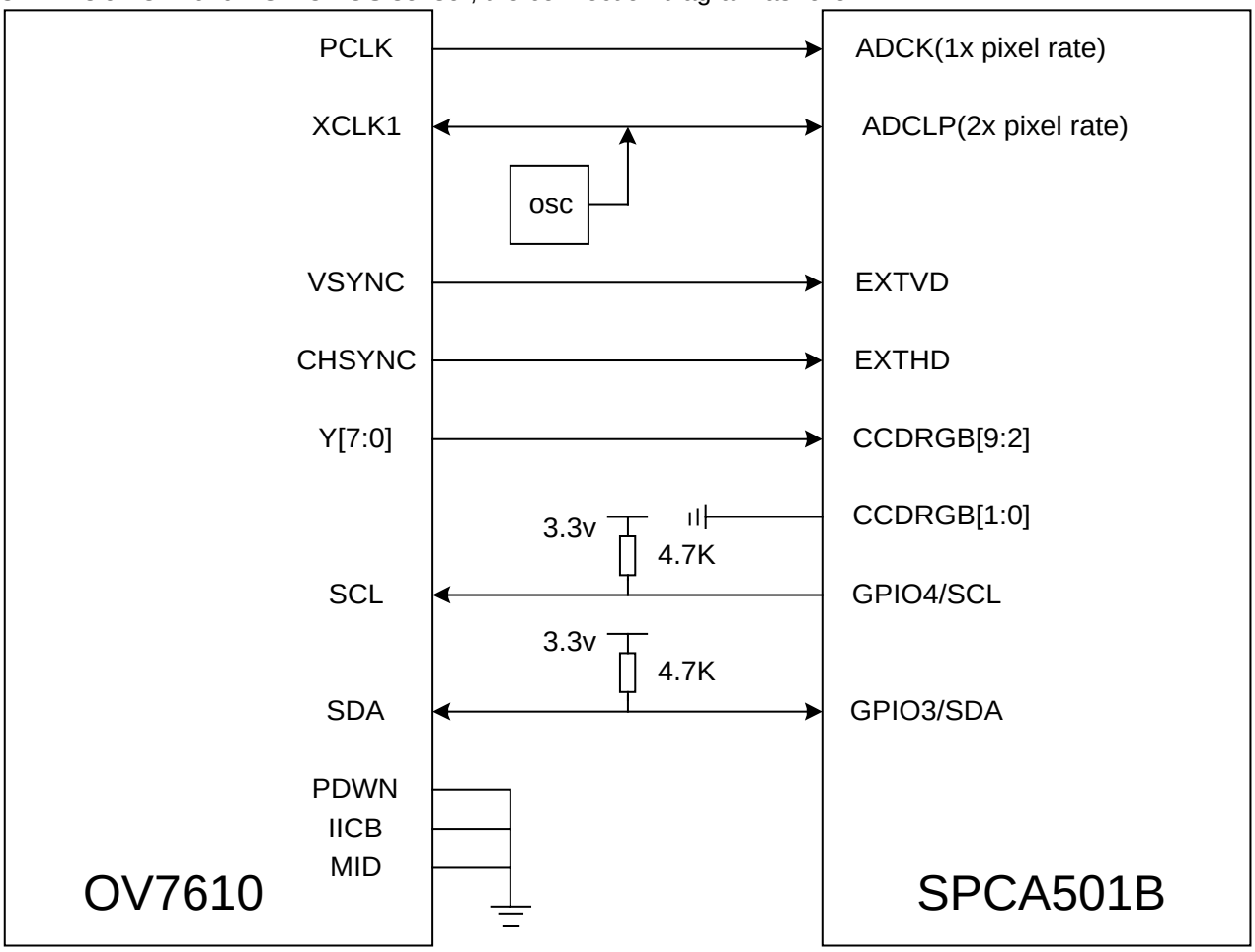
■ CONNECTION DIAGRAM FOR HV7131B AND OV7610BI

SPCA501B can support CMOS sensor by set TGType(control register0 [7:5]) to external sync and enable synchronous serial interface bit(control register0 [13]).

For Hyundai HV7131B VGA CMOS sensor, the connection diagram as follow



For OmniVision OV7610 VGA CMOS sensor, the connection diagram as follow :



Note:DOVDD should be connected to 3.3v

IO TRAP DESCRIPTION

The Output pins ma0 and ma3 are used as IO-trap pins. These signals can be pulled high or low on the system board to configure the SPCA501B operation. The hardware setting is as follows:

Trap Pin	Function
ma[0]	The vendor/product ID selection: 0: by hardwire 1: from the serial EEPROM
ma[3]	The internal USB transceiver selection: 0: disable 1: enable

INTERNAL REGISTER DESCRIPTION

■ TG REGISTER

Addr	Bit	Field	Att	Description	Default
0	7:0	SD[9:8]	r/w	Shutter Speed Values (2 high bits)	2'h0
1	1:0	SD[7:0]	r/w	Shutter Speed Values (8 low bits) SD[9:0] determines the Shutter Speed. Shutter Speed definition (See below)	8'h00
2	2:0	RATE	r/w	Clock Rate compensation for flicker reduction 3'b000 : 1/30 sec/frame 3'b001 : 1/25 sec/frame 3'b100 : No frame rate compensation others: reserved	3'b000
3	3:0	MDCLK	r/w	DCLK clock phase adjustment (for CCDSP to sample CCD image data) MDCLK[3:0] : adjust internal DCLK phase 16-value adjustable, 5~7ns difference per value	4'h0
4	3:0	MDCLKX2	r/w	DCLK*2 clock phase adjustment (for internal CCDSP use)	4'h0
5	7:5	MADCK	r/w	ADCK phase adjustment	3'b100
	4:0	MEXT	r/w	bit[4] - when '1' : Inverting external VD bit[3] - FORBIDDEN bit[2] - when '1' : External HD is treated as a horizontal valid signal, and internal HD will be generated from horizontal valid signal. bit[1] – when '1' : all TG register is updated during vertical blank time, otherwise TG register is updated immediately. bit[0] – when '1' : Additional 5ns delay for ADCK output. Note: TG reg24, 25, 26, 27 will be ignored when bit[2] =1.	5'h0
6	7:0	MFR	r/w	FR phase adjustment	8'h00
7	7:0	MFCDS	r/w	FCDS phase adjustment	8'h40

Addr	Bit	Field	Att	Description	Default
8	7:0	MFS	r/w	FS phase adjustment	8'C0
9	7:0	MRS	r/w	RS phase adjustment	8'h4A
46	5:0	MFRW	r/w	FR pulse width adjustment	6'h00
47	5:0	MFCDSW	r/w	FCDS pulse width adjustment	0
48	5:0	MFSW	r/w	FS pulse width adjustment	0
49	5:0	MRSW	r/w	RS pulse width adjustment	0
4A	3:0	MPOL	r/w	FR, FCDS, FS, RS polarity selection	4'b1000
0A	5:0	MH1	r/w	FH1 phase and delay adjustment	0
0B	5:0	MH2	r/w	FH2 phase and delay adjustment	0
0C	0:0	MD	r/w	Select DMCLP or OBPX to be ADCLP output	1
0D	0:0	MBC	r/w	OBP always toggle or not	1
0E	3:0	MADCLP	r/w	ADCLP delay	0
0F	1:0	MLXID	r/w	pixel identification	2'b10
10	1:0	MHCK	r/w	High Speed clock enable	0
11	3:0	MCKSRC	r/w	Clock source selection	0
12	2:0	MCK_INV	r/w	DCLK/ DCLK*2 inverting	0
20	10:8	HDT_W	r/w	HDT width	
21	7:0	HDT_W	r/w	HDT width	640
22	10:8	VDT_W		VDT width	
23	7:0	VDT_W		VDT width	480
24	9:8	H_OFFSET		H_OFFSET	
25	7:0	H_OFFSET		H_OFFSET	10'h088
26	9:8	V_OFFSET		V_OFFSET	
27	7:0	V_OFFSET		V_OFFSET	10'h018
**					
**					
B0	2:0	EZ_MODE		EZ_MODE selection	0
BF	1:0	CCD_TYPE		CCD Type selection	0
CE	0:0	CDS_PRG		Select CDS or external TG to program	1
C0	2:0	PRG_MODE		Serial Mode selection	3'b001
C1-CA	7:0	CDS_REGs		Serial data registers	0
CB	6:0	CDSBITS		Serial data bits number	16
CC	0:0	SEN		LOAD signal inverting selection	0

Addr	Bit	Field	Att	Description	Default
CD	7:0	CNTDIV		Serial clock divider	128

Shutter Speed Definition:

Explosion time =~ (1/30 - 63.5 us * SD[9:0]) sec

The serial programming sequence is as follows:
First, you set data bits to 0xCB[6:0] and 0xC0[2:0] as programming mode (described later), then you write serial data into 0xC1, 0XC2, 0xC3, .. 0xCA, depending on how many bits you will program. Every writing of 0xCA will schedule a serial data programming at next frame start.
Bits that exceed number of 0xCB will be disregarded. Serial data sequence is listed :

0xC1[7]-0xC1[6]-0xC1[5]-….0XC1[0]-0xC2[7]-0xC2[6]-….0xC2[0],0xC3[7],…..

0xC0[2:0] is defined as follows:

3'b000: (1) Need no SLOAD signal. ONLY SCK, SDATA
(2) Need ONE Dummy SCK pulse cycle to lead actual data
(3) Every rising SCK to latch SDATA
(4) Last falling edge of SCK must latch SDATA@HIGH
(5) AFTER (4), a negedge@SDATA will actually activate the programmed data into internal registers

EXAMPLE: SHARP IR3Y38M, 10-bit series data

3'b001: (1) Need SLOAD signal, SCK, SDATA, SLOAD
(2) SCK start to FALL after SLOAD is LOW
(3) Every rising SCK to latch SDATA
* (4) Rising of SLOAD to actually activate the programmed data into internal registers

EXAMPLE: HITACHI HD49322F, 16-bit series data

3'b010: (1) Need SLOAD signal, SCK, SDATA, SLOAD
(2) SLOAD falls at negedge of SCK
(3) Every rising SCK to latch SDATA
* (4) Rising of SLOAD to actually activate the programmed data into internal registers

EXAMPLE: EXAR XRD44L61/2, 10-bit series data

3'b011: (1) Need SLOAD signal, SCK, SDATA, SLOAD
(2) Every rising SCK to latch DATA
(3) SLOAD stays LOW during SCK CLOCKING, then one PULSE to actually activate the programmed data into internal registers

EXAMPLE :PANASONIC AN2104FHQ, 11-bit series data

3'b100: (1) Need SLOAD signal, SCK, SDATA, SLOAD
(2) SLOAD falls at negedge of SCK
(3) Every rising SCK to latch SDATA
* (4) Rising of SLOAD to actually activate the programmed data into internal registers

EXAMPLE: ADI AD9803, 14-bit series data

3'b101 - 3'b111 : RESERVED for future extension

■ **CCDSP REGISTER**

Addr	Default Parameter	Att	Description
0	f4	r/w	Line memory read counter
1	38	r/w	Bit7-6: edge enhancement gain Bit5: edge enhancement enable Bit4: pixel selection for color separation Bit3: line selection for color separation Bit2: TG control enable Bit1-0: Reserved
2	40	r/w	Optical black level for user setting
3	0a	r/w	Bit7: OB level calculation enable "1" : auto "0" : manual bit6: back-light compensation enable bit5-0: optical black offset
4	40	r/w	Bit7-6: Reserved Bit5-0: edge enhancement noise clip
5			Reserved
6			Reserved
7	66	r/w	Bit7-4: Reserved

Addr	Default Parameter	Att	Description
			Bit3: UV selection Bit2: UV LPF enable Bit1: Y LPF enable Bit0: CRT gamma enable
8	11	r/w	A11 coefficient for color correction and YUV transformation
9	31	r/w	A12 coefficient for color correction and YUV transformation
a	fd	r/w	A13 coefficient for color correction and YUV transformation
b	38	r/w	A21 coefficient for color correction and YUV transformation
c	d2	r/w	A22 coefficient for color correction and YUV transformation
d	f7	r/w	A23 coefficient for color correction and YUV transformation
e	ee	r/w	A31 coefficient for color correction and YUV transformation
f	db	r/w	A32 coefficient for color correction and YUV transformation
10	38	r/w	A33 coefficient for color correction and YUV transformation
11	00	r/w	R offset for white balance
12	00	r/w	G offset for white balance
13	00	r/w	B offset for white balance
14	00	r/w	Gb offset for white balance
15	ff	r/w	High luminance threshold for white balance
16	01	r/w	Low luminance threshold for white balance
17	32	r/w	Window1 start X (x2)
18	23	r/w	Window1 start Y (x2)
19	ce	r/w	Window2 start X (x2)
1a	23	r/w	Window2 start Y (x2)
1b	32	r/w	Window3 start X (x2)
1c	8d	r/w	Window3 start Y (x2)
1d	ce	r/w	Window4 start X (x2)
1e	8d	r/w	Window4 start Y (x2)
1f	00	r/w	Window5 start X (x2)
20	00	r/w	Window5 start Y
21		r	Window1 average luminance
22		r	Window2 average luminance
23		r	Window3 average luminance
24		r	Window4 average luminance
25		r	Window5 average luminance
26		r	Window6 average luminance

Addr	Default Parameter	Att	Description
27		r	Window1 average R-G for white balance
28		r	Window1 average B-G for white balance
29		r	Window2 average R-G for white balance
2a		r	Window2 average B-G for white balance
2b		r	Window3 average R-G for white balance
2c		r	Window3 average B-G for white balance
2d		r	Window4 average R-G for white balance
2e		r	Window4 average B-G for white balance
2f		r	Window5 average R-G for white balance
30		r	Window5 average B-G for white balance
33		r	Window1 white balance spot count (L)
34		r	Window1 white balance spot count (H)
35		r	Window2 white balance spot count (L)
36		r	Window2 white balance spot count (H)
37		r	Window3 white balance spot count (L)
38		r	Window3 white balance spot count (H)
39		r	Window4 white balance spot count (L)
3a		r	Window4 white balance spot count (H)
3b		r	Window5 white balance spot count (L)
3c		r	Window5 white balance spot count (H)
3d		r	Average optical value of build-in accumulator
3e	ff	r/w	Luminance noise clip level
3f	03	r/w	Bit7: line memory reset selection “1”: frame by frame reset “0”: TG control bit6: luminance LPF enable bit5: luminance noise clip enable bit4-bit1: Reserved bit0: CCD gamma enable
40	00	r/w	CCD gamma look-up table
41	10	r/w	CCD gamma look-up table
42	20	r/w	CCD gamma look-up table
43	30	r/w	CCD gamma look-up table
44	40	r/w	CCD gamma look-up table
45	50	r/w	CCD gamma look-up table

Addr	Default Parameter	Att	Description
46	60	r/w	CCD gamma look-up table
47	70	r/w	CCD gamma look-up table
48	80	r/w	CCD gamma look-up table
49	90	r/w	CCD gamma look-up table
4a	a0	r/w	CCD gamma look-up table
4b	b0	r/w	CCD gamma look-up table
4c	c0	r/w	CCD gamma look-up table
4d	d0	r/w	CCD gamma look-up table
4e	e0	r/w	CCD gamma look-up table
4f	f0	r/w	CCD gamma look-up table
50	ff	r/w	CCD gamma look-up table
51	9a	r/w	R gain for white balance(L)
52	43	r/w	Gr gain for white balance(L)
53	5a	r/w	B gain for white balance(L)
54	40	r/w	Gb gain for white balance(L)
55	00	r/w	Bit7:Reserved Bit6: R gain for white balance(H) Bit5:Reserved Bit4: Gr gain for white balance(H) Bit3:Reserved Bit2: B gain for white balance(H) Bit1:Reserved Bit0: Gb gain for white balance(H)
56	01	r/w	Bit7-bit4:Reserved Bit3-bit2: 00: UV no change 01: UV div 2 10: UV div 4 11: UV div 8 bit1: CCD gamma look-up enable bit0: new edge enhancement enable
57	60	r/w	Edge gain high threshold
58	20	r/w	Edge gain low threshold
59	15	r/w	Edge bandwidth high threshold
5a	05	r/w	Edge bandwidth low threshold
7d		r	USB burst read spot count(widow4 to window1)

Addr	Default Parameter	Att	Description
7e		r	USB burst read average B-G/R-G(window4 to window1)
7f		r	USB burst read average luminance(window4 to window1)

■ **CONTROL/STATUS REGISTER**

Addr	Bit	Field	Att	Description
0	0	IDSel	r	The vendor/product ID selection 0: by hardwire 1: from the serial EEPROM
	1	InTrxEn	r	The internal USB transceiver selection 0: disable 1: enable
	2	BlkUSBReset	r/w	Block the USB reset to reset the device 0: disable 1: enable
	3	BlkSuspend	r/w	Block USB suspend 0: disable 1: enable
	4	TCSoftReset	r/w	The soft reset to the TG and CCDSP module 0: disable 1: enable
	7:5	TGType	r/w	The TG type selection (affected pins #63, #64, #90, #95, #96, #98) 000: internal sync 001: reserved 010: external sync, with 2x clock input, low active VD, HD 011: external sync, with 3x clock input, low active VD, HD 100: reserved 101: reserved 110: external sync, with 2x clock input, high active VD, HD 111: external sync, with 3x clock input, high active VD, HD
	12:8	Reserved		
	13	Synchronous Serial Interfaceen	r/w	Synchronous serial interface function 0: disable 1: enable
	14	Reserved	r/w	Reserved
	15	TGMemOutEn	r/w	The TG and memory controller output buffer

Addr	Bit	Field	Att	Description
				0: disable 1: enable
1	0	Reserved		
	1	ISOEn	r/w	The ISO packet machine 0: disable 1: enable
	2	PrefetEn	r/w	Prefetch DRAM enable for the USB host 0: disable 1: enable
	5:3	Reserved		
	6	SnapControl	r/w	Snap control 0: normal mode 1: toggle mode
	13:7	Reserved		
	15:14	TurnPoint3A		Filtering 3A band turn point 00: 0 01: 32 10: 64 11: 96
2		SwSnapButton	w	Software-emulated snap button. When this port is written, whatever the write data is, it will trigger the chip to emulate the behavior of pressing the hardware snap button on the camera.
3	15:0	VID[15:0]	r	The vendor ID in the serial EEPROM
4	15:0	PID[15:0]	r	The product ID in the serial EEPROM
5	7:0	GPIOO	r/w	The general purpose I/O output data
	8	HwSnapButnSta	r	The status for the hardware snap button Set : when the hardware snap button is pressed Cleared : when the register is read
	15:9	Reserved		
6	9:0	VideoComp	r/w	VideoComp filed (total 22 bits) consists of Port 0006 (bit 9:0) & Port 0007 (bit 11:0): Port 0006 (bit 9:0) = VideoComp[9:0] Port 0007 (bit 11:0) = VideoComp[21:10] Definition of VideoComp[21:0]

Addr	Bit	Field	Att	Description
				VideoComp[0]: image compression enable 0: without compression 1: with compression VideoComp[3:1]: threshold for 1D band VideoComp[6:4]: threshold for 2D band VideoComp[9:7]: threshold for 3D band 000: threshold = 0; 001: threshold = 2; 010: threshold = 4; 011: threshold = 8; 100: threshold = 16; 101: threshold = 32; else: threshold = 0; VideoComp[12:10]: quantization factor for 1D band VideoComp[15:13]: quantization factor for 2D band VideoComp[18:16]: quantization factor for 3D band VideoComp[21:19]: quantization factor for 3A band 000: quantization factor = 1 001: quantization factor =2 010: quantization factor = 4 011: quantization factor = 8 100: quantization factor = 16 else: quantization factor = 1
	15:10	Reserved		
7	11:0	VideoComp	r/w	Please refer to Port 0006h (VideoComp[21:10]).
	15:12	ImageType	r/w	Image type Two alternating definitions are determined by the snap control bit Snap control = 0 (normal mode) : (Software control) Bits [14:12] (compression supported) 000: 640x480 YUV 4:2:0 001: 320x240 YUV 4:2:0 010: 160x120 YUV 4:2:0 011: reserved (compression not supported)

Addr	Bit	Field	Att	Description
				100: 640x480 RGB 10 bits 101: 640x480 YUV 4:2:2 110: 640x480 RGB 8 bits 111: 640x480 YUV 4:2:0 bit [15]: reserved bit Snap control = 1 (toggle mode) : (Hardware control) bits [13:12] 00: 640x480 YUV 4:2:0 01: 320x240 YUV 4:2:0 10: 160x120 YUV 4:2:0 11: reserved bits [15:14] 00: 640x480 RGB 10 bits 01: 640x480 YUV 4:2:2 10: 640x480 RGB 8 bits 11: 640x480 YUV 4:2:0
8	15:0	RevNum	r	The revision number
9	15:0	RelNum	r	The release number in the serial EEPROM
10	15:0	TestMode	r/w	The hardware test mode
11	7:0	GPIOIEn	r/w	The general purpose I/O input enable 0: disable 1: enable
	15:8	GPIOI	r	The general purpose I/O input data
12	7:0	Str0Index	r	The starting address of the string descriptor index 0 in the serial EEPROM
	15:8	Str1Index	r	The starting address of the string descriptor index 1 in the serial EEPROM
13	7:0	Str2Index	r	The starting address of the string descriptor index 2 in the serial EEPROM
	15:8	Str3Index	r	The starting address of the string descriptor index 3 in the serial EEPROM
14	7:0	Str4Index	r	The starting address of the string descriptor index 4 in the serial EEPROM
	15:8	Str5Index	r	The starting address of the string descriptor index 5 in the serial EEPROM

■ EEPROM

The EEPROM is organized as 256x16 bits, there are 8 address bits. There are four operation modes as follows:

Mode	Windex-High	Windex-Low
Read	8'h00	access address
Write	8'h01	access address
Write disable	8'h02	don't care
Write enable	8'h03	don't care

■ MEMORY REGISTER

Addr	Bit	Field	Att	Description
0	15:0	Data[15:0]	r/w	The host accesses the data of DRAM.
1	9:0	RowAdr	r/w	The starting row address to access DRAM.
	15:10	Reserved		
2	9:0	ColAdr	r/w	The starting column address to access DRAM.
	15:10	Reserved		
3	9:0	RowAdr	r/w	The return row address to access DRAM.
	15:10	Reserved		
4	9:0	ColAdr	r/w	The return column address to access DRAM.
	15:10	Reserved		

■ REGISTERS FOR SYNCHRONOUS SERIAL INTERFACE

Addr	Bit	Field	Att	Description	Default
0	7:0	DATA[7:0]	r/w	The data transfer buffer. Writing This buffer will initiate write sequence.	8'h00
1	7:0	ADDR[7:0]	w	The register address	8'h00
2	7:0	PREFETCH[0]	w	Writing this bit will initiate read sequence	1'h0
		RSTA[1]		Repeat start condition when rsta is high, otherwise will stop then start.(only work in read)	1'h0
3	7:0	BUSY[0]	r	Busy is high when read or write.	1'h0
4	7:0	SLA[7:0]	w	The slave address	8'h00

Note1 : For write programming : write SLA -> write ADDR -> write DATA ->polling BUSY ->next write

2 : For read programming: write SLA -> decide RSTA -> write ADDR -> write PREFETCH -> polling BUSY -> read DATA

PIN DESCRIPTION

Mnemonic	PIN No.	Type	Description	Memo
dpo/ mclkx	1	O	When the USB external transceiver is enabled, it is as the USB data plus output to external transceiver.	
dmo/ fsx	2	O	When the USB external transceiver is enabled, it is as the USB data minus output to external transceiver.	
usboenn/ bclkx	3	O	When the USB external transceiver enabled, it is as the USB data output enable.	
dpi	4	I	USB data single ended data input from external USB transceiver	pull-up inside the chip
dmi	5	I	USB data single ended data input from external USB transceiver	pull-down inside the chip
din/dx	6	I	When the USB external transceiver is enabled, it is as the USB differential data input from external USB transceiver.	pull-down inside the chip
suspend	7	O	USB suspend signal	
ovdd	8	PWR	Power for IO	
ovss	9	GND	Ground for IO	
xtalin	10	I	Crystal pad	
xtalout	11	O	Crystal pad	
ma0	12	B	DRAM address	IO trap pins
ma1	13	O		
ma2	14	O		
ma3	15	B		IO trap pins
ma4	16	O		
ma5	17	O		
ma6	18	O		
dvdd	19	PWR	Power for internal cell	
dvss	20	GND	Ground for internal cell	
ma7	21	O		
ma8	22	O		
ma9	23	O		
md0	24	B	DRAM data	pull-down inside the chip, 5v tolerant
md1	25	B		pull-down inside the chip, 5v

Mnemonic	PIN No.	Type	Description	Memo
				tolerant
md2	26	B		pull-down inside the chip, 5v tolerant
md3	27	B		pull-down inside the chip, 5v tolerant
md4	28	B		pull-down inside the chip, 5v tolerant
md5	29	B		pull-down inside the chip, 5v tolerant
md6	30	B		pull-down inside the chip, 5v tolerant
md7	31	B		pull-down inside the chip, 5v tolerant
ovdd	32	PWR	Power for IO	
ovss	33	GND	Ground for IO	
md8	34	B		pull-down inside the chip, 5v tolerant
md9	35	B		pull-down inside the chip, 5v tolerant
md10	36	B		pull-down inside the chip, 5v tolerant
md11	37	B		pull-down inside the chip, 5v tolerant
md12	38	B		pull-down inside the chip, 5v tolerant
dvdd	39	PWR	Power for internal cells	
dvss	40	GND	Ground for internal cells	
md13	41	B		pull-down inside the chip, 5v tolerant
md14	42	B		pull-down inside the chip, 5v tolerant
md15	43	B		pull-down inside the chip, 5v tolerant
rasnn	44	O	DRAM row address strobe	
casnn	45	O	DRAM column address strobe	

Mnemonic	PIN No.	Type	Description	Memo
moenn	46	O	DRAM data output enable	
mwenn	47	O	DRAM data write enable	
ecs	48	O	EPROM chip select	pull-down inside the chip
edi	49	O	EPROM data input	pull-down inside the chip
edo	50	I	EPROM data output	pull-down inside the chip
esk	51	O	EPROM clock	pull-down inside the chip
gpio0	52	B	General purpose input/output port	pull-down inside the chip
gpio1	53	B	General purpose input/output port	pull-down inside the chip
gpio2	54	B	General purpose input/output port	pull-down inside the chip
gpio3/ sda	55	B	When synchronous serial interface is enabled, it is as the serial data; otherwise it is as general purpose input/output port.	pull-down inside the chip; need external pull-high when used as sda
uvdd	56	PWR	Power for internal USB transceiver	
dm	57	B	USB data	
dp	58	B		
uvss	59	GND	Ground for internal USB transceiver	
ovdd	60	PWR	Power for IO	
ovss	61	GND	Ground for IO	
gpio4/ scl	62	B	When synchronous serial interface is enabled, it is as the serial clock; otherwise it is as general purpose input/output port.	pull-down inside the chip; need external pull-high when used as scl
extvd	63	I	External VD	pull-down inside the chip
exthd	64	I	External HD	pull-down inside the chip
dvdd	65	PWR	Power for internal cells	
dvss	66	GND	Ground for internal cells	
ccdrgb0	67	I	CCD module raw data inputs	pull-down inside the chip
ccdrgb1	68	I		ref. to pin 67
ccdrgb2	69	I		ref. to pin 67
ccdrgb3	70	I		ref. to pin 67
ccdrgb4	71	I		ref. to pin 67
ccdrgb5	72	I		ref. to pin 67
ccdrgb6	73	I		ref. to pin 67
ccdrgb7	74	I		ref. to pin 67
ccdrgb8	75	I		ref. to pin 67
ccdrgb9	76	I		ref. to pin 67

Mnemonic	PIN No.	Type	Description	Memo
vtax	77	O	CCD vertical shift clock	
vtbx	78	O	CCD vertical shift clock	
vtdx	79	O	CCD vertical shift clock	
vhax	80	O	CCD vertical shift clock	
ofd	81	O	CCD over flow drain	
fr	82	O	CCD reset gate	
fh1	83	O	CCD horizontal shift clock	
fh2	84	O	CCD horizontal shift clock	
ovdd	85	PWR	Power for IO (pin 77 to pin 98)	
ovss	86	GND	Ground for IO (pin 77 to pin 98)	
load	87	O	CDS/AGC register programming chip select	for Hitachi chip HD49322BF
sck	88	O	CDS/AGC register programming clock	
sdi	89	O	CDS/AGC register programming data	
adclp/ mmck	90	B	When the external TG is enabled, it is as the double frequency clock input pin; otherwise it is as the CCD dummy output clamp pulse.	pull-down inside the chip
bpx	91	O	Optical black clamp pulse	
pblk	92	O	Pre-blanking pulse	
dvdd	93	PWR	Power for internal cells	
dvss	94	GND	Ground for internal cells	
Fcds/ ck24m	95	O	CDS S/H pulse or 24Mhz clock output	
Fs/ck12m	96	O	CDS S/H pulse or 12Mhz clock output	
rs	97	O	CDS S/H pulse	
adck/ mck	98	B	When the external TG is enabled, it is as the single frequency clock input pin; otherwise it is as the ADC S/H pulse	pull-down inside the chip
rstnn	99	I	Global reset signal to the chip	active low
snapnn	100	I	snapshot signal	active low

AC/DC CHARACTERIZATION

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to VSS	V_T	-0.4 to 4.0	V
Supply Voltage relative to VSS	V_{DD}	-0.4 to 4.0	V
Short Circuit Output Current	I_{OUT}	50	mA
Power Dissipation	P_D	0.2	W
Operating Temperature	T_{OPT}	0 to +70	°C
Storage Temperature	T_{STG}	-55 to 125	°C

■ RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}	3.1	3.3	3.45	V
Input low voltage	V_{IL}	-0.3	-	0.3VDD	V
Input high voltage	V_{IH}	0.7VDD	-	VDD+10%	V

■ DC CHARACTERISTICS

T_A=0°C - 70°C, VDD=3.3V ±5%, VSS=0V

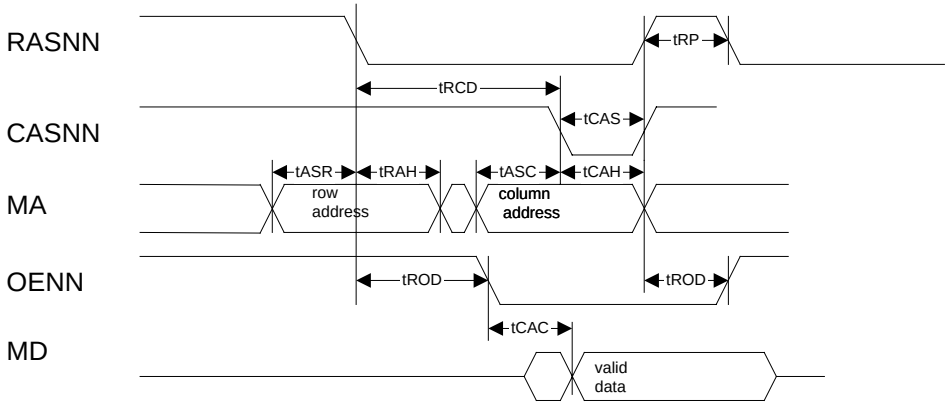
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Condition
V_{OL}	Output low voltage	-	-	0.4	V	4mA buffer I_{OL}=4mA 8mA buffer I_{OL}=8mA 12mA buffer I_{OL}=12mA
V_{OH}	Output high voltage	2.4	-	-	V	4mA buffer I_{OH}=-4mA 8mA buffer I_{OH}=-8mA 12mA buffer I_{OH}=-12mA

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Condition
I_{DD} (un-configured)	Power supply current	-	80	-	mA	fop=48MHz
I_{DD} (normal)	Power supply current	-	100	-	mA	fop=48MHz
I_{DD} (suspend)	Power supply current	-	-	75	uA	
I_{IL}	Input leakage current	-	10	-	μA	V_{IN}=0V

Notes: (1) All DC electrical characteristics are measured at 25°C

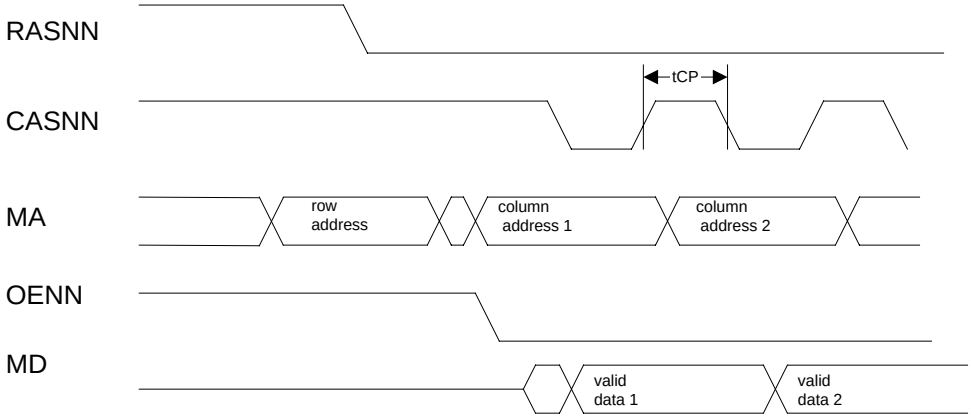
■ AC CHARACTERISTICS

1. DRAM Single Read Timing :



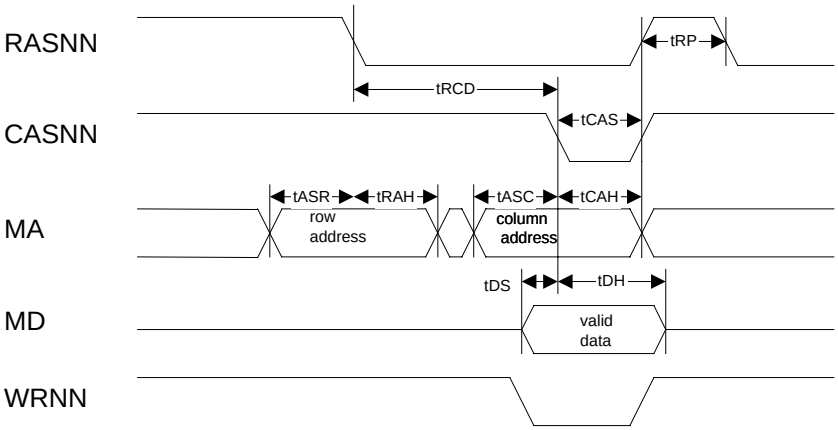
Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
tRCD	RAS to CAS delay	-	60	-	ns	
tRP	RAS recovery time	-	40	-	ns	
tCAS	CAS pulse width	10	20	-	ns	
tASR	Address to RAS setup time	-	40	-	ns	
tRAH	RAS to address hold time	-	40	-	ns	
tASC	Address to CAS setup time	-	20	-	ns	
tCAH	RAS to address hold time	-	20	-	ns	
tROD	RAS to OE delay	-	40	-	ns	
tCAC	CAS to valid data delay	-	-	30	ns	

2. DRAM Page Mode Read Timing :



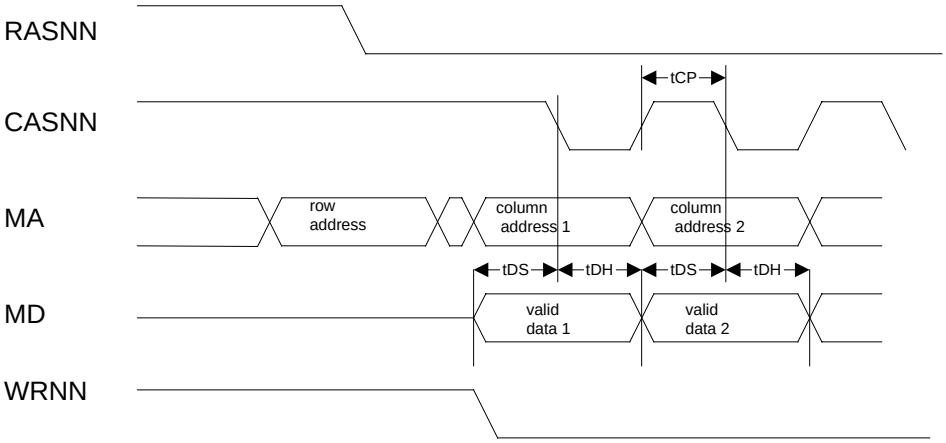
Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
TCP	CAS recovery time	-	20	-	ns	

3. DRAM Single Write Timing :



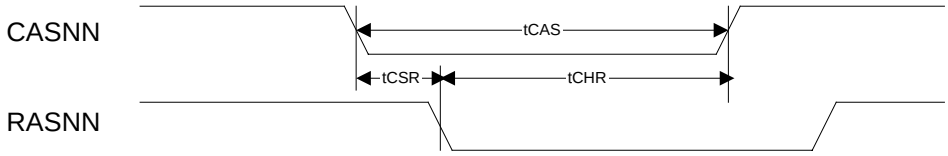
Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
tRCD	RAS to CAS delay	-	60	-	ns	
tRP	RAS recovery time	-	40	-	ns	
tCAS	CAS pulse width	-	20	-	ns	
tASR	Address to RAS setup time	-	40	-	ns	
tRAH	RAS to address hold time	-	40	-	ns	
tASC	Address to CAS setup time	-	20	-	ns	
tCAH	RAS to address hold time	-	20	-	ns	
tDS	data to CAS setup time	-	20	-	ns	
tDH	data to CAS hold time	-	20	-	ns	

4. DRAM Page Mode Write Timing :



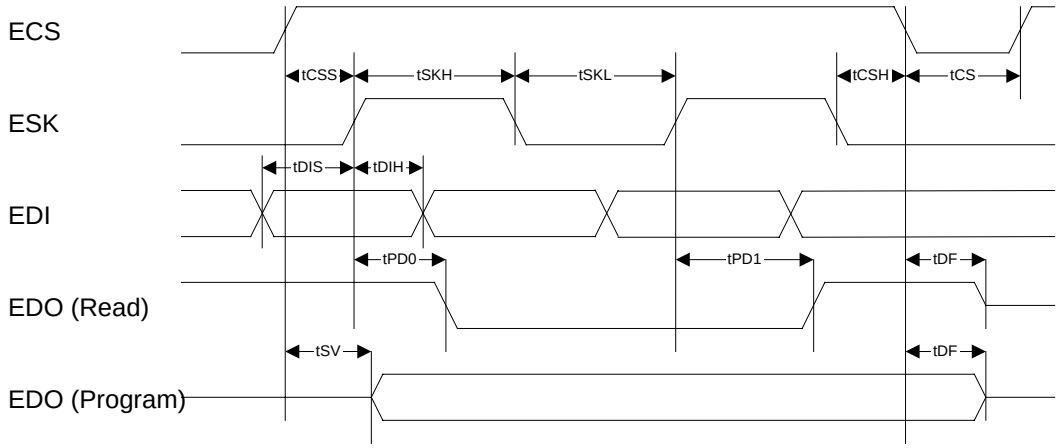
Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
tCP	CAS recovery time	-	20	-	ns	
tDS	data to CAS setup time	-	20	-	ns	
tDH	data to CAS hold time	-	20	-	ns	

5. Refresh Cycle Timing :



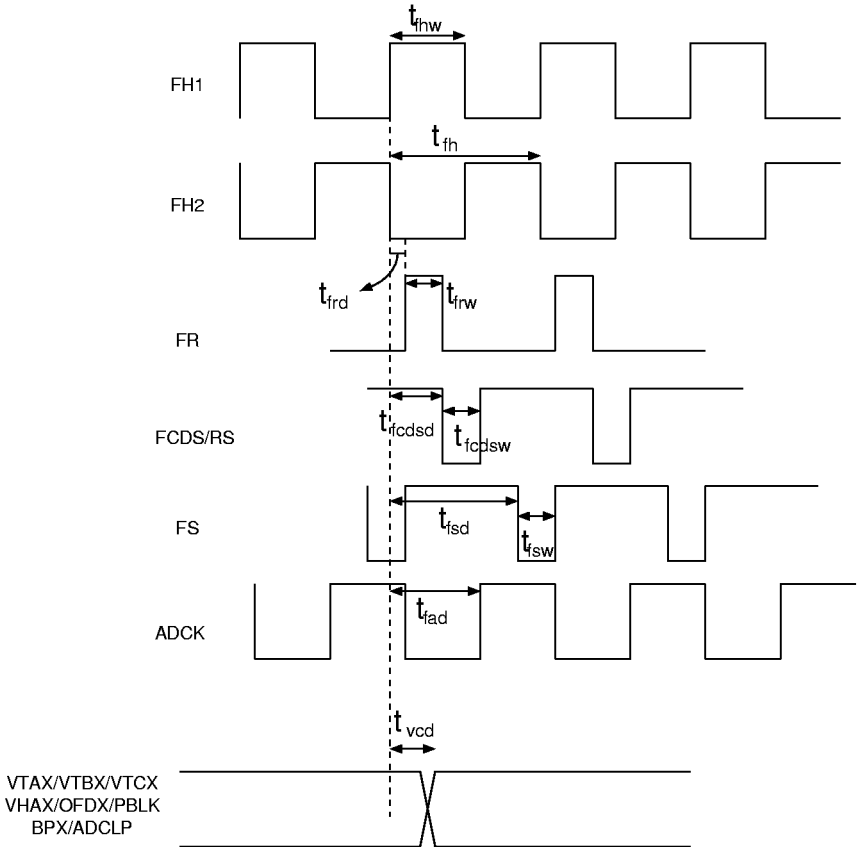
Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
tCAS	CAS low pulse width	-	80	-	ns	
tCSR	CAS to RAS setup time	-	40	-	ns	
tCHR	RAS to CAS hold time	-	40	-	ns	

6. Serial EEPROM Timing :



Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
tSKH	ESK High Time	-	2.5	-	us	
tSKL	ESK Low Time	-	2.5	-	us	
tCS	Minimum ECS Low Time	-	5	-	us	
tCSS	ECS Setup Time	-	2.5	-	us	
tDIS	EDI Setup Time	-	2.5	-	us	
tCSH	ECS Hold Time	-	2.5	-	us	
tPD1	Output Delay to 1	0	-	2.5	us	
tPD0	Output Delay to 0	0	-	2.5	us	
tSV	ECS to Status Valid	0	-	5.0	us	
tDF	ECS to EDO in Z	0	-	5.0	us	

7. Timing Generator Dynamic Timing Diagram :



Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
tFHW	FH1 and FH2 High Time	-	40	-	ns	*1
tFH	FH1/FH2 period	-	83	-	ns	*2
tFRD	FR Delay Time	-	4.0	-	ns	*3
tFRW	FR pulse width	9.0	20	30	ns	*4
tFCDSD	FCDS Delay Time	-	26	-	ns	*3
tFCDSW	FCDS pulse width	12	20	32	ns	*4
tFSD	FS Delay Time	-	66	-	ns	*3
tFSW	FS pulse width	12	20	35	ns	*4
tFAD	ADCK Delay Time	-	46	-	ns	*3
tVCD	Vertical signals delay time	-	5.0	-	ns	*5

Notes:

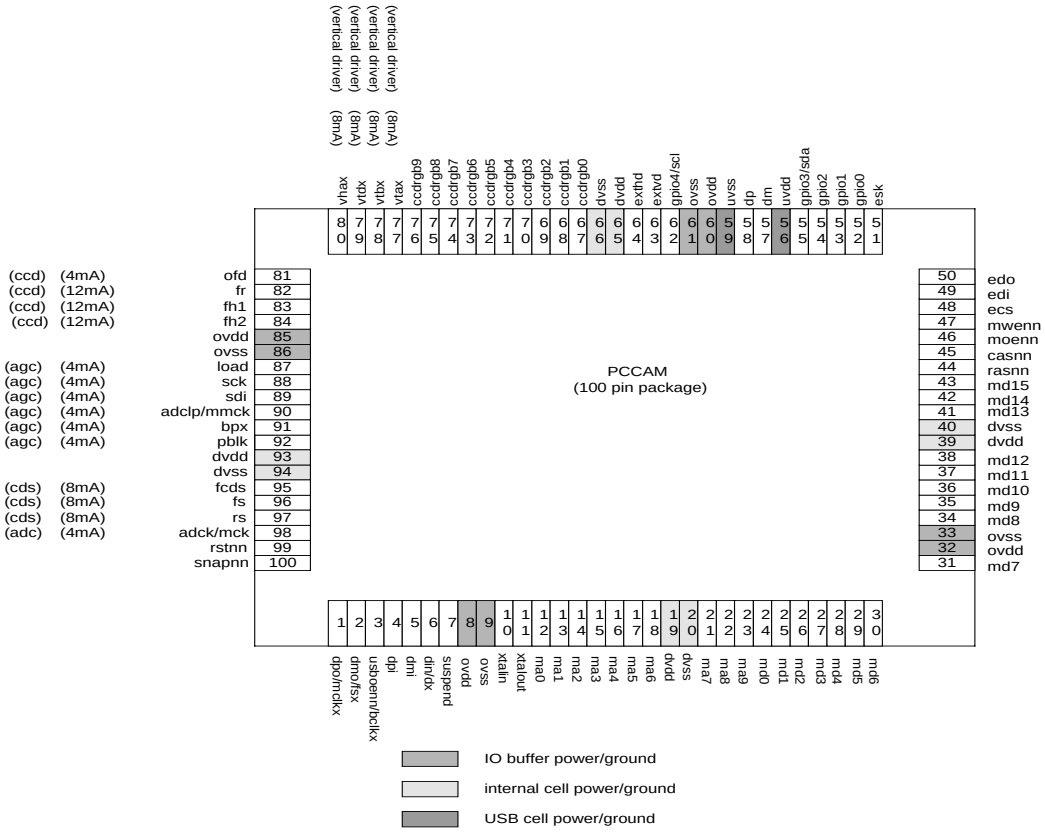
1. FH1 and FH2 high time is determined by the internal 48MHz clock period
2. FH1 and FH2 period is the same as the internal 48MHz clock and they are mutually inverted
3. All CDS/AGC/ADC sampling signals (FR, FCDS, FS, ADCK) are programmable to sample CCD output signal correctly. The delay values in this table are default at power-on reset. However, these signals can

be adjusted to fit CDS/AGC/ADC chip requirement. See related sections in this datasheet for programming these delay values.

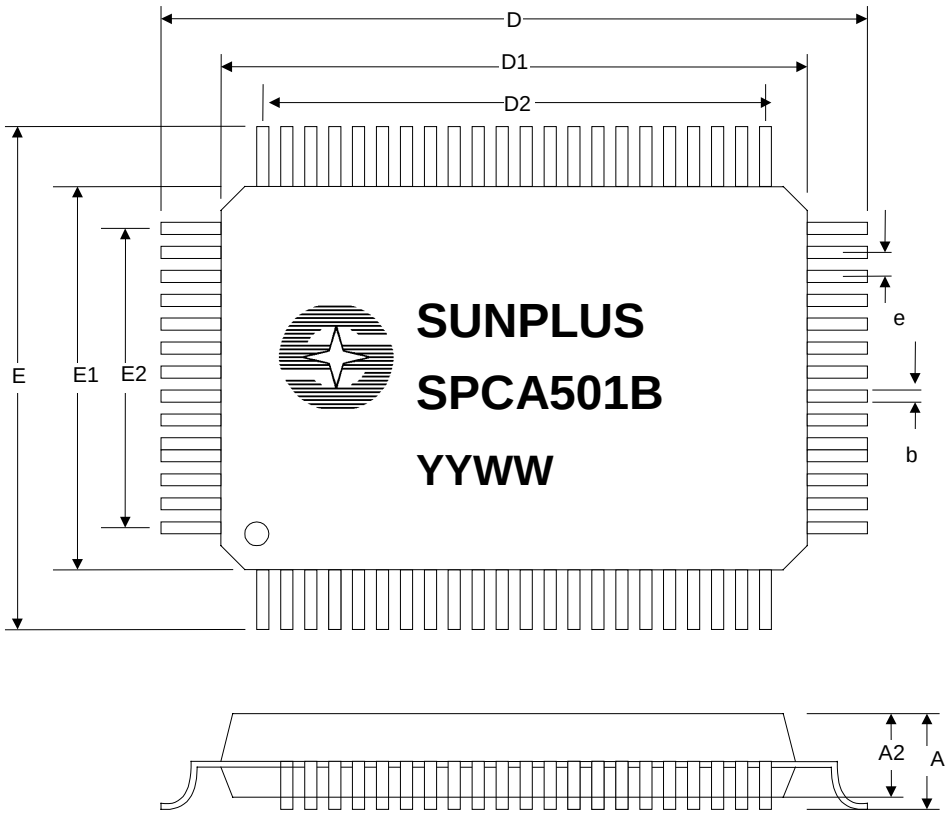
4. FR, FCDS ad FS pulse widths can be adjusted. The widths in this table show the adjustment range. Typical values are default at power-on reset. See related sections in this datasheet for programming these pulse widths.
5. All other signals (VTAX, VTBX, VTCX, VHAX, OFDX, PBLK, BPX, ADCLP) changes state at rising edge of FH1, except ADCLP, which can be adjusted according to CDS/AGC/ADC requirement. Like other programming delays, the adjustable values can be found in previous sections.

PACKAGE

■ PIN Name Outline



■ **PAKCAGE Dimension**



Symbol	Min.	Nom.	Max.
A	-	-	3.4
A2	2.5	2.72	2.9
E	17.20	17.20	17.20
E1	14.00	14.00	14.00
E2	12.35	12.35	12.35
D	23.20	23.20	23.20
D1	20.00	20.00	20.00
D2	18.85	18.85	18.85
e	0.65	0.65	0.65
b	0.20	0.30	0.38

Unit: millimeter

NOTE: SUNPLUS TECHNOLOGY CO., LTD reserves the right to make changes at any time without notice in order to improve the design and performance and to supply the best possible product.

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