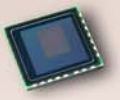
OmniVision



# datasheet

PRODUCT SPECIFICATION

1/13" CMOS VGA (640x480) image sensor
with OmniPixel3-HS™ technology

OV7690/OV7191

**CMOS VGA (640 x 480) image sensor with OmniPixel3-HS™ technology**

datasheet (CSP3)
PRODUCT SPECIFICATION

version 2.1
february 2009

To learn more about OmniVision Technologies, visit www.ovt.com.
OmniVision Technologies is publicly traded on NASDAQ under the symbol OVTI.

## applications

- cellular phones
- toys
- PC multimedia
- digital still cameras

## ordering information

- **OV07690-A20A** (color, lead-free)
  20-pin CSP3
- **OV07191-A20A** (b&w, lead-free)
  20-pin CSP3

## features

- ultra low power and low cost
- automatic image control functions: automatic exposure control (AEC), automatic white balance (AWB) and automatic black level calibration (ABLC)
- programmable controls for frame rate, AEC/AGC, mirror and flip, scaling and windowing
- image quality controls: color saturation, hue, gamma, sharpness (edge enhancement), lens correction, defective pixel canceling, and noise canceling
- support for output formats: RAW RGB, RGB565, CCIR656 and YCbCr422
- support for video or snapshot operations
- support for images sizes: VGA, scaling CIF and sub-sampling QVGA and scaling QCIF
- support for horizontal and vertical sub-sampling
- standard serial SCCB interface
- digital video port (DVP) parallel output interface
- on-chip phase lock loop (PLL)
- programmable I/O drive capability
- support for black sun cancellation
- built-in 1.5V regulator for sensor core power
- suitable for module size of 4.5 mm x 4.5mm

## key specifications

- **active array size:** 640 x 480
- **power supply:**
  analog: 2.6 ~ 3.0V
  I/O: 1.7 ~ 3.0V
- **power requirements:**
  active: 100 mW
  standby: 20 µA
- **temperature range:**
  operating: -30°C to 70°C (see **table 8-1**)
  stable image: 0°C to 50°C (see **table 8-1**)
- **output formats (8-bit):** YUV 422 / YCbCr422, RGB565, CCIR656, raw RGB data
- **lens size:** 1/13"
- **lens chief ray angle:** 25°
- **input clock frequency:** 6 ~ 27 MHz
- **S/N ratio:** 38 dB
- **dynamic range:** 66 dB
- **maximum image transfer rate:**
  VGA (640x480): 30 fps for VGA
  QVGA (320x240): 60 fps for QVGA
- **sensitivity:** 960 mV/(Lux • sec)
- **shutter:** rolling shutter
- **scan mode:** progressive
- **maximum exposure interval:** 511 x $t_{ROW}$
- **gamma correction:** programmable
- **pixel size:** 1.75 µm x 1.75 µm
- **well capacity:** 5.7 $Ke^-$
- **dark current:** 4.7 mV/s @ 60°C
- **fixed pattern noise (FPN):** 0.7 $e^-$
- **image area:** 1148 µm x 861 µm
- **package dimensions:** 2467 µm x 2917 µm

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# 1 signal descriptions

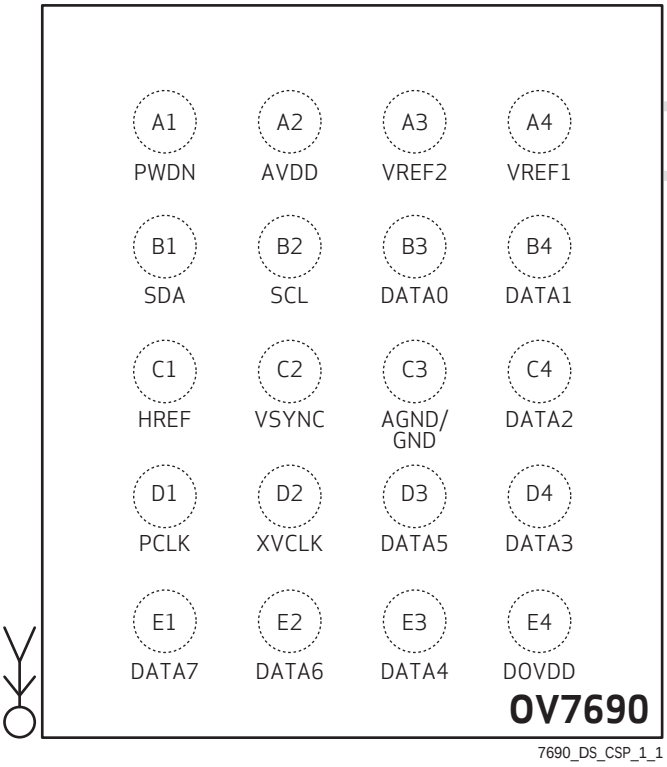
**table 1-1** lists the signal descriptions and their corresponding pin numbers for the OV7690/OV7191 image sensor. The package information is shown in **section 9**.

**table 1-1** signal descriptions

| pin number | signal name | pin type | description | default I/O status |
|---|---|---|---|---|
| A1 | PWDN | input | power down active high with internal pull-down resistor | input |
| A2 | AVDD | power | analog power | |
| A3 | VREF2 | reference | internal analog reference | |
| A4 | VREF1 | reference | internal analog reference | |
| B1 | SDA | I/O | SCCB data | |
| B2 | SCL | input | SCCB input clock | |
| B3 | DATA0 | I/O | digital video port (DVP) bit[0] | output |
| B4 | DATA1 | I/O | digital video port (DVP) bit[1] | output |
| C1 | HREF | I/O | horizontal reference output | output |
| C2 | VSYNC | I/O | vertical sync output | output |
| C3 | AGND/GND | ground | ground for circuit | |
| C4 | DATA2 | I/O | digital video port (DVP) bit[2] | output |
| D1 | PCLK | I/O | pixel clock output | output |
| D2 | XVCLK | input | system input clock | input |
| D3 | DATA5 | I/O | digital video port (DVP) bit[5] | output |
| D4 | DATA3 | I/O | digital video port (DVP) bit[3] | |
| E1 | DATA7 | I/O | digital video port (DVP) bit[7] | |
| E2 | DATA6 | I/O | digital video port (DVP) bit[6] | |
| E3 | DATA4 | I/O | digital video port (DVP) bit[4] | |
| E4 | DOVDD[a] | power | power for I/O circuit | |

a. for different DOVDDs, register 0x49[3:0] must be set according to the settings in **section 2.8,** DOVDD power requirements.

figure 1-1 pin diagram




top view

# 2 system level description

## 2.1 overview

The OV7690/OV7191 (color) image sensor is a low voltage, high-performance 1/13-inch VGA CMOS image sensor that provides the full functionality of a single chip VGA (640x480) camera using OmniPixel3-HS™ technology in a small footprint package. It provides full-frame, sub-sampled, windowed and images in CIF or QCIF formats via the control of the Serial Camera Control Bus (SCCB) interface.

The OV7690/OV7191 has an image array capable of operating at up to 30 frames per second (fps) in VGA resolution with complete user control over image quality, formatting and output data transfer. All required image processing functions, including exposure control, gamma, white balance, color saturation, hue control, defective pixel canceling, noise canceling, etc., are programmable through the SCCB interface. In addition, Omnivision image sensors use proprietary sensor technology to improve image quality by reducing or eliminating common lighting/electrical sources of image contamination, such as fixed pattern noise, smearing, etc., to produce a clean, fully stable, color image.

## 2.2 architecture

The OV7690/OV7191 sensor core generates streaming pixel data at a constant frame rate indicated by HREF, VSYNC, and PCLK.

The timing generator outputs signals to access the rows of the image array, precharging and sampling the rows of the sensor array in series. In the time between pre-charging and sampling a row, the charge in the pixels decreases with the time exposed to the incident light. This is known as exposure time.

The exposure time is controlled by adjusting the time interval between precharging and sampling. After the data of the pixels in the row has been sampled, it is processed through analog circuitry to correct the offset and multiply the data with corresponding gain. Following analog processing is the ADC which outputs 10-bit data for each pixel in the array.

figure 2-1 OV7690/OV7191 block diagram

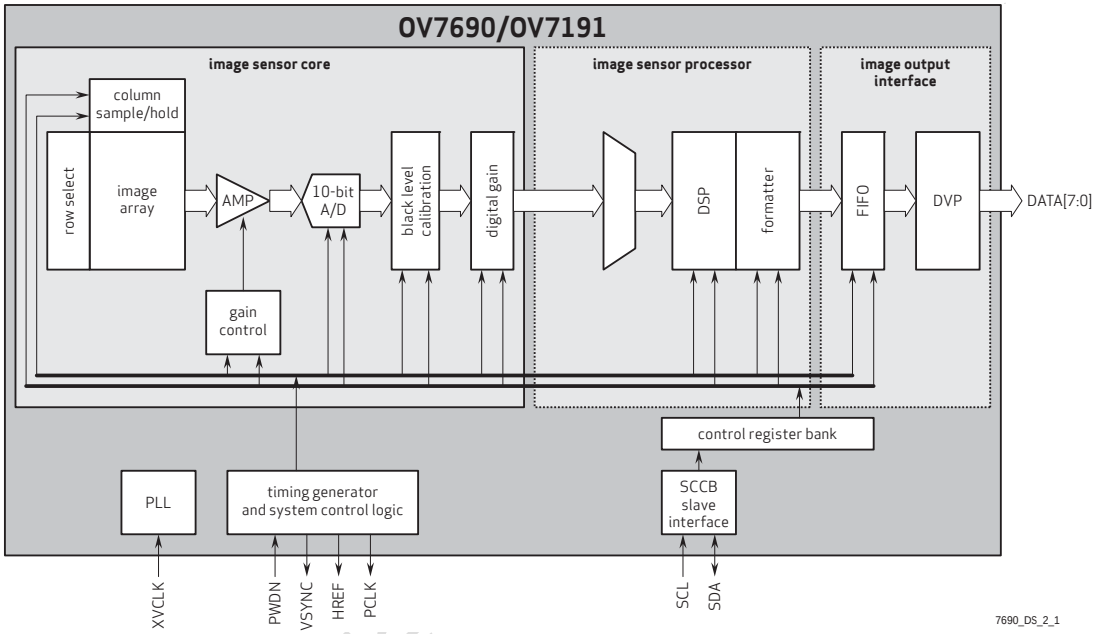
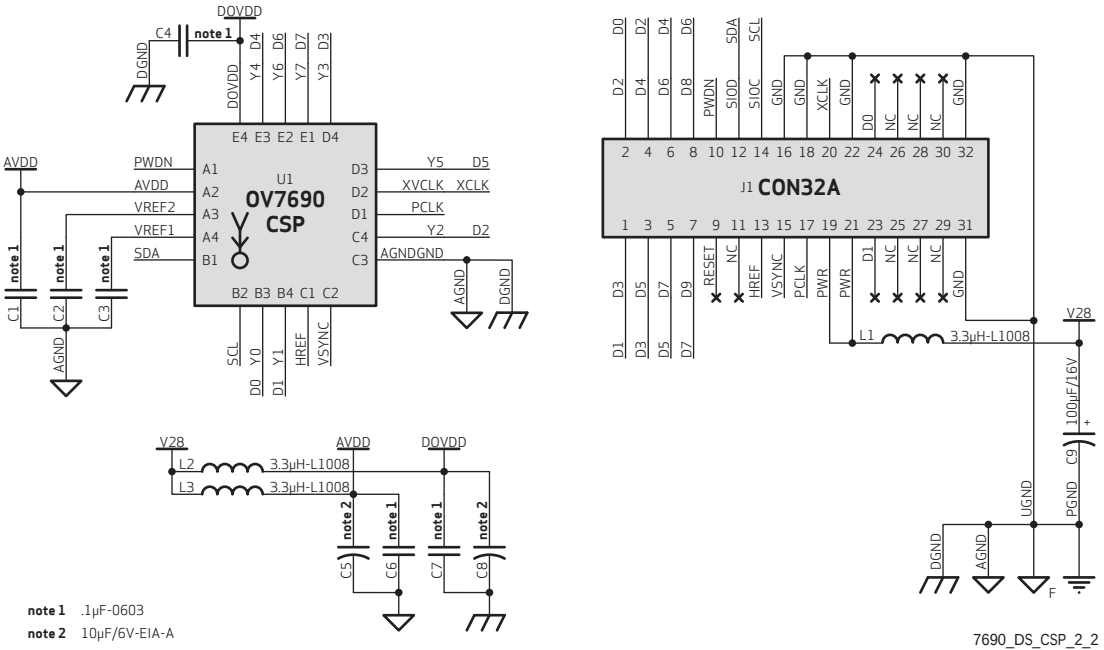



figure 2-2 reference design schematic



## 2.3 I/O control

The OV7690/OV7191 I/O pad direction and driving capability can be easily adjusted. **table 2-1** lists the driving capability and direction control registers of the I/O pins.

**table 2-1** driving capability and direction control for I/O pads

| function | register | description |
|---|---|---|
| output drive capability control | 0x0E | Bit[1:0]: digital video port output drive capability<br>00: 1x<br>01: 2x<br>10: 3x<br>11: 4x |

## 2.4 format and frame rate

**table 2-2** format and frame rate

| format | resolution | frame rate | scaling method | pixel clock (YUV/RAW) |
|---|---|---|---|---|
| VGA | 640x480 | 30 fps | full | 24/12 MHz |
| CIF | 352x288 | 30 fps | scaling down from VGA | 24/12 MHz |
| QVGA | 320x240 | 60 fps | sub sampling from VGA | 24/12 MHz |
| QCIF | 176x144 | 60 fps | scaling down from QVGA | 24/12 MHz |
| any size | | 30 fps | windowing | 24/12 MHz |

## 2.5 SCCB interface

The Serial Camera Control Bus (SCCB) interface controls the image sensor operation. Refer to the OmniVision Technologies Serial Camera Control Bus (SCCB) Specification for detailed usage of the serial control port.

The OV7690 SCCB supported clock rate is dependent on the input clock (XVCLK). **table 2-3** details the supported speeds.

**table 2-3** SCCB support speeds

| input clock (XVCLK) | SCCB clock |
|---|---|
| 15 ≤ XVCLK ≤ 27 Mhz | 400 Kbps |
| 10 ≤ XVCLK < 15 Mhz | 300 Kbps |
| 6 ≤ XVCLK < 10 Mhz | 150 Kbps |

## 2.6 power up sequence

Powering up the OV7690/OV7191 sensor does not require a special power supply sequence. The sensor includes an on-chip initial power-up reset feature. It will reset the whole chip during power up.

## 2.7 standby and sleep

Two suspend modes are available for the OV7690/OV7191:

- hardware standby
- SCCB software sleep

To initiate hardware standby mode, the PWDN pin must be tied to high. When this occurs, the OV7690/OV7191 internal device clock is halted and all internal counters are reset and registers are maintained.

Executing a software power-down through the SCCB interface suspends internal circuit activity but does not halt the device clock. All register content is maintained in standby mode.

## 2.8 DOVDD power requirements

The OV7690 requires two power supplies, AVDD and DOVDD. For different DOVDDs, register 0x49[3:0] must be set to the settings in **table 2-4**.

**table 2-4** DOVDD power requirements

| DOVDD | 0x49[3:0] |
|---|---|
| 1.7 ~ 2.0V | 4'hC |
| 2.1 ~ 2.5V | 4'h4 |
| 2.6 ~ 3.0V | 4'hD |

# 3 block level description

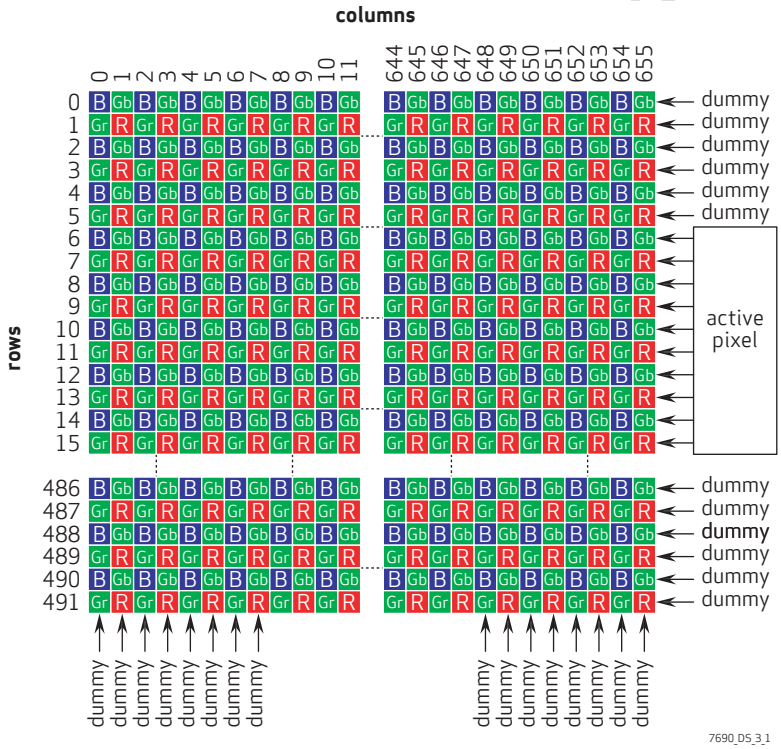
## 3.1 pixel array structure

The OV7690/OV7191 sensor has an image array of 656 columns by 492 rows (322,752 pixels). **figure 3-1** shows a cross-section of the image sensor array.

The color filters are arranged in a Bayer pattern. The primary color BG/GR array is arranged in line-alternating fashion. Of the 322,572 pixels, 307,200 (640x480) are active pixels and can be output. The other pixels are used for black level calibration and interpolation.

The sensor array design is based on a field integration read-out system with line-by-line transfer and an electronic shutter with a synchronous pixel read-out scheme.

**figure 3-1** sensor array region color filter layout



# 4 image sensor core digital functions

## 4.1 mirror and flip

The OV7690/OV7191 provides Mirror and Flip read-out modes, which respectively reverse the sensor data read-out order horizontally and vertically (see **figure 4-1**).

**figure 4-1** mirror and flip samples

original image | mirrored image | flipped image | mirrored and flipped image

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**table 4-1** mirror and flip function control

| function | register | description |
|---|---|---|
| mirror | 0x0C | Bit[6]: mirror ON/OFF select<br>0: mirror OFF<br>1: mirror ON |
| flip | 0x0C | Bit[7]: flip ON/OFF select (see **table 4-2**)<br>0: flip OFF<br>1: flip ON |

**table 4-2** flip ON and flip OFF control settings

| function | subsampling OFF<br>0x12[6] = 0 | subsampling ON<br>0x12[6] = 1 |
|---|---|---|
| flip ON | 0x22[5:4] = 2'b00 | 0x22[5:4] = 2'b10 |
| flip OFF | 0x22[5:4] = 2'b00 | 0x22[5:4] = 2'b01 |

## 4.2 image windowing

An image windowing area is defined by four parameters, HS (horizontal start), HW (horizontal width), VS (vertical start), and VH (vertical height). By properly setting the parameters, any portion within the sense array size can be windowed as a visible area. This windowing is achieved by simply masking the pixels outside the windowing window; thus, it will not affect original timings. It will also not conflict with the flip and mirror functions.

figure 4-2 image windowing

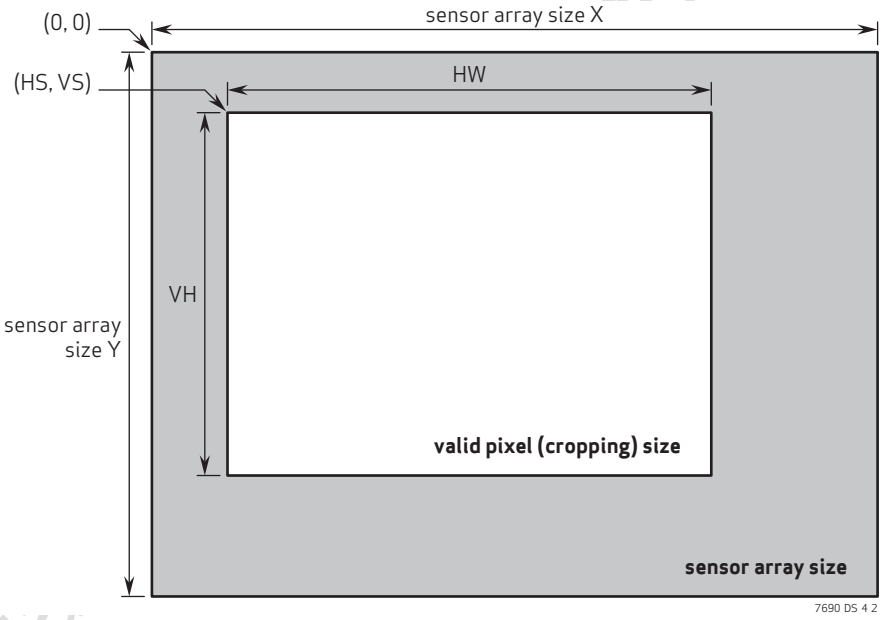


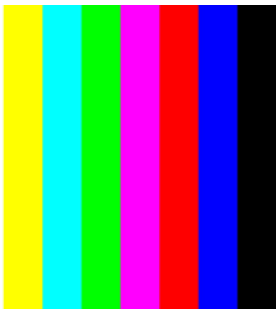

table 4-3 image windowing control functions

| function | register | description |
|---|---|---|
| horizontal start | 0x17 | |
| vertical start | 0x19 | |
| horizontal width | {0x18[7:0], 0x16[6]} | |
| vertical height | 0x1A | |

## 4.3 test pattern

For testing purposes, the OV7690/OV7191 offers one type of test pattern, color bar.

figure 4-3 test pattern



color bar

table 4-4 test pattern selection control

| function | register | description |
|---|---|---|
| color bar | 0x0C | Bit[0]: color bar enable<br>0: color bar OFF<br>1: color bar enable |

## 4.4 AEC/AGC algorithms

### 4.4.1 overview

The Auto Exposure Control (AEC) and Auto Gain Control (AGC) allows the image sensor to adjust the image brightness to a desired range by setting the proper exposure time and gain applied to the image. Besides automatic control, exposure time and gain can be set manually from external control.

## 4.5 black level calibration

The pixel array contains several optically shielded (black) lines. These lines are used to provide the data for black level calibration.

## 4.6 digital gain

After black level subtraction, multiplication may apply to all pixel values based on an optional digital gain. By default, the sensor will use analog gain up to its maximum before applying digital gain to the pixels.

# 5 image sensor processor digital functions

## 5.1 ISP_TOP

The ISP_TOP includes all module enable signals, buffer power down control, top level control signals as well as ISP modules that require control bytes (WBC, UV_AVG, and YUV444to422).

- WBC: White Black pixel Canceling is used to detect and remove defect pixels.
- VarioPixel: This module is used to do pixel 2:1 sub sample in horizontal view. There are various ways to use VarioPixel function such as give out the average of 2 pixels, give out the first pixel and drop the second, or give out the second and drop the first.
- UV_AVG: The U and V average module is used to smooth chrominance to let color image looks better around edge.
- YUV444to422: This module is used to convert YUV444 to YUV422. This module has two options: average mode and drop mode.

## 5.2 ISP DCW, border cutting

This part includes the size registers for ISP input windowing, ISP output windowing, and Scaling input windowing. The ISP input windowing is designed to support digital zoom. The ISP output windowing and Scaling input windowing are both for cutting some border pixels or border lines which are not good enough due to algorithm limitation.

## 5.3 auto white balance (AWB)

The main purpose of the Auto White Balance (AWB) function is to automatically correct the white balance of the image. There are two main functions AWB: AWB_Stat and AWB_Gain.

- AWB_Stat is used to automatically generate digital gains for different light sources
- AWB_Gain is used to apply the AWB_Stat gains on RAW data to remove unrealistic color

## 5.4 gamma

The main purpose of the Gamma (GMA) function is to compensate for the non-linear characteristics of the sensor. GMA converts the pixel values according to the Gamma curve to compensate the sensor output under different light strengths. The non-linear gamma curve is approximately constructed with different linear functions.

## 5.5 lens correction (LENC)

The main purpose of the Lens Correction (LENC) function is to compensate for lens imperfection. According to the radius of each pixel to the lens, the module calculates a gain for the pixel, correcting each pixel with its gain calculated to compensate for the light distribution due to lens curvature.

## 5.6 black level correction (BLC)

Black Level Correction (BLC) is used to adjust black level situations.

## 5.7 color interpolation (CIP), DNS and sharpen

The color interpolation (CIP) functions include de-noising of raw images, RAW to RGB interpolation, and edge enhancement. CIP functions work in both manual and auto modes.

## 5.8 color matrix (CMX)

The main purpose of the Color Matrix (CMX) function is to convert images from the RGB domain to YUV domain. For different color temperatures, the parameters in the transmitting function will be changed.

## 5.9 UV adjust (UV_ADJ)

UV adjust (UV_ADJ) is used to reduce chrominance values in low light conditions to improve image quality. The higher AGC gain is, the lower the chrominance values. UV_ADJ has an automatic and manual mode.

## 5.10 special digital effect (SDE)

The Special Digital Effects (SDE) functions include hue/saturation control, brightness, contrast, etc. Use SDE_CTRL to add some special effects to the image. Calculate the new U and V from Hue Cos, Hue Sin, and parameter signs. Saturate U and V using the Sat_u and Sat_v registers. Calculate Y using Y offset, Y gain, and Ybright or set the Y value. SDE supports negative, black/white, sepia, greenish, blueish, reddish and other image effects which combine the effects already listed.

## 5.11 ISP system control

System control registers include clock and gated controls. Individual modules are clock gated by setting registers 0x80 and 0x81.

## 5.12 format description

Format control converts internal data format into the desirable output format including YUV, RGB and raw.

**table 5-1** format control register list

| register address | register name | function |
|---|---|---|
| 12 | REG12 | Bit[7]: System register reset<br>0: No change<br>1: Resets system<br>Bit[6]: Subsampled (skip) mode enable<br>0: Subsample disabled<br>1: Subsample enable<br>Bit[5]: ITU656 protocol on/off selection<br>Bit[4]: Reserved<br>Bit[3:2]: RGB output format control<br>00: Reserved<br>01: RGB565<br>10: Reserved<br>11: Reserved<br>Bit[1:0]: Output format control<br>00: YUV<br>01: Bayer RAW<br>10: RGB<br>11: Bayer RAW |
| 82 | REG82 | Bit[7:5]: Reserved<br>Bit[4]: RBLUE_P<br>0: Internal Rblue is the same as ISP port<br>1: Inverse Rblue inside ISP<br>Bit[3]: BAR_EN<br>Bit[2]: BAR_OPT_EN<br>0: Color bar data is from vertical counter<br>1: Color bar data is constant<br>Bit[1:0]: OUT_SEL<br>00: Raw from WBC<br>01: Raw from CIP<br>10: YUV422<br>11: YUV422 |

# 6 image sensor output interface digital functions

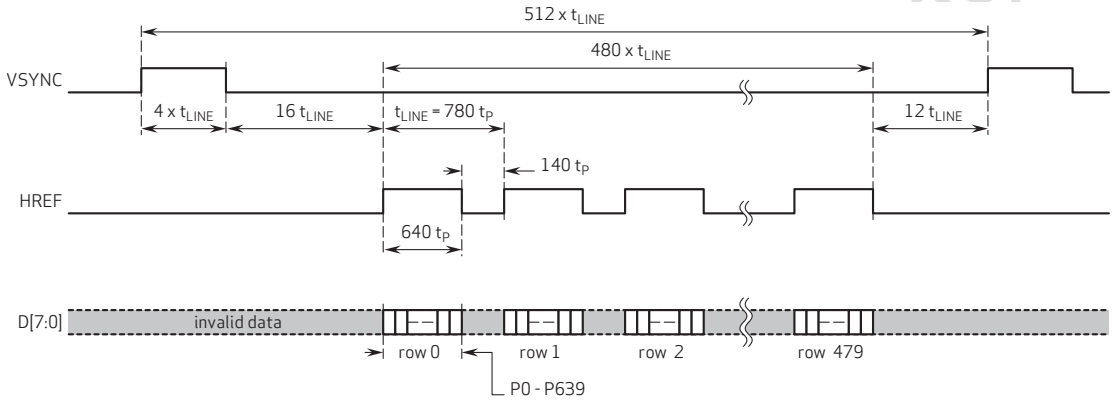
## 6.1 digital video port (DVP)

### 6.1.1 overview

The Digital Video Port (DVP) provides 10-bit parallel data output in all formats supported, and extended features including HSYNC mode and test pattern output.

### 6.1.2 VGA timing

figure 6-1 VGA timing diagram

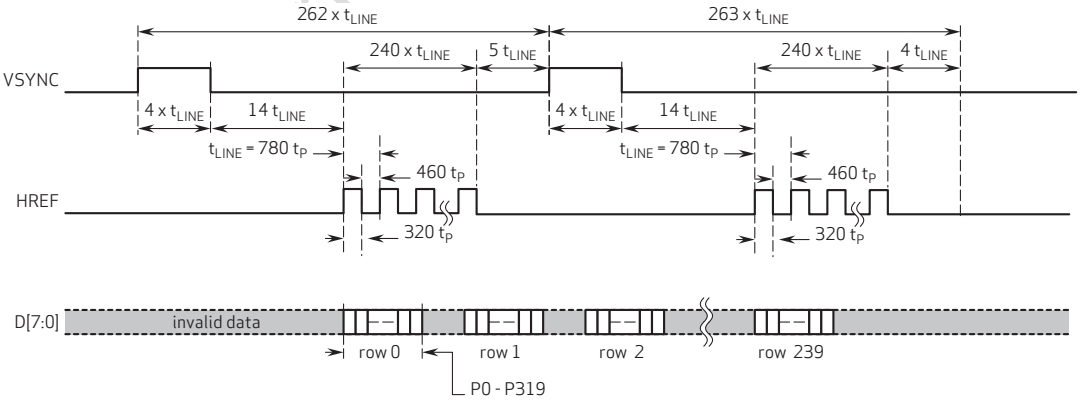



**note 1** for raw data, $t_P = t_{PCLK}$

**note 2** for YUV/RGB, $t_P = 2 \times t_{PCLK}$

7690_DS_6_1

figure 6-2 QVGA timing diagram




**note 1** for YUV/RGB, $t_P = 2 \times t_{PCLK}$ (only to be used with YUV/RGB)

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# 7 register tables

The following tables provide descriptions of the device control registers contained in the OV7690/OV7191. For all register enable/disable bits, enable = 1 and DISABLE = 0. The device slave addresses are 0x42 for write and 0x43 for read.

**table 7-1** system control registers (sheet 1 of 16)

| address | register name | default value | R/W | description |
|---|---|---|---|---|
| 0x00 | GAIN | 0x00 | RW | AGC Gain Control 10 bits (**REG15**[1:0] as MSB 2 bits) **REG15**[1:0]: digital gain<br>Bit[7:0]: Analog gain<br>Range: 1x to 128x Gain = (Bit[9]+1) × (Bit[8]+1) × (Bit[7]+1) × (Bit[6]+1) × (Bit[5]+1) × (Bit[4]+1) × (1+Bit[3:0]/16) |
| 0x01 | BGAIN | 0x40 | RW | AWB Blue Gain Control<br>Range: 0 to 4x([00] to [FF]) |
| 0x02 | RGAIN | 0x40 | RW | AWB Red Gain Control<br>Range: 0 to 4x([00] to [FF]) |
| 0x03 | GGAIN | 0x40 | RW | AWB Green Gain Control<br>Range: 0 to 4x([00] to [FF]) |
| 0x04 | YAVG | 0x00 | R | Frame Average Level<br>Automatically updated based on chip output format |
| 0x05 | BAVG | 0x00 | R | B Pixel Average (ISP)<br>Automatically updated based on chip output format |
| 0x06 | RAVG | 0x00 | R | R Pixel Average (ISP)<br>Automatically updated based on chip output format |
| 0x07 | GAVG | 0x00 | R | G Pixel Average (ISP)<br>Automatically updated based on chip output format |
| 0x08~ 0x09 | RSVD | – | – | Reserved |
| 0x0A | PIDH | 0x76 | R | Product ID Number MSB (Read only) |
| 0x0B | PIDL | 0x90 | R | Product ID Number LSB (Read only) |

table 7-1 system control registers (sheet 2 of 16)

| address | register name | default value | R/W | description |
|---|---|---|---|---|
| 0x0C | REG0C | 0x00 | RW | Bit[7]: Vertical flip<br>Bit[6]: Horizontal mirror<br>Bit[5]: BR swap when in RGB format<br>Bit[4]: YU/YV swap when in YUV format<br>Bit[3]: Reverse order of data bus<br>Bit[2]: Clock output pin status<br>0: Data pin (D[7:0]) tri-state<br>1: Data pin (D[7:0]) output state<br>Bit[1]: Data output pin status selection<br>0: VSYNC, HREF, and PCLK tri-state<br>1: VSYNC, HREF, and PCLK output state<br>Bit[0]: Enable color bar (overlay) |
| 0x0D | REG0D | 0x44 | RW | Bit[7]: Reserved<br>Bit[6:4]: VS start point<br>Bit[3]: Reserved<br>Bit[2:0]: VS width |
| 0x0E | REG0E | 0x00 | RW | Bit[7:4]: Reserved<br>Bit[3]: Sleep mode enable<br>0: Normal mode<br>1: Sleep mode<br>Bit[2]: Output data range selection<br>0: Full range<br>1: Data from [10] to [F0] (8 MSBs)<br>Bit[1:0]: Output drive current select<br>00: 1x<br>01: 2x<br>10: 3x<br>11: 4x |
| 0x0F | AECH | 0x00 | RW | Automatic Exposure Control MSBs (see register **AECL** (0x10) for LSBs) |
| 0x10 | AECL | 0x00 | RW | Automatic Exposure Control LSBs (see register **AECH** (0x0F) for MSBs)<br>AEC[15:0]: Exposure time<br>TEX = $t_{LINE}$ × AEC[15:0]<br>Note: The maximum exposure time is 1 frame period even if TEX is longer than 1 frame period. |

table 7-1 system control registers (sheet 3 of 16)

| address | register name | default value | R/W | description |
|---|---|---|---|---|
| 0x11 | CLKRC | 0x00 | RW | Bit[7]: Reserved<br>Bit[6]: Use external clock directly (no clock pre-scale available)<br>Bit[5:0]: Internal clock pre-scalar<br>F(internal clock) = F(input clock)/(Bit[5:0]+1)<br>Range: [0 0000] to [1 1111] |
| 0x12 | REG12 | 0x11 | RW | Bit[7]: System register reset<br>0: No change<br>1: Resets system<br>Bit[6]: Subsampled (skip) mode enable<br>0: Subsample disabled<br>1: Subsample enable<br>Bit[5]: ITU656 protocol on/off selection<br>Bit[4]: selection sensor original raw data output<br>Bit[3:2]: RGB output format control<br>00: Reserved<br>01: RGB565<br>1x: Not valid<br>Bit[1:0]: Output format control<br>00: YUV<br>01: Bayer RAW<br>10: RGB<br>11: Bayer RAW |
| 0x13 | REG13 | 0xE5 | RW | Bit[7]: Enable fast AGC/AEC algorithm<br>Bit[6]: AEC - step size limit<br>0: Step size limited to vertical blank<br>1: Unlimited step size (current AEC value)<br>Bit[5]: Banding filter ON/OFF<br>Bit[4]: Enable AEC below banding value<br>Bit[3]: Sub-line level exposure ON/OFF selection<br>Bit[2]: AGC auto/manual control selection<br>Bit[1]: AWB auto/manual control selection<br>Bit[0]: Exposure auto/manual control selection |

table 7-1 system control registers (sheet 4 of 16)

| address | register name | default value | R/W | description |
|---|---|---|---|---|
| 0x14 | REG14 | 0x30 | RW | Bit[7]: Reserved<br>Bit[6:4]: Automatic gain ceiling<br>Maximum AGC value<br>000: 2x<br>001: 4x<br>010: 8x<br>011: 16x<br>100: 32x<br>101: 64x<br>110: 128x<br>Bit[3]: Reserved<br>Bit[2]: Drop VSYNC output of corrupt frame<br>Bit[1]: Reserved<br>Bit[0]: Manually set banding<br>0: 60 Hz<br>1: 50 Hz |
| 0x15 | REG15 | 0x00 | RW | Bit[7]: Auto frame rate control on/off selection<br>Bit[6:4]: Auto frame rate max rate control<br>000: No reduction of frame rate<br>001: Max reduction to 1/2 frame rate<br>010: Max reduction to 1/3 frame rate<br>011: Max reduction to 1/4 frame rate<br>100: Max reduction to 1/8 frame rate<br>Bit[3:2]: Auto frame rate active point control<br>00: Add frame when AGC reaches 1 × (1 + 15/16) gain<br>01: Add frame when AGC reaches 2 × (1 + 15/16) gain<br>10: Add frame when AGC reaches 4 × (1 + 15/16) gain<br>11: Add frame when AGC reaches 8 × (1 + 15/16) gain<br>Bit[1:0]: Digital gain<br>00: No digital gain<br>01: 2x<br>11: 4x |

table 7-1 system control registers (sheet 5 of 16)

| address | register name | default value | R/W | description |
|---|---|---|---|---|
| 0x16 | REG16 | 0x08 | RW | Bit[7]: Reserved<br>Bit[6]: Horizontal sensor size[0] (see register **HSize**[7:0] (0x18) for MSBs)<br>Bit[5]: Roff1<br>Vertical window start line adjustment<br>Bit[4]: Hoff1<br>Horizontal window start line adjustment<br>Bit[3:0]: Reserved |
| 0x17 | HSTART | 0x69 | RW | Horizontal Window Start Point Control |
| 0x18 | HSize | 0xA0 | RW | Horizontal Sensor Size[8:1] (see **REG16**[0] (0x16) for LSB)<br>Actual horizontal size = 2 × {**HSize**[7:0], **REG16**[6]} |
| 0x19 | VSTART | 0x0E | RW | Vertical Window Start Line Control |
| 0x1A | VSize | 0xF0 | RW | Vertical Sensor Size 8 bits<br>Actual vertical size = 2 × **VSize**[7:0] |
| 0x1B | SHFT | 0x17 | RW | Pixel Shift |
| 0x1C | MIDH | 0x7F | R | Manufacturer ID Byte – High |
| 0x1D | MIDL | 0xA2 | R | Manufacturer ID Byte – Low |
| 0x1E~ 0x1F | RSVD | – | – | Reserved |
| 0x20 | REG20 | 0x00 | RW | Bit[7]: MSB of banding filter maximum step for 50 Hz light source (4 LSBs are in **AECGM**[7:4] (0x21))<br>Bit[6]: MSB of banding filter maximum step for 60 Hz light source (4 LSBs are in **AECGM**[3:0] (0x21))<br>Bit[5:0]: Manual banding counter |
| 0x21 | AECGM | 0x44 | RW | Bit[7:4]: Banding filter maximum step for 50 Hz light source (see register **REG20**[7] (0x20) for MSB)<br>Bit[3:0]: Banding filter maximum step for 60 Hz light source (see register **REG20**[6] (0x20) for MSB) |

table 7-1 system control registers (sheet 6 of 16)

| address | register name | default value | R/W | description |
|---|---|---|---|---|
| 0x22 | REG22 | 0x00 | RW | Bit[7]: Optical black output selection<br>0: Disable<br>1: Enable<br>Bit[6:0]: Reserved |
| 0x23 | RSVD | – | – | Reserved |
| 0x24 | WPT | 0x78 | RW | AGC/AEC - Stable Operating Region (Upper Limit) |
| 0x25 | BPT | 0x68 | RW | AGC/AEC - Stable Operating Region (Lower Limit) |
| 0x26 | VPT | 0xD4 | RW | AGC/AEC Fast Mode Operating Region<br>Bit[7:4]: High nibble of upper limit of fast mode control zone<br>Bit[3:0]: High nibble of lower limit of fast mode control zone |
| 0x27 | REG27 | 0x00 | RW | Bit[7]: Dark sun enable (digital part)<br>Bit[6:4]: Vertical window position adjustment (when center average is used)<br>Bit[3]: Reserved<br>Bit[2:0]: Horizontal window position adjustment (when center average is used) |
| 0x28 | REG28 | 0x00 | RW | Bit[7]: Output negative data<br>Bit[6]: HREF changes to HSYNC<br>Bit[5]: HSYNC reverse<br>Bit[4]: HREF reverse<br>Bit[3]: Reserved<br>Bit[2]: VSYNC option<br>0: VSYNC active on falling edge of PCLK<br>1: VSYNC active on rising edge of PCLK<br>Bit[1]: VSYNC negative<br>Bit[0]: Reserved |

table 7-1 system control registers (sheet 7 of 16)

| address | register name | default value | R/W | description |
|---|---|---|---|---|
| 0x29 | PLL | 0xA2 | RW | Bit[7:6]: PLL divider<br>00: /1<br>01: /2<br>10: /3<br>11: /4<br>Bit[5:4]: PLL output control<br>00: Bypass PLL<br>01: 4x<br>10: 6x<br>11: 8x<br>Bit[3]: Reset PLL<br>Bit[2:1]: Y_AVERAGE selection options<br>00: Use ISP output as data source<br>01: Use sensor output as data source<br>Bit[0]: Reserved |
| 0x2A | EXHCL | 0x30 | RW | Bit[7]: Contrast center auto adjustment<br>0: Manual mode by setting **REGD5**[7:0]<br>1: Auto mode<br>Bit[6:4]: Dummy pixel insert in horizontal direction 3 MSBs (see register **EXHCH** (0x2B) for LSBs)<br>Bit[3:0]: Dummy line 4 MSBs (see register **DM_LN** (0x2C) for LSBs) |
| 0x2B | EXHCH | 0x0B | RW | Dummy Pixel Insert in Horizontal Direction 8 LSBs (see register **EXHCL**[6:4] (0x2A) for MSBs) |
| 0x2C | DM_LN | 0x00 | RW | Dummy Line 8 LSBs (see register **EXHCL**[3:0] (0x2A) for MSBs) |
| 0x2D | ADVFL | 0x00 | RW | Dummy Line Insert in Vertical direction LSBs (1 bit equals 1 line)<br>(see register **ADVFH** (0x2E) for MSBs) |
| 0x2E | ADVFH | 0x00 | RW | Dummy Line Insert in Vertical Direction MSBs (1 bit equals 1 line)<br>(see register **ADVFL** (0x2D) for LSBs) |
| 0x2F~ 0x37 | RSVD | – | – | Reserved |

table 7-1 system control registers (sheet 8 of 16)

| address | register name | default value | R/W | description |
|---|---|---|---|---|
| 0x38 | 4MSBs(Strobe)<br>4LSBs(ADC) | 0x10 | RW | Bit[7]: Reserved<br>Bit[6:4]: Stream off control<br>VSYNC Y HREF PCLK<br>0xx: f f f f<br>100: k k k f<br>101: k k k k<br>11x: hz hz hz hz<br>Note: f stand for free running<br>hz stand for high impedance<br>Bit[3:0]: Reserved |
| 0x39~<br>0x3D | RSVD | – | – | Reserved |
| 0x3E | REG3E | 0x20 | RW | Bit[7]: Reserved<br>Bit[6]: PCLK output gated<br>0: PCLK always output<br>1: PCLK output qualified by HREF<br>Bit[5]: Reserved<br>Bit[4]: PCLK output selection<br>0: For RAW format<br>1: For YUV format, PCLK will be double than PCLK in RAW format<br>Bit[3:0]: Reserved |
| 0x3F | REG3F | 0x44 | RW | Bit[7]: Reserved<br>Bit[6]: Reverse PCLK<br>0: HREF goes high at PCLK rising edge<br>1: HREF goes high at PCLK falling edge<br>Bit[5:0]: Reserved |
| 0x40~<br>0x47 | RSVD | – | – | Reserved |
| 0x48 | ANA1 | 0x40 | RW | Bit[7:0]: Reserved |
| 0x49~<br>0x4F | RSVD | – | – | Reserved |
| 0x50 | BD50st | 0x9A | RW | 50 Hz Banding AEC 8 Bits |
| 0x51 | BD60ST | 0x80 | RW | 60 Hz Banding AEC 8 Bits |
| 0x52~<br>0x59 | RSVD | – | – | Reserved |
| 0x5A | UV_CTR0 | 0x01 | RW | Slope of UV Curve |

table 7-1 system control registers (sheet 9 of 16)

| address | register name | default value | R/W | description |
|---|---|---|---|---|
| 0x5B | UV_CTR1 | 0xFF | RW | Bit[7:6]: UV adjustment gain high threshold control 2 LSBs (see register **UV_CTR2**[7:5] (0x5C) for 3 MSBs)<br>Bit[5:0]: Y intercept point of UV curve |
| 0x5C | UV_CTR2 | 0x1F | RW | Bit[7:5]: UV adjustment gain high threshold control 3 MSBs (see register **UV_CTR1**[7:6] (0x5B) for 2 LSBs)<br>Bit[4:0]: Manual UV adjustment |
| 0x5D | UV_CTR3 | 0x00 | RW | Bit[7:4]: UV adjustment gain low threshold control<br>Bit[3:2]: Reserved<br>Bit[1]: Center average selection<br>0: Choose whole image average value to system<br>1: Choose center 1/4 average value to system<br>Bit[0]: Reserved |
| 0x5E~ 0x61 | RSVD | – | – | Reserved |
| 0x62 | REG62 | 00 | RW | Bit[7] Reserved<br>Bit[6] Bit shift test pattern output enable<br>0: Disable<br>1: Enable<br>Bit[5:4]: Bit shift test pattern mode options<br>00: Not valid<br>01: Not valid<br>10: Test pattern mode 1<br>11: Test pattern mode 2<br>Bit[3:0]: Reserved |
| 0x63~ 0x67 | RSVD | – | – | Reserved |
| 0x68 | BLC8 | 0x80 | RW | Bit[7:4]: Reserved<br>Bit[3:0]: BLC target offset |
| 0x69~ 0x6A | RSVD | – | – | Reserved |
| 0x6B | BLCOUT | 0x00 | R | Read-out BLC Values |
| 0x6C~ 0x6E | RSVD | – | – | Reserved |

table 7-1 system control registers (sheet 10 of 16)

| address | register name | default value | R/W | description |
|---|---|---|---|---|
| 0x6F | REG6F | 0x43f | RW | Bit[7]: Reset enable/disable when sensor working mode changes<br>0: Sensor not reset timing when mode changes<br>1: Sensor timing will reset when mode changes<br>Bit[6:0]: Reserved |
| 0x70~ 0x7F | RSVD | – | – | Reserved |
| 0x80 | REG80 | 0x7E | RW | Bit[7]: VarioPixel enable<br>0: Disable<br>1: Enable<br>Bit[6]: Color interpolation enable<br>0: Disable<br>1: Enable<br>Bit[5]: Black pixel correction enable<br>0: Disable<br>1: Enable<br>Bit[4]: White pixel correction enable<br>0: Disable<br>1: Enable<br>Bit[3]: Gamma enable<br>0: Disable<br>1: Enable<br>Bit[2]: AWB gain enable<br>0: Disable<br>1: Enable<br>Bit[1]: AWB enable<br>0: Disable<br>1: Enable<br>Bit[0]: Lens correction enable<br>0: Disable<br>1: Enable |

table 7-1 system control registers (sheet 11 of 16)

| address | register name | default value | R/W | description |
|---|---|---|---|---|
| 0x81 | REG81 | 0x41 | RW | Bit[7:6]: Reserved<br>Bit[5]: Special Digital Effects (SDE) enable<br>0: Disable<br>1: Enable<br>Bit[4]: UV adjust enable<br>0: Disable<br>1: Enable<br>Bit[3]: Vertical scaling enable<br>0: Disable<br>1: Enable<br>Bit[2]: Horizontal scaling enable<br>0: Disable<br>1: Enable<br>Bit[1]: UV average enable<br>0: Disable<br>1: Enable<br>Bit[0]: Color matrix enable<br>0: Disable<br>1: Enable |
| 0x82 | REG82 | 0x00 | RW | Bit[7:5]: Reserved<br>Bit[4]: RBLUE_P<br>0: Internal rblue is the same as ISP port<br>1: Inverse rblue inside ISP<br>Bit[3]: ISP color bar<br>Bit[2]: Color bar options enable<br>0: Color bar data is from vertical counter<br>1: Color bar data is constant<br>Bit[1:0]: Output options<br>00: Raw from WBC<br>01: Raw from CIP<br>10: YUV422<br>11: YUV422 |
| 0x83~ 0x84 | RSVD | – | – | Reserved |
| 0x85 | LCC0 | 0x00 | RW | Bit[7:5]: Reserved<br>Bit[4]: LENC Bias enable<br>Bit[3]: VSKIP<br>Bit[2]: HSKIP<br>Bit[1:0]: Reserved |
| 0x86 | LCC1 | 0x00 | RW | Bit[7:0]: Radius of the circular section where no compensation applies |
| 0x87 | LCC2 | 0x00 | RW | Bit[7:0]: X coordinate of lens correction center relative to array center |

table 7-1 system control registers (sheet 12 of 16)

| address | register name | default value | R/W | description |
|---|---|---|---|---|
| 0x88 | LCC3 | 0x00 | RW | Bit[7:0]: Y coordinate of lens correction center relative to array center |
| 0x89 | LCC4 | 0x00 | RW | Bit[7:0]: R channel compensation coefficient |
| 0x8A | LCC5 | 0x00 | RW | Bit[7:0]: G channel compensation coefficient |
| 0x8B | LCC6 | 0x00 | RW | Bit[7:0]: B channel compensation coefficient |
| 0x8C~ 0xA2 | AWB CTRL | – | RW | AWB Control Registers |
| 0xA3 | GAM1 | 0x10 | RW | Gamma Curve 1st Segment Input End Point 0x04 Output Value |
| 0xA4 | GAM2 | 0x12 | RW | Gamma Curve 2nd Segment Input End Point 0x08 Output Value |
| 0xA5 | GAM3 | 0x35 | RW | Gamma Curve 3rd Segment Input End Point 0x10 Output Value |
| 0xA6 | GAM4 | 0x5A | RW | Gamma Curve 4th Segment Input End Point 0x20 Output Value |
| 0xA7 | GAM5 | 0x69 | RW | Gamma Curve 5th Segment Input End Point 0x28 Output Value |
| 0xA8 | GAM6 | 0x76 | RW | Gamma Curve 6th Segment Input End Point 0x30 Output Value |
| 0xA9 | GAM7 | 0x80 | RW | Gamma Curve 7th Segment Input End Point 0x38 Output Value |
| 0xAA | GAM8 | 0x88 | RW | Gamma Curve 8th Segment Input End Point 0x40 Output Value |
| 0xAB | GAM9 | 0x8F | RW | Gamma Curve 9th Segment Input End Point 0x48 Output Value |
| 0xAC | GAM10 | 0x96 | RW | Gamma Curve 10th Segment Input End Point 0x50 Output Value |
| 0xAD | GAM11 | 0xA3 | RW | Gamma Curve 11th Segment Input End Point 0x60 Output Value |
| 0xAE | GAM12 | 0xAF | RW | Gamma Curve 12th Segment Input End Point 0x70 Output Value |
| 0xAF | GAM13 | 0xC4 | RW | Gamma Curve 13th Segment Input End Point 0x90 Output Value |
| 0xB0 | GAM14 | 0xD7 | RW | Gamma Curve 14th Segment Input End Point 0xB0 Output Value |

table 7-1 system control registers (sheet 13 of 16)

| address | register name | default value | R/W | description |
|---|---|---|---|---|
| 0xB1 | GAM15 | 0xE8 | RW | Gamma Curve 15th Segment Input End Point 0xD0 Output Value |
| 0xB2 | SLOPE | 0x20 | RW | Gamma Curve Highest Segment Slope – calculated as follows:<br>**SLOPE**[7:0] = (0x100 – **GAM15**[7:0]) × 4/3 |
| 0xB3 | RSVD | – | – | Reserved |
| 0xB4 | REGB4 | 0x06 | RW | Bit[7:6]: Reserved<br>Bit[5]: Sharpening mode<br>0: Manual<br>1: Auto<br>Bit[4]: De-noise mode manual<br>0: Manual<br>1: Auto<br>Bit[3:0]: EDGE_TH |
| 0xB5 | REGB5 | 0x08 | RW | Bit[7:0]: De-noise magnitude (manual mode) |
| 0xB6 | REGB6 | 0x04 | RW | Bit[7:5]: Reserved<br>Bit[4:0]: Sharpening magnitude (manual mode) |
| 0xB7 | REGB7 | 0x10 | RW | Bit[7:0]: OFFSET |
| 0xB8 | REGB8 | 0x1E | RW | Bit[7:5]: Reserved<br>Bit[4:0]: BASE1 |
| 0xB9 | REGB9 | 0x02 | RW | Bit[7:5]: Reserved<br>Bit[4:0]: BASE2 |
| 0xBA | REGBA | 0x09 | RW | Bit[7]: Reserved<br>Bit[6]: GAIN_SEL_EN<br>Bit[5:4]: GAIN_SEL<br>00: GAIN_4X is limited to 8<br>01: GAIN_4X is limited to 16<br>10: GAIN_4X is limited to 32<br>11: GAIN_4X is limited to 64<br>Bit[3:2]: DNS_TH_SEL<br>Bit[1:0]: EDGE_MT_RANGE |
| 0xBB | REGBB | 0x2C | RW | Bit[7:0]: Color matrix coefficient 1 |
| 0xBC | REGBC | 0x24 | RW | Bit[7:0]: Color matrix coefficient 2 |
| 0xBD | REGBD | 0x08 | RW | Bit[7:0]: Color matrix coefficient 3 |
| 0xBE | REGBE | 0x14 | RW | Bit[7:0]: Color matrix coefficient 4 |
| 0xBF | REGBF | 0x24 | RW | Bit[7:0]: Color matrix coefficient 5 |
| 0xC0 | REGC0 | 0x38 | RW | Bit[7:0]: Color matrix coefficient 6 |

table 7-1 system control registers (sheet 14 of 16)

| address | register name | default value | R/W | description |
|---|---|---|---|---|
| 0xC1 | REGC1 | 0x1E | RW | Bit[7]: CMX_BIAS<br>Bit[6]: M_DB<br>Bit[5:0]: M_SIGN |
| 0xC2 | REGC2 | 0x00 | RW | Bit[7:2]: Reserved<br>Bit[1]: VFIRST<br>Bit[0]: UV_CNV_OPT<br>0: Average mode<br>1: Drop mode |
| 0xC3 | REGC3 | 0x80 | RW | Bit[7]: WIN_SEL<br>Bit[6]: SCALE_MAN<br>Bit[5]: H_ROUND<br>Bit[4]: H_DROP<br>Bit[3:2]: V_DIV_MAN<br>Bit[1:0]: H_DIV_MAN |
| 0xC4 | REGC4 | 0x02 | RW | Bit[7:3]: Reserved<br>Bit[2:0]: XSC_MAN[10:8] |
| 0xC5 | REGC5 | 0x00 | RW | Bit[7:0]: XSC_MAN[7:0] |
| 0xC6 | REGC6 | 0x02 | RW | Bit[7:3]: Reserved<br>Bit[2:0]: YSC_MAN[10:8] |
| 0xC7 | REGC7 | 0x00 | RW | Bit[7:0]: YSC_MAN[7:0] |
| 0xC8 | REGC8 | 0x02 | RW | Bit[7:2]: Reserved<br>Bit[1:0]: IH[9:8]<br>2 MSBs of horizontal input size (see register **REGC9**[7:0] (0xC9) for LSBs) |
| 0xC9 | REGC9 | 0x80 | RW | Bit[7:0]: IH[7:0]<br>8 LSBs of horizontal input size (see register **REGC8**[1:0] (0xC8) for MSBs) |
| 0xCA | REGCA | 0x01 | RW | Bit[7:1]: Reserved<br>Bit[0]: IV[8]<br>MSB of vertical input size (see register **REGCB**[7:0] (0xCB) for LSBs) |
| 0xCB | REGCB | 0xE0 | RW | Bit[7:0]: IV[7:0]<br>8 LSBs of vertical input size (see register **REGCA**[0] (0xCA) for MSB) |
| 0xCC | REGCC | 0x02 | RW | Bit[1:0]: OH[9:8]<br>2 MSBs of horizontal output size (see register **REGCD**[7:0] (0xCD) for LSBs) |

table 7-1 system control registers (sheet 15 of 16)

| address | register name | default value | R/W | description |
|---|---|---|---|---|
| 0xCD | REGCD | 0x80 | RW | Bit[7:0]: OH[7:0]<br>8 LSBs of horizontal output size (see register **REGCC**[7:0] (0xCC) for MSBs) |
| 0xCE | REGCE | 0x01 | RW | Bit[7:1]: Reserved<br>Bit[0]: OV[8]<br>MSB of vertical output size (see register **REGCF**[7:0] (0xCF) for LSBs) |
| 0xCF | REGCF | 0xE0 | RW | Bit[7:0]: OV[7:0]<br>8 LSBs of vertical output size (see register **REGCE**[0] (0xCE) for MSB) |
| 0xD0 | REGD0 | 0x48 | RW | Boundary Offset<br>Bit[7:4]: WIN_VOFF<br>Bit[3:0]: WIN_HOFF |
| 0xD1 | RSVD | – | – | Reserved |
| 0xD2 | REGD2 | 0x00 | RW | SDE_CTRL<br>Bit[7]: FIXY_EN<br>Bit[6]: NEG_EN<br>Bit[5]: GRAY_EN<br>Bit[4]: FIXV_EN<br>Bit[3]: FIXU_EN<br>Bit[2]: CONT_EN<br>Bit[1]: SAT_EN<br>Bit[0]: HUE_EN |
| 0xD3 | REGD3 | 0x00 | RW | Bit[7:0]: YBRIGHT |
| 0xD4 | REGD4 | 0x20 | RW | Bit[7:0]: YGAIN |
| 0xD5 | REGD5 | 0x00 | RW | Bit[7:0]: YOFFSET |
| 0xD6 | REGD6 | 0x80 | RW | Bit[7:0]: HUE_COS |
| 0xD7 | REGD7 | 0x00 | RW | Bit[7:0]: HUE_SIN |
| 0xD8 | REGD8 | 0x40 | RW | Bit[7:0]: SAT_U |
| 0xD9 | REGD9 | 0x40 | RW | Bit[7:0]: SAT_V |
| 0xDA | REGDA | 0x80 | RW | Bit[7:0]: UREG |
| 0xDB | REGDB | 0x80 | RW | Bit[7:0]: VREG |

table 7-1 system control registers (sheet 16 of 16)

| address | register name | default value | R/W | description |
|---|---|---|---|---|
| 0xDC | REGDC | 0x01 | RW | Bit[7:6]: Reserved<br>Bit[5:0]: SgnSet<br>Hue: sgn0=1, sgn1=0, sgn4=sgn5=0 => 0<theta< pi/2 sgn0=0, sgn1=1, sgn4=sgn5=0 => -pi/2<theta< 0 sgn0=1, sgn1=0, sgn4=sgn5=1 => pi/2<theta< pi sgn0=0, sgn1=1, sgn4=sgn5=1 => -pi<theta< -pi/2<br>YContrast: sign2: YOffset sign3: YBrightness |
| 0xDD | REGDD | 0x00 | RW | Bit[7:5]: Reserved<br>Bit[4]: FIFO_MAN<br>0: FIFO auto mode enable<br>1: FIFO manual mode enable<br>Bit[3:2]: FIFO_OPT - offset selection<br>00: Offset = 4<br>01: Offset = 8<br>10: Offset = 12<br>11: Offset = 15<br>Bit[1:0]: FIFO_OPT<br>Output speed |
| 0xDE | REGDE | 0x10 | RW | Bit[7:0]: FIFO_delay output delay<br>Only works in manual mode |
| 0xDF | REGDF | 0x11 | RW | Bit[7:0]: VARIO_SEL<br>Bit[7:6]: VarioPixel mode for B<br>Bit[5:4]: VarioPixel mode for Gb<br>Bit[3:2]: VarioPixel mode for Gr<br>Bit[1:0]: VarioPixel mode for R<br>00: Average mode<br>01: Select second pixel<br>1x: Select first pixel |
| 0xE0 | REGE0 | 0x00 | RW | Bit[7:0]: REG_ADDR |
| 0xE1 | REGE1 | – | R | Bit[7:0]: REG_DOUT |

# 8 electrical specifications

**table 8-1** absolute maximum ratings

| parameter | | absolute maximum rating[a] |
|---|---|---|
| operating temperature range[b] | | -30°C to +70°C |
| stable image temperature range[c] | | 0°C to 50°C |
| ambient storage temperature | | -40°C to +125°C |
| supply voltage (with respect to ground) | $V_{DD-A}$ | 4.5V |
| | $V_{DD-IO}$ | 4.5V |
| electro-static discharge (ESD) | human body model | 2000V |
| | machine model | 200V |
| all input/output voltages (with respect to ground) | | -0.3V to $V_{DD-IO}$ + 1V |
| I/O current on any input or output pin | | ± 200 mA |
| peak solder temperature (10 second dwell time) | | 260°C |

a. exceeding the absolute maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

b. sensor functions but image quality may be noticeably different at temperatures outside of stable image range

c. image quality remains stable throughout this temperature range

**table 8-2** DC characteristics (-30°C < $T_A$ < 70°C)

| symbol | parameter | min | typ | max | unit |
|---|---|---|---|---|---|
| **supply** | | | | | |
| $V_{DD-A}$ | supply voltage (analog) | 2.6 | 2.8 | 3.0 | V |
| $V_{DD-IO}$ | supply voltage (digital I/O) | 1.7 | 1.8 | 3.0 | V |
| $I_{DD-A}$ | active (operating) current | | 16[a] | 19[a] | mA |
| $I_{DD-IO}$ | | | 18[a] | 22[a] | mA |
| $I_{DDS-SCCB}$ | standby current | | 1.2[a] | 2.2[a] | mA |
| $I_{DDS-PWDN}$ | | | 20[a] | 25[a] | µA |
| **digital inputs (typical conditions: AVDD = 2.8V, DOVDD = 1.8V)** | | | | | |
| $V_{IL}$ | input voltage LOW | | | 0.54 | V |
| $V_{IH}$ | input voltage HIGH | 1.26 | | | V |
| $C_{IN}$ | input capacitor | | | 10 | pF |
| **digital outputs (standard loading 25 pF)** | | | | | |
| $V_{OH}$ | output voltage HIGH | 1.62 | | | V |
| $V_{OL}$ | output voltage LOW | | | 0.18 | V |
| **serial interface inputs** | | | | | |
| $V_{IL}$[a] | SCL and SDA | -0.5 | 0 | 0.54 | V |
| $V_{IH}$[a] | SCL and SDA | 1.26 | 1.8 | 2.3 | V |

a. based on DOVDD = 1.8V.

**table 8-3** AC characteristics ($T_A$ = 25°C, $V_{DD-A}$ = 2.8V, $V_{DD-IO}$ = 1.8V)

| symbol | parameter | min | typ | max | unit |
|---|---|---|---|---|---|
| ADC parameters | | | | | |
| B | analog bandwidth | | 30 | | MHz |
| DLE | DC differential linearity error | | 0.5 | | LSB |
| ILE | DC integral linearity error | | 1 | | LSB |
| | settling time for software reset | | | <1 | ms |
| | settling time for resolution mode change | | | <1 | ms |
| | settling time for register setting | | | <300 | ms |

**table 8-4** timing characteristics

| symbol | parameter | min | typ | max | unit |
|---|---|---|---|---|---|
| oscillator and clock input | | | | | |
| $f_{OSC}$ | frequency (XVCLK) | 6 | 24 | 27 | MHz |
| $t_r$, $t_f$ | clock input rise/fall time | | | 5 (10[a]) | ns |

a. if using the internal PLL

# 9 mechanical specifications

## 9.1 physical specifications

figure 9-1 package specifications

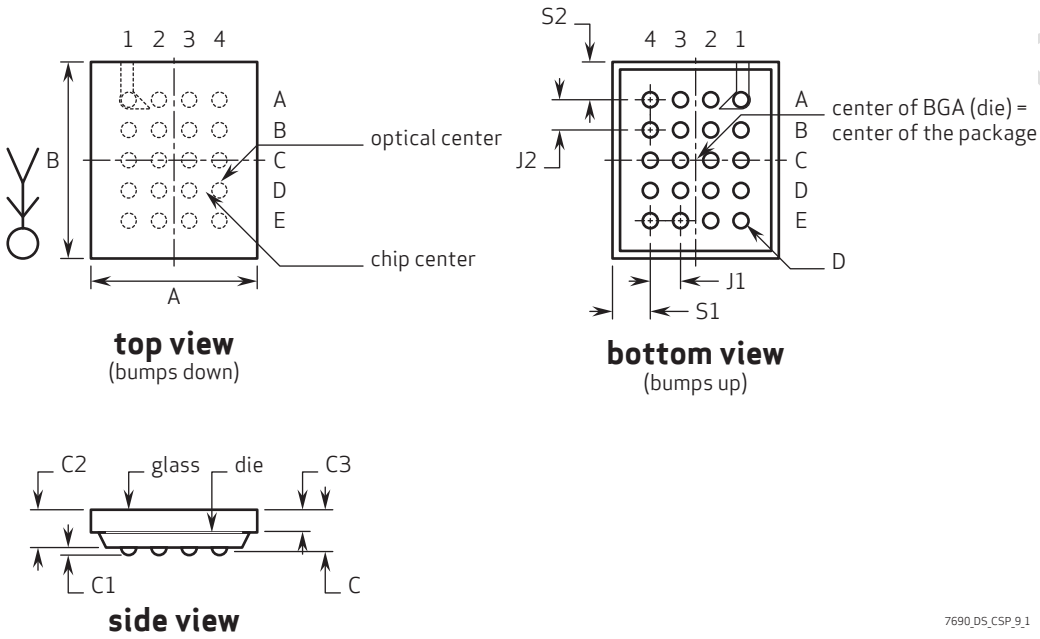



table 9-1 package dimensions (sheet 1 of 2)

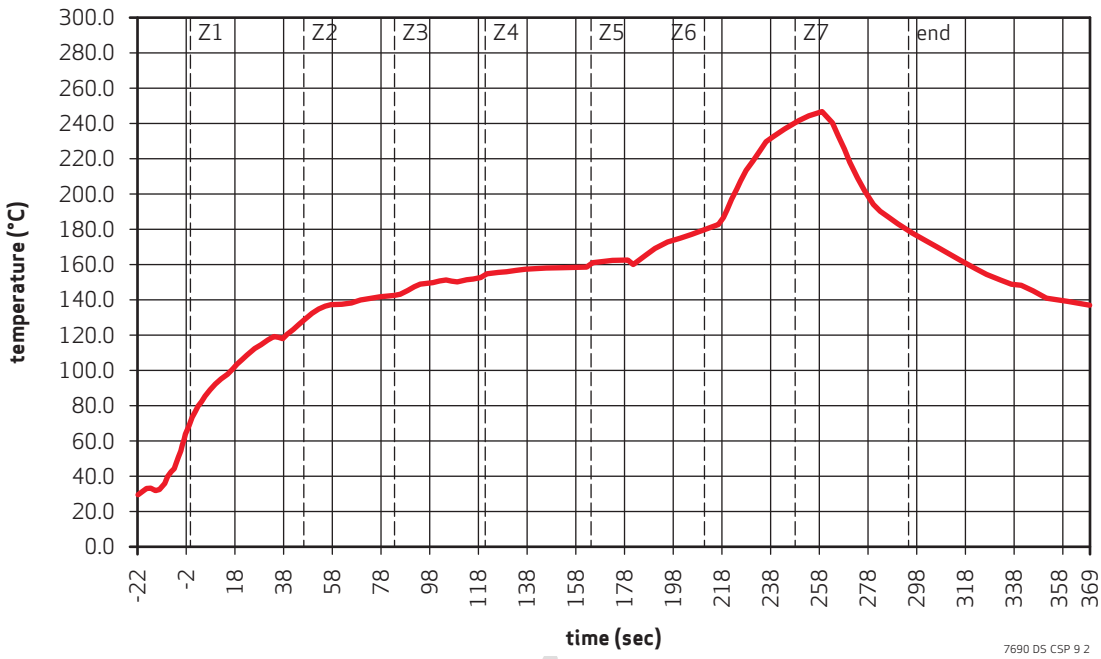
| parameter | symbol | min | typ | max | unit |
|---|---|---|---|---|---|
| package body dimension x | A | 2442 | 2467 | 2492 | µm |
| package body dimension y | B | 2892 | 2917 | 2942 | µm |
| package height | C | 690 | 750 | 810 | µm |
| ball height | C1 | 100 | 130 | 160 | µm |
| package body thickness | C2 | 575 | 620 | 665 | µm |
| thickness of glass surface to wafer | C3 | 425 | 445 | 465 | µm |
| ball diameter | D | 220 | 250 | 280 | µm |
| total pin count | N | | 20 | | |
| pin count x-axis | N1 | | 4 | | |

table 9-1 package dimensions (sheet 2 of 2)

| parameter | symbol | min | typ | max | unit |
|---|---|---|---|---|---|
| pin count y-axis | N2 | | 5 | | |
| pins pitch x-axis | J1 | | 500 | | µm |
| pins pitch y-axis | J2 | | 500 | | µm |
| edge-to-pin center distance analog x | S1 | 454 | 484 | 514 | µm |
| edge-to-pin center distance analog y | S2 | 426 | 456 | 486 | µm |

## 9.2 IR reflow specifications

figure 9-2 IR reflow ramp rate requirements




**note**

The OV7690/OV7191 uses a lead free package.

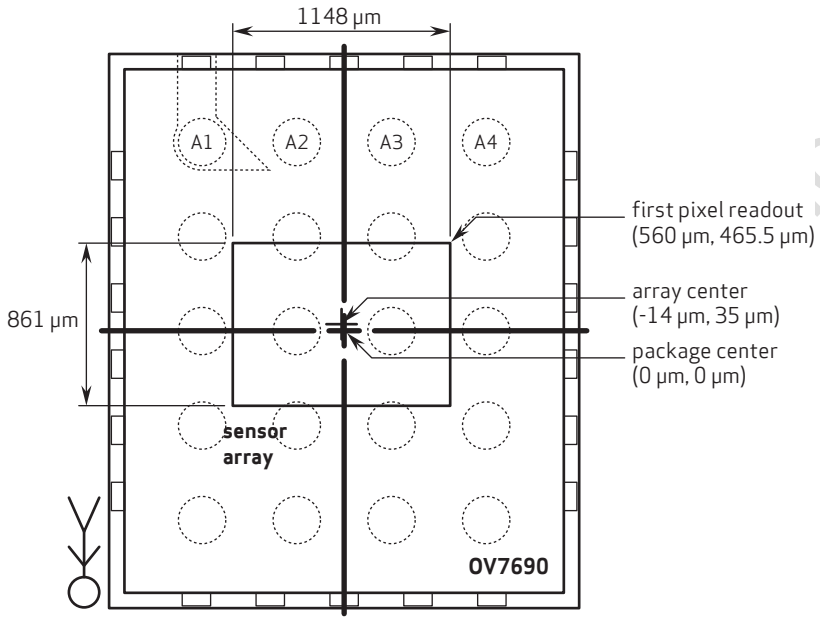
table 9-2 reflow conditions

| condition | exposure |
|---|---|
| average ramp-up rate (30°C to 217°C) | less than 3°C per second |
| > 100°C | between 330 - 600 seconds |
| > 150°C | at least 210 seconds |
| > 217°C | at least 30 seconds (30 ~ 120 seconds) |
| peak temperature | 245°C |
| cool-down rate (peak to 50°C) | less than 6°C per second |
| time from 30°C to 245°C | no greater than 390 seconds |

# 10 optical specifications

## 10.1 sensor array center

figure 10-1 sensor array center




**top view**

**note 1** this drawing is not to scale and is for reference only.

**note 2** as most optical assemblies invert and mirror the image, the chip is typically mounted with pins A1 to A4 oriented down on the PCB.

7690_DS_10_1

## 10.2 lens chief ray angle (CRA)

figure 10-2 chief ray angle (CRA)

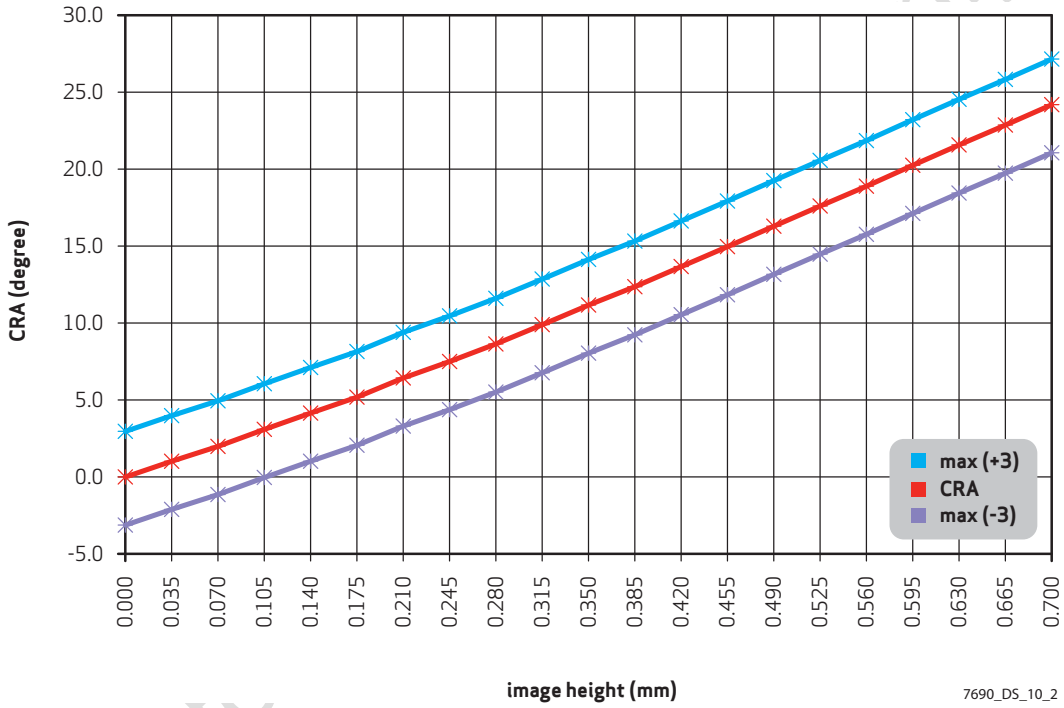



table 10-1 CRA versus image height plot (sheet 1 of 2)

| field (%) | image height (mm) | CRA (degrees) |
|---|---|---|
| 0 | 0 | 0 |
| 0.05 | 0.035 | 1 |
| 0.1 | 0.070 | 2 |
| 0.15 | 0.105 | 3.1 |
| 0.2 | 0.140 | 4.2 |
| 0.25 | 0.175 | 5.2 |
| 0.3 | 0.210 | 6.4 |
| 0.35 | 0.245 | 7.5 |
| 0.4 | 0.280 | 8.7 |
| 0.45 | 0.315 | 9.9 |

table 10-1 CRA versus image height plot (sheet 2 of 2)

| field (%) | image height (mm) | CRA (degrees) |
|---|---|---|
| 0.5 | 0.350 | 11.2 |
| 0.55 | 0.385 | 12.4 |
| 0.6 | 0.420 | 13.7 |
| 0.65 | 0.455 | 15 |
| 0.7 | 0.490 | 16.3 |
| 0.75 | 0.525 | 17.6 |
| 0.8 | 0.560 | 18.9 |
| 0.85 | 0.595 | 20.3 |
| 0.9 | 0.630 | 21.6 |
| 0.95 | 0.665 | 22.9 |
| 1 | 0.700 | 24.2 |

# revision history

**version 1.0** 02.11.2008

- initial release

**version 1.01** 05.05.2008

- in the features section on page iii, updated the ordering information from OV07690-AL9A (color, lead-free) 20-pin CSP2 changed to: OV07690-AL9A (color, lead-free) 20-pin CSP3
- in the features section on page iii, updated the image area from: 1440µm x 1653µm changed to 1148µm x 861µm
- in the features section on page iii, updated the lens chief ray angle from TBD to 25°
- in chapter 6, section 6.1 on page 6-1, removed table 6-1 VGA timing specifications
- in chapter 6 section 6.1 on page 6-1, added figure 6-2 QVGA timing diagram
- in chapter 7, updated the values of the register tables description on page 7-1 from: “The device slave addresses are 0x60 for write and 0x61 for read” to “The device slave addresses are 0x42 for write and 0x43 for read”
- in chapter 7, updated register 0x12 Bit[3:2]: RGB output format control, 00: GBR4:2:2; changes to Bit[3:2]: RGB output format control, 00: Reserved
- in table 9-1 on page 9-1, changed min, typ, and max for cover glass thickness parameter from "425", "445", and "465" to "390", "400", and "410", respectively
- in table 9-1 on page 9-1, changed min, typ, and max for airgap between cover glass and sensor parameter from "40, "45", and "60" to "37", "41", and "45", respectively

**version 2.0** 07.10.2008

- changed document from Preliminary Specification to Product Specification
- added throughout the entire document OV7191 product number
- updated ordering information from OV07690-AL9A changed to OV07690-A20A
- added to the ordering information OV07191-A20A
- under the key specifications on page iii, changed power requirements standby: TBD changed to standby: 20 µA
- under the key specifications on page iii, changed well capacity: TBD changed to 5.7 $Ke^-$
- under the key specifications on page iii, changed dark current: TBD changed to 4.7 mV/s @ 60°C
- under the key specifications on page iii, changed fixed pattern noise (FPN): from TBD changed to 0.7 $e^-$
- under chapter 1 on page 1-1, added a table note to table 1-1: for different DOVDDs, register 0x49[3:0] must be changed according to settings in section 2.8, DOVDD power requirements.
- under chapter 2 on page 2-2, updated figure 2-1 block diagram
- under chapter 2 on page 2-4, added section 2.8: power requirements
- under chapter 4 on page 4-1, added table 4-2 flip ON and flip OFF control settings

- under chapter 5 on page 5-3, changed register 0x12 Bit[6]: Skip model enable changed to Bit[6]: Subsampled (skip) mode enable 0: Subsample disabled 1: Subsample enable
- under chapter 7 on page 7-3, changed register 0x12 Bit[6]: Skip model enable changed to Bit[6]: Subsampled (skip) mode enable 0: subsample disabled 1: subsample enable
- under chapter 7 on page 7-11, reserved register 0x85 Bit[7:5]
- under chapter 7 on page 7-11, register 0x85 Bit[4]: LENC gain enable changed to Bit[4]: LENC Bias enable
- under chapter 7 on page 7-12, register 0xB4 Bit[5] EDGE_MT_MAN_EN changed to Sharpening mode 0: Manual; 1: Auto
- under chapter 7 on page 7-12, register 0xB4 Bit[4]: DNS_TH_MAN_EN added De-noise mode manual 0: Manual; 1: Auto
- under chapter 7 on page 7-12, register 0xB5 Bit[7:0]: DNS_TH_MAN changed to De-noise magnitude (manual mode)
- under chapter 7 on page 7-13, register 0xB6 Bit[4:0]: EDGE_MT_MAN changed to Bit[4:0]: Sharpening magnitude (manual mode)
- under chapter 8 on page 8-1, replaced table 8-1 with new absolute maximum ratings table
- under chapter 8 on page 8-2, updated table 8-2 DC characteristics from:

| symbol | parameter | min | typ | max | unit |
|---|---|---|---|---|---|
| supply | | | | | |
| $V_{DD-A}$ | supply voltage (analog) | 2.6 | 2.8 | 3.0 | V |
| $V_{DD-IO}$ | supply voltage (digital I/O) | 1.7 | 1.8 | 3.0 | V |
| $I_{DD-A}$ | active (operating) current | TBD | TBD | TBD | mA |
| $I_{DD-IO}$ | | TBD | TBD | TBD | mA |
| $I_{DDS-SCCB}$ | standby current | TBD | TBD | TBD | mA |
| $I_{DDS-PWDN}$ | | TBD | TBD | TBD | µA |

changed to:

| symbol | parameter | min | typ | max | unit |
|---|---|---|---|---|---|
| supply | | | | | |
| $V_{DD-A}$ | supply voltage (analog) | 2.6 | 2.8 | 3.0 | V |
| $V_{DD-IO}$ | supply voltage (digital I/O) | 1.7 | 1.8 | 3.0 | V |
| $I_{DD-A}$ | active (operating) current | | | 16[a] | mA |
| $I_{DD-IO}$ | | | | 18[a] | mA |
| $I_{DDS-SCCB}$ | standby current | | | 1.2[a] | mA |
| $I_{DDS-PWDN}$ | | | | 20[a] | µA |

- under chapter 10 on page 10-1, updated figure 10-1 sensor array center

**version 2.1** **02.26.2009**

- added table 2-3 to section 2.5, SCCB interface

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