

VGA resolution USB2.0 web camera sensor

Preliminary Data

Features

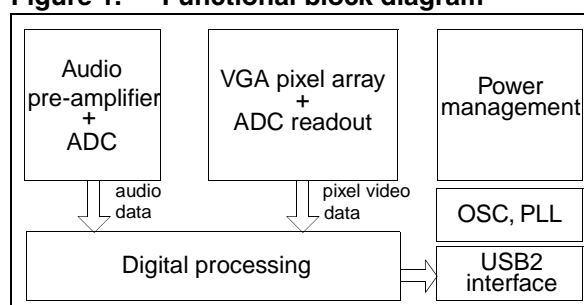
- 640 x 480 (VGA) USB2.0 Web camera
- RGB Bayer color filter array
- 3.6 μm pixel size
- Integrated 10-bit video ADC and processing
- 16-bit audio pre-amplifier, $\Sigma - \Delta$ ADC and processing
- USB2.0 high speed interface for data transfer and control
- I²C master capability
- USB audio class type 1 compliance
- USB video YUV2 compliance
- On-chip 3.3 V and 1.8 V regulators
- Requires single 5 V supply
- Minimum required PCB support components
- Video format: 640 x 480 YUV2 up to 30 fps
- Single 12 MHz input clock
- Integrated image processing functions:
 - Automatic exposure
 - Automatic white balance
 - Dark level compensation
 - Lens shading correction
 - Image sub-sampling
 - Flicker cancellation
 - Sharpening
 - Gamma correction
 - RGB to YUV 422
- Audio processing:
 - Audio class compliance PCM16
 - Preamplifier + ADC + processing
 - Audio rates of 8 kHz to 48 kHz, 16 bits
 - Audio dynamic range from mic. input to USB data output > 60 dB

Description

The VL6522 is a VGA imager on chip (IOC), fabricated in a high performance 0.18 μm CMOS imaging process. The device produces a YUV 4:2:2 digital video data stream at up to 60^(a) frames per second, and supports a microphone input.

Video and audio data is output via a USB2.0 high speed (480 Mbps) interface and allows simple interfacing to a host PC using generic audio and video class drivers under the appropriate operating system (Windows XP). Audio/video class compliance and vendor command sets allow development of other O/S drivers with relative ease.

Figure 1. Functional block diagram



a. 60 fps max at QVGA resolution, 30 fps max at VGA resolution

Contents

1	Overview	5
1.1	Architecture	5
1.2	Technical specifications	5
1.3	Power consumption	5
1.4	Interface	6
1.4.1	USB	6
1.4.2	User customizing	6
1.4.3	Video data standard	6
1.4.4	Audio data standard	6
1.4.5	Software	6
2	Block diagram	7
3	Pinout and pin description	8
3.1	Pinout	8
3.2	Pin description	9
4	Detailed description	11
4.1	Image data pipeline (IDP)	11
4.1.1	Overview	11
4.1.2	Dark level compensation	11
4.1.3	Flicker cancellation	11
4.1.4	Statistics	11
4.1.5	Lens shading correction	11
4.1.6	Channel offset	12
4.1.7	Channel gain	12
4.1.8	Defect correction	12
4.1.9	Interpolation (demosaic)	12
4.1.10	Color matrix	12
4.1.11	Sharpening	12
4.1.12	Gamma correction	12
4.1.13	RGB to YUV 422	12
4.1.14	Automatic frame rate control	13
4.1.15	Fade to black	13

4.2	Audio data pipeline (ADP)	13
4.2.1	Audio overview	13
4.3	ICB system control	13
4.3.1	System control overview	13
4.3.2	I ² C mastering	14
5	Register description	15
5.1	Register interpreter	15
5.2	Hardware control registers	16
5.2.1	Status	16
5.2.2	SETUP register	16
5.2.3	MAN_SPEC_AV register	16
5.2.4	MAN_SPEC_AUDIO register	17
5.2.5	MAN_SPEC_I2C_MASTER register	17
5.3	Firmware control registers	19
5.3.1	ID codes	19
5.3.2	Misc controls	19
5.3.3	Exposure controls	19
5.3.4	Fade to black	20
5.3.5	Frame dimension parameter host inputs	21
5.3.6	White balance controls	21
5.3.7	Automatic frame rate control	22
5.3.8	Video control processing unit descriptors	24
6	Electrical characteristics	26
6.1	Absolute maximum ratings	26
6.2	Operating conditions	26
6.3	DC electrical characteristics	27
6.4	AC electrical characteristics	28
6.4.1	USB2.0 interface	28
6.4.2	External crystal	28
6.4.3	RESETN	28
6.4.4	I ² C Interface	28
7	User precaution	29

8	Package mechanical data	30
9	Glossary	33
10	Ordering information	34
11	Revision history	34

1 Overview

1.1 Architecture

The design includes an image control bus (ICB) mastering unit in the form of a microcontroller used for top-level autonomous management of power, SFPs, USB standard, audio and video class command handling and translation to IDP video and audio processing modules. The microcontroller is also used to run auto exposure and white balance functions.

There are two data pipelines: the audio data pipe (ADP) and the image data pipe (IDP).

1.2 Technical specifications

Table 1. Technical specifications

Parameter	Values		
Image size	640 x 480 (VGA)		
Pixel size	3.6 μm x 3.6 μm		
Array size	2.32 mm x 1.74 mm		
Exposure control	auto		
Frame rate	auto or adjustable up to 60 fps		
Clock frequency	12 MHz		
Output format	USB2.0 (YUV2)		
Output data rate	480 MHz (USB2)		
Audio analogue gain	24 dB		
Audio signal/noise ratio	59 dB		
Supply voltage (V)	5	3.3	1.8
Supply current (mA typ.) VGA 30 fps + audio	14.7	16.3	45.1
Total current consumption from single 5 V supply ⁽¹⁾	74.8 mA		
Operating temperature	-30° C to 70° C		
Package type	LGA36		

1. Typical value VGA @ 30 fps + audio

1.3 Power consumption

From a power consumption perspective the principal modes are:

1. Active - high speed streaming of audio and video, or video only, or audio only.
2. Suspend - standby mode, with lowest current consumption in conformance with the USB2.0 standard.

1.4 Interface

1.4.1 USB

The details of the USB interface are summarized in [Table 2](#).

Table 2. Details of USB interface

Function	Description	Comments
Scope	Standard to which device will comply	USB endpoints
Control	USB spec. rev2.0 HS	Control (default, audio, video)
		Interrupt (snapshot button, video class interrupt)
Video	USB video class rev1.0	Isochronous (video class data)
Audio	USB audio class rev2.0	Isochronous (audio class data)

1.4.2 User customizing

Four special function port pins can allow PID/VID selections, support EEPROM (I²C mastering) and customization for driving LED(s) and sensing switch or button states. VID/PIDs can be programmed into EEPROM.

1.4.3 Video data standard

The video processing pipeline delivers fully reconstructed VGA (640 x480) color data conforming to YUV 4:2:2 at up to 30 fps in accordance with video class specification (Packed YUV Format - YUV2, GUID 32595559-0000-0010-8000-00AA00389B71).

1.4.4 Audio data standard

The audio processing pipeline delivers audio data (to 48 kHz, 16 bits) in accordance with the audio class specification Type 1 (PCM, Pulse Coded Modulation, uncompressed). 16-bit signed two's-complement fixed point format (left-justified meaning the sign bit is the MSB). The binary point is located to the right of the sign bit so that all values lie within the range [-1 to +1].

1.4.5 Software

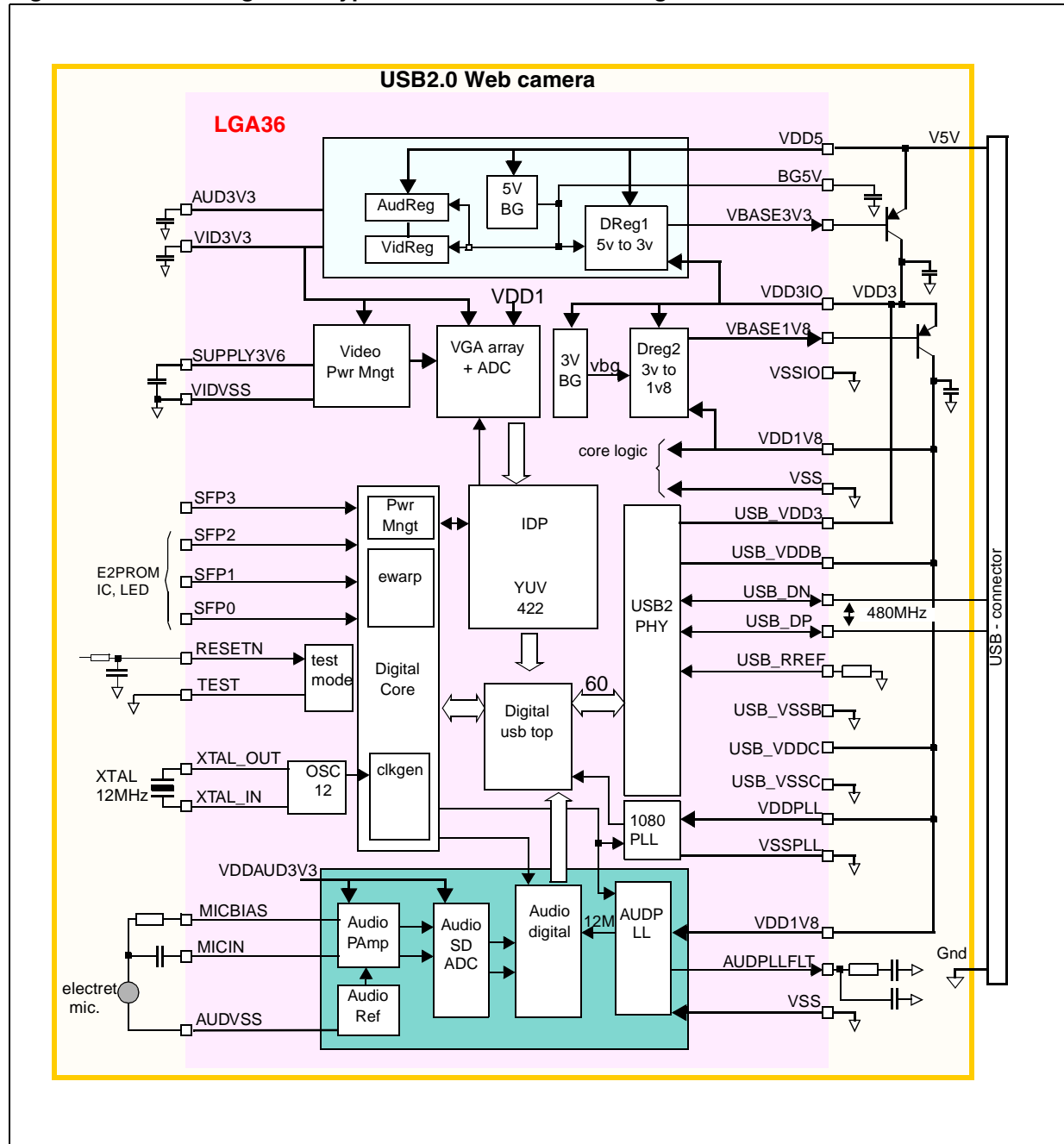
As the VL6522 is video/audio class, no software drivers are necessary to operate with Windows operating systems from XP SP2 onwards.

A unified windows driver is available to allow operation under Windows 2000. This driver is also compatible with Windows XP, XP64, Vista 32 and Vista 64. Although the driver is not necessary for use with these operating systems, it does offer additional benefits to the user, such as the face finding and tracking function, to keep the user's face in frame when video-conferencing for example.

A linux driver is available to allow the VL6522 to be used with a linux based system.

2 Block diagram

Figure 2. Block diagram of typical USB Web camera using VL6522

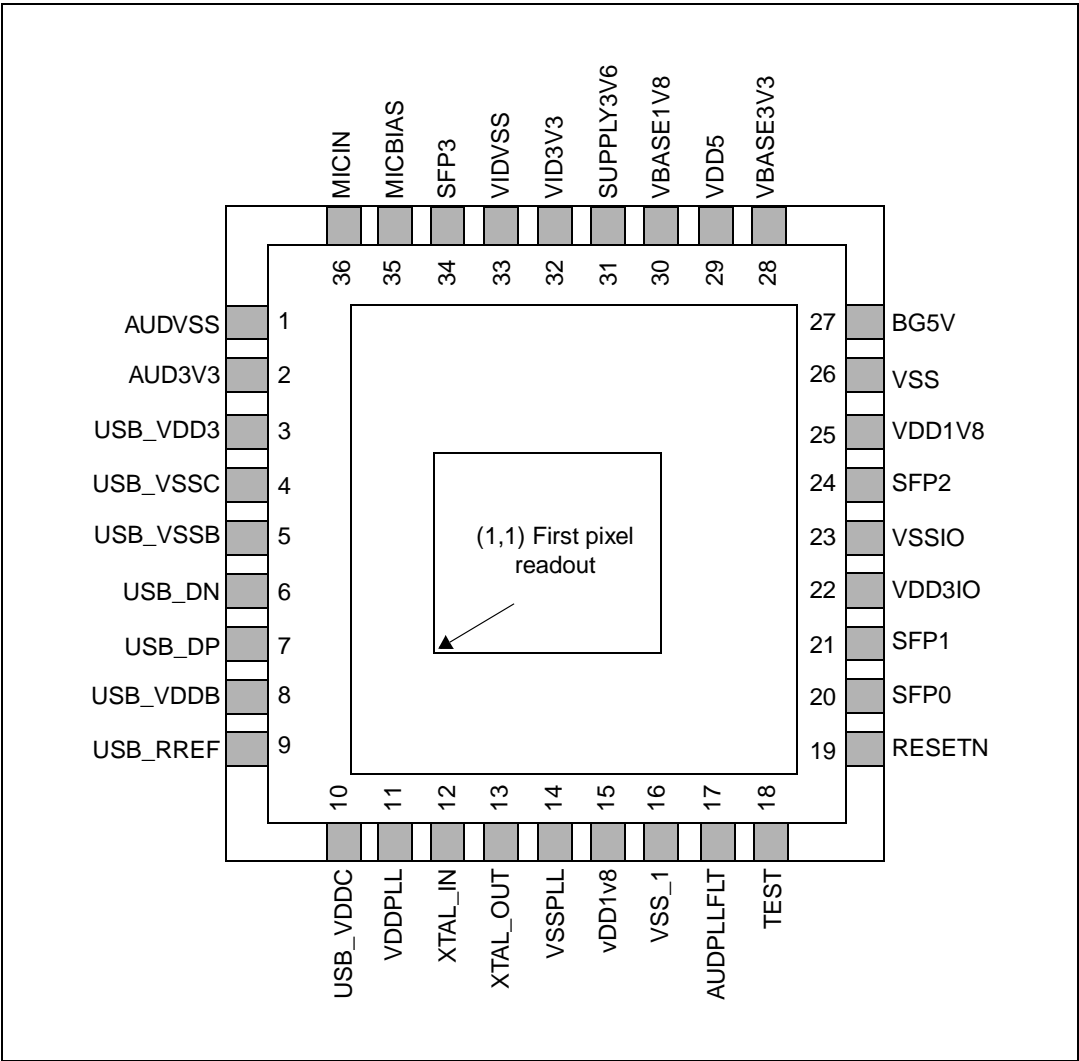


3 Pinout and pin description

3.1 Pinout

The device is available in LGA36 package. The first pixel (1,1) will appear as illustrated in [Figure 3](#).

Figure 3. Device pinout



3.2 Pin description

Table 3. Pin description

Pin number	Pin name	Pin type	Description	Comments
1	AUDVSS	POWER	Ground for audio analog	
2	AUD3V3	POWER	3.3 V supply for audio analog	
3	USB_VDD3	POWER	3.3 V supply for USB2.0 core	
4	USB_VSSC	POWER	Ground for USB2.0 core	
5	USB_VSSB	POWER	Ground for USB2.0 output	
6	USB_DN	I/O/Z	USB D- signal	
7	USB_DP	I/O/Z	USB D+ signal	
8	USB_VDDDB	POWER	1.8 V supply for USB2.0 output	
9	USB_RREF	I	USB2.0 compensation block reference resistor	
10	USB_VDDC	POWER	1.8 V supply for USB2.0 core	
11	VDDPLL	POWER	1.8 V supply for master PLL	
12	XTAL_IN	I	External crystal input	Connect to 12 MHz crystal
13	XTAL_OUT	O	External crystal output	
14	VSSPLL	POWER	Ground for master PLL	
15	VDD1V8	POWER	1.8 V supply for core digital and audio PLL	
16	VSS	POWER	Ground for core digital and audio PLL	
17	AUDPLLFLT	I	Audio PLL filter network	External components required if audio used, leave open if no audio
18	TEST	I	Test mode select	Required external pull down
19	RESETN	I	VL6522 reset signal from POR	Active low
20	SFP0	I/O/Z	I2C SCL (EEPROM) or GPIO port	3v3
21	SFP1	I/O/Z	I2C SDA (EEPROM) or GPIO port	3v3
22	VDD3IO	POWER	3.3 V supply for IO	
23	VSSIO	POWER	Ground for IO	
24	SFP2	I/O/Z	GPIO port	3v3
25	VDD1V8	POWER	1.8 V supply for digital core	
26	VSS	POWER	Ground for digital core	
27	BG5V	O	Bandgap output	External capacitor required
28	VBASE3V3	PWR	3.3 V digital regulator control output	Connect to ext. PNP base
29	VDD5	POWER	5.0 V Supply	
30	VBASE1V8	PWR	1.8 V digital regulator control output	Connect to ext. PNP base

Table 3. Pin description (continued)

Pin number	Pin name	Pin type	Description	Comments
31	SUPPLY3V6	POWER	External reservoir cap.	
32	VID3V3	POWER	3.3 V supply for video analog	
33	VIDVSS	POWER	Ground for video analog	
34	SFP3	I	GPI (input only)	3v3
35	MICBIAS	O	Microphone bias voltage	
36	MICIN	I	Microphone input signal	

4 Detailed description

4.1 Image data pipeline (IDP)

4.1.1 Overview

The video processing blocks included in the VL6522 IDP are listed below:

- Dark level compensation
- Flicker cancellation
- Statistics
- Lens shading correction
- Channel offset
- Channel gain
- Defect correction
- Interpolation
- Color matrix
- Sharpening
- Gamma correction
- RGB to YUV 422
- Automatic frame rate control
- Fade to black

4.1.2 Dark level compensation

A dedicated DSP uses information from special dark lines within the pixel array to apply an offset to the video data and ensure a consistent 'black' level.

4.1.3 Flicker cancellation

The 50/60 Hz flicker frequency present in the lighting (due to fluorescent lighting) can be cancelled by the system.

4.1.4 Statistics

The function of the statistics processor is to gather statistics on Bayer IDP data. The statistics are made available to the Imaging Control Bus Host for tasks such as automatic exposure control and white balance.

4.1.5 Lens shading correction

The lens shading correction module is used to reduce the visible effect of vignetting where inherent problems in lens design can cause non-uniformities in levels of light transmission across the image plane. The extent of transmission loss is primarily a function of lens quality and fabrication tolerances, but generally increases radially from the lens' optical centre towards the edges of the scene.

Typically, the visual effect is at its worst where the distance from the optical centre to the edge of the image is at its maximum and manifests itself as the familiar 'darkening of the image corners'.

4.1.6 Channel offset

The channel offset module is used to add or subtract a programmable offset from each of the four Bayer color channels of the incoming IDP. These offsets are typically used to remove a data pedestal or cancel a dark offset introduced at an earlier stage in the pipe.

4.1.7 Channel gain

The channel gain module is used to apply a programmable gain to each of the four Bayer color channels of input data. These gains are used as controls of Automatic Exposure Control (AEC) and Automatic White Balance (AWB).

4.1.8 Defect correction

This function runs a defect correction filter over the data in order to remove defects from the final output. This function has been optimized to attain the minimum level of defects from the system.

4.1.9 Interpolation (demosaic)

The interpolation module converts Bayer pixel data to RGB and applies an anti-alias filter to the data.

4.1.10 Color matrix

The color matrix correction transformation is performed on the outputs of the interpolation module.

4.1.11 Sharpening

The sharpening module's function is to add a certain amount of peaking components to the original interpolated RGB. Indeed, the interpolation process involves a certain degree of low-pass filtering that blurs the original sharpness of the image.

In order to realize 2-dimensional sharpness easily, the sharpening filter is only applied on the green components (green carries the highest luma component). The output of the filter is re-injected into the R, G, and B components from the matrix, via a process called coring.

4.1.12 Gamma correction

The gamma correction module applies a non-linear compensation to the IDP RGB data stream in order to achieve correct reproduction of intensity on the host display.

4.1.13 RGB to YUV 4:2:2

Conversion of RGB to YUV 4:2:2. The YUV comprises luminance (Y) and chrominance (U and V) components.

4.1.14 Automatic frame rate control

When enabled, the automatic frame rate control will reduce the frame rate in low light levels to improve image quality. By default the minimum frame rate that the device will use is 5 fps.

4.1.15 Fade to black

Using programmable levels the microprocessor will fade the output signal to black. This ensures that under the darkest conditions, when the image is not of sufficient quality, the device will output black. This operation is achieved by scaling the RGB to the YCbCr matrix.

4.2 Audio data pipeline (ADP)

The audio block contains functions allowing the capture and processing of audio data from an external microphone. The processed data is then written into an external FIFO which is in turn read by the USB control.

4.2.1 Audio overview

The audio processing blocks used in the VL6522 ADP are listed below:

- Microphone amplifier with programmable gain
- 16-bit sigma delta ADC
- Digital AGC^(b), volume and noise gate
- Variable sample rate at both 8 and 16 bits
- Interface to external async audio FIFO
- ICB register bank to provide control and status

4.3 ICB system control

4.3.1 System control overview

In the VL6522, the embedded microcontroller has five main functions:

- USB management
- Power management
- SFP management
- Auto exposure control (AEC)

The task of the exposure control is to ensure that all scenes are correctly exposed to provide a good level of contrast. In normal operation the VL6522 will use hardware-generated statistics to determine appropriate exposure settings for a particular scene and adjust the system accordingly to give a correctly exposed image.

- Auto white balance (AWB)

Using hardware-generated statistics the microcontroller adjusts the gains applied to the individual color channels in order to achieve a correctly color balanced image.

b. The Automatic Gain Control is disabled by default

4.3.2 I²C mastering

This allows the control of the slave I²C lines, which can be useful for reading from and writing to an EEPROM, or for control of any other I²C device.

If 'manual_mode' is set, then the SCL/SDA lines can be bit bashed by writing direct to 'sda' and 'scl'. Otherwise these are controlled automatically. The 'clk_div' reg is used to slow down the clock if necessary (default is zero which should result in approx 400 kHz SCL).

The 'start' bit will generate an I2C start bus condition when set high.

The 'cmd_processed' bit will initially be set low and then go high when the command is complete.

The 'stop' bit will generate an I²C stop bus condition when set high. The 'cmd_processed' bit will initially be set low and then go high when the command is complete.

The 'read' bit will kick off a read from the current address. The 'cmd_processed' bit will be set low and then go high when the command is complete. At this point the READ_BYTE register will contain the data.

If the 'multiple_read' bit is set, then the address will be auto-incremented after each 'read'. That is, you can kick off another read without first having to set the address.

To write a byte, write the data value into the WRITE_BYTE register, then wait for the 'cmd_processed' bit to go high. Finally check that the 'ack_rx' (acknowledge recieved) bit is high.

The 'eeprom_present' bit is set by the firmware when it first attempts to address the eeprom. If it gets an acknowledge then this bit is set high, otherwise it is set low.

Note: See [Table 10 on page 17](#) for locations of and information on relevant registers.

5 Register description

5.1 Register interpreter

Register contents represent different data types as described in [Table 4](#).

Table 4. Register naming prefix

Prefix	Description
UIA_BYTE = b	One byte unsigned data
UIA_UINT16 = w	Twobyte data
UIA_UINT16 = uw	Two byte unsigned data
Flag_e(F) = f	One byte data. Only two possible values
UIA_FLOAT = fp	Two byte data. Expect value in Floating Point 16 notation
UIA_INT8 = sb	One byte signed data

Registers not listed in this datasheet should be considered as reserved or read-only and should **not** be written to, as this may cause unpredictable results.

The VL6522 registers can be written to using the extension units within the Windows video class.

All register locations contain an 8-bit byte. However, certain parameters require 16 bits to represent them and are therefore stored in more than 1 location.

Note: For all 16 bit parameters, the MSB register must be written before the LSB register.

The data stored in each location can be interpreted in different ways as shown below. Register contents represent different data types as described in [Table 5](#).

Table 5. Data type

Data type	Description
BYTE	Single field register 8 bit parameter
UINT_16	Multiple field registers - 16 bit parameter
FLAG_e	Bit 0 of register must be set/cleared
CODED	Coded register - function depends on value written
FLOAT	Float Value

Float number format

Float 900 is used in ST co-processors to represent floating point numbers in 2 bytes of data. It conforms to the following structure:

Bit[15] = Sign bit (1 represents negative)

Bit[14:9] = 6 bits of exponent, biased at decimal 31

Bit[8:0] = 9 bits of mantissa

5.2 Hardware control registers

5.2.1 Status

Table 6. Status

Index	Status register [read only]	
0x0002	REVISION_NUMBER	
	Default value	0x04
	Purpose	Identifies the cut of silicon ⁽¹⁾
	Type	BYTE
	Possible values	<0x00> Cut 1.0 <0x01> Cut 1.1 <0x02> Cut 1.2 <0x03> Cut 1.3 <0x04> Cut 1.4

1. This document refers to cut 1.4 of silicon.

5.2.2 SETUP register

Table 7. SETUP register

Index	SETUP register	
0x0002	IMAGE_ORIENTATION	
	Default value	0x00
	Purpose	Selects the orientation of the image
	Type	BYTE
	Possible values	<0x00> Normal <0x01> Horizontal flip (mirrored) <0x02> Vertical flip <0x03> Horizontal & vertical flip

5.2.3 MAN_SPEC_AV register

Table 8. MAN_SPEC_AV register

Index	MAN_SPEC_AV register	
0x322a	R2_COEFF	
	Default value	0x04
	Purpose	Radial R2 anti-vignetting (lens shading) coefficient, to allow lightening and darkening of image corners (for special effects, as well as standard av compensation).
	Type	BYTE
	Possible values	-127 to 127

5.2.4 MAN_SPEC_AUDIO register

Table 9. MAN_SPEC_AUDIO register

Index	MAN_SPEC_AUDIO register	
0x3340	ALC	
	Default value	0x00
	Purpose	Automatic gain control enable
	Type	BYTE
	Possible values	<0x00> Automatic gain control off <0x80> Automatic gain control on
0x3346	VOLUME	
	Default value	0x3f
	Purpose	Audio volume
	Type	BYTE
	Possible values	0 to 63
0x3348	MIC_GAIN	
	Default value	0x06
	Purpose	Microphone input stage gain
	Type	BYTE
	Possible values	0 to 7

5.2.5 MAN_SPEC_I2C_MASTER register

Table 10. MAN_SPEC_I2C_MASTER register

Index	MAN_SPEC_I2C_MASTER register ⁽¹⁾	
0x3350	CTRL	
	Default value	0x07
	Purpose	Control for the I2C
	Type	CODED
	Possible values	<0> SCL <1> SDA <2> Manual mode <4:3> Clock divider

Table 10. MAN_SPEC_I2C_MASTER register (continued)

Index	MAN_SPEC_I2C_MASTER register ⁽¹⁾	
0x3351	CMD	
	Default value	0x00
	Purpose	I2C command
	Type	CODED
	Possible values	<0> Start <1> Stop <2> Read <3> Multiple read
0x3352	WRITE_BYTE	
	Default value	0x00
	Purpose	
	Type	BYTE
	Possible values	0 to 255
0x3353	READ_BYTE [read only]	
	Default value	0x00
	Purpose	
	Type	BYTE
	Possible values	0 to 255
0x3354	STATUS [read only]	
	Default value	0x01
	Purpose	I2C Status
	Type	CODED
	Possible values	<0> Command processed <1> Acknowledge received <2> EEPROM present <3> EEPROM error

1. More detail on how to use the I²C master can be found in the I²C mastering section [4.3.2](#)

5.3 Firmware control registers

5.3.1 ID codes

Table 11. ID codes

Index	IDCodes ⁽¹⁾ register	
0x8008	idVendor	
	Default value	0x0553
	Purpose	Vendor identification
	Type	UINT_16
	Possible values	0x0000 to 0xffff ⁽¹⁾
0x800a	idProduct	
	Default value	0x0522
	Purpose	Product identification
	Type	UINT_16
	Possible values	0x0000 to 0xffff ⁽¹⁾

1. This data is stored in little endian format: the LSB is located at the lower index.

5.3.2 Misc controls

Table 12. Misc controls

Index	MiscControls register	
0x84dc	fDisableVideoClassGUI	
	Default value	0x00
	Purpose	Disables the GUI
	Type	FLAG_e
	Possible values	<0x00> GUI enabled <0x01> GUI disabled

5.3.3 Exposure controls

Table 13. Exposure controls

Index	ExposureControls register	
0x8510	bAntiFlickerMode	
	Default value	<0> AntiFlickerMode_Inhibit
	Purpose	Anti flicker mode
	Type	CODED
	Possible values	<0> AntiFlickerMode_Inhibit <1> AntiFlickerMode_ManualEnable <2> AntiFlickerMode_AutomaticEnable

5.3.4 Fade to black

Table 14. Fade to black

Index	FadeToBlack register	
0x85cb	fDisable	
	Default value	0x00
	Purpose	Disables the Fade to Black
	Type	FLAG_e
	Possible values	<0x00> Fade to Black enabled <0x01> Fade to Black disabled
0x85cc	fpBlackValue	
	Default value	0x0000 (0.0000)
	Purpose	Black Value
	Type	FLOAT
	Possible values	-8581545984 to 8581545984 (0xffff to 0x7fff)
0x85ce	fpDamperLowThreshold	
	Default value	0x6a25 (4497408)
	Purpose	Low Threshold for exposure for calculating the damper slope
	Type	FLOAT
	Possible values	-8581545984 to 8581545984 (0xffff to 0x7fff)
0x85d0	fpDamperHighThreshold	
	Default value	0x6c9f (10993664)
	Purpose	High Threshold for exposure for calculating the damper slope
	Type	FLOAT
	Possible values	-8581545984 to 8581545984 (0xffff to 0x7fff)
0x85d2	fpDamperOutput [read only]	
	Default value	0x00 (0.0000)
	Purpose	Minimum possible damper output.
	Type	FLOAT
	Possible values	0 to 1 (0x0000 to 0x3e00)

5.3.5 Frame dimension parameter host inputs

Table 15. Frame dimension parameter host inputs

Index	FrameDimensionParameterHostInputs register	
0x85fa	bLightingFrequency_Hz	
	Default value	0x64
	Purpose	AC Frequency - used for flicker free time period calculations this mains frequency determines the flicker free time period.
	Type	BYTE
	Possible values	0 to 255 Note: The value is double the desire frequency in Hz. i.e. 0x64 = 100 which equates to 50 Hz.

5.3.6 White balance controls

Table 16. White balance controls

Index	WhiteBalanceControls register	
0x8652	bMode	
	Default value	0x00
	Purpose	Disables the GUI
	Type	CODED
	Possible values	<0> OFF - No White balance, all gains will be unity in this mode <1> AUTOMATIC - Automatic mode, relative step is computed here <3> MANUAL_RGB - User manual mode, gains are applied manually <4> DAYLIGHT_PRESET - DAYLIGHT and all the modes below, fixed value of gains are applied here. <5> TUNGSTEN_PRESET <6> FLUORESCENT_PRESET <7> HORIZON_PRESET <8> MANUAL_COLOUR_TEMP <9> FLASHGUN_PRESET
0x8653	bManualRedGain	
	Default value	0x00
	Purpose	User setting for Red Channel gain.
	Type	BYTE
	Possible values	0 to 255 Applied_Red_Gain = (1 + bManualRedGain / 128) / MinGain Where MinGain = the smallest value from either Applied_Red_Gain , Applied_Green_Gain or Applied_Blue_Gain

Table 16. White balance controls (continued)

Index	WhiteBalanceControls register	
0x8654	bManualGreenGain	
	Default value	0x00
	Purpose	User setting for Green Channel gain.
	Type	BYTE
	Possible values	0 to 255 $\text{Applied_Green_Gain} = (1 + \text{bManualGreenGain} / 128) / \text{MinGain}$ Where MinGain = the smallest value from either Applied_Red_Gain , Applied_Green_Gain or Applied_Blue_Gain
0x8655	fManualBlueGain	
	Default value	0x00
	Purpose	User setting for Blue Channel gain.
	Type	BYTE
	Possible values	0 to 255 $\text{Applied_Blue_Gain} = (1 + \text{bManualBlueGain} / 128) / \text{MinGain}$ Where MinGain = the smallest value from either Applied_Red_Gain , Applied_Green_Gain or Applied_Blue_Gain

5.3.7 Automatic frame rate control

Table 17. Automatic frame rate control

Index	AutomaticFrameRateControl register	
0x8680	bMode	
	Default value	0x00
	Purpose	Sets manual or auto frame rate
	Type	FLAG_e
	Possible values	<0x00> Manual frame rate. <0x01> Automatic frame rate.
0x8681	bImpliedGainThresholdLow_num	
	Default value	0x05
	Purpose	Numerator for calculation of low threshold of automatic framerate control
	Type	BYTE
	Possible values	0 to 255

Table 17. Automatic frame rate control (continued)

Index	AutomaticFrameRateControl register	
0x8682	bImpliedGainThresholdLow_den	
	Default value	0x01
	Purpose	Denominator for calculation of low threshold of automatic framerate control.
	Type	BYTE
	Possible values	0 to 255
0x8683	bImpliedGainThresholdHigh_num	
	Default value	0x08
	Purpose	Numerator for calculation of high threshold of automatic framerate control
	Type	BYTE
	Possible values	0 to 255
0x8684	bImpliedGainThresholdHigh_den	
	Default value	0x01
	Purpose	Denominator for calculation of high threshold of automatic framerate control
	Type	BYTE
	Possible values	0 to 255
0x8685	bUserMinimumFrameRate_Hz	
	Default value	0x05
	Purpose	Sets the minimum framerate employed when in automatic framerate mode.
	Type	BYTE
	Possible values	0 to 255
0x8686	bUserMaximumFrameRate_Hz	
	Default value	0x3c
	Purpose	Sets the maximum framerate employed when in automatic framerate mode.
	Type	BYTE
	Possible values	0 to 255
0x8687	bRelativeChange_num	
	Default value	0x02
	Purpose	Numerator for calculation of relative change in framerate.
	Type	BYTE
	Possible values	0 to 255

Table 17. Automatic frame rate control (continued)

Index	AutomaticFrameRateControl register	
0x8688	bRelativeChange_den	
	Default value	0x02
	Purpose	Denominator for calculation of relative change in framerate
	Type	BYTE
	Possible values	0 to 255

5.3.8 Video control processing unit descriptors

Table 18. Video control processing unit descriptors

Index	VideoControlProcessingUnitDescriptors register ⁽¹⁾	
0x8709	Brightness	
	Default value	0x0018
	Purpose	Video class brightness control
	Type	UINT_16
	Possible values	0x0000 to 0x0025 ⁽¹⁾
0x870b	Contrast	
	Default value	0x007c
	Purpose	Video class contrast control
	Type	UINT_16
	Possible values	0x0000 to 0x00c8 ⁽¹⁾
0x870d	Saturation	
	Default value	0x0079
	Purpose	Video class saturation control
	Type	UINT_16
	Possible values	0x0000 to 0x00c8 ⁽¹⁾
0x870f	Sharpness	
	Default value	0x000f
	Purpose	Video class sharpness control
	Type	UINT_16
	Possible values	0x0000 to 0x003f ⁽¹⁾

Table 18. Video control processing unit descriptors (continued)

Index	VideoControlProcessingUnitDescriptors register ⁽¹⁾	
0x8711	Gamma	
	Default value	0x0012
	Purpose	Video class gamma control
	Type	UINT_16
	Possible values	0x0001 to 0x001f ⁽¹⁾

1. This data is stored in little endian format: the LSB is located at the lower index.

6 Electrical characteristics

6.1 Absolute maximum ratings

Table 19. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
T _{STO}	Storage temperature	-40	85	° C
V _{5V}	5 V supply	4.1	5.6	V

Caution: Stresses above those listed under “Absolute Maximum Ratings” can cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

6.2 Operating conditions

Table 20. Supply specifications

Symbol	Parameter	Min.	Max.	Unit
T _{AF}	Operating temperature, functional (Camera is electrically functional)	-30	70	° C
T _{AN}	Operating temperature, nominal (Camera produces acceptable images)	-25	55	° C
T _{AO}	Operating temperature, optimal (Camera produces optimal optical performance)	5	30	° C
V _{5V}	5 V supply	4.1	5.6	V

6.3 DC electrical characteristics

Note: Over operating conditions unless otherwise specified.

Table 21. DC electrical characteristics (non-characterized data, guide values only)

Symbol	Description	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low voltage		-0.3	TBD	$0.3 V_{DD3IO}$	V
V_{IH}	Input high voltage		$0.7 V_{DD3IO}$	TBD	$V_{DD3IO} + 0.3$	V
V_{OL}	Output low voltage	$I_{OL} < 2.29 \text{ mA}$	TBD	TBD	$0.4 V_{DD}$	V
V_{OH}	Output high voltage	$I_{OH} < 1.48 \text{ mA}$	2.6	TBD	TBD	V
I_{IL}	Input leakage current Input pins I/O pins	$0 < V_{IN} < V_{DD}$	TBD	TBD	+/- 10 +/- 1	μA μA
C_{IN}	Input capacitance, SCL	$T_A = 25^\circ \text{C}$, freq = 1 MHz	TBD	TBD	TBD	pF
C_{OUT}	Output capacitance	$T_A = 25^\circ \text{C}$, freq = 1 MHz	TBD	TBD	TBD	pF
$C_{I/O}$	I/O capacitance, SDA	$T_A = 25^\circ \text{C}$, freq = 1 MHz	TBD	TBD	TBD	pF

Table 22. Typical current consumption (non-characterised data, guide values only)

Symbol	Description	Suspend	Active ⁽¹⁾	Video ⁽²⁾	Video + Audio ⁽³⁾	Units
I_{VDD5}	Total 5 V supply to device	0.1	0.1	9.5	14.7	mA
$I_{3V3total}$	Total 3.3 V supply to device	0.3	7.2	14.5	16.3	mA
$I_{1V8total}$	Total 1.8 V supply to device	0.0	28.6	44.1	45.1	mA

1. VL6522, enumerated but not streaming

2. VL6522, streaming 30 fps VGA

3. VL6522, streaming 30 fps VGA and streaming audio

Note: *Note: Total current drawn on single 5 V input is 0.38 mA in suspend mode. This assumes transistors are in place to provide the 3.3 V & 1.8 V from the single 5 V supply.*

6.4 AC electrical characteristics

6.4.1 USB2.0 interface

Conforms to the USB2.0 chapter 7.1.

6.4.2 External crystal

The primary reason for choosing the crystal frequency and tolerance is because of the USB data rate. To comply with the USB2.0 specification, when in high speed mode (480 Mb/s), the bit accuracy has to be +/- 500 ppm.

It is recommended to use a crystal with a frequency of 12 MHz and a frequency accuracy of +/- 100 ppm or better.

6.4.3 RESETN

After RESETN is pulsed low (during power up for example), the device shall start up in it's default condition. This will include reading the EEPROM, if fitted.

During startup, the RESETN line should be held low for between 100 μ s and 50 ms after the supplies are stable. On the reference design board, an RC circuit is used to delay the rise of RESETN using values of 470 k Ω and 100 nF. This gives a delay of approximately 20 ms between VDD3IO reaching 3 V and the device coming out of reset.

6.4.4 I²C Interface

The VL6522 can be used as a I²C master. By writing to the video class extension units on the device over usb, the SDA & SCL pins can be controlled. This allows the slaving of such devices as servos, EEPROMs or any device with an I²C interface. More detail on this interface can be found in section [4.3.2](#).

7 User precaution

As is common with many CMOS imagers the camera should not be pointed at bright static objects for long periods of time as permanent damage to the sensor may occur.

8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an STMicroelectronics trademark. ECOPACK specifications are available at: www.st.com.

Caution: The LGA package is not hermetically sealed. To prevent contamination, handle the device carefully in a clean environment and avoid contact with any liquids.

Table 23. POA for optical 36LGA 10X10X1.9 0.8

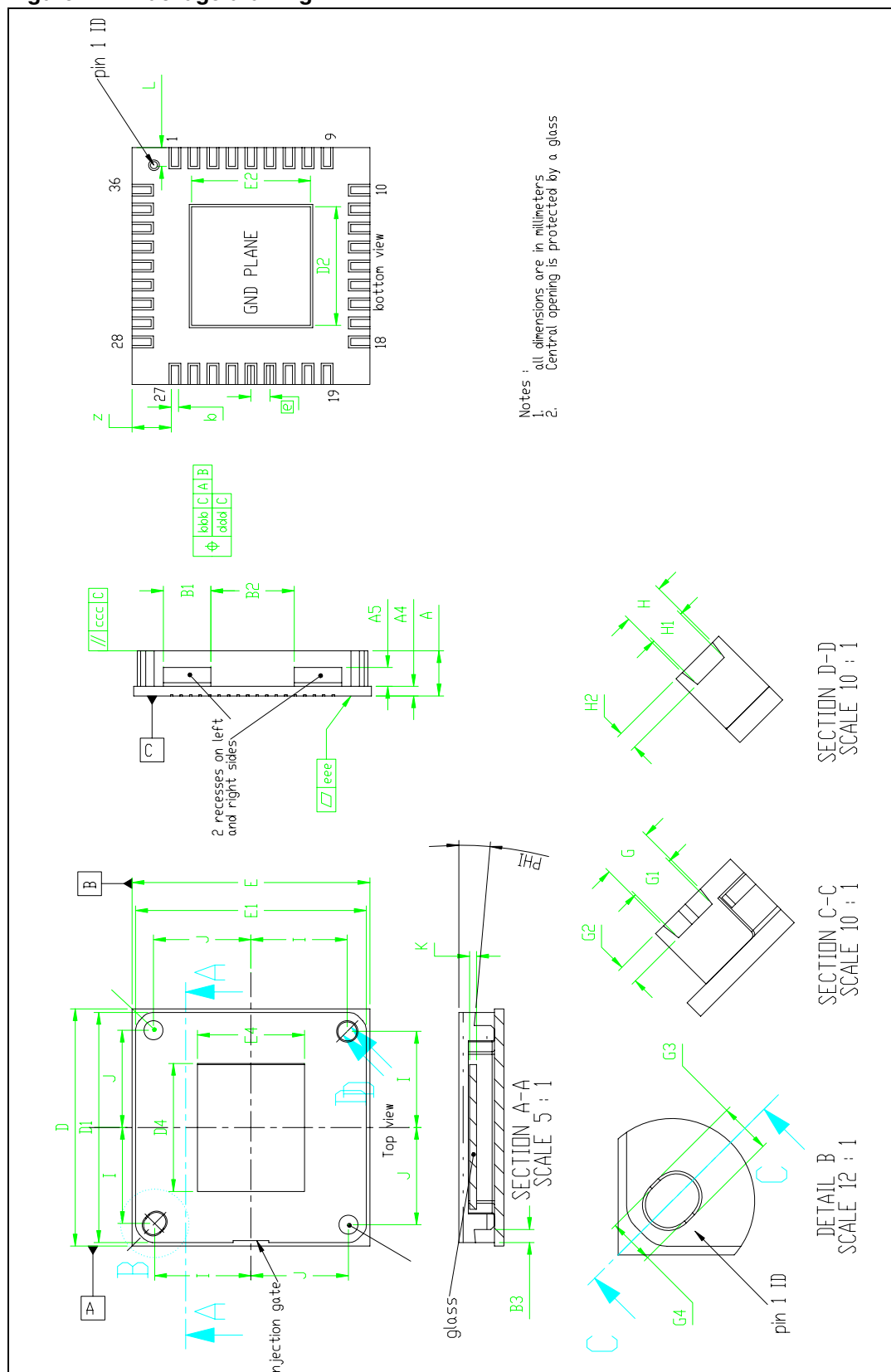
Reference	Data book (mm)		
	Typ.	Min.	Max.
A	1.90	1.80	2.00
A4	0.4	0.35	0.45
A5	0.8	0.7	0.9
B1	2.0		
B2	3.5		
B3	0.55		
b	0.30	0.25	0.35
D	10.00	9.90	10.10
D1	9.70	9.60	9.80
D2	5		
D4	5.4		
e	0.8		
E	10.00	9.90	10.10
E1	9.70	9.60	9.80
E2	5		
E4	4.5		
G	1.1	1.0	1.2
G1	1		
G2	0.4	0.3	0.5
G3	0.9	0.8	1.0
G4	0.8		
H	0.9	0.8	1.0
H1	0.8		
H2	0.4	0.3	0.5

Table 23. POA for optical 36LGA 10X10X1.9 0.8 (continued)

Reference	Data book (mm)		
	Typ.	Min.	Max.
I	4.05	3.95	4.15
J	4.1		
K	0.3		
PHI	5°	4°	6°
z	1.65		
L	0.8	0.7	0.9
bbb	0.01		
ccc	0.1		
ddd	0.08		
eee	0.08		
nD	9		
nE	9		
n	36		

- Note: 1 Optical- LGA stands for Optical Land Grid Array.
- 2 The optical centre of the imaging array is the same as the mechanical centre of the LGA package. This allows for easy alignment of the lens to the imaging array.

Figure 4. Package drawing



9 Glossary

Table 24. Glossary

Acronym	Description
ADC	Analogue to Digital Converter
ADP	Audio Data Pipeline
AEC	Automatic Exposure Control
AGC	Automatic Gain Control
AWB	Automatic White Balance
CMOS	Complementary Metal Oxide Semiconductor
EEPROM	Electrically Erasable Programmable Read Only Memory
FIFO	First In First Out
ICB	Image Control Bus
IDP	Image Data Pipeline
JEDEC	Joint Electron Device Engineering Council
LED	Light Emitting Diode
LGA	Land Grid Array
LSB	Least Significant Bit
MSB	Most Significant Bit
OSC	Oscillator
PCM	Pulse Coded Modulation
PID	Product Identification
PLL	Phase Locked Loop
POA	Package Outline Assembly
RGB	Red Green Blue
SCL	Serial Clock
SDA	Serial Data
SFP	Special Function Pin (Port)
USB	Universal Serial Bus
VGA	Video Graphic Array
VID	Vendor Identification
YUV	Y stands for the luminance component (the brightness) and U and V are the chrominance (color) components

10 Ordering information

Table 25. Order codes

Part number	Package	Packing
VL6522V0MH	LGA36	Tray

11 Revision history

Table 26. Document revision history

Date	Revision	Changes
14-Mar-2007	1	Initial release.
05-Jul-2007	2	Added Chapter 7: User precaution and a caution in Chapter 8: Package mechanical data .

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2007 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com