R-Type Control Signal List

Cycle no.	1	2	3	4	
State no.	1	2	7	8	
Control Signals:					
PCWRITE	1	0	0	0	
IRWRITE	1	0	0	0	
WRITEPORTSELECT	0	0	0	0	
WRITEDATASELECT	00	00	00	00	
REGWRITE	0	0	0	1	
ALUSRCA	0	0	1	0	
ALUSRCB	01	10	00	00	
ALUOP	00	00	10	00	
PCSRC	0	0	0	0	
MEMWRITE	0	0	0	0	
BRANCH	0	0	0	0	

Jump Control Signal List

Cycle no.	1	2	3		
State no.	1	2	10		
Control Signals:					
PCWRITE	1	0	1		
IRWRITE	1	0	0		
WRITEPORTSELECT	0	0	0		
WRITEDATASELECT	00	00	00		
REGWRITE	0	0	0		
ALUSRCA	0	0	0		
ALUSRCB	01	10	00		
ALUOP	00	00	00		
PCSRC	0	0	1		
MEMWRITE	0	0	0		
BRANCH	0	0	0		

JAL Control Signal List

Cycle no.	1	2	3		
State no.	1	2	11		
Control Signals:					
PCWRITE	1	0	1		
IRWRITE	1	0	0		
WRITEPORTSELECT	0	0	1		
WRITEDATASELECT	00	00	10		
REGWRITE	0	0	1		
ALUSRCA	0	0	0		
ALUSRCB	01	10	00		
ALUOP	00	00	00		
PCSRC	0	0	1		
MEMWRITE	0	0	0		
BRANCH	0	0	0		

JR Control Signal List

Cycle no.	1	2	3		
State no.	1	2	13		
Control Signals:					
PCWRITE	1	0	1		
IRWRITE	1	0	0		
WRITEPORTSELECT	0	0	0		
WRITEDATASELECT	00	00	00		
REGWRITE	0	0	0		
ALUSRCA	0	0	1		
ALUSRCB	01	10	11		
ALUOP	00	00	00		
PCSRC	0	0	0		
MEMWRITE	0	0	0		
BRANCH	0	0	0		

Branch Control Signal List

Cycle no.	1	2	3		
State no.	1	2	9		
Control Signals:					
PCWRITE	1	0	0		
IRWRITE	1	0	0		
WRITEPORTSELECT	0	0	0		
WRITEDATASELECT	00	00	00		
REGWRITE	0	0	0		
ALUSRCA	0	0	1		
ALUSRCB	01	10	00		
ALUOP	00	00	01		
PCSRC	0	0	1		
MEMWRITE	0	0	0		
BRANCH	0	0	1		

I-type without Mem access Control Signal List (exclude LI/LUI)

Cycle no.	1	2	3	4	
State no.	1	2	3	8	
Control Signals:					
PCWRITE	1	0	0	0	
IRWRITE	1	0	0	0	
WRITEPORTSELECT	0	0	0	0	
WRITEDATASELECT	00	00	00	00	
REGWRITE	0	0	0	1	
ALUSRCA	0	0	1	0	
ALUSRCB	01	10	10	00	
ALUOP	00	00	10	00	
PCSRC	0	0	0	0	
MEMWRITE	0	0	0	0	
BRANCH	0	0	0	0	

I-type without Mem access Control Signal List (LI and LUI)

Cycle no.	1	2	3	4	
State no.	1	2	12	8	
Control Signals:					
PCWRITE	1	0	0	0	
IRWRITE	1	0	0	0	
WRITEPORTSELECT	0	0	0	0	
WRITEDATASELECT	00	00	00	00	
REGWRITE	0	0	0	1	
ALUSRCA	0	0	1	0	
ALUSRCB	01	10	10	00	
ALUOP	00	00	10	00	
PCSRC	0	0	0	0	
MEMWRITE	0	0	0	0	
BRANCH	0	0	0	0	

I-type with Mem read access Control Signal List

Cycle no.	1	2	3	4	5
State no.	1	2	3	4	5
Control Signals:					
PCWRITE	1	0	0	0	0
IRWRITE	1	0	0	0	0
WRITEPORTSELECT	0	0	0	0	0
WRITEDATASELECT	00	00	00	00	01
REGWRITE	0	0	0	0	1
ALUSRCA	0	0	1	0	0
ALUSRCB	01	10	10	00	00
ALUOP	00	00	10	00	00
PCSRC	0	0	0	0	0
MEMWRITE	0	0	0	0	0
BRANCH	0	0	0	0	0

I-type with Mem write access Control Signal List

Cycle no.	1	2	3	4	
State no.	1	2	3	6	
Control Signals:					
PCWRITE	1	0	0	0	
IRWRITE	1	0	0	0	
WRITEPORTSELECT	0	0	0	0	
WRITEDATASELECT	00	00	00	00	
REGWRITE	0	0	0	0	
ALUSRCA	0	0	1	0	
ALUSRCB	01	10	10	00	
ALUOP	00	00	10	00	
PCSRC	0	0	0	0	
MEMWRITE	0	0	0	1	
BRANCH	0	0	0	0	