Computational Structure - Cheatsheet - Quiz 1

Information

information $\propto$ uncertainty $\propto \frac{1}{p}$
In laymen terms: If an event is bound to happen, then the fact that the event happens does not give any kind of information
$I(X) = \log_2 \frac{1}{p_i}$
$I(X)_{N \to M} = \log_2 \frac{N}{M}$ bits , where N is the number of equally probably choice with M possible choices

2's complement

Step 1 : Inverse
Step 2 : Add 1 to binary

Number Range

Given X bits
−Signed bit : -2^{x-1} to $2^{x-1} - 1$
−Unsigned bit : 0 to $2^x - 1$
−We can encode 2X choices, or random variables

CMOS Recipe

−Only use NFETs in pulldown circuits and PFETs in pullup circuits
− PO-NI - PFETs conducts when 0, NFETs when 1 − AB is parallel in PD, but series in PU. − Ensure no direct connection from VDD to GND

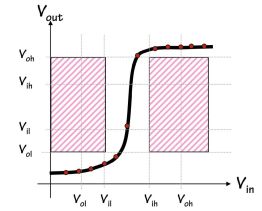
Combinational Device

1. Inputs
2. Outputs
3. Functional specification that details the output for each input
4. The propagation time to get a valid output given a valid input

Static Discipline

Propagation time to get valid output given valid input

VTC



1. Gain ¿ 1
2. Non-Linear Gain

Noise Margin

1. V_{ol} or V_{oh} is the voltage that your system outputs, depending on whether its '0' or '1'. It is going to be received by another system after traversing through some wire.
2. V_{ih} or V_{ih} is the voltage that your system receive as input from another system.
3. Wire has noise, it can cause voltages to change as it traverse through it

The MOSFET

1. The current flow between source and drain IDS is proportional to W=L (the width and the length) of the FET.
2. The side with the higher potential is drain, the one with the lower potential is source.
3. The p-type : majority care holes (impurities), bulk is connected to VDD
4. The n-type : majority are electrons, bulk is connected to GND
5. A FET that is "ON" means that there's connection between D and S, current can flow through them.

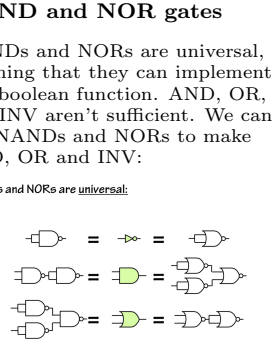
Timings

1. The Propagation Delay t_{pd} - the time delay from valid input to valid output. The effective tpd of an entire circuit is the maximum cumulative propagation delay over all paths from inputs to outputs.
2. The Contamination Delay t_{cd} - the time delay from invalid input to invalid output. The effective tcd of an entire circuit is the minimum cumulative contamination delay over all paths from inputs to outputs.

Logic Synthesis

NAND and NOR gates

NANDs and NORs are universal, meaning that they can implement any boolean function. AND, OR, and INV aren't sufficient. We can use NANDs and NORs to make AND, OR and INV:



BOOLEAN ALGEBRA:

OR rules:	a + 1 = 1, a + 0 = a, a + a = a
AND rules:	a1 = a, a0 = 0, aa = a
Commutative:	a + b = b + a, ab = ba
Associative:	(a + b) + c = a + (b + c), (ab)c = a(bc)
Distributive:	a(b+c) = ab + ac, a + bc = (a+b)(a+c)
Complements:	$a+\bar{a}=1$, $a\bar{a}=0$
Absorption:	$a+ab=a$, $a+\bar{a}b=a+b$
	$a(a+b)=a$, $a(\bar{a}+b)=ab$
Reduction:	$ab+\bar{a}b=b$, $(a+b)(\bar{a}+b)=b$
DeMorgan's Law:	$\overline{a+b}=\bar{a}\bar{b}$, $\overline{ab}=\bar{a}+\bar{b}$

Karnaugh Map

1. "1" cells, No diagonal grouping, Cells can overlap.
2. The top/bottom and left/right edges of map are continuous

Multiplexer (MUX)

It is made up of logic gates (INV, AND, and OR, or NANDs).

1. Muxes are universal,
2. A Mux can have 2^k data inputs, and k bits select inputs, and only can have 1 output
3. A mux always has three components: the inputs, the selector signal(s), and the output.

Decoder

1. A Decoder is the opposite of Mux
2. It has k select inputs, and 2^k possible data outputs
3. The selected output i is HIGH (1), and the rest of the $2^k - 1$ data output is LOW (0).

Read-Only-Memories (ROM)

A decoder's function is to create a read-only-memories.

1. ROMs ignore the structure of combinational functions (hardcoded)
2. The selectors are like "addresses" of an entry
3. For an N-input boolean function, the size of ROM is roughly $2^N x$ number of outputs. For example, the Full Adder has 3 inputs (A, B, C_{in}), and 2 outputs (S and C_{out}). Hence the size of the ROM is $2^3 x 2 = 16$.

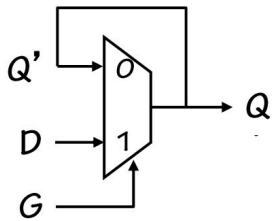
Schematic explanation

1. At the output of the decoder, the little circuit with inverted triangle symbol signifies a pulldown circuit (connected to ground), which will "drain" a signal into 0.
2. At each combination of A, B, and Ci , only one of the 8 outputs of the decoder will be 1. For example, when A = 0;B = 0;Ci = 1, the second output from the top is 1. There's a pulldown for S (it is connected to the ground), which makes it 0, and no pulldown for the C_{out} , which makes it 1.
3. Note the presence of inverters
4. By invention, the location of the "pulldown" circuits correspond to a 1 in the truth table for that particular output (S or Cout).

Week 3

D-Latch

Mux with a feedback loop



-G represents the clock signal
-When G is 1, D is selected in the mux. (Write Mode)
-When G is 0, Q follows Q'. (Read memory mode)

The Dynamic Discipline

The input to a synchronous sequential circuit must be stable during the aperture (setup and hold) time around the clock edge. The dynamic discipline states that

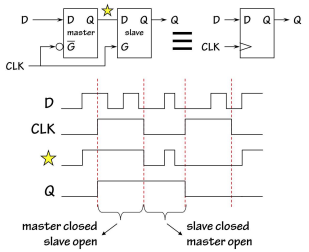
1. $T_{setup} = 2t_{pd}$
2. $T_{hold} = t_{pd}$
1. T_{setup} = the minimum amount of time that the voltage on wire D needs to be stable before the clock edge changes from 0 to 1.
2. T_{hold} = the minimum amount of time that the voltage on wire D needs to be stable after the clock edge changes from 0 to 1.
3. t_{pd} is the propagation delay of the D-latch

Flip-Flop

Created by putting 2 D-latches in series

1. There is an inverter on the G input on the master flip flop
2. When CLK signal is 0, the G wire of master latch receive a 1 while slave flip flop receive a 0
   Master latch : Write mode
   Slave latch : Read mode
3. Vice-versa when CLk signal is 1
4. 1 D-Latch is on write mode why 1 D-latch is on memory mode at anytime.

Flip Flop Waveforms



Note that output wire Q only changes when CLK rises from 0 to 1

Timing Constraint

1. t_{CD} of a D-latch is the time taken for invalid CLK input to produce an invalid output on wire G
2. T_{PD} of a D-latch is the time taken for valid CLK input to produce a valid output on wire G

Sequential Logic Timing Constraint
$t_1 = t_{CD,R1} + t_{CD,1} > t_{HOLD,R2}$
$t_2 = t_{PD,R1} + t_{PD,1} < t_{CLK} - t_{SETUP,R2}$

Metastable State

Properties

1. It corresponds to an invalid logic level
2. Unstable equilibrium which will settle to valid 0 or 1 eventually
3. Settling can be arbitraily long
4. All bistable system exhibits at least 1 metastable state
5. Cannot be avoided but can be minimize

Clock Skew

$t_1 = t_{CD,R1} + t_{CD,R1} > t_{HOLD,R2} + t_{skew}$
$t_2 = t_{PD,R1} + t_{PD,CL1} < t_{CLK} - t_{SETUP,R2} + t_{skew}$
Insert FSM

Week 4 material

Programmable Machines

Programmable control system

1. Control processing at each step with FSM
2. Allow different control sequences to be loaded into control FSM
3. Re-use data path and reconfigure FSM to compute new function

Short-comings

1. Tiny repertoire of operation
2. Unable to generate and execute a new program
3. Limited storage

Finate State Machine: Enumeration

FSM with i inputs, o outputs, s states

1. Truth table has 2^{i+s} rows with (o + s) columns each
2. $2^{(o+s)2^{i+s}}$ max state
3. Limitation : cannot solve problems with arbitrarily many states

Turing Machines

Turing Machine Specification

1. Doubly-infinite tape
2. Discrete symbol positions
3. Finite alphabet
4. Control FSM
   Inputs - Current Symbol
   Outputs - Write 0/1 , move Left/Right
5. Initial Starting State S0
6. Halt StateHalt

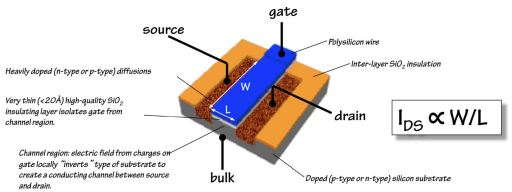
Properties

1. Can be used to compute integer functions of form $y = T_k[x]$
2. Where k: FSM index, x: input tape configuration, y: output tape configuration.
   *Not all integer functions can be computed with Turing Machines
3. Computable functions : f(x) computable $\Leftrightarrow \exists k : \forall x : f(x) = T_k[x] = f_k(x)$
4. Church-Turing Hypothesis states that any computable function is computable by a TM

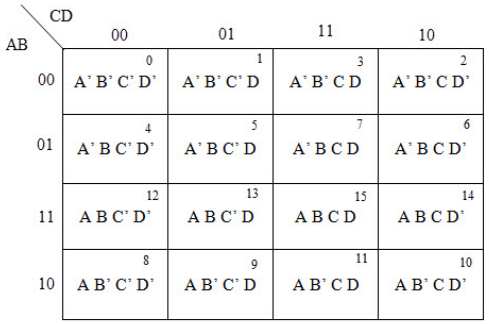
Universal Functions and Universality

Universal function:
$U(k, j) = T_k(j)$
U is comptable by a Turing Machine
→ k encodes a 'program'
→ j encodes the input data to be used
→ T_u interprets program

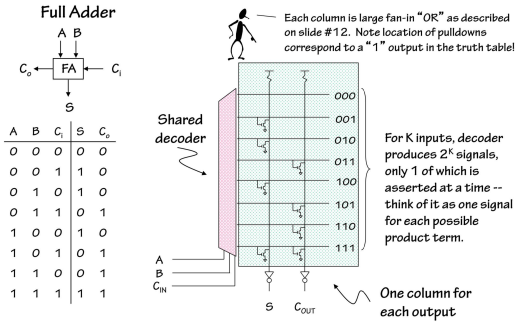
Hex	Binary	Octal	Decimal
0	0	0	0
1	1	1	1
2	10	2	2
3	11	3	3
4	100	4	4
5	101	5	5
6	110	6	6
7	111	7	7
8	1000	10	8
9	1001	11	9
A	1010	12	10
B	1011	13	11
C	1100	14	12
D	1101	15	13
E	1110	16	14
F	1111	17	15
10	1 0000	20	16
11	1 0001	21	17
24	10 0100	44	36
5E	101 1110	136	94
100	1 0000 0000	400	256
3E8	11 1110 1000	1750	1000
1000	1 0000 0000 0000	10000	4096
FACE	1111 1010 1100 1110	175316	64206



MOSFETs (metal-oxide-semiconductor field-effect transistors) are four-terminal voltage-controlled switches. Current flows between the diffusion terminals if the voltage on the gate terminal is large enough to create a conducting "channel", otherwise the mosfet is off and the diffusion terminals are not connected.



Read-only memories (ROMs)



Logic Gates

Name	NOT	AND	NAND	OR	NOR	XOR	XNOR
Alg. Expr.	$\overline{A}$	AB	$\overline{AB}$	$A+B$	$\overline{A+B}$	$A \oplus B$	$\overline{A \oplus B}$
Symbol							
Truth Table	A X 0 1 1 0	B A X 0 0 0 0 1 0 1 0 0 1 1 1	B A X 0 0 1 0 1 1 1 0 1 1 1 0	B A X 0 0 0 0 1 1 1 0 1 1 1 1	B A X 0 0 1 0 1 0 1 0 0 1 1 0	B A X 0 0 0 0 1 1 1 0 1 1 1 0	B A X 0 0 1 0 1 0 1 0 0 1 1 1