DS4001 Timing and Digital I/O Board

Features

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dSPACE

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dSPACE strongly recommends that you download and install the most recent patches for your current dSPACE installation. Visit http://www.dspace.com/go/patches for software updates and patches.

Important Notice

Contents

About This Document

Contents

This document provides feature-oriented access to the information you need to implement the functions of the DS4001.

Symbols

dSPACE user documentation uses the following symbols:

Symbol	Description
DANGER	Indicates a hazardous situation that, if not avoided, will result in death or serious injury.
WARNING	Indicates a hazardous situation that, if not avoided, could result in death or serious injury.
CAUTION	Indicates a hazardous situation that, if not avoided, could result in minor or moderate injury.
NOTICE	Indicates a hazard that, if not avoided, could result in property damage.
Note	Indicates important information that you should take into account to avoid malfunctions.
Tip	Indicates tips that can make your work easier.
	Indicates a link that refers to a definition in the glossary, which you can find at the end of the document unless stated otherwise.
	Precedes the document title in a link that refers to another document.

Naming conventions

dSPACE user documentation uses the following naming conventions:

%name% Names enclosed in percent signs refer to environment variables for file and path names.

< > Angle brackets contain wildcard characters or placeholders for variable file and path names, etc.

Special folders

Some software products use the following special folders:

Common Program Data folder A standard folder for application-specific configuration data that is used by all users.

`%PROGRAMDATA%\dSPACE\<InstallationGUID>\<ProductName>`

or

`%PROGRAMDATA%\dSPACE\<ProductName>\<VersionNumber>`

Documents folder A standard folder for user-specific documents.

`%USERPROFILE%\Documents\dSPACE\<ProductName>\<VersionNumber>`

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`%USERPROFILE%\AppData\Local\dSPACE\<InstallationGUID>\<ProductName>`

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dSPACE Help (local) You can open your local installation of dSPACE Help:

- On its home page via Windows Start Menu
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dSPACE Help (Web) You can access the Web version of dSPACE Help at www.dspace.com.

To access the Web version, you must have a *mydSPACE* account.

PDF files You can access PDF files via the icon in dSPACE Help. The PDF opens on the first page.

Introduction to the Features of the DS4001

Introduction

The DS4001 Timing and Digital I/O Board provides 32 digital I/O lines (TTL) and 5 timers with one timing I/O channel (TTL) each.

Where to go from here

Information in this section

DS4001 Architecture 8
Gives an overview of the functional units and architecture of the DS4001

Feature Overview 8
Provides an overview of the board's features.

DS4001 Interfaces 9
The DS4001 has interfaces for connection to a PHS-bus-based system and external devices.

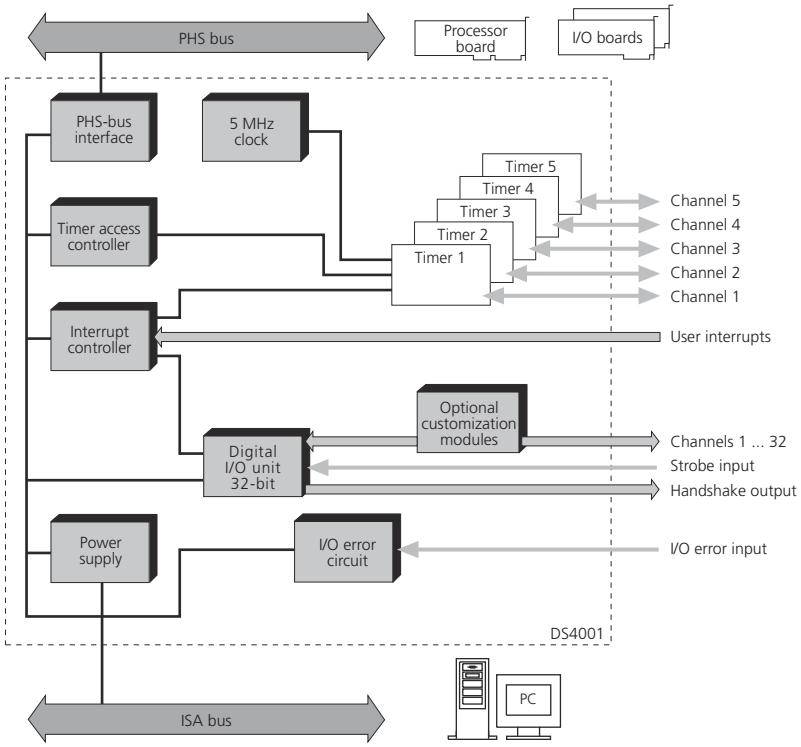
Information in other sections

Data Sheets (PHS Bus System Hardware Reference 🕮)
Summarizes the technical specifications of the hardware components.

DS4001 Architecture

Architecture

The following illustration gives an overview of the functional units and architecture of the DS4001:



Related topics

Basics

DS4001 Interfaces 9
Feature Overview 8

Feature Overview

Features

The DS4001 provides the following features:

Digital I/O unit Provides access to 32 digital I/O lines. Refer to Digital I/O Unit on page 11.

Timing I/O unit Provides access to 5 separately programmable 16-bit timers with one timing I/O channel each. Refer to Timing I/O Unit on page 19.

Interrupt control Provides access to various hardware interrupts. Refer to Interrupts Provided by the DS4001 on page 29.

Limitations

There are some limitations when you work with the DS4001. Refer to Limitations on page 35.

Related topics

Basics

DS4001 Interfaces

Introduction

The DS4001 has interfaces for connection to a PHS-bus-based system and external devices.

Integration into a PHS-bus-based system

To be used, the DS4001 must be integrated into a PHS-bus-based system. While the DS4001 performs the required I/O tasks, the processor board takes over the calculation of the real-time model. That is, applications using DS4001 I/O features are implemented on the processor board.

Communication between processor board and I/O board is performed via the peripheral high-speed bus: That is the PHS bus for a connection to a dSPACE processor board.

Partitioning the PHS bus with the DS802 With the DS802 PHS Link Board you can spatially partition the PHS bus by arranging the I/O boards in several expansion boxes.

The DS802 can be used in combination with many types of available dSPACE I/O boards. However, some I/O boards and some functionalities of specific I/O boards are not supported.

The I/O board support depends on the dSPACE software release which you use. For a list of supported I/O boards, refer to DS802 Data Sheet (PHS Bus System Hardware Reference 🕮).

Connection to external devices

There are two different ways to connect external devices to the DS4001. To access the I/O units of the DS4001, connect external devices

- To the 50-pin I/O connector P1 of the DS4001. Refer to I/O Connector (P1) (PHS Bus System Hardware Reference 🕮).

- To the optional connector panel CP4001 or the additional LED panel LP4001. Refer to CP4001 Components (PHS Bus System Hardware Reference 🕮) and LP4001 Components (PHS Bus System Hardware Reference 🕮).

Related topics

Basics

Digital I/O Unit

Where to go from here

Information in this section

Basics of the Digital I/O Unit

Introduction

The DS4001 provides a digital I/O unit.

Characteristics

The DS4001 contains a digital I/O unit with the following characteristics:

- 32 TTL-compatible digital I/O lines
- Direction programmable in 8-bit groups (bits 0 … 7, 8 … 15, 16 … 23, 24 … 31)
- Handshake control lines for acknowledge and ready
- I/O error input line
- Connectors for up to 4 customization modules

Direct and strobed input mode

The four 8-bit groups can be driven in two input modes:

- In the *direct input mode*, the current status of the I/O pins is returned when the data register is read. No additional strobe signal is necessary in this mode.
- In the *strobed input mode*, new data is latched into the digital I/O unit with a strobe signal at the PSTB line. For details, see Strobing Inputs on page 15.

  This mode is not supported by RTI.

The input mode can be selected independently for each group.

Initialization to output direction

If the digital I/O lines are initialized to output direction the output lines can be initialized to either high or low.

Specifying output on termination

With RTI, you can specify the termination output values:

- By default, all digital I/O lines hold their last digital output values.
- You can specify a user-defined value, to which the output lines are set on termination. It is selectable for each digital I/O line.

With RTLib, specifying termination states is not supported by default. If you want to specify termination states using RTLib you have to explicitly define such a function using C code.

Note

If you stop an application via the Stop RTP command of ControlDesk, the termination code will not be executed and the I/O will not output the termination values of the application. Instead, undefined values are output.

Customizing signals

With the DS4001, you can customize signals. Other signal levels than TTL can be achieved by inserting a customization module that you design for your needs. Up to 4 customization modules can be connected to the 32 digital I/O lines, each to an 8-bit group.

For more information on designing your customization module, refer to Customization Modules (PHS Bus System Hardware Reference 🕮).

Interrupt handling

The digital I/O unit provides a strobe interrupt. Refer to Strobe Interrupt on page 30.

Power-up state

On power-up of the DS4001, the direction of the digital I/O lines is set to input and the *direct input mode* is selected.

The digital I/O lines are set to the logical high level by built-in 10 kΩ pull-up resistors.

RTI/RTLib support

You can access the digital I/O unit via DS4001 Blockset and RTLib. Refer to

- RTI blockset: Digital I/O Unit (DS4001 RTI Reference 🕮)
- RTLib functions: Digital I/O Unit (DS4001 RTLib Reference 🕮)

Execution times

The execution times required by the RTLib functions have been measured. For details on the results and the corresponding measurement setup, refer to Function Execution Times (DS4001 RTLib Reference 🕮).

Connecting external devices

An excerpt from the circuit diagram that shows the I/O circuit and information on the electrical characteristics of the digital I/O unit are available. You can also get information on signal conditioning and the handshake lines. Refer to Signal Connection to External Devices (PHS Bus System Hardware Reference 🕮).

I/O mapping

The following table shows the mapping between the RTI blocks and RTLib functions and the corresponding pins used by the digital I/O unit.

Related RTI Block	Ch (RTI)	Related RTLib Functions	Ch (RTLib)	Conn. Pin	Pin on CP	Signal

`DS4001IN_Bx_Gy/`
`DS4001IN8_Bx_Gy/`
`DS4001OUT_Bx_Gy/`
	Bit 0	Digital I/O Unit	Bit 0	P1 1	CP1 1	IO0

	Bit 1		Bit 1	P1 34	CP1 18	IO1
	Bit 2		Bit 2	P1 18	CP1 2	IO2

Related RTI Block	Ch (RTI)	Related RTLib Functions	Ch (RTLib)	Conn. Pin	Pin on CP	Signal
DS4001OUT8_Bx_Gy	Bit 3		Bit 3	P1 2	CP1 19	IO3
	Bit 4		Bit 4	P1 35	CP1 3	IO4
	Bit 5		Bit 5	P1 19	CP1 20	IO5
	Bit 6		Bit 6	P1 3	CP1 4	IO6
	Bit 7		Bit 7	P1 36	CP1 21	IO7
	Bit 8		Bit 8	P1 20	CP1 5	IO8
	Bit 9		Bit 9	P1 4	CP1 22	IO9
	Bit 10		Bit 10	P1 37	CP1 6	IO10
	Bit 11		Bit 11	P1 21	CP1 23	IO11
	Bit 12		Bit 12	P1 5	CP11 7	IO12
	Bit 13		Bit 13	P1 38	CP1 24	IO13
	Bit 14		Bit 14	P1 22	CP1 8	IO14
	Bit 15		Bit 15	P1 6	CP1 25	IO15
	Bit 16		Bit 16	P1 39	CP1 9	IO16
	Bit 17		Bit 17	P1 23	CP1 26	IO17
	Bit 18		Bit 18	P1 7	CP1 10	IO18
	Bit 19		Bit 19	P1 40	CP1 27	IO19
	Bit 20		Bit 20	P1 24	CP1 11	IO20
	Bit 21		Bit 21	P1 8	CP1 28	IO21
	Bit 22		Bit 22	P1 41	CP1 12	IO22
	Bit 23		Bit 23	P1 25	CP1 29	IO23
	Bit 24		Bit 24	P1 9	CP1 13	IO24
	Bit 25		Bit 25	P1 42	CP1 30	IO25
	Bit 26		Bit 26	P1 26	CP1 14	IO26
	Bit 27		Bit 27	P1 10	CP1 31	IO27
	Bit 28		Bit 28	P1 43	CP1 15	IO28
	Bit 29		Bit 29	P1 27	CP1 32	IO29
	Bit 30		Bit 30	P1 11	CP1 16	IO30
	Bit 31		Bit 31	P1 44	CP1 33	IO31

Related topics

References

Digital I/O Unit (DS4001 RTLib Reference 🕮)
DS4001IN_Bx_Gy (DS4001 RTI Reference 🕮)
DS4001IN8_Bx_Gy (DS4001 RTI Reference 🕮)
DS4001OUT_Bx_Gy (DS4001 RTI Reference 🕮)
DS4001OUT8_Bx_Gy (DS4001 RTI Reference 🕮)
Signal Connection to External Devices (PHS Bus System Hardware Reference 🕮)
Stop RTP (ControlDesk Platform Management 🕮)

Strobing Inputs

Introduction

The four 8-bit groups of the digital I/O unit can be used in the *strobed input mode*. In this case, new data is latched into the digital I/O unit with a strobe signal.

The *strobed input mode* is not supported by RTI.

PSTB signal

The strobe signal must be connected to the PSTB line. Input data is latched with the rising edge of the strobe signal.

Before the rising edge, the strobe signal must be low for at least 100 ns. After the rising edge, the strobe signal must be high for at least 50 ns.

Tip

The PSTB input can also be used as an external interrupt source. PSTB issues an interrupt to the processor board. Refer to Strobe Interrupt on page 30.

I/O mapping

The following table shows the mapping between the RTLib functions and the corresponding pin used by the PSTB line:

Related RTLib Functions	Ch/Bit (RTLib)	Conn. Pin	Pin on CP	Signal
`ds4001_pio_init` and `ds4001_pio_initialize`	–	P1 28	CP1 35	PSTB

Related topics

Basics

Introduction to the Features of the DS4001 7

References

ds4001_pio_init (DS4001 RTLib Reference 🕮)
ds4001_pio_initialize (DS4001 RTLib Reference 🕮)

Handshaking with External Devices

Introduction

The DS4001 provides two output signals that acknowledge that data was written to or read from the digital I/O unit successfully.

PRDY handshake line

When data was written to the digital I/O unit, this is indicated by a 1 µs low pulse at the PRDY handshake line.

PACK handshake line

When data was read from the digital I/O unit, this is indicated by a 1 µs low pulse at the PACK handshake line.

Output pins for the handshake lines

The following table shows the pins used by the handshake lines:

Connector Pin	Pin on CP	Signal
P1 45	CP1 37	$\overline{\text{PACK}}$
P1 12	CP1 39	$\overline{\text{PRDY}}$

Related topics

Basics

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I/O Error Requesting

Introduction

The PHS bus that connects I/O boards to the processor board contains an I/O error line.

I/O errors

The DS4001 is able to detect I/O errors and activate the I/O error line.

Other error situations that may lead to erroneous I/O signals can be detected by external devices. Errors that are detected by external devices can be signaled to the system via the DS4001 I/O error input line (PIOERR).

Activating the PHS-bus I/O error line

The DS4001 provides an I/O error input line called PIOERR. If the PIOERR signal is set to low level, the DS4001 activates the I/O error line of the PHS bus to indicate that an I/O error occurred. The I/O error line of the PHS bus remains in the active state, even if the PIOERR signal is no longer low. The I/O error line of the bus can be released by using the `ds4001_read_status` function, if PIOERR is no longer active (not on low level).

This function is not supported by RTI. You have to implement an S-function for using the functionality.

I/O mapping

The following table shows the mapping between the RTLib functions and the corresponding pins used for I/O error requesting:

Related RTLib Functions	Ch (RTLib)	Conn. Pin	Pin on CP	Signal
`ds4001_read_status`	–	P1 29	CP1 41	$\overline{\text{PIOERR}}$

Related topics

Basics

Introduction to the Features of the DS4001 7

References

ds4001_read_status (DS4001 RTLib Reference 🕮)

Timing I/O Unit

Introduction

The DS4001 offers a timing I/O unit that you can use to generate signals and measure timings.

Where to go from here

Information in this section

Basics of the Timing I/O Unit

Introduction

The DS4001 offers a timing I/O unit that you can use to generate signals and measure timings. It has the following characteristics:

- 5 separately programmable 16-bit timers with one timing I/O channel (TTL) each
- 5 MHz time base, 200 ns resolution for each timer

Signal generation

The timing I/O unit of the DS4001 can be used to generate two types of digital signals:

- Pulse-width modulated (PWM) signals
- Square-wave signals

Limitations

There are some limitations when you work with the timing I/O unit. Refer to Limitations on page 35.

Related topics

Basics

Introduction to the Features of the DS4001 7

References

Signal Connection to External Devices (PHS Bus System Hardware Reference 🕮)

PWM Signal Generation

Introduction

PWM signal generation is crucial to many engine and motion control applications. PWM signals are pulse trains with variable frequency and pulse-width.

PWM signal

The width of the pulses changes according to a modulating signal. When a PWM signal is applied to the gate of a power transistor, it causes the turn-on/turn-off intervals of the transistor to change according to the modulating signal. The frequency of a PWM signal is usually much higher than that of the modulating signal, so that the energy delivered to the motor and its load depends mainly on the modulating signal.

The timing I/O unit of the DS4001 provides outputs for 1-phase PWM signal generation on up to 4 channels.

Note

Channel 5 is used to generate the PWM period common to all PWM channels. The output of timer 5 (TMROUT5) must be connected to the gate inputs (TMRGS1 … TMRGS4) of the timers to be used for PWM generation. Thus only timers 1 … 4 are available for PWM generation.

PWM period

You can set the PWM period T_p (= T_{high} + T_{low}) in common to all PWM channels by specifying the frequency:

- The minimum PWM period T_{p_min} corresponds to the absolute maximum frequency value 833.33 kHz.
- The maximum PWM period T_{p_max} corresponds to the absolute minimum frequency value 7.63 mHz.

The PWM period T_p starts with the rising edge of the signal.

Because channel 5 is used as the common clock generator all four channels have the same PWM period T_p and are always synchronous.

The PWM period T_p cannot be changed during run time.

Frequency ranges

The possible values for the frequency depend on the frequency range you select. There are five valid frequency ranges for PWM signal generation. Each range corresponds to one of the frequency prescalers F1 … F5:

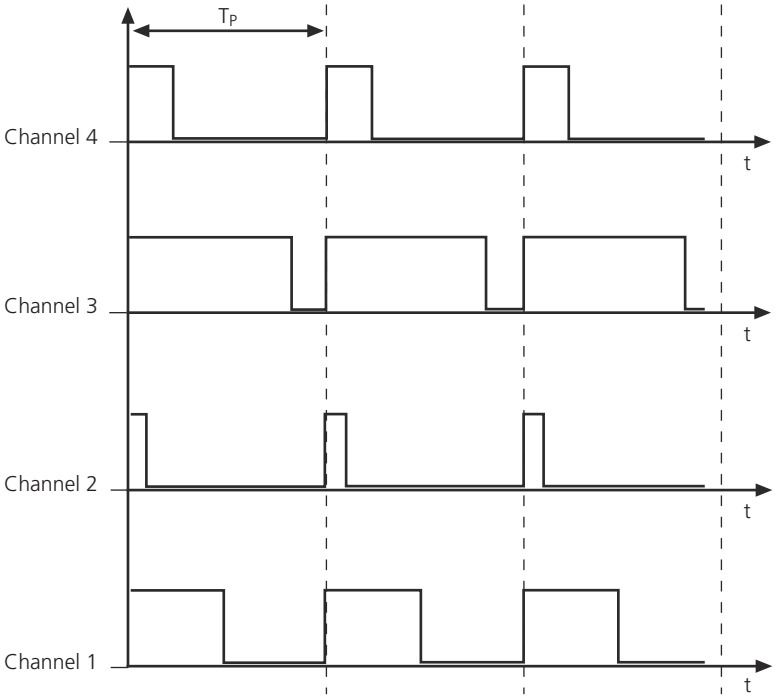
Range Number	Prescaler	Min. Frequency	Max. Frequency
1	F1	76.3 Hz	833.3 kHz
2	F2	7.63 Hz	83.33 kHz
3	F3	763 mHz	8.333 kHz
4	F4	76.3 mHz	833.3 Hz
5	F5	7.63 mHz	83.33 Hz

Note

To optimize the resolution of the generated PWM signal, you should always choose the frequency range with the lowest possible range number.
For example, if your desired PWM frequency is 81 kHz, you should use frequency range 1 (76.3 Hz … 833.3 kHz) rather than frequency range 2.

Duty cycle

You can specify the duty cycle during run time. The following illustration shows how the duty cycle d (= T_{high}/T_p) is defined. The available duty cycle range is 0 … 1 (0 … 100%).



When the duty cycle d is changed during run time, the new value becomes effective with the next PWM period, beginning with the rising edge.

Note

- Due to quantization effects, you will encounter considerable deviations between the desired PWM period T_p and the generated PWM period, especially for high PWM frequencies. Refer to Quantization Effects on page 36.
- Due to technical restrictions, the DS4001 does not exactly generate a duty cycle of 0% or 100%. For a duty cycle of 0%, there remains a high pulse that depends on the frequency range used. For a duty cycle of 100%, there remains a low pulse that also depends on the frequency range used.

Remaining high and low pulses

The following table shows the remaining high and low pulses:

Range Number	Remaining High Pulse at 0%	Remaining Low Pulse at 100%
1	0.4 µs	0.6 µs
2	4 µs	6 µs
3	40 µs	60 µs
4	400 µs	600 µs
5	4 ms	6 ms

Inverted PWM signal

On the DS4001, you can select inverse PWM generation via RTLib. The generated signal is inverted before it is output.

Interrupt via PWM signal generation

When you perform PWM signal generation, you can enable interrupt generation. Each timer provides an interrupt. The interrupt is generated on the rising edge of the PWM signal. Refer to Timer Interrupts on page 31.

Note

The PWM signals generated by the DS4001 are synchronous. Interrupts are generated on the rising edge. Therefore it is recommended to enable interrupt generation via PWM signal generation on one channel only.

RTI/RTLib support

You can perform PWM signal generation via DS4001 Blockset and RTLib. Refer to

- RTI blockset: DS4001PWM_Bx (DS4001 RTI Reference 🕮)
- RTLib functions: PWM Signal Generation (DS4001 RTLib Reference 🕮)

Execution times

The execution times required by the RTLib functions have been measured. For details on the results and the corresponding measurement setup, refer to Function Execution Times (DS4001 RTLib Reference 🕮).

Connecting external devices

For an excerpt from the circuit diagram that shows the I/O circuit and for information on the electrical characteristics and signal conditioning of the timing I/O unit, refer to Signal Connection to External Devices (PHS Bus System Hardware Reference 🕮).

I/O mapping

The following table shows the mapping between the RTI block and the RTLib functions and the corresponding pins used to provide PWM signals.

PWM signal generation conflicts with other I/O features of the DS4001. For details, see Limitations on page 35.

Related RTI Blocks	Ch (RTI)	Related RTLib functions	Ch (RTLib)	Conn. Pin	Pin on CP	Signal
DS4001PWM_Bx	Ch 1	See PWM Signal Generation (DS4001 RTLib Reference 🕮)	Ch 1	P1 14 P1 32	CP2 2 CP2 8	TMROUT1 TMRGS1
	Ch 2		Ch 2	P1 47 P1 49	CP2 3 CP2 9	TMROUT2 TMRGS2
	Ch 3		Ch 3	P1 31 P1 16	CP2 4 CP2 10	TMROUT3 TMRGS3
	Ch 4		Ch 4	P1 48 P1 33	CP2 5 CP2 11	TMROUT4 TMRGS4
	Ch 1 … Ch 4		Ch 1 … Ch 4	P1 15	CP2 6	TMROUT5

Note

Channel 5 is used to generate the PWM period common to all PWM channels. The output of timer 5 (TMROUT5) must be connected to the gate inputs (TMRGS1 … TMRGS4) of the timers to be used for PWM generation. Thus only timers 1 … 4 are available for PWM generation.

Related topics

References

DS4001PWM_Bx (DS4001 RTI Reference 🕮)
PWM Signal Generation (DS4001 RTLib Reference 🕮)
Timing I/O Unit 19

Square-Wave Signal Generation (D2F)

Introduction

Using the timing I/O unit of the DS4001 to generate square-wave signals with variable frequencies, you can use up to 5 channels for signal generation.

Frequency range

For square-wave signal generation (D2F) on the DS4001, you can specify the frequency f_{D2F} for each channel separately in one of the following ranges:

Range Number	Prescaler	Min. Frequency	Max. Frequency
1	F1	38.15 Hz	1.25 MHz
2	F2	3.815 Hz	125 kHz
3	F3	381.5 mHz	12.5 kHz

Range Number	Prescaler	Min. Frequency	Max. Frequency
4	F4	38.15 mHz	1.25 kHz
5	F5	3.815 mHz	125 Hz

Note

To optimize the resolution of the generated square-wave signal, you should always choose the frequency range with the lowest possible range number. For example, if your desired frequency is 100 kHz, you should use frequency range 1 (38.15 Hz … 1.25 MHz) rather than frequency range 2.

The frequency f_{D2F} can be changed during run time.

Interrupt via D2F signal generation

When you perform square-wave signal generation, you can enable interrupt generation. Each timer provides an interrupt. The interrupt is generated on the rising edge of the square-wave signal. Refer to Timer Interrupts on page 31.

RTI/RTLib support

You can perform square-wave signal generation via DS4001 Blockset and RTLib. Refer to

- RTI blockset: DS4001D2F_Bx_Cy (DS4001 RTI Reference 🕮)
- RTLib functions: Square-Wave Signal Generation (D2F) (DS4001 RTLib Reference 🕮)

Execution times

The execution times required by the RTLib functions have been measured. For details on the results and the corresponding measurement setup, refer to Function Execution Times (DS4001 RTLib Reference 🕮).

Connecting external devices

For an excerpt from the circuit diagram that shows the I/O circuit and for information on the electrical characteristics and signal conditioning of the timing I/O unit, refer to Signal Connection to External Devices (PHS Bus System Hardware Reference 🕮).

I/O mapping

The following table shows the mapping between the RTI block and RTLib functions and the corresponding pins used to provide square-wave signal generation.

Square-wave signal generation (D2F) conflicts with other I/O features of the DS4001. Refer to Limitations on page 35.

Related RTI Block	Ch (RTI)	Related RTLib Functions	CH (RTLib)	Conn. Pin	Pin on CP	Signal
DS4001D2F_Bx_Cy	Ch 1	See Square-Wave Signal Generation (D2F) (DS4001 RTLib Reference 🕮)	Ch 1	P1 14	CP2 2	TMROUT1
	Ch 2		Ch 2	P1 47	CP2 3	TMROUT2
	Ch 3		Ch 3	P1 31	CP2 4	TMROUT3
	Ch 4		Ch 4	P1 48	CP2 5	TMROUT4
	Ch 5		Ch 5	P1 15	CP2 6	TMROUT5

Related topics

References

DS4001D2F_Bx_Cy (DS4001 RTI Reference 🕮)
Square-Wave Signal Generation (D2F) (DS4001 RTLib Reference 🕮)
Timing I/O Unit 19

Square-Wave Signal Measurement (F2D)

Introduction

The timing I/O unit of the DS4001 provides inputs to measure the frequency of a square-wave signal on up to 5 channels.

Frequency ranges

You can measure frequencies within the range 7.63 Hz … 1.67 MHz.

The maximum frequency value to be measured depends on the range used.

Range Number	Prescaler	Min. Frequency	Max. Frequency
1	F1	76.3 Hz	1.67 MHz
2	F2	7.63 Hz	167 kHz
3	F3	763 mHz	16.7 kHz
4	F4	76.3 mHz	1.67 kHz
5	F5	7.63 mHz	167 Hz

Note

To optimize the resolution of the frequency measurement, you should always choose the frequency range with the lowest possible range number. For example, if the frequency to be measured is 100 kHz, you should use frequency range 1 (76.3 Hz … 1.67 MHz) rather than frequency range 2.

RTI/RTLib support

You can perform square-wave signal measurement via DS4001 blockset and RTLib. Refer to

- RTI blockset: DS4001F2D_Bx_Cy (DS4001 RTI Reference 🕮)
- RTLib functions: Square-Wave Signal Measurement (F2D) (DS4001 RTLib Reference 🕮)

Execution times

The execution times required by the RTLib functions and RTI blocks have been measured. For details on the results and the corresponding measurement setup, refer to Function Execution Times (DS4001 RTLib Reference 🕮).

Connecting external devices

An excerpt from the circuit diagram that shows the I/O circuit and information on the electrical characteristics are available. You can also get information on signal conditioning of the timing I/O unit. Refer to Signal Connection to External Devices (PHS Bus System Hardware Reference 🕮).

I/O mapping

The following table shows the mapping between the RTI block and the RTLib functions and the corresponding pins used for square-wave signal measurement.

Square-wave signal measurement (F2D) conflicts with other I/O features of the DS4001. Refer to Limitations on page 35.

Related RTI Block	Ch (RTI)	Related RTLib Functions	Ch (RTLib)	Conn. Pin	Pin on CP	Signal
DS4001F2D_Bx_Cy	Ch 1	See Square-Wave Signal Measurement (F2D) (DS4001 RTLib Reference 🕮)	Ch 1	P1 32	CP2 8	TMRGS1
	Ch 2		Ch 2	P1 49	CP2 9	TMRGS2
	Ch 3		Ch 3	P1 16	CP2 10	TMRGS3
	Ch 4		Ch 4	P1 33	CP2 11	TMRGS4
	Ch 5		Ch 5	P1 50	CP2 12	TMRGS5

Related topics

References

DS4001F2D_Bx_Cy (DS4001 RTI Reference 🕮)
Square-Wave Signal Measurement (F2D) (DS4001 RTLib Reference 🕮)
Timing I/O Unit 19

Interrupts Provided by the DS4001

Introduction

The DS4001 provides access to 8 hardware interrupts.

Where to go from here

Information in this section

Basics of the DS4001 Interrupts

Interrupts

The DS4001 provides access to 8 hardware interrupts including a PSTB interrupt from the digital I/O unit, 5 timer interrupts from the timing I/O unit and 2 user interrupts:

Interrupt Type	Description
PIO strobe interrupt	The PSTB input can be used as an external interrupt source.
Timer interrupt 1 … 5	During signal generation, interrupts can be triggered by the corresponding timer outputs TMROUT.

Interrupt Type	Description
	As an alternative, TMROUT can be configured as an external interrupt input if the corresponding timer is not used for signal generation.
User interrupt 1 … 2	Interrupt defined by the user. The user interrupts are triggered by an external signal and can be used freely.

Interrupt processing

Via the interrupt lines of the PHS bus, interrupts from the DS4001 are sent to the interrupt controller of the connected dSPACE processor board. Using RTI, the interrupts of the DS4001 can therefore be used to implement interrupt-driven tasks. Refer to Tasks Driven by Interrupt Blocks (RTI and RTI-MP Implementation Guide 🕮).

Strobe Interrupt

Introduction

The DS4001 provides a strobe interrupt. The PSTB input can be used as an additional external interrupt source.

Basics

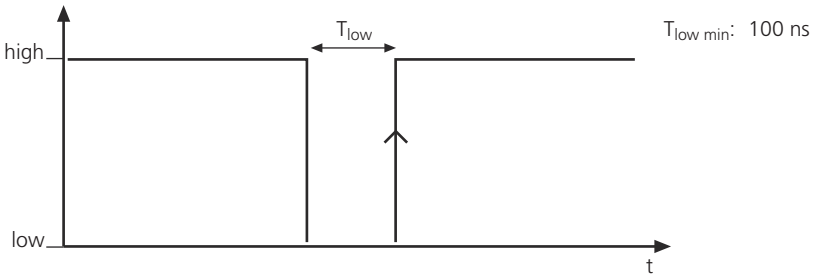
The strobe interrupt is independent of the *strobed input mode* or the *direct input mode*. For more information on the *input modes*, refer to Direct and strobed input mode on page 12.

Timing requirements

The strobe interrupt is triggered at the rising edge of the corresponding external signal.

The interrupt signal should be high all the time, and it should be set to low for approximately 100 ns before the interrupt, so that the interrupt is triggered by the rising edge of the signal.

The following illustration shows the timing of the strobe interrupt:



I/O mapping

The following table shows the mapping between the RTI block and the RTLib functions and the corresponding pin used by the PSTB line:

Related RTI Block	Int (RTI)	Related RTLib Functions	Int (RTLib)	Conn. Pin	Pin on CP	Signal
DS4001_HWINT_Bx_Iy	Strobe int	ds4001_set_int_input (DS4001 RTLib Reference 🕮) and refer to PHS-Bus Interrupt Handling (DS1006 RTLib Reference 🕮) (DS1006) or PHS-Bus Interrupt Handling (DS1007 RTLib Reference 🕮) (DS1007)	–	P1 28	CP1 35	$\overline{\text{PSTB}}$

Related topics

Basics

Introduction to the Features of the DS4001 7
Strobing Inputs 15

References

DS4001_HWINT_Bx_Iy (DS4001 RTI Reference 🕮)

Timer Interrupts

Introduction

The DS4001 contains 5 timers allowing up to 5 independent timer interrupts. Each of the timers may issue interrupts to the processor board via the interrupt control unit of the DS4001.

Two different kinds of timer interrupts are possible: signal generation interrupts or external interrupt inputs. They cannot be used at the same time on the same channel.

Signal generation interrupt

If you perform PWM or D2F signal generation, interrupts can be generated on the rising edge of the corresponding TMROUT signal.

Note

The PWM signals generated by the DS4001 are synchronous. Interrupts are generated on the rising edge. Therefore it is recommended to enable interrupt generation via PWM signal generation on one channel only.

TMROUT as external interrupt input

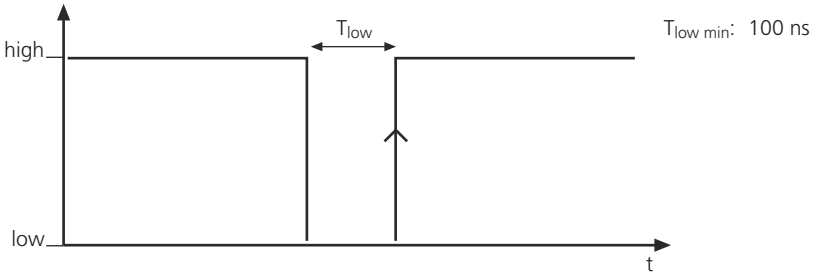
If the timer is not in use for signal generation or measurement the timer output can be used as an external interrupt input.

For external interrupt inputs, the signal must remain high until the processor has recognized the interrupt.

Therefore the interrupt signal should be high all the time, and it should be set to low for approximately 100 ns before the interrupt, so that the interrupt is triggered by the rising edge of the signal.

With RTLib, you have to use the `ds4001_set_int_input` function to use the TMROUT signal as external interrupt input.

The following illustration shows the timing of the timer interrupt:



RTI/RTLib support

For information on how to access the timer interrupts, refer to

- RTI blockset: DS4001_HWINT_Bx_Iy (DS4001 RTI Reference 🕮)
- RTLib functions: ds4001_set_int_input (DS4001 RTLib Reference 🕮) (only if TMROUT is used as external interrupt input)

I/O mapping

The following table shows the mapping between the RTI block and the RTLib functions and the corresponding pins used for handling the timer interrupts:

Related RTI Block	Int (RTI)	Related RTLib Functions	Int (RTLib)	Conn. Pin	Pin on CP	Signal
DS4001_HWINT_Bx_Iy	Timer int 1	See ds4001_set_int_input (DS4001 RTLib Reference 🕮)[1] and PHS-Bus Interrupt Handling (DS1006 RTLib Reference 🕮), or PHS-Bus Interrupt Handling (DS1007 RTLib Reference 🕮)	–	P1 14	CP2 2	TMROUT1
	Timer int 2		–	P1 47	CP2 3	TMROUT2
	Timer int 3		–	P1 31	CP2 4	TMROUT3
	Timer int 4		–	P1 48	CP2 5	TMROUT4
	Timer int 5		–	P1 15	CP2 6	TMROUT5

[1] Only if TMROUT is used as external interrupt input

Related topics

Basics

Introduction to the Features of the DS4001 7

References

DS4001_HWINT_Bx_Iy (DS4001 RTI Reference 🕮)

User Interrupts

Introduction

The DS4001 provides two user interrupts that you can use as trigger sources in a real-time application. The user interrupt sources have to be connected externally to the DS4001.

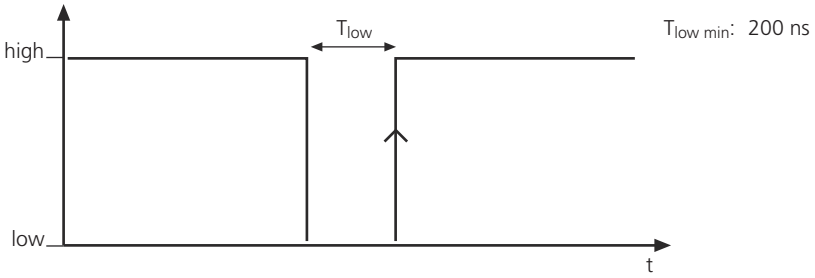
The PSTB input can be used as an additional external interrupt source for the user interrupt, but only if the *direct input mode* is used.

Timing requirements

User interrupts are triggered at the rising edge of the corresponding external signal.

The interrupt signal should be high all the time, and it should be set to low for approximately 200 ns before the interrupt, so that the interrupt is triggered by the rising edge of the signal.

The following illustration shows the timing of the interrupt.



RTI/RTLib support

For information on how to access the user interrupts, refer to DS4001_HWINT_Bx_Iy (DS4001 RTI Reference 🕮).

I/O mapping

The following table shows the mapping between the RTI block and the RTLib functions and the corresponding pins used for handling the user interrupts.

Related RTI Block	Int (RTI)	Related RTLib Functions	Int (RTLib)	Conn. Pin	Pin on CP	Signal
DS4001_HWINT_Bx_Iy	User int 1	See ds4001_set_int_input (DS4001 RTLib Reference 🕮) and PHS-Bus Interrupt Handling (DS1006 RTLib Reference 🕮), or PHS-Bus Interrupt Handling (DS1007 RTLib Reference 🕮)	–	P1 46	CP2 43	IRQ1
	User int 2		–	P1 13	CP2 45	IRQ2

Related topics

Basics

Introduction to the Features of the DS4001 7

References

DS4001_HWINT_Bx_Iy (DS4001 RTI Reference 🕮)

Limitations

Introduction

There are some limitations you have to take into account when working with the DS4001.

Where to go from here

Information in this section

Information in other sections

Quantization Effects

Introduction

Signal generation and measurement are only feasible within the limits of the DS4001's time base, which causes quantization errors that increase with increasing frequencies.

When performing square-wave signal generation, for example, you will encounter considerable deviations between the desired frequency $f_{desired}$ and the generated frequency $f_{generated}$, especially for higher frequencies. The (quantized) generated signal frequencies can be calculated according to the following equation:

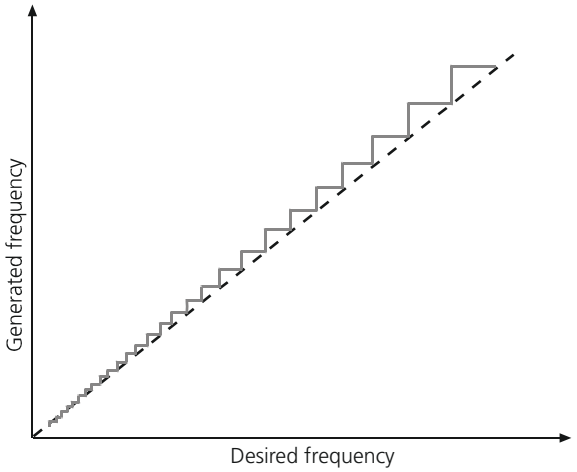
$$f_{generated} = 1/(n \cdot R)$$

where R is the time base (in seconds), and n is the integer part of $(1/(f_{desired} \cdot R))$.

Example

Suppose you want to generate a D2F signal with $f_{desired}$ = 130 kHz. Calculating the integer part of (1/(130 kHz · 200 ns)) yields n = 38. According to $f_{generated}$ = 1/(n · R), the generated frequency is 131.58 kHz.

The following illustration shows the increasing quantization effect for increasing desired frequencies:



Conflicting I/O Features

Conflicts for the DS4001

The following I/O features of the DS4001 conflict with other I/O features:

- Conflicts for PWM Signal Generation on page 37
- Conflicts for Square-Wave Signal Generation (D2F) on page 37
- Conflicts for Square-Wave Signal Measurement (F2D) on page 38

Conflicts for PWM Signal Generation

The following I/O features of the DS4001 conflict with PWM Signal Generation:

PWM Signal Generation *)		Signal	Conflicting I/O Feature **)		
Ch (RTI)	**Ch (RTLib)**			**Ch (RTI)**	**Ch (RTLib)**
Conflicts Concerning Single Channels					
Ch 1	Ch 1	TMROUT1	▪ D2F, F2D	▪ Ch 1	▪ Ch 1
			▪ External Interrupts	▪ Timer Int 1	▪ Timer Int 1
		TMRGS1	D2F, F2D	Ch 1	Ch 1
Ch 2	Ch 2	TMROUT2	▪ D2F, F2D	▪ Ch 2	▪ Ch 2
			▪ External Interrupts	▪ Timer Int 2	▪ Timer Int 2
		TMRGS2	D2F, F2D	Ch 2	Ch 2
Ch 3	Ch 3	TMROUT3	▪ D2F, F2D	▪ Ch 3	▪ Ch 3
			▪ External Interrupts	▪ Timer Int 3	▪ Timer Int 3
		TMRGS3	D2F, F2D	Ch 3	Ch 3
Ch 4	Ch 4	TMROUT4	▪ D2F, F2D	▪ Ch 4	▪ Ch 4
			▪ External Interrupts	▪ Timer Int 4	▪ Timer Int 4
		TMRGS4	D2F, F2D	Ch 4	Ch 4
Ch 1 … Ch 4	Ch 1 … Ch 4	TMROUT5	▪ D2F, F2D	▪ Ch 5	▪ Ch 5
			▪ External Interrupts	▪ Timer Int 5	▪ Timer Int 5
*) Related RTI blocks and RTLib functions: ▪ *DS4001PWM_Bx (DS4001 RTI Reference 🕮)* ▪ See *PWM Signal Generation (DS4001 RTLib Reference 🕮)*			**) Related RTI blocks and RTLib functions: ▪ D2F: ▪ *DS4001D2F_Bx_Cy (DS4001 RTI Reference 🕮)* ▪ See *Square-Wave Signal Generation (D2F) (DS4001 RTLib Reference 🕮)* ▪ F2D: ▪ *DS4001F2D_Bx_Cy (DS4001 RTI Reference 🕮)* ▪ See *Square-Wave Signal Measurement (F2D) (DS4001 RTLib Reference 🕮)* ▪ External Interrupts: ▪ *DS4001_HWINT_Bx_Iy (DS4001 RTI Reference 🕮)* ▪ See *ds4001_set_int_input (DS4001 RTLib Reference 🕮)*		

Conflicts for Square-Wave Signal Generation (D2F)

The following I/O features of the DS4001 conflict with Square-Wave Signal Generation:

Square-Wave Signal Generation *)		Signal	Conflicting I/O Feature **)		
Ch (RTI)	**Ch (RTLib)**			**Ch (RTI)**	**Ch (RTLib)**
Conflicts Concerning Single Channels					
Ch 1	Ch 1	TMROUT1	▪ PWM, F2D	▪ Ch 1	▪ Ch 1
			▪ External Interrupts	▪ Timer Int 1	▪ Timer Int 1
Ch 2	Ch 2	TMROUT2	▪ PWM, F2D	▪ Ch 2	▪ Ch 2
			▪ External Interrupts	▪ Timer Int 2	▪ Timer Int 2

Square-Wave Signal Generation *)		Signal	Conflicting I/O Feature **)		
Ch (RTI)	**Ch (RTLib)**			**Ch (RTI)**	**Ch (RTLib)**
Ch 3	Ch 3	TMROUT3	▪ PWM, F2D ▪ External Interrupts	▪ Ch 3 ▪ Timer Int 3	▪ Ch 3 ▪ Timer Int 3
Ch 4	Ch 4	TMROUT4	▪ PWM, F2D ▪ External Interrupts	▪ Ch 4 ▪ Timer Int 4	▪ Ch 4 ▪ Timer Int 4
Ch 5	Ch 5	TMROUT5	▪ PWM ▪ F2D ▪ External Interrupts	▪ Any ▪ Ch 5 ▪ Timer Int 5	▪ Any ▪ Ch 5 ▪ Timer Int 5
*) Related RTI blocks and RTLib functions: D2F: ▪ *DS4001D2F_Bx_Cy (DS4001 RTI Reference 🕮)* ▪ See *Square-Wave Signal Generation (D2F) (DS4001 RTLib Reference 🕮)*			**) Related RTI blocks and RTLib functions: ▪ PWM: ▪ *DS4001PWM_Bx (DS4001 RTI Reference 🕮)* ▪ See *PWM Signal Generation (DS4001 RTLib Reference 🕮)* ▪ F2D: ▪ *DS4001F2D_Bx_Cy (DS4001 RTI Reference 🕮)* ▪ See *Square-Wave Signal Measurement (F2D) (DS4001 RTLib Reference 🕮)* ▪ External Interrupts: ▪ *DS4001_HWINT_Bx_Iy (DS4001 RTI Reference 🕮)* ▪ See *ds4001_set_int_input (DS4001 RTLib Reference 🕮)*		

Conflicts for Square-Wave Signal Measurement (F2D)

The following I/O features of the DS4001 conflict with Square-Wave Signal Measurement:

Square-Wave Signal Measurement *)		Signal	Conflicting I/O Feature **)		
Ch (RTI)	**Ch (RTLib)**			**Ch (RTI)**	**Ch (RTLib)**
Conflicts Concerning Single Channels					
Ch 1	Ch 1	TMRGS1	▪ PWM, D2F ▪ External Interrupts	▪ Ch 1 ▪ Timer Int 1	▪ Ch 1 ▪ Timer Int 1
Ch 2	Ch 2	TMRGS2	▪ PWM, D2F ▪ External Interrupts	▪ Ch 2 ▪ Timer Int 2	▪ Ch 2 ▪ Timer Int 2
Ch 3	Ch 3	TMRGS3	▪ PWM, D2F ▪ External Interrupts	▪ Ch 3 ▪ Timer Int 3	▪ Ch 3 ▪ Timer Int 3
Ch 4	Ch 4	TMRGS4	▪ PWM, D2F ▪ External Interrupts	▪ Ch 4 ▪ Timer Int 4	▪ Ch 4 ▪ Timer Int 4
Ch 5	Ch 5	TMRGS5	▪ PWM ▪ D2F ▪ External Interrupts	▪ Any ▪ Ch 5 ▪ Timer Int 5	▪ Any ▪ Ch 5 ▪ Timer Int 5
*) Related RTI blocks and RTLib functions: ▪ *DS4001F2D_Bx_Cy (DS4001 RTI Reference 🕮)*			**) Related RTI blocks and RTLib functions: ▪ PWM: ▪ *DS4001PWM_Bx (DS4001 RTI Reference 🕮)*		

Square-Wave Signal Measurement *)		Signal	Conflicting I/O Feature **)		
Ch (RTI)	Ch (RTLib)			Ch (RTI)	Ch (RTLib)
▪ See *Square-Wave Signal Measurement (F2D) (DS4001 RTLib Reference 🕮)*			▪ See *PWM Signal Generation (DS4001 RTLib Reference 🕮)* ▪ D2F: ▪ *DS4001D2F_Bx_Cy (DS4001 RTI Reference 🕮)* ▪ See *Square-Wave Signal Generation (D2F) (DS4001 RTLib Reference 🕮)* ▪ External Interrupts: ▪ *DS4001_HWINT_Bx_Iy (DS4001 RTI Reference 🕮)* ▪ See *ds4001_set_int_input (DS4001 RTLib Reference 🕮)*		