TargetLink

Evaluation Board Reference

For TargetLink 5.1

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dSPACE

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About This Reference

Contents

This reference provides concise information on the various target boards and compilers supported for TargetLink PIL simulation.

Symbols

dSPACE user documentation uses the following symbols:

Symbol	Description
DANGER	Indicates a hazardous situation that, if not avoided, will result in death or serious injury.
WARNING	Indicates a hazardous situation that, if not avoided, could result in death or serious injury.
CAUTION	Indicates a hazardous situation that, if not avoided, could result in minor or moderate injury.
NOTICE	Indicates a hazard that, if not avoided, could result in property damage.
Note	Indicates important information that you should take into account to avoid malfunctions.
Tip	Indicates tips that can make your work easier.
	Indicates a link that refers to a definition in the glossary, which you can find at the end of the document unless stated otherwise.
	Precedes the document title in a link that refers to another document.

Naming conventions

dSPACE user documentation uses the following naming conventions:

%name% Names enclosed in percent signs refer to environment variables for file and path names.

< > Angle brackets contain wildcard characters or placeholders for variable file and path names, etc.

Special folders

Some software products use the following special folders:

Common Program Data folder A standard folder for application-specific configuration data that is used by all users.

```
%PROGRAMDATA%\dSPACE\<InstallationGUID>\<ProductName>
```

or

```
%PROGRAMDATA%\dSPACE\<ProductName>\<VersionNumber>
```

Documents folder A standard folder for user-specific documents.

```
%USERPROFILE%\Documents\dSPACE\<ProductName>\
<VersionNumber>
```

Local Program Data folder A standard folder for application-specific configuration data that is used by the current, non-roaming user.

```
%USERPROFILE%\AppData\Local\dSPACE\<InstallationGUID>\
<ProductName>
```

Accessing dSPACE Help and PDF Files

After you install and decrypt dSPACE software, the documentation for the installed products is available in dSPACE Help and as Adobe® PDF files.

dSPACE Help (local) You can open your local installation of dSPACE Help:

- On its home page via Windows Start Menu
- On specific content using context-sensitive help via **F1**

dSPACE Help (Web) You can access the Web version of dSPACE Help at www.dspace.com.

To access the Web version, you must have a *mydSPACE* account.

PDF files You can access PDF files via the icon in dSPACE Help. The PDF opens on the first page.

Overview of Supported Evaluation Boards

Combinations of Evaluation Boards and Compilers

Overview

TargetLink supports evaluation boards (physical and virtual) that each contain a microcontroller unit (MCU). A microcontroller unit (MCU) consists of a specific processor with additional peripherals, e.g., RAM or AD converters.

Virtual evaluation board A virtual EVB is a combination of an instruction set simulator (ISS) and a simulated periphery.

Physical evaluation board A hardware evaluation board that is equipped with the same target processor as the electronic control unit (ECU).

Target Simulation Module

To perform a PIL simulation on a specific evaluation board, TargetLink requires a suitable compiler. The following table shows the combinations of evaluation boards and compilers included in the Target Simulation Module (TSM). The TSM is licensed separately from the TargetLink Base Suite.

Microcontroller Family	Microcontroller Unit	Evaluation Board	Compiler[1)]	Patch[2)]
ARM Cortex-M3	STMicroelectronics STM32F107	Emerge-Engineering ARM MEDKit	Keil 5.2	.0
ARM Cortex-M3	ARM Cortex M3	Lauterbach Simulator for ARM CortexM3	Keil 5.2	.0
Freescale MPC5700VLE	Freescale MPC5748G	Freescale MPC5748GEVB	Green Hills 2019	.1.4
Freescale MPC5700VLE	Freescale MPC5748G	Freescale MPC5748GEVB	Wind River Diab 5.9	.0
Freescale S12X	Freescale MC9S12XEP100	Freescale EVB9S12XEP100	Cosmic 4.8	.11
Freescale S12X	Freescale MC9S12XEP100	Freescale EVB9S12XEP100	Metrowerks CodeWarrior 5.1	5.0.41 build 10203
Infineon c166	Infineon c167	I+ME Promotion Package 166	Altium TASKING C166/ST10 Toolset 8.6	r1 p3
Infineon TriCore 1-1.3	Infineon TC1766	Infineon TriBoard TriCore 1766	Altium TASKING TriCore VX-Toolset 3.2	r1

Microcontroller Family	Microcontroller Unit	Evaluation Board	Compiler[1)]	Patch[2)]
Infineon TriCore 1-1.3	Infineon TC1766	Infineon TriBoard TriCore 1766 20 MHz	Altium TASKING TriCore VX-Toolset 3.2	r1
Infineon TriCore 1-1.3	Infineon TC1767	Infineon TriBoard TriCore 1767	Altium TASKING TriCore VX-Toolset 3.2	r1
Infineon TriCore 1-1.3	Infineon TC1796	Infineon TriBoard TriCore 1796	Altium TASKING TriCore VX-Toolset 3.2	r1
Infineon TriCore 1-1.6	Infineon TC275	Infineon TriBoard TriCore 275	Altium TASKING TriCore VX-Toolset 6.3	r1
Infineon TriCore 1-1.6	Infineon TC275	Infineon TriBoard TriCore 275	HighTec GNU 4.9	.2
Infineon TriCore 1-1.6	Infineon TC275	Lauterbach Simulator for TriCore 275	Altium TASKING TriCore VX-Toolset 4.2	r2
Infineon XC2000	Infineon XC2287	Infineon EasyKit XC2287	Altium TASKING C166/ST10 VX-Toolset 3.0	r3
Renesas RH850	Renesas RH850/F1L_R7F7010354	Renesas YRH850F1L_R7F7010354	Green Hills 2019	.1.5
Renesas SH-2	Renesas SH-2E/SH7058	Renesas EVB7058	Renesas 9.3	.0
Renesas SH-2	Renesas SH-2A-FPU/SH72513	Renesas SH72513 System Development Kit	Renesas 9.4	.0
Renesas V850E2	Renesas V850E2/Fx4-µPD70F4012	Renesas AB_050_Fx4_70F4012	Green Hills 2019	.1.5
Texas Instruments TMS570	Texas Instruments TMS570LC43	Texas Instruments LAUNCHXL2570LC43	Texas Instruments Code Composer Studio 7.0	.3.0

1) Compiler Suite Version Supported
2) Tested with Compiler Version

Target Simulation Module Extensions

For a full list of all supported evaluation board and compiler combinations, refer to www.dspace.com/go/tlpil. The combinations in the list are free of charge if you have a valid Software Maintenance Service (SMS) contract.

If you do not have a valid SMS contract or are looking for a different combination, contact dSPACE Support or your sales representative.

All Target Simulation Module Extensions will be delivered as TSM Extension Packages and can be installed via the TargetLink Preferences Editor. For more information on the installation, refer to How To Install TSM Extension Packages (📖 TargetLink Customization and Optimization Guide).

Target Simulation Module Extensions require the Target Simulation Module.

Physical Evaluation Boards

Overview

Physical evaluation boards are supported for the following microcontroller units. The list is sorted by microcontroller families and shows only boards included in the Target Simulation Module (TSM).

Tip

For a full list of all supported evaluation board and compiler combinations, refer to www.dspace.com/go/tlpil. The combinations in this list are free of charge if you have a valid Software Maintenance Service (SMS) contract. If you do not have a valid SMS contract or are looking for a different combination, contact dSPACE Support or your sales representative.

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ARM Cortex (STMicroelectronics STM32F107)

Introduction

The evaluation boards that are equipped with STMicroelectronics STM32F107, an ARM Cortex-M3 derivate, microcontrollers, and are supported by the Target Simulation Module (TSM) are described. In addition, the compilers that can be used for these microcontrollers and are supported by TargetLink are described.

TargetLink supports virtual evaluation boards for this microcontroller family. For more information, refer to ARM Cortex (ARM Cortex-M3) on page 92.

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Evaluation Boards

Emerge-Engineering ARM MEDKit

Technical characteristics

The Emerge-Engineering ARM MEDKit evaluation board (MEDKit_ARM) has the following characteristics:

Microcontroller unit The board uses the STM32F107 microcontroller.

On-Chip Memory	Size
FLASH ROM	256 kB
RAM	64 kB

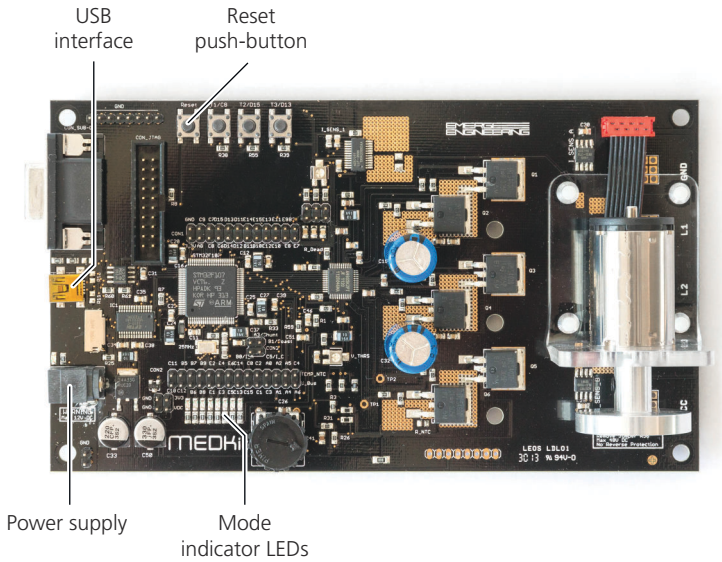
Onboard memory No onboard memory installed.

System clock PIL simulation is performed at 72 MHz.

Interface TargetLink uses the USB interface for program download and PIL simulation.

Important hardware elements

The following illustration shows the Emerge-Engineering ARM MEDKit evaluation board. Only components that are relevant for operating the board or simulating in PIL simulation mode are labeled. These are described in more detail below.



LEDs

Mode indicator LEDs These LEDs indicate the following modes:

- When the board is switched on or reset, the boot loader starts automatically. The six right mode indicator LEDs show a running light.
- When the host PC communicates with the board, the two mode indicator LEDs on the left-hand side flash.
- After a successful download, the boot loader automatically starts the application. The fourth mode indicator LED flashes.

Power

Power supply Connect a plug-in power supply unit (+12 V=) to the power connector.

Reset push-button Resets the evaluation board.

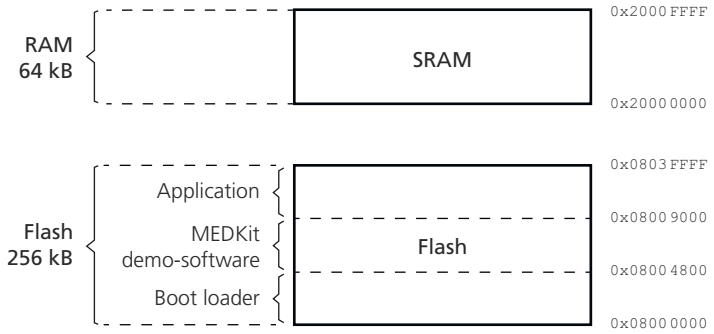
Jumpers and switches

The dip switches must be set as follows:

Dip Switch	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
BOOTCFG	Off	Off	Off	On	—	—	—	—

Memory configuration

The following illustration shows the memory configuration in detail:



Download

Note

Connect the evaluation board to the host PC by using a USB cable.

When you switch on or reset the MEDKit,the boot loader starts automatically. The six mode indicator LEDs on the right-hand side show a running light.

When you download an application for PIL simulation (PIL application), the loader program of the host PC communicates with the loader program of the MEDKit via the USB interface.

1. The memory areas that are not reserved are cleared.
2. The loader of the host PC sends an executable image of the application to the memory areas that are not reserved. The two mode indicator LEDs on the left-hand side flash.
3. After a successful download, the board's loader automatically starts the application. The fourth mode indicator LED flashes.

To check whether board and serial interface work correctly, connect the MEDKit to an ASCII terminal. After reset or power-on, the board sends the following message to the host PC (baud rate of 115,200 bps with 8 data bits, none parity, one stop bit, xon/xoff flow control):

```
TargetLink MEDKit ARM Flashloader (115200 Baud) V1.8.0
a) Erase FLASH
b) Program FLASH
c) Execute Program
d) Verify Program
```

Virtual evaluation board

TargetLink supports a virtual counterpart of this physical evaluation board. For more information, refer to Lauterbach TRACE32 Simulator for ARM Cortex-M3 on page 92.

Compilers

Keil Compiler

Introduction

The various options for the compiler, assembler, and linker that influence the generated code are described. These options are specified in the relevant makefile.

Compiler versions

The following compiler versions are supported:

Emerge-Engineering ARM MEDKit	Keil 5.2

Compiler

This table lists the options used for the compiler:

Option (CC_OPTS)	Result/Description
`--cpu Cortex-M3`	Enables code generation for the selected ARM processor or architecture.
`--fpu=softvfp`	Specifies the target FPU architecture.
`-Ospace`	Instructs the compiler to perform optimizations to reduce image size at the expense of a possible increase in execution time.
`-Onum`	Specifies the level of optimization to be used when compiling source files.

Assembler

This table lists the options used for the assembler:

Option (AS_OPTS)	Result/Description
`--cpu Cortex-M3`	Specifies the target CPU.

Linker

This table lists the options used for the linker:

Option (LD_OPTS)	Result/Description
`--cpu Cortex-M3`	Enables the linker to determine the target ARM processor or architecture.
`--fpu=softvfp`	Specifies the target FPU architecture.

Freescale S12X (Freescale MC9S12XEP100)

Introduction

The evaluation boards that are equipped with Freescale MC9S12XEP100 microcontrollers, and are supported by the Target Simulation Module (TSM) are described. In addition, the compilers that can be used for these microcontrollers and are supported by TargetLink are described.

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Evaluation Boards

Freescale EVB9S12XEP100

Technical characteristics

The Freescale EVB9S12XEP100 evaluation board has the following characteristics:

Microcontroller unit The board uses the MC9S12XEP100 microcontroller.

On-Chip Memory	Size
EEPROM	4 kB
RAM	64 kB
FLASH	1 MB

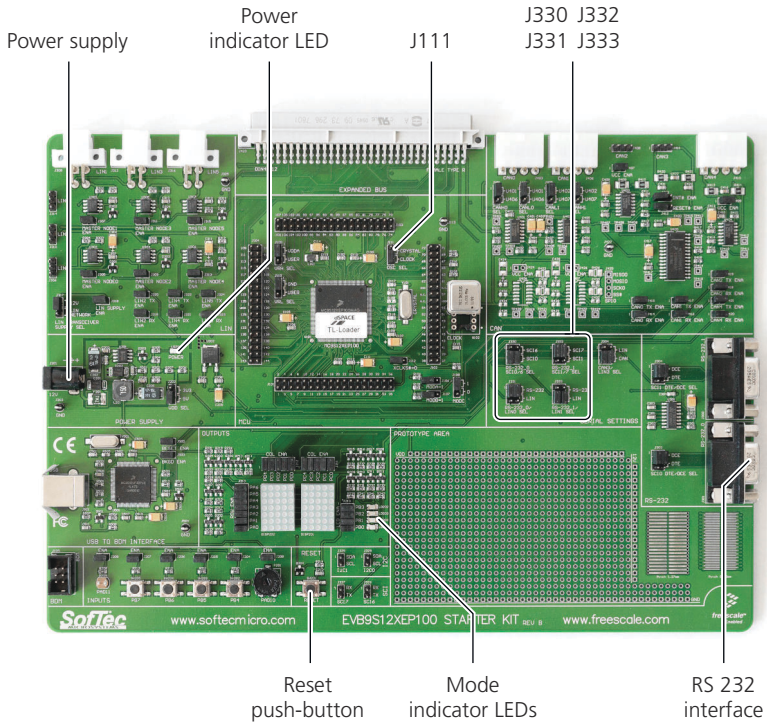
Onboard memory No onboard memory installed.

System clock PIL simulation is performed at 16 MHz.

Interface TargetLink uses the RS232 interface for program download and processor-in-the-loop (PIL) simulation.

Important hardware elements

The following illustration shows the Freescale EVB9S12XEP100. Only components that are relevant for operating the board or simulating in PIL simulation mode are labeled. These are described in more detail below.



LEDs

Power indicator LED After you connect the board to the power supply, the green power indicator LED lights up.

Mode indicator LEDs These LEDs indicate the following modes:

- When the board is switched on or reset, the boot loader starts automatically. One of the mode indicator LEDs lights up when the boot loader is ready.
- After a successful download, the boot loader automatically starts the application. The mode indicator LEDs show a running light.

Power

Power supply Connect a plug-in power supply of +12 V=. After you connect the board to the power supply, the green power indicator LED lights up.

Reset push-button Resets the evaluation board.

Jumpers and switches

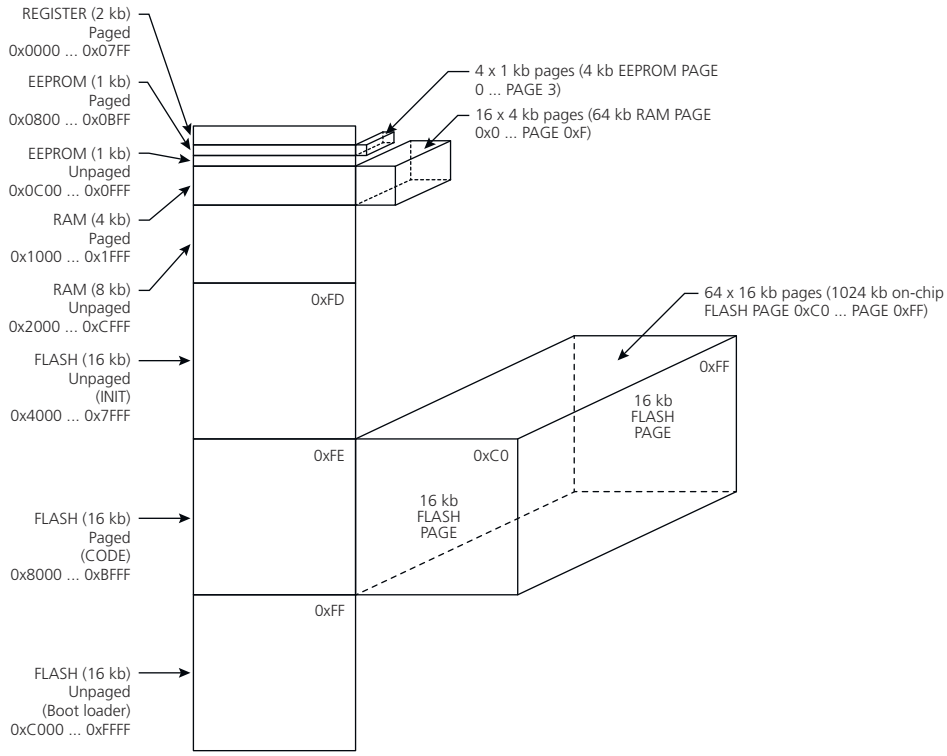
The jumpers must be set as follows (✓ means closed, and – means open):

Jumper	1–2	2–3	Remark
JP 111	–	✓	The 16 MHz oscillator module is used as clock (instead of the 4 MHz crystal)
JP 330	–	✓	The RS232 channel 0 transceiver is connected to the pin 1 and pin 2 of the JP 331.
JP 331	✓	–	The microcontroller's SCI0 peripheral is connected to the RS232_0 transceiver.
JP 332	✓	–	The RS232 channel 1 transceiver is connected to the pin 1 and pin 2 of the JP 333.
JP 333	✓	–	The microcontroller's SCI1 peripheral is connected to the RS232_1 transceiver.

Memory configuration

The Freescale EVB9S12XEP100 is a 16-bit microcontroller with a 16-bit program counter. It can directly address a maximum memory of 64 kB. An 8-bit paging register, however, called PPAGE register, allows more memory to be addressed. The PPAGE register can address a set of 32 pages located in 0x8000-0xBFFF. Each page has a 16 kB memory and a unique PPAGE register value, for example, 0xC0. As an exception, pages 0xFD and 0xFF are also accessible without using the PPAGE register – in 0x4000-0x7FFF and 0xC000-0xFFFF.

The following illustration shows the memory configuration in detail:



Download

Note

Use a serial extension cable to connect the evaluation board to the host PC.

When you switch on or reset the Freescale EVB9S12XEP100, the boot loader starts automatically. The mode indicator LED is lit when the boot loader is ready.

When you download an application for PIL simulation (PIL application), the loader program of the host PC communicates with the loader program of the Freescale EVB9S12XEP100 via the RS232 interface.

1. The loader program of the host PC reads the `<application>.s28` S-Record file (or its fast load format form `<application>.fld`, respectively) and downloads it to the EVB9S12XEP100.
2. After a successful download, the board's loader automatically starts the application. The mode indicator LEDs show a running light.

To check whether board and serial interface work correctly, connect the Freescale EVB9S12XEP100 to an ASCII terminal. After reset or power-on, the board should send the following message to the host PC (baud rate of 38,400 bps with 8 data bits, none parity, one stop bit, xon/xoff flow control):

```
TargetLink EVB9S12XEP100 FlashLoader (38400 Baud) V1.0.0
a) Erase FLASH
b) Program FLASH
c) Execute Program
d) Verify Program
```

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Cosmic C Cross-Compiler for MC9S12X(E)

Introduction

The various options for the compiler, assembler, and linker that influence the generated code are described. These options are specified in the corresponding makefile.

Compiler versions

The following compiler versions are supported:

Freescale EVB9S12XEP100	Cosmic 4.8

Compiler

This table lists the options used for the compiler:

Option (CC_OPTS)	Result/Description
`+xe`	Enables support for S12XE processor
`+nowiden`	Does not widen char and float arguments
`-g-a`	Optimizes inline assembly code
`+modf`	Compiles all functions as far functions.

Linker

This table lists the options used for the linker:

Option (LD_OPTS)	Result/Description
`-bs14`	Sets bank size to 2^14 [16 kB]

Metrowerks C Compiler CodeWarrior for MC9S12X(E)

Introduction

The various options for the compiler, assembler, and linker that are used for PIL simulation are described. These options are specified in the corresponding makefile.

Compiler versions

The following compiler versions are supported:

Freescale EVB9S12XEP100	Metrowerks CodeWarrior 5.1

Compiler

This table lists the options used for the compiler:

Option (CC_OPTS)	Result/Description
`-CpuHCS12X`	Generates code for S12X.
`-Mb`	Uses the banked memory model.
`-Cf`	Sets the type for Double to the IEEE64 format.
`-Ot`	Sets the time optimization.

Assembler

This table lists the options used for the assembler:

Option (AS_OPTS)	Result/Description
`-CpuHCS12X`	Generates code for S12X.

Linker

This table lists the options used for the linker:

Option (LD_OPTS)	Result/Description
`-bs14`	Sets bank size to 2^14 [16 kB] (workaround for linker error).

The memory location process of the linker is controlled by the temporary linker command file: `ld.lkf`. This file is created while the makefile is being processed and will be deleted automatically after a successful build process. If you want to change TargetLink's default memory settings you have to modify the corresponding lines of the makefile, which define the contents of the linker

command file. The most important instructions are listed below. For detailed information, refer to the corresponding linker manual.

Typedef for Bool

The includes of the Metrowerks compilers (`stdtypes.h`) define the Bool type to be `Int16`. The corresponding `TargetConfig.xml` files of TargetLink also describe the Bool type as `Int16`. If you want to change it to `Int8`, for example, you must change both the XML file and the compiler include accordingly.

Freescale MPC5700VLE (Freescale MPC5748G)

Introduction

The evaluation boards that are equipped with Freescale MPC5748G microcontrollers, and are supported by the Target Simulation Module (TSM) are described. In addition, the compilers that can be used for these microcontrollers and are supported by TargetLink are described.

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Evaluation Boards

Freescale MPC5748GEVB

Technical characteristics

The Freescale MPC5748GEVB evaluation board has the following characteristics:

Microcontroller unit The board uses the MPC5748G microcontroller.

On-Chip Memory	Size
FLASH ROM	6 MB
RAM	768 kB

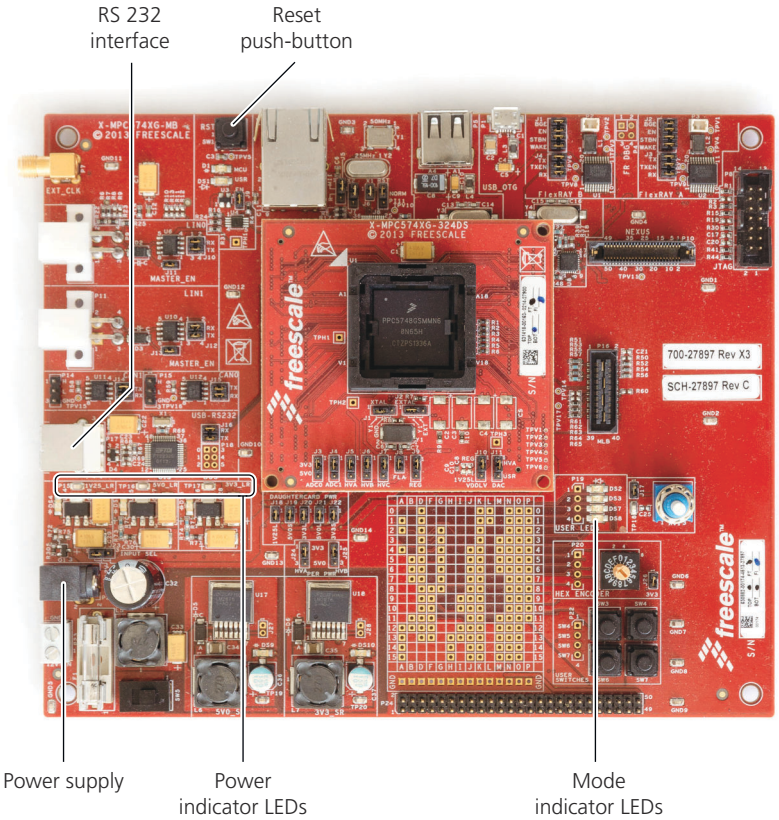
Onboard memory No onboard memory installed.

System clock PIL simulation is performed at 160 MHz.

Interface TargetLink uses an USB interface, which passes through the processor's UART interface, for program download and processor-in-the-loop (PIL) simulation. The interface appears to the Windows system as a virtual COM port. A virtual COM port driver must be installed on the host PC.

Important hardware elements

The following illustration shows the Freescale MPC5748G evaluation board: Only components that are relevant for operating the board or simulating in PIL simulation mode are labeled. These are described in more detail below.



LEDs

Power indicator LEDs After you connect the board to the power supply, the power indicator LEDs light up.

Mode indicator LEDs These LEDs indicate the following modes:

- When the board is switched on or reset, the boot loader starts automatically. The mode indicator LEDs show a running light.
- After a successful download, the boot loader automatically starts the application. The DS2 mode indicator LED flashes.

Power

Power supply Use the 5 V= power supply delivered with the board. After you connect the board to the power supply, the 1,25 V, the 3,3 V and the 5 V (from left to right) power indicator LEDs light up.

Reset push-button Resets the evaluation board.

Cache configuration

To disable the unified cache a "#define NO_CACHE" has to be set for the C preprocessor. You can do this via the compiler option `-DNO_CACHE` as follows:

- In the makefile, or
- By entering **`-DNO_CACHE`** in the Production code PIL application field on the Options page of the TargetLink Main Dialog block (which is local for the model).

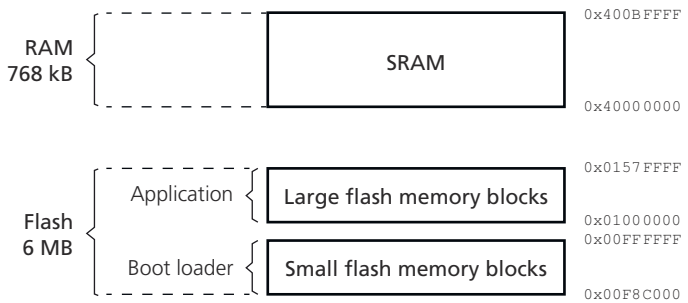
Floating-point exception handling

To disable the floating-point data exception handling a "#define NOFLPEXCEPTIONS" has to be set for the C preprocessor. You can do this via the compiler option `-DNOFLPEXCEPTIONS` as follows:

- In the makefile, or
- By entering **`-DNOFLPEXCEPTIONS`** in the Production code PIL application field on the Options page of the TargetLink Main Dialog block (which is local for the model).

Memory configuration

The following illustration shows the memory configuration in detail:



Download

> **Note**
>
> Connect the evaluation board to the host PC by using the serial cable with USB connector that is delivered with the board.

When you switch on or reset the Freescale MPC5748GEVB, the boot loader starts automatically. The mode indicator LEDs show a running light.

When you download an application for PIL simulation (PIL application), the loader program of the host PC communicates with the loader program of the Freescale MPC5748GEVB via the RS232 interface.

1. The unreserved flash memory areas are cleared, the mode indicator LEDs flash.
2. The loader of the host PC sends an executable image of the application to the unreserved flash memory areas.
3. After a successful download, the boot loader automatically starts the application. The DS2 mode indicator LED flashes.

To check whether board and serial interface work correctly, connect the Freescale MPC5748GEVB to an ASCII terminal. After reset or power-on, the board should send the following message to the host PC (baud rate of 115,200 bps with 8 data bits, none parity, one stop bit, xon/xoff flow control):

```
TargetLink Freescale MPC5748GEVB Flashloader (115200 Baud) V1.8.0
a) Erase FLASH
b) Program FLASH
c) Execute Program
d) Verify Program
```

Compilers

Where to go from here

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Green Hills PowerPC C Compiler..... 26

Wind River Diab PowerPC Family C Compiler..... 27

Green Hills PowerPC C Compiler

Introduction

This section shows the various options for the compiler, assembler, and linker that influence the generated code. These options are specified in the corresponding makefile.

Compiler versions

The following compiler versions are supported:

Freescale MPC5748GEVB	Green Hills 2019

Compiler

This table lists the options used for the compiler:

Option (CC_OPTS)	Result/Description
`-ansi`	The compiler operates in permissive ANSI mode.
`-cpu=ppc5748gz4204`	The compiler produces code for the Freescale MPC5604BEVB device.
`-Ospace`	Enables optimizations that improve both size and performance.

Option (CC_OPTS)	Result/Description
`-vle`	Enables VLE code generation.
`-sda=all`	Enables Small Data Area optimization without size restriction.

Assembler

This table lists the options used for the assembler:

Option (AS_OPTS)	Result/Description
`-cpu=ppc5748gz4204`	Specifies the CPU of the controller.

Linker

This table lists the options used for the linker:

Option (LD_OPTS)	Result/Description
`-cpu=ppc5748gz4204`	Specifies the CPU of the controller.
`-vle`	Enables linkage with VLE libraries.

Wind River Diab PowerPC Family C Compiler

Introduction

The various options for the compiler, assembler, and linker that influence the generated code are described. These options are specified in the corresponding makefile.

Compiler versions

The following compiler versions are supported:

Freescale MPC5748GEVB	Wind River Diab 5.9

Compiler

This table lists the options used for the compiler:

Option (CC_OPTS)	Result/Description
`-tPPCVLEEF:simple`	Specifies the target (PPCVLE), the binary format ELF, the floating point mode S (software) and the character I/O model (simple).
`-X0`	An object file is produced not an executable file.
`-Xopt-count=n`	The compiler's optimization stage is executed n times.
`-Xenum-is-best`	The compiler uses the smallest integer type permitted by the range of values.
`-Xbss-common-off`	Put variables directly into the output section `.bss` instead of using the COMMON section.

Option (CC_OPTS)	Result/Description
`-Xrestart=1`	Optimization is restarted from scratch, if too many optimistic predictions were made.
`-Xtest-at-both`	The compiler is forced to always test loops both before the loop is started and at the bottom of the loop.

Assembler

This table lists the options used for the assembler:

Option (AS_OPTS)	Result/Description
`-tPPCVLEEF:simple`	Specifies the target (PPCVLE), the binary format ELF, the floating point mode S (software) and the character I/O model (simple).

Linker

This table lists the options used for the linker:

Option (LD_OPTS)	Result/Description
`-tPPCVLEEF:simple`	Specifies the target (PPCVLE), the binary format ELF, the floating point mode S (software) and the character I/O model (simple).

Infineon c166 (Infineon c167)

Introduction

The evaluation boards that are equipped with Infineon c167 microcontrollers, and are supported by the Target Simulation Module (TSM) are described. In addition, the compilers that can be used for these microcontrollers and are supported by TargetLink are described.

Where to go from here

Information in this section

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Evaluation Boards

I+ME Promotion Package 166

Technical characteristics

The i+ME eCAN C167C Promo evaluation board (I+ME Promotion Package 166) has the following characteristics:

Microcontroller unit The board uses the SAB-C167CR microcontroller.

On-Chip Memory	Size
SRAM	2 kB

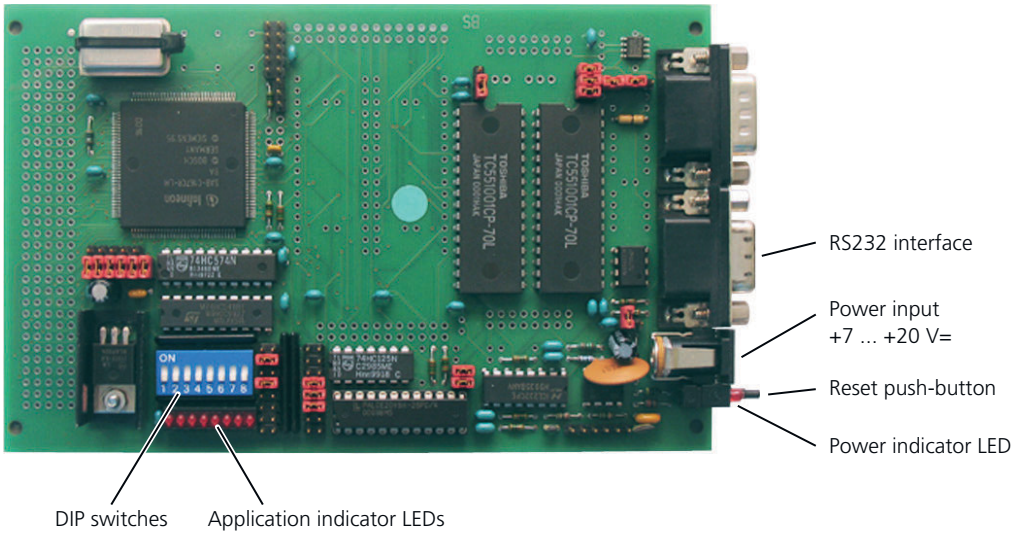
On-board memory The board is equipped with 256 kB onboard RAM.

System clock PIL simulation is performed at 20 MHz.

Interface TargetLink uses the RS232 interface for program download and processor-in-the-loop (PIL) simulation.

Important hardware elements

The following illustration shows the i+ME eCAN C167C Promo Evaluation Board (I+ME Promotion Package 166). Only components that are relevant for operating the board or simulating in PIL simulation mode are labeled. These are described in more detail below.



LEDs

Power indicator LED After you connect the board to the power supply, the red power indicator LED lights up.

Application indicator LEDs After a successful download, the board's loader starts the application and the LED array will count up. If you do not see some kind of running LED display the simulation might have stopped or is finished.

Power

Power supply Connect a plug-in power supply unit (7V ... 20V=) to the connector shown in the photo above.

Reset push-button Resets the evaluation board.

Note

After switching on the power supply you must reset the evaluation board so that it inherits a defined status.

Jumpers and switches

The jumpers must be set as follows (✓ means closed, and – means open).

Jumper	1–2	2–3	3–4	4–5
JP 3	–	✓	n.a.	n.a.
JP 5, JP 7	–	✓	–	✓
JP 8, JP 16, JP 35 ... JP 38	✓	–	n.a.	n.a.
JP 40	–	✓	n.a.	n.a.

Jumper	1–2
JP 9 ... JP 14, JP 21, JP 23, JP 27 ... JP 29, JP 39, JP 42	✓
JP 17 ... JP 20, JP 22, JP 24 ... JP 26, JP 30 ... JP 32	–

Note

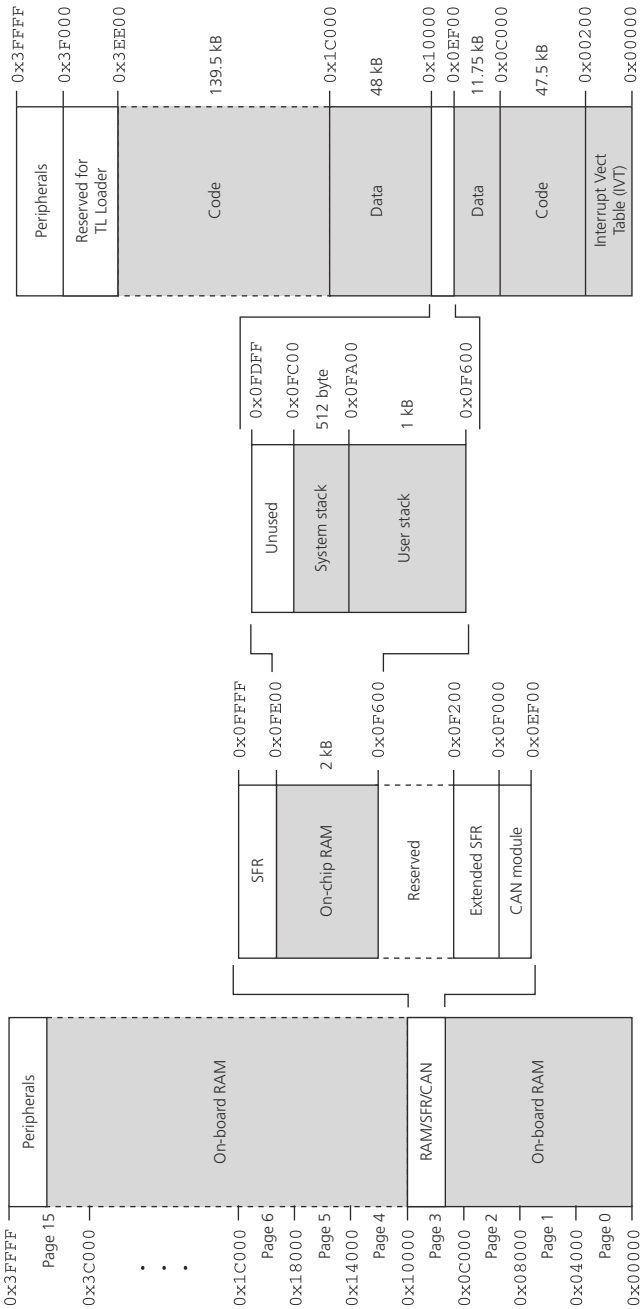
Do not change the jumper settings. Leave them in the positions shown above.

Memory configuration

The C16x family microcontrollers support a linear addressing of only 64 kB memory segments. To address a larger memory address range, the C167 splits up the total memory range into 16 kB memory pages, which can be selected via a data page pointer (there are four independent data page pointers). As a result, the following three steps have to be carried out to address a specific memory cell:

- Point one of the four data page pointers (DPP) to the desired 16 kB memory page.
- Select this data page pointer via the upper two bits of the 16-bit address value.
- Specify the rest of the desired memory cell's address via the remaining 14 bit of the 16-bit address. These 14 bit can linearly address a memory page of 16 kB. For details, refer to the *C167 Derivatives User's Manual* available from Infineon.

During startup, the boot code assigns the address ranges to the different memory modules. The following illustration shows the memory configuration in detail:



- The Tasking Compiler uses an implementation with two independent stacks: the system stack and the user stack.
  - The system stack holds return vectors, segment pointers, and processor status information (for procedures and interrupt routines).
  - The user stack holds task-specific data, meaning temporary, local variables of the user program's functions if there are not enough internal CPU registers.

TargetLink measures the stack consumption for both stacks individually, which results in two simulation plots. `get_stack_size()` returns two stack measurements that result in a single 32-bit value: the system stack consumption in the upper 16 bits and the user stack consumption in the lower 16 bits. A single 32-bit variable is used to keep the model-dependent target frame file free from target-dependent code.

- The system stack's size and position can be selected via three bits of the C167's SYSCON register. The size and position for the processor-in-the-loop (PIL) simulation is 256 words (512 bytes) in the address range `0x0FA00 ... 0x0FBFF`. To select this size and position, the corresponding three bits have to be set to the value `000b`.
- The size and position of the user stack is configured via the linker command file. The size and position for the processor-in-the-loop (PIL) simulation is 1 kB in the address range `0x0F600 ... 0x0F9FF` of the on-chip RAM.
- The memory area in the address range `0x0F200 ... 0x0F5FF` is reserved and cannot be used for the user program.
- The memory area in the address range `0x3EE00 ... 0x3FFFF` holds the loader program and data for some peripherals (for example, the I/O for the LEDs and DIP switches) and also cannot be used for the user program.
- The C167 has a built-in bootstrap loader mechanism that can be used to download programs via the RS232 interface.
- Since the C167's CAN function is not needed for the processor-in-the-loop (PIL) simulation, part of the XRAM/CAN area is mapped as onboard RAM.

Memory areas

The C167 can be used with different memory models. For the TargetLink processor-in-the-loop (PIL) simulation a memory model called *small – address linear* is selected by corresponding linker commands, which results in a total of 193.5 kB RAM for code (program code, constants, strings, and initialization values) and 48 kB RAM for data (meaning variables).

Stack consumption

TargetLink measures the stack consumption for system stack and user stack individually which results in two simulation plots.

Download

Note

Use a serial extension cable to connect the evaluation board to the host PC.

When you switch on the power supply of the I+ME Promotion Package 166, you should always reset the evaluation board so that it inherits a defined status. The red power indicator LED will light up and the bootstrap loader will be started automatically.

To download an application for PIL simulation (PIL application) after a hardware reset, the loader program on the host PC carries out the following steps:

- It sends the binary value `0` to the evaluation board using the desired baud rate. From this character the C167's bootstrap loader recognizes the selected baud rate, which it will use for the following downloads.
- It downloads the first level loader. This can be done via the bootstrap loader, which places the first level loader in the C167's on-chip RAM.
- It downloads the second level loader. This can be done via the first level loader, which places the second level loader in the C167's onboard RAM and starts it immediately.
- It downloads the actual PIL application. This can be done via the second level loader. TargetLink chooses the PIL application's memory configuration in a manner so that it does not overwrite the second level loader. Therefore, if the evaluation board processes a software reset, you do not need to download the second level loader again but can directly download the PIL application (the loader will issue a message).

Compilers

Altium Tasking 80166 C Cross-Compiler

Introduction

The various options for the compiler and macro preprocessor that influence the generated code are described. These options are specified in the corresponding makefile.

Compiler versions

The following compiler versions are supported:

I+ME Promotion Package 166	Altium TASKING C166/ST10 Toolset 8.6

Compiler

This table lists the options used for the compiler:

Option (CC_OPTS)	Result/Description
`-ng`	No additional debug information.
`-O3`	Enables a standard set of optimizations for speed.
`-Ms`	Selects the memory model *small*.
`-AM`	Forces the compiler to use ANSI C conform division.
`-x`	Enables the tasking C167 extensions.

Infineon TriCore (Infineon TC1766)

Introduction

The evaluation boards that are equipped with Infineon TriCore TC1766 microcontrollers, and are supported by the Target Simulation Module (TSM) are described. In addition, the compilers that can be used for these microcontrollers and are supported by TargetLink are described.

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Evaluation Boards

Where to go from here

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Infineon TBTC1766 V1.2

Support information

Note

The Infineon TriBoard TC1766 V1.2 evaluation board (Infineon TBTC1766 V1.2) is no longer distributed by dSPACE but is still supported for downward compatibility.

Technical characteristics

The Infineon TriBoard TC1766 V1.2 evaluation board (Infineon TBTC1766 V1.2) has the following characteristics:

Microcontroller unit The board uses the TC1766B microcontroller (TriCore 1766).

On-Chip Memory	Size
Code Scratch Pad RAM (CSRAM)[1]	16 kB
Data Scratch Pad RAM (DSRAM)[2]	56 kB
Program FLASH (PFLASH)	1.5 MB

[1] aka Scratch Pad RAM (SPRAM)
[2] aka Local Data RAM (LDRAM)

On-board memory No onboard memory installed.

System clock PIL simulation is performed at 80 MHz.

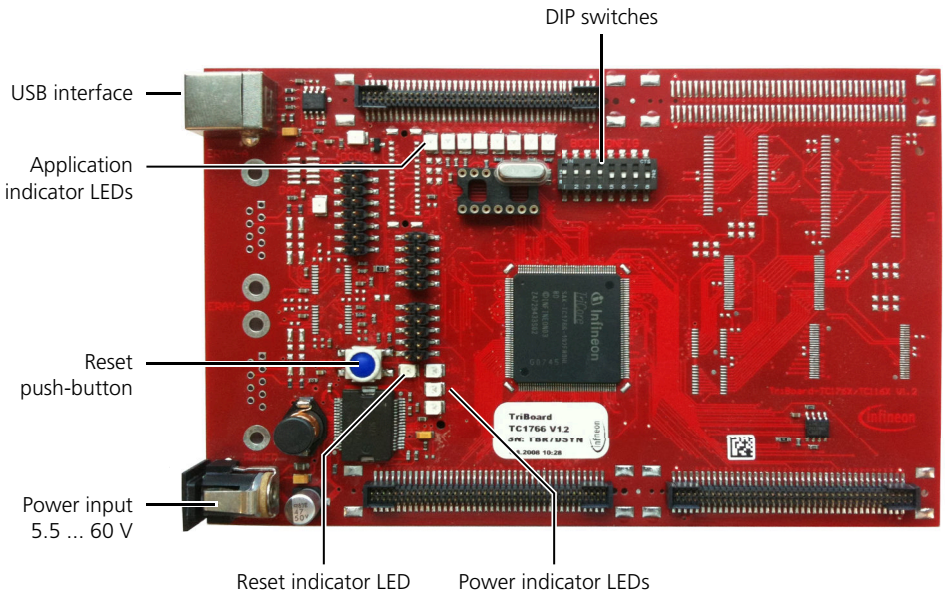
Interface TaregtLink uses the USB interface, which passes through the processor´s UART interface, for program download and processor-in-the-loop (PIL) simulation. The interface appears to the Windows system as a virtual COM port. A virtual COM port driver must be installed on the host PC (please refer to http://www.infineon.com/das for further information).

Note

Select the TBTC1766_20MHz/Taskxx simulation configuration in the dialog of the TargetLink Main Dialog block (Simulation page) when using an Infineon TBTC1766 V1.2 evaluation board for PIL simulation.

Important hardware elements

The following illustration shows the Infineon TriBoard TC1766 Evaluation Board (Infineon TBTC1766 V1.2). Only components that are relevant for operating the board or simulating in PIL simulation mode are labeled. These are described in more detail below.



LEDs

Power indicator LEDs After you connect the board to the power supply, the green power indicator LEDs light up.

Application indicator LEDs After a successful download, the board's loader starts the application and the blue LEDs show a running light.

Reset indicator LED As long as the Reset push-button is being pressed the Reset indicator LED lights.

Power

Power supply Connect a plug-in power supply unit (5.5...60 V=) to the power connector shown above.

Reset push-button Resets the evaluation board.

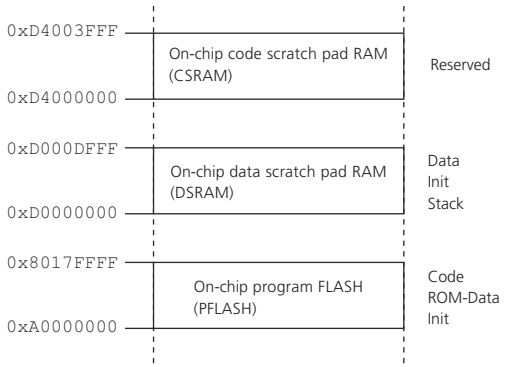
Jumpers and switches

The dip switches must be set as follows.

Dip Switch	1	2	3	4	5	6	7	8
S 301	On	On	On	On	–	–	–	–

Memory configuration

The following illustration shows the memory configuration in detail (not all modules are listed here, refer to *TC1766 32-Bit Single Chip Microcontroller User's Manual, Infineon 2005* for details):



Download

Note

Use an USB extension cable to connect the evaluation board to the host PC.

The Infineon TBTC1766 V1.2 is to be configured for the bootstrap loader mechanism using the USB interface. After applying power to the board, 3 green LEDs light up and the bootstrap loader starts automatically.

To download an application for PIL simulation after a hardware reset, the loader program on the host PC carries out the following steps:

1. It sends the binary value 0 to the evaluation board using the desired baud rate. From this character the Infineon TBTC1766 V1.2's bootstrap loader recognizes the selected baud rate, which it uses for the following downloads.
2. It downloads the first level loader of 80 Bytes. This is done via the bootstrap loader, which places the first level loader in the SPRAM at 0xD4000000
3. It downloads the second level loader. This is done via the first level loader, which places the second level loader in the SPRAM at 0xD4000080 and starts it immediately.
4. It downloads the actual PIL application. This is done via the second level loader. TargetLink chooses the PIL application's memory configuration in a manner so that it does not overwrite the first and second level loaders. Therefore, if the evaluation board processes a software reset, you do not need to download the first and second level loaders again but can directly download the PIL application (the loader issues a message).

The PIL application is saved into the on-chip Program FLASH of the TC1766. Therefore the FLASH is erased when the download is being started. After a successful download, the board's loader starts the application and the blue LEDs show a running light.

Infineon TBTC1766.300

Support information

Note

The Infineon TriBoard TC1766 evaluation board (Infineon TBTC1766.300) is no longer distributed by dSPACE but is still supported for downward compatibility.

Technical characteristics

The Infineon TriBoard TC1766 evaluation board (Infineon TBTC1766.300) has the following characteristics:

Microcontroller unit The board uses the TC1766B microcontroller (TriCore 1766).

On-Chip Memory	Size
Code Scratch Pad RAM (CSRAM)[1)]	16 kB

On-Chip Memory	Size
Data Scratch Pad RAM (DSRAM)[2]	56 kB
Program FLASH (PFLASH)	1.5 MB

[1] aka Scratch Pad RAM (SPRAM)
[2] aka Local Data RAM (LDRAM)

Onboard memory No onboard memory installed.

System clock PIL simulation is performed at 75 MHz.

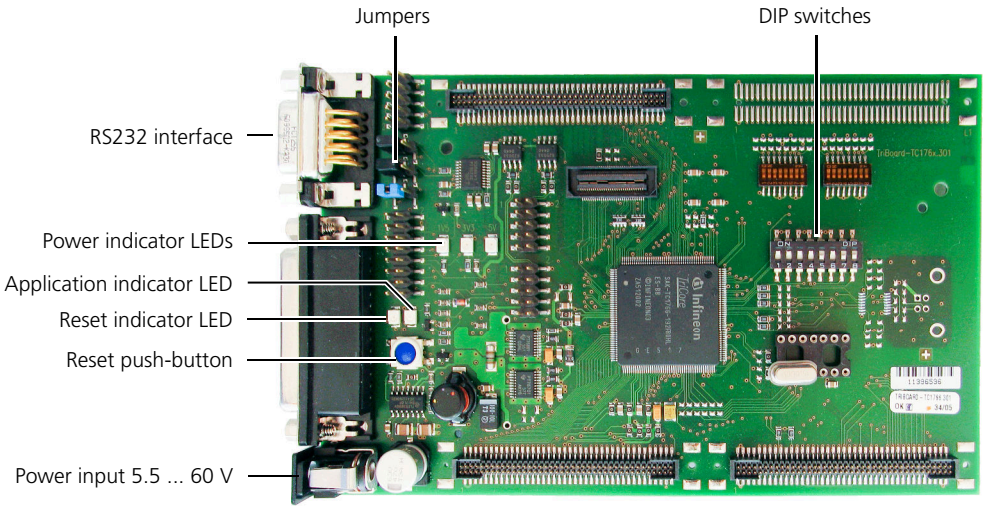
Interface TargetLink uses the RS232 interface for program download and processor-in-the-loop (PIL) simulation .

Note

Select the TBTC1766/Taskxx simulation configuration in the dialog of the TargetLink Main Dialog block (Simulation page) when using an Infineon TBTC1766.300 evaluation board for PIL simulation.

Important hardware elements

The following illustration shows the Infineon TriBoard TC1766 Evaluation Board (Infineon TBTC1766.300). Only components that are relevant for operating the board or simulating in PIL simulation mode are labeled. These are described in more detail below.



LEDs

Power indicator LEDs After you connect the board to the power supply, the green power indicator LEDs light up.

Application indicator LED After a successful download, the board's loader starts the application and the Application indicator LED starts flashing.

Reset indicator LED As long as the Reset push-button is being pressed the Reset indicator LED lights.

Power

Power supply Connect a plug-in power supply unit (5.5 V ... 60 V=) to the power connector shown above.

Reset push-button Resets the evaluation board.

Jumpers and switches

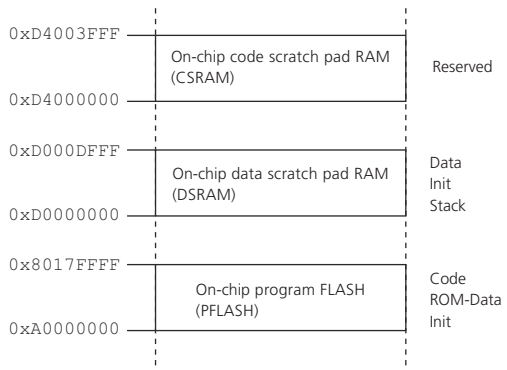
The jumpers and dip switches must be set as follows (✓ means closed, and – means open).

Jumper	1–2	2–3
JP 401, JP 402, JP 501	✓	–

Dip Switch	1	2	3	4	5	6	7	8
S 301	On	On	On	On	Off	On	Off	Off

Memory configuration

The following illustration shows the memory configuration in detail (not all modules are listed here, refer to *TC1766 32-Bit Single Chip Microcontroller User's Manual, Infineon 2005* for details):



Download

Note

Use a serial extension cable to connect the evaluation board to the host PC.

The Infineon TBTC1766.300 is to be configured for the bootstrap loader mechanism using the serial interface. After applying power to the board, 3 green LEDs light up and the bootstrap loader is started automatically.

To download an application for PIL simulation (PIL application) after a hardware reset, the loader program on the host PC carries out the following steps:

1. It sends the binary value 0 to the evaluation board using the desired baud rate. From this character the Infineon TBTC1766.300's bootstrap loader recognizes the selected baud rate, which it uses for the following downloads.
2. It downloads the first level loader of 80 Bytes. This is done via the bootstrap loader, which places the first level loader in the SPRAM at 0xD4000000.

3. It downloads the second level loader. This is done via the first level loader, which places the second level loader in the SPRAM at 0xD4000080 and starts it immediately.
4. It downloads the actual PIL application. This is done via the second level loader. TargetLink chooses the PIL application's memory configuration in a manner so that it does not overwrite the first and second level loaders. Therefore, if the evaluation board processes a software reset, you do not need to download the first and second level loaders again but can directly download the PIL application (the loader issues a message).

The PIL application is saved into the on-chip Program FLASH of the TC1766. Therefore the FLASH is erased when the download is being started. After a successful download, the board's loader starts the application and the yellow indicator LED starts flashing.

Compilers

Altium Tasking TriCore C Cross-Compiler

Introduction

The various options that are used for the compiler, and influence the generated code are described. These options are specified in the corresponding makefile.

Compiler versions

The following compiler versions are supported:

Infineon TriBoard TriCore 1766	Altium TASKING TriCore VX-Toolset 3.2
Infineon TriBoard TriCore 1766 20 MHz	Altium TASKING TriCore VX-Toolset 3.2

Compiler

The following options are used for the compiler.

Option (CC_OPTS)	Description
--iso=90	Use ISO C90 standard
--optimize=2	Optimization level 2
--tradeoff=2	Balanced optimization for speed/size
--align=2	16 Bit alignment of objects of four bytes or larger
--align=4	32 Bit alignment of objects of four bytes or larger
--default-near-size=8	Threshold for _near allocation
--cpu=tc1766b	Generate code for TC1766B

Option (CC_OPTS)	Description
--silicon-bug=all-tc1766	Bypass TC1766 problems
--silicon-bug=cpu-tc060	Bypass CPU-TC060 problem

Assembler

The following options are used for the assembler.

Option (AS_OPTS)	Description
`--debug-info=+smart`	Enables smart debug information
`--cpu=tc1766b`	Assemble for TC1766B
`--silicon-bug=all-tc1766`	Bypass TC1766 problems
`--silicon-bug=cpu-tc060`	Bypass CPU-TC060 problem

Linker

The following options are used for the linker.

Option (LD_OPTS)	Description
`--optimize=1-delete-unreferenced-sections`	Keep unreferenced sections, because the TargetLink step function is called by reference, which is not recognized by the linker

Disabling the instruction cache

To disable the instruction cache a #define NOICACHE has to be set for the C preprocessor. You can do this via the compiler option `(-DNOICACHE)`, either in the makefile (which is local for an installation), or by entering `-DNOICACHE` in the Production code PIL application edit field on the Options page of the TargetLink Main Dialog block (which is local for the model).

Infineon TriCore (Infineon TC1767)

Introduction

The evaluation boards that are equipped with Infineon TriCore TC1767 microcontrollers, and are supported by the Target Simulation Module (TSM) are described. In addition, the compilers that can be used for these microcontrollers and are supported by TargetLink are described.

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Evaluation Boards

Infineon TBTC1767

Technical characteristics

The Infineon TriBoard TC1767 evaluation board (Infineon TBTC1767) has the following characteristics:

Microcontroller unit The board uses the TC1767 microcontroller (TriCore 1767).

On-Chip Memory	Size
Local Data RAM (LDRAM)	68 kB
Program FLASH (PFLASH)	2 MB

Onboard memory No onboard memory installed.

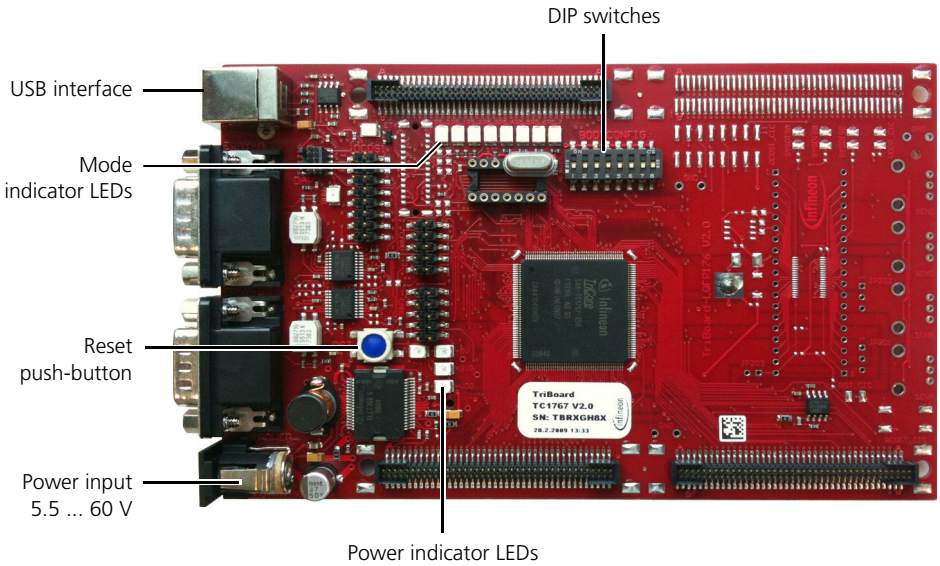
System clock PIL simulation is performed at 133 MHz.

Interface TargetLink uses the USB interface, which passes through the processor´s UART interface, for program download and processor-in-the-loop (PIL) simulation. The interface appears to the Windows system as a virtual COM port. A virtual COM port driver must be installed on the host PC (please refer to http://www.infineon.com/das for further information).

Important hardware elements

The following illustration shows the Infineon TriBoard TC1767 Evaluation Board (Infineon TBTC1767). Only components that are relevant for operating the board

or simulating in PIL simulation mode are labeled. These are described in more detail below.



LEDs

Power indicator LEDs After you connect the board to the power supply, the green power indicator LEDs light up.

Mode indicator LEDs These LEDs indicate the following modes:

- After applying power to the board, the boot loader starts automatically. Then the two left LEDs flash alternately.
- After a successful download, the boot loader starts the application and the LEDs show a running light.

Power

Power supply Connect a plug-in power supply unit (5.5...60 V=) to the power connector shown above.

Reset push-button Resets the evaluation board.

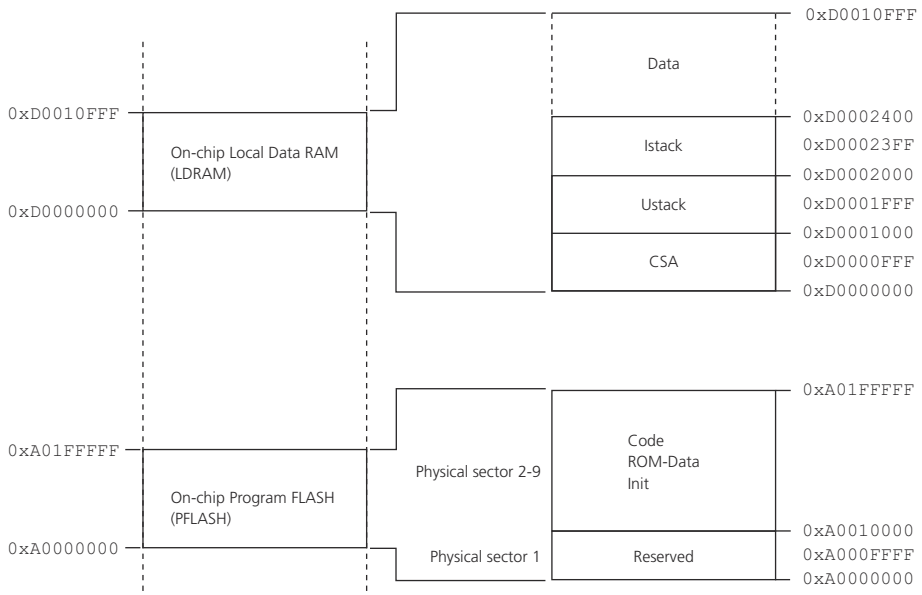
Jumpers and switches

The dip switches must be set as follows.

Dip Switch	1	2	3	4	5	6	7	8
S 201	–	–	–	–	–	–	Off	Off

Memory configuration

The following illustration shows the memory configuration in detail (not all modules are listed here, refer to *TC1767 32-Bit Single Chip Microcontroller User's Manual, Infineon 2008* for details):



Download

Note

Use an USB extension cable to connect the evaluation board to the host PC.

A loader program is located in the on-chip flash memory of the TriBoard TC1767. After applying power to the board, the loader is automatically started. Then two blue LEDs of the board flash alternately.

To download an application for PIL simulation, a loader of the host PC communicates with the loader of the board.

After a successful download, the board's loader starts the application and the blue LEDs show a running light.

To check whether board and serial interface work correctly, connect the Infineon TBTC1767 to an ASCII terminal. After reset or power-on, the board should send the following message to the host PC (baud rate of 115,200 bps with 8 data bits, none parity, one stop bit, xon/xoff flow control):

```
TargetLink TBTC1767 Flashloader (115200 Baud) V1.4.0
a) Erase FLASH
b) Program FLASH
c) Execute Program
d) Verify Program
```

Compilers

Altium Tasking TriCore C Cross-Compiler

Introduction

The various options that are used for the compiler, and influence the generated code are described. These options are specified in the corresponding makefile.

Compiler versions

The following compiler versions are supported:

Infineon TriBoard TriCore 1767	Altium TASKING TriCore VX-Toolset 3.2

Compiler

The following options are used for the compiler.

Option (CC_OPTS)	Description	Version
--iso=90	Use ISO C90 standard	all
--optimize=2	Optimization level 2	all
--tradeoff=0	Optimize for speed	all
--align=2	16-bit alignment of objects of four bytes or larger	3.2
--align=4	32-bit alignment of objects of four bytes or larger	6.2
--default-near-size=0	Threshold for _near allocation	all
--cpu=tc1767	Generate code for TC1767	all
--silicon-bug=all-tc1767	Bypass TC1767 problems	all

Assembler

The following options are used for the assembler.

Option (AS_OPTS)	Description	Version
`--debug-info=+smart`	Enables smart debug information	all
`--cpu=tc1767`	Assemble for TC1767	all
`--silicon-bug=all-tc1767`	Bypass TC1767 problems	all

Linker

The following options are used for the linker.

Option (LD_OPTS)	Description	Version
`--optimize=1-delete-unreferenced-sections`	Keep unreferenced sections, because the TargetLink step function is called by reference, which is not recognized by the linker	all

Disabling the instruction cache

To disable the instruction cache a #define NOICACHE has to be set for the C preprocessor. You can do this via the compiler option `(-DNOICACHE)`, either in the makefile (which is local for an installation), or by entering `-DNOICACHE` in the Production code PIL application field on the Options page of the TargetLink Main Dialog block (which is local for the model).

Infineon TriCore (Infineon TC1796)

Introduction

The evaluation boards that are equipped with Infineon TriCore TC1796 microcontrollers, and are supported by the Target Simulation Module (TSM) are described. In addition, the compilers that can be used for these microcontrollers and are supported by TargetLink are described.

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Evaluation Boards

Where to go from here

Information in this section

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Infineon TBTC1796.400

Support information

Note

The Infineon TriBoard TC1796 evaluation board (Infineon TBTC1796.400) is no longer distributed by dSPACE but is still supported for downward compatibility.

Technical characteristics

The Infineon TriBoard TC1796 evaluation board (Infineon TBTC1796.400) has the following characteristics:

Microcontroller unit The board uses the TC1796B microcontroller (TriCore 1796).

On-Chip Memory	Size
Code Scratch Pad RAM (CSRAM)[1]	48 kB
Data Scratch Pad RAM (DSRAM)[2]	56 kB
Program FLASH(PFLASH)	2 MB

[1] aka Scratch Pad RAM
[2] aka Local Data RAM

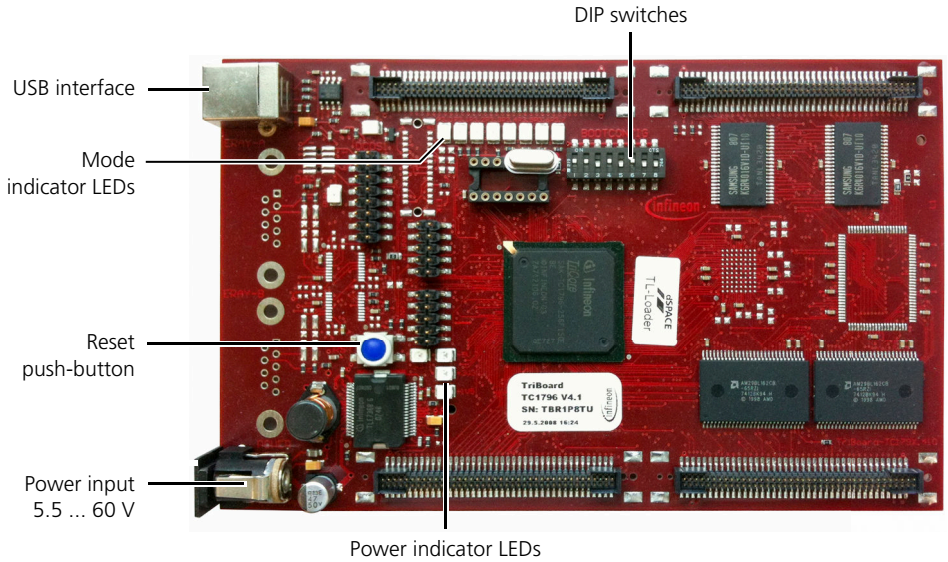
Onboard memory The board is equipped with 1 MB onboard asynchronous SRAM and 4 MB onboard FLASH.

System clock PIL simulation is performed at 150 MHz.

Interface TargetLink uses the USB interface, which passes through the processor´s UART interface, for program download and processor-in-the-loop (PIL) simulation. The interface appears to the Windows system as a virtual COM port. A virtual COM port driver must be installed on the host PC (please refer to http://www.infineon.com/das for further information).

Important hardware elements

The following illustration shows the Infineon TriBoard TC1796 Evaluation Board (Infineon TBTC1796.400). Only components that are relevant for operating the board or simulating in PIL simulation mode are labeled. These are described in more detail below.



LEDs

Power indicator LEDs After you connect the board to the power supply, the green power indicator LEDs light up.

Mode indicator LEDs These LEDs indicate the following modes:

- After applying power to the board, the boot loader starts automatically. Then the two LEDs on the left-hand side flash alternately.
- After a successful download, the boot loader starts the application and the blue LEDs show a running light.

Power

Power supply Connect a plug-in power supply unit (5.5...60 V=) to the power connector shown above.

Reset push-button Resets the evaluation board.

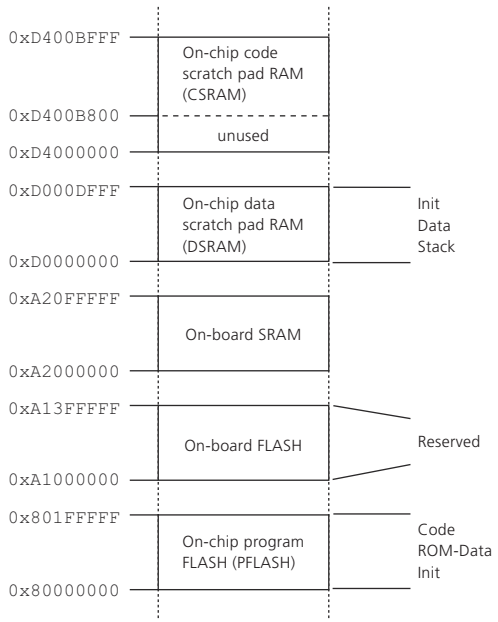
Jumpers and switches

The dip switches must be set as follows.

Dip Switch	1	2	3	4	5	6	7	8
S 301	On	On	Off	On	Off	–	–	–

Memory configuration

The following illustration shows the memory configuration in detail (not all modules are listed here, refer to *TriCore Family, TC1796 A-Step User's Manual, Infineon 2000* for details):



Download

Note

Use an USB extension cable to connect the evaluation board to the host PC.

A loader program is located in the onboard flash memory of the TriBoard TC1796. After applying power to the board, the loader is automatically started. Then two blue LEDs of the board flash alternately.

To download an application for PIL simulation, a loader of the host PC communicates with the loader of the board.

After a successful download, the board's loader starts the application and the blue LEDs show a running light.

To check whether board and serial interface work correctly, connect the Infineon TBTC1796 to an ASCII terminal. After reset or power-on, the board should send the following message to the host PC (baud rate of 115,200 bps with 8 data bits, none parity, one stop bit, xon/xoff flow control):

```
TargetLink TBTC1796 Flashloader (115200 Baud) V1.8.4
a) Erase FLASH
b) Program FLASH
c) Execute Program
d) Verify Program
```

Infineon TBTC1796.300

Support information

Note

The Infineon TriBoard TC1796 evaluation board (Infineon TBTC1796.300) is no longer distributed by dSPACE but is still supported for downward compatibility.

Technical characteristics

The Infineon TriBoard TC1796 evaluation board (Infineon TBTC1796.300) has the following characteristics:

Microcontroller unit The board uses the TC1796B microcontroller (TriCore 1796).

On-Chip Memory	Size
Code Scratch Pad RAM (CSRAM)[1)]	48 kB
Data Scratch Pad RAM (DSRAM)[2)]	56 kB
Program FLASH(PFLASH)	2 MB

[1)] aka Scratch Pad RAM
[2)] aka Local Data RAM

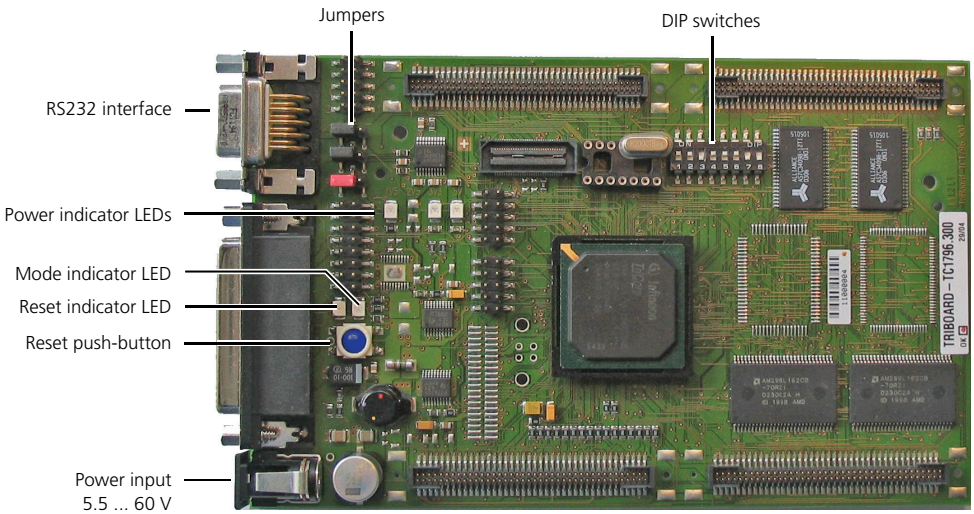
Onboard memory The board is equipped with 1 MB onboard asynchronous SRAM and 4 MB onboard FLASH.

System clock PIL simulation is performed at 150 MHz.

Interface TargetLink uses the RS232 interface for program download and processor-in-the-loop (PIL) simulation .

Important hardware elements

The following illustration shows the Infineon TriBoard TC1796 Evaluation Board (Infineon TBTC1796.300). Only components that are relevant for operating the board or simulating in PIL simulation mode are labeled. These are described in more detail below.



LEDs

Power indicator LEDs After you connect the board to the power supply, the green power indicator LEDs light up.

Mode indicator LED These LED indicates the following modes:

- After applying power to the board, the boot loader starts automatically. Then the LED flashes periodically.
- After a successful download, the boot loader starts the application and the LED continues flashing.

Power

Power supply Connect a plug-in power supply unit (5.5 V ... 60 V=) to the power connector shown above.

Reset push-button Resets the evaluation board.

Jumpers and switches

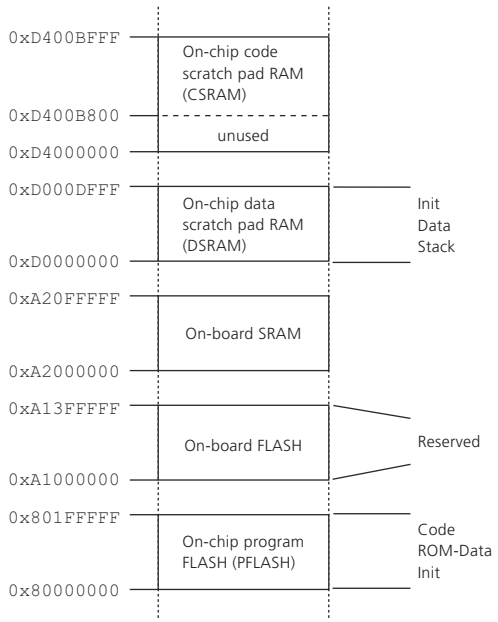
The jumpers and dip switches must be set as follows (✓ means closed, and – means open).

Jumper	1–2	2–3
JP 401, JP 402, JP 501	✓	–

Dip Switch	1	2	3	4	5	6	7	8
S 301	On	On	–	On	On	On	–	–
S 1 (bottom)	–	–	–	–	–	–	–	–
S 2 (bottom)	–	–	–	–	–	–	–	–

Memory configuration

The following illustration shows the memory configuration in detail (not all modules are listed here, refer to *TriCore Family, TC1796 A-Step User's Manual, Infineon 2000* for details):



Download

Note

Use a serial extension cable to connect the evaluation board to the host PC.

A loader program is located in the onboard flash memory of the TriBoard TC1796. After applying power to the board, the loader starts automatically. Then the yellow indicator LED of the board flashes periodically.

To download an application for PIL simulation, a loader of the host PC communicates with the loader of the board.

After a successful download, the board's loader starts the application and the yellow indicator LED continues flashing.

To check whether board and serial interface work correctly, connect the Infineon TBTC1796 to an ASCII terminal. After reset or power-on, the board should send the following message to the host PC (baud rate of 115,200 bps with 8 data bits, none parity, one stop bit, xon/xoff flow control):

```
TargetLink TBTC1796 Flashloader (115200 Baud) V1.8.4
a) Erase FLASH
b) Program FLASH
c) Execute Program
d) Verify Program
```

Compilers

Altium Tasking TriCore C Cross-Compiler

Introduction

The various options that are used for the compiler, and influence the generated code are described. These options are specified in the corresponding makefile.

Compiler versions

The following compiler versions are supported:

Infineon TriBoard TriCore 1796	Altium TASKING TriCore VX-Toolset 3.2

Compiler

The following options are used for the compiler.

Option (CC_OPTS)	Description
--iso=90	Use ISO C90 standard
--optimize=2	Optimization level 2
--tradeoff=2	Optimize for speed
--align=2	16 Bit alignment of objects of four bytes or larger
--default-near-size=8	Threshold for _near allocation
--cpu=tc1796b	Generate code for TC1796B
--silicon-bug=all-tc1796	Bypass TC1796 problems
--silicon-bug=cpu-tc060	Bypass CPU-TC060 problem

Assembler

The following options are used for the assembler.

Option (AS_OPTS)	Description
--debug-info=+smart	Enables smart debug information
--cpu=tc1796b	Assemble for TC1796B
--silicon-bug=all-tc1796	Bypass TC1796 problems
--silicon-bug=cpu-tc060	Bypass CPU-TC060 problem

Linker

The following options are used for the linker.

Option (LD_OPTS)	Description
--optimize=1-delete-unreferenced-sections	Keep unreferenced sections, because the TargetLink step function is only called by reference, which is not recognized by the linker

Disabling the instruction cache

To disable the instruction cache a #define NOICACHE has to be set for the C preprocessor. You can do this via the compiler option `(-DNOICACHE)`, either in the makefile (which is local for an installation), or by entering `-DNOICACHE` in the Production code PIL application field on the Options page of the TargetLink Main Dialog block (which is local for the model).

Infineon TriCore (Infineon TC275)

Introduction

The evaluation boards that are equipped with Infineon TriCore TC275 microcontrollers, and are supported by the Target Simulation Module (TSM) are described. In addition, the compilers that can be used for these microcontrollers and are supported by TargetLink are described.

TargetLink supports virtual evaluation boards for this microcontroller family. For more information, refer to Infineon TriCore (Infineon TC275) on page 95.

Where to go from here

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Evaluation Boards

Infineon TBTC275

Technical characteristics

The Infineon TBTC275 evaluation board has the following characteristics:

Microcontroller unit The board uses the TC275 microcontroller.

On-Chip Memory	Size
FLASH ROM	4 MB
RAM	32 kB

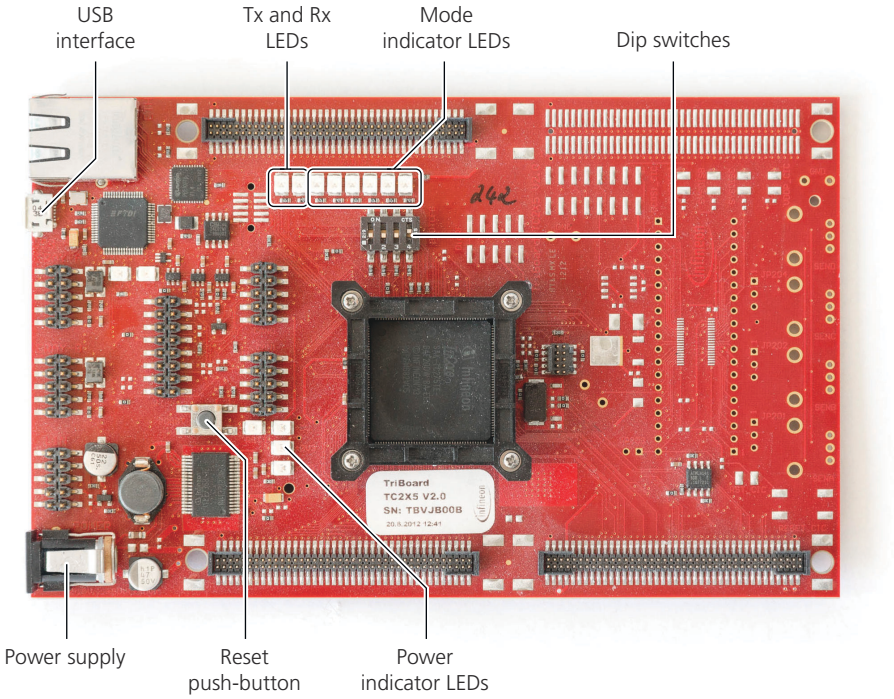
Onboard memory No onboard memory installed.

System clock PIL simulation is performed at 200 MHz.

Interface TargetLink uses the USB interface, which passes through the processor´s UART interface, for program download and processor-in-the-loop (PIL) simulation. The interface appears to the Windows system as a virtual COM port. A virtual COM port driver must be installed on the host PC (please refer to http://infineon.com/das for further information).

Important hardware elements

The following illustration shows the Infineon TriBoard TBTC275 evaluation board. Only components that are relevant for operating the board or simulating in PIL simulation mode are labeled. These are described in more detail below.



LEDs

Power indicator LEDs After you connect the board to the power supply, the three power indicator LEDs light up.

Mode indicator LEDs These LEDs indicate the following modes:

- When the board is switched on or reset, the boot loader starts automatically. The six blue mode indicator LEDs show a running light.
- After a successful download, the boot loader automatically starts the application. The mode indicator LED on the left-hand side flashes.

Tx and Rx LEDs When the host PC communicates with the board, the Tx and Rx LEDs flash.

Power

Power supply Connect a plug-in power supply unit (+5,5 ... +40 V=) to the power connector. After you connect the board to the power supply, the four power indicator LEDs light up.

Reset push-button Resets the evaluation board.

Switches

The dip switches must be set as follows.

Dip Switch:	1	2	3	4	5	6	7	8
BOOTCFG	Off	Off	Off	On	—	—	—	—

Cache configuration

To disable the unified cache a "#define NO_CACHE" has to be set for the C preprocessor. You can do this via the compiler option `-DNO_CACHE` as follows:

- In the makefile, or
- By entering **`-DNO_CACHE`** in the Production code PIL application field on the Options page of the TargetLink Main Dialog block (which is local for the model).

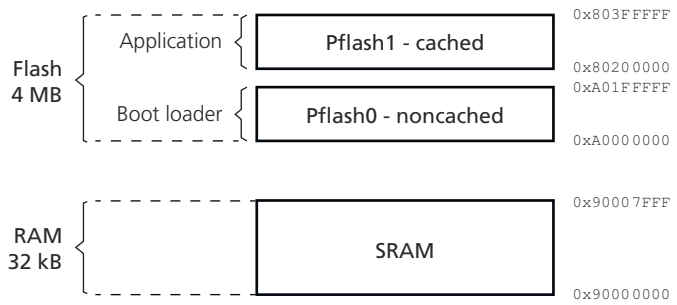
Floating-point exception handling

To disable the floating-point data exception handling a "#define NOFLPEXCEPTIONS" has to be set for the C preprocessor. You can do this via the compiler option `-DNOFLPEXCEPTIONS` as follows:

- In the makefile, or
- By entering **`-DNOFLPEXCEPTIONS`** in the Production code PIL application field on the Options page of the TargetLink Main Dialog block (which is local for the model).

Memory configuration

The following illustration shows the memory configuration in detail:



Download

Note

Connect the evaluation board to the host PC by using the serial cable with micro USB connector that is delivered with the board.

When you switch on or reset the Infineon TriBoard TBTC275, the boot loader starts automatically. The six blue mode indicator LEDs show a running light.

When you download an application for PIL simulation (PIL application), the loader program of the host PC communicates with the loader program of the Infineon TriBoard TBTC275 via the RS232 interface.

1. The unreserved flash memory areas are cleared.
2. The loader of the host PC sends an executable image of the application to the unreserved flash memory areas. The Tx and Rx LEDs flash.
3. After a successful download, the board's loader automatically starts the application. The mode indicator LED on the left-hand side flashes.

To check whether board and serial interface work correctly, connect the Infineon TBTC275 to an ASCII terminal. After reset or power-on, the board should send the following message to the host PC (baud rate of 115,200 bps with 8 data bits, none parity, one stop bit, xon/xoff flow control):

```
TargetLink TBTC275 Flashloader (115200 Baud) V1.8.5
a) Erase FLASH
b) Program FLASH
c) Execute Program
d) Verify Program
```

Virtual evaluation board

TargetLink offers you support for a virtual counterpart of this physical evaluation board. For more information, refer to Lauterbach TRACE32 Simulator for Infineon TC 275 on page 95.

Compilers

Where to go from here

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HighTec GNU Toolchain for TriCore..... 60

Altium Tasking TriCore C Cross-Compiler

Introduction

The various options that are used for the compiler, and influence the generated code are described. These options are specified in the corresponding makefile.

Compiler versions

The following compiler versions are supported:

Infineon TriBoard TriCore 275	Altium TASKING TriCore VX-Toolset 6.3

Compiler

The following options are used for the compiler.

Option (CC_OPTS)	Result/Description
`--optimize=3`	Sets the optimization level as high.
`--tradeoff=4`	Sets the tradeoff between speed and size.
`--core=tc1.6.x`	Specifies the core used by controller.
`--align=4`	32-bit alignment of objects of four bytes or larger

Assembler

The following options are used for the assembler.

Option (AS_OPTS)	Result/Description
`--core=tc1.6.x`	Specifies the core used by controller.

Linker

The following options are used for the linker.

Option (LD_OPTS)	Result/Description
`-cpu=tc27x`	Specifies the CPU of the controller.

HighTec GNU Toolchain for TriCore

Introduction

The various options for the compiler, assembler, and linker that influence the generated code are described. These options are specified in the corresponding makefile.

Compiler versions

The following compiler versions are supported:

Infineon TriBoard TriCore 275	HighTec GNU 4.9

Compiler

This table lists the options used for the compiler:

Option (CC_OPTS)	Result/Description
`-Os`	Sets the optimization level as high
`-falign-functions=4`	Aligns function entries to word addresses.
`-mcpu=tc27xx`	Specifies the CPU of the controller.
`-mabs=8`	Allocates data of up to 8 Bytes in absolute addressable memory

Assembler

This table lists the options used for the assembler:

Option (AS_OPTS)	Result/Description
`-mtc16`	Assembles for TriCore1 1.6

Linker

This table lists the options used for the linker:

Option (LD_OPTS)	Result/Description
`-Wl, --mcpu=tc27xx`	Specifies the CPU of the controller.

Infineon XC2000 (Infineon XC2287)

Introduction

The evaluation boards that are equipped with Infineon XC2287 microcontrollers, and are supported by the Target Simulation Module (TSM) are described. In addition, the compilers that can be used for these microcontrollers and are supported by TargetLink are described.

Where to go from here

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Evaluation Boards

Infineon EasyKit XC2287

Support information

Note

The Infineon EasyKit XC2287 evaluation board is no longer distributed by dSPACE but is still supported for downward compatibility.

Technical characteristics

The Infineon SK-EB XC2287 evaluation board has the following characteristics:

Microcontroller unit The board uses the XC2287 96F66L microcontroller.

On-Chip Memory	Size
Data SRAM (DSRAM)	16 kB
Dual-port RAM (DPRAM)	2 kB
Program SRAM (PSRAM)	64 kB
Program FLASH[1)]	764 kB

On-Chip Memory	Size
Reserved FLASH[2)]	4 kB

[1)] FLASH 0, FLASH 1, FLASH 2
[2)] Not accessible to the software

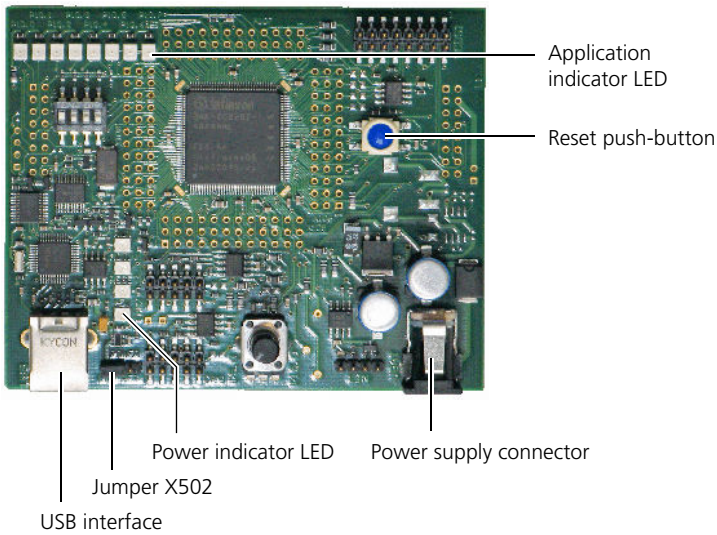
Onboard memory No onboard memory installed.

System clock PIL simulation is performed at 80 MHz.

Interface TargetLink uses the USB interface, which passes through the processor´s UART interface, for program download and processor-in-the-loop (PIL) simulation. The interface appears to the Windows system as a virtual COM port. A virtual COM port driver must be installed on the host PC.

Important hardware elements

The following illustration shows the Infineon SK–EB XC2287. Only components that are relevant for operating the board or simulating in PIL simulation mode are labeled. These are described in more detail below.



LEDs

Power indicator LED After you connect the board to the power supply, the power indicator LED lights up.

Application indicator LED After a successful download, the board's loader starts the application and the LED starts flashing.

Power

Power supply The USB power supply concept lets you work with the board without an external power supply. If the USB power supply is not sufficient, an additional regulated DC power supply can be used. By default, the X502 jumper is set to power supply via USB interface.

Reset push-button Resets the evaluation board.

Jumpers and switches

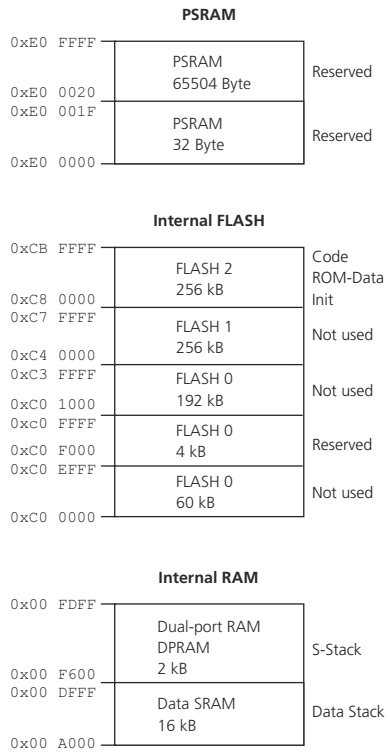
The jumpers and dip switches must be set as follows (✓ means closed, and – means open).

Dip Switch	On/Off
1	On
2	Off
3	Off
4	Off

Jumper	1–2	2–3
X502	✓	–

Memory configuration

The following illustration shows the memory configuration in detail (not all modules are listed here):



For details of data and code addressing, refer to *User Manual - XC2000 Derivatives 16/32- Bit Single-Chip Microcontroller with 32-Bit Performance Volume 1 (of 2): System Units* (from Infineon).

Stack consumption

TargetLink measures the stack consumption for system stack and user stack individually which results in two simulation plots.

Download

Note

A virtual COM port driver must be installed on the host PC. For details, refer to http://www.infineon.com/das.

When you switch on the SK-EB XC2287 power supply, the D101 LED connected to P10.0 should FLASH, otherwise press the Reset button. The XC2287 starts in bootstrap loader mode.

To download an application for PIL simulation (PIL application), the loader program on the host PC first has to download a first-level loader which itself loads the second-level loader which loads the actual PIL application.

While the second-level loader is running, the D105 LED connected to P10.4 starts flashing.

After a successful download, the board's loader starts the application and the D108 LED connected to P10.7 starts flashing.

Compilers

Altium Tasking VX – Toolset for C166 Compiler (Altium Tasking C166 VX)

Introduction

The various options for the compiler and macro preprocessor that influence the generated code are described. These options are specified in the corresponding makefile.

Compiler versions

The following compiler versions are supported:

Infineon EasyKit XC2287	Altium TASKING C166/ST10 VX-Toolset 3.0

Compiler

The table lists the options used for the compiler. For more information, refer to the *TASKING VX-toolset for C166 User Guide*.

Option (CC_OPTS)	Result/Description
`--iso=90`	C standard ISO C90
`--model=near`	Selects the NEAR memory model
`--cpu=xc2287`	Defines the target processor xc2287
`--tradeoff=1`	Compiler optimizes code size and code speed

Option (CC_OPTS)	Result/Description
`--language=+cmp14,+div32,-gcc,-strings`	▪ Enables 14-bit arithmetic for far pointer comparison ▪ Enables 32/16 -> 16-bit division and modulo instructions ▪ Disables the GNU C extensions ▪ Disables relaxed const check for string literals
`--optimize=2`	Default optimization

Assembler

The table lists the options used for the assembler. For more information, refer to the *TASKING VX-toolset for C166 User Guide*.

Option (AC_OPTS)	Result/Description
`--cpu=xc2287`	Defines the target processor xc2287

Linker

The memory location process of the linker is controlled by the linker script files. If you want to change TargetLink's memory settings you have to modify these files.

The table lists the options used for the linker. For more information, refer to the *TASKING VX-toolset for C166 User Guide*.

Option (LC_OPTS)	Result/Description
`--define=__CPU__=xc2287`	Defines a macro used in the linker script file
`--define=XC2287_96F`	Defines a macro used in the linker script file
`--optimize=0`	No optimization

Renesas RH850 (Renesas RH850/F1L_R7F7010354)

Introduction

The evaluation boards that are equipped with Renesas RH850/F1L R7F7010354 microcontrollers, and are supported by the Target Simulation Module (TSM) are described. In addition, the compilers that can be used for these microcontrollers and are supported by TargetLink are described.

Where to go from here

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Evaluation Boards

Renesas YRH850F1L_R7F7010354

Technical characteristics

The Renesas YRH850F1L_R7F7010354 evaluation board has the following characteristics:

Microcontroller unit The board uses the R7F7010354 microcontroller.

On-Chip Memory	Size
FLASH ROM	2 MB
RAM	160 kB

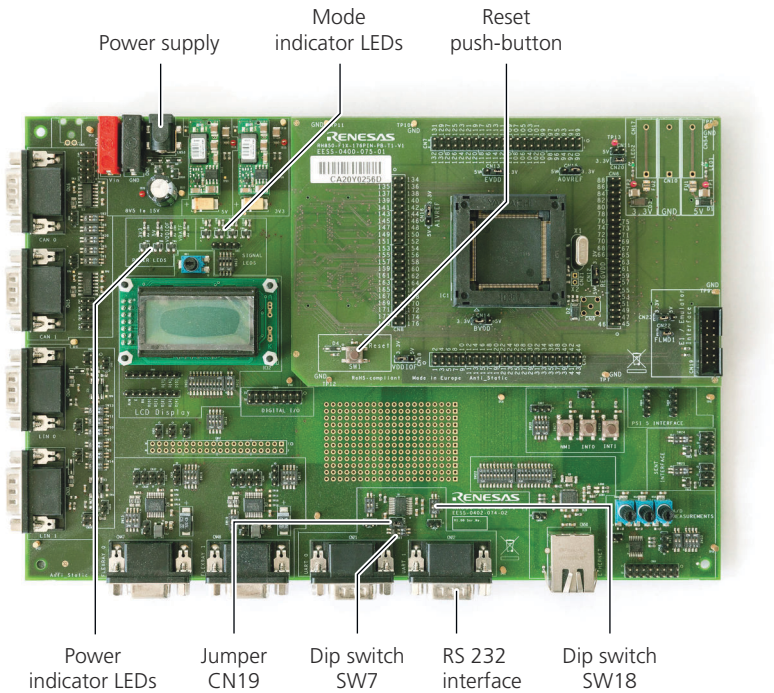
Onboard memory No onboard memory installed.

System clock PIL simulation is performed at 40 MHz.

Interface TargetLink uses the RS232 interface for program download and processor-in-the-loop (PIL) simulation.

Important hardware elements

The following illustration shows the Renesas YRH850F1L_R7F7010354 evaluation board. Only components that are relevant for operating the board or simulating in PIL simulation mode are labeled. These are described in more detail below.



LEDs

Power indicator LEDs After you connect the board to the power supply, the power indicator LEDs are light up.

Mode indicator LEDs These LEDs indicate the following modes:

- When the board is switched on or reset, the boot loader starts automatically. The mode indicator LEDs show a running light.
- After a successful download, the boot loader automatically starts the application. The mode indicator LEDs flash alternately.

Power

Power supply Connect a plug-in power supply unit (+12 V= / 1.2 A) to the power connector. After you connect the board to the power supply, the power indicator LEDs light up.

Reset push-button Resets the evaluation board.

Jumpers and switches

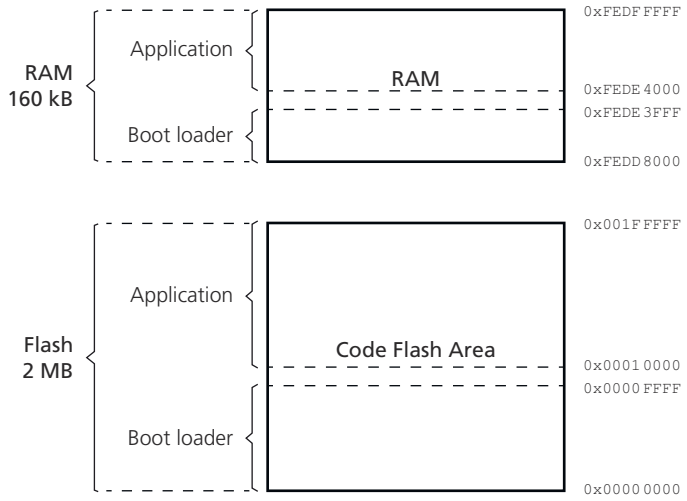
The jumpers and dip switches must be set as follows (✓ means closed, and – means open).

DipSwitch	Setting
SW 7	Off
SW 18	On

Jumper	1–2
CN19	✓

Memory configuration

The following illustration shows the memory configuration in detail:



Download

Note

Use an RS-232 extension cross cable to connect the evaluation board to the host PC.

When you switch on or resetthe Renesas YRH850F1L_R7F7010354, the boot loader starts automatically. The mode indicator LEDs show a running light.

When you download an application for PIL simulation (PIL application), the loader program of the host PC communicates with the loader program of the Renesas YRH850F1L_R7F7010354 via the RS232 interface.

1. The unreserved flash memory areas are cleared, the mode indicator LEDs flash concurrently.
2. The loader of the host PC sends an executable image of the application to the unreserved flash memory areas.
3. After a successful download, the board's loader automatically starts the application. The mode indicator LEDs flash alternately.

To check whether board and serial interface work correctly, connect the Renesas YRH850F1L_R7F7010354to an ASCII terminal. After reset or power-on, the board should send the following message to the host PC (baud rate of 115,200 bps with 8 data bits, none parity, one stop bit, xon/xoff flow control):

```
TargetLink Renesas YRH850F1L_R7F7010354 Flashloader (115200 Baud) V1.8.0
a) Erase FLASH
b) Program FLASH
c) Execute Program
d) Verify Program
```

Compilers

Green Hills RH850 C Compiler

Introduction

This section shows the various options for the compiler, assembler, and linker that influence the generated code. These options are specified in the corresponding makefile.

Compiler versions

The following compiler versions are supported:

Renesas YRH850F1L_R7F7010354	Green Hills 2019

Compiler

This table lists the options used for the compiler:

Option (CC_OPTS)	Result/Description
`-fsoft`	Uses Software Floating point
`-cpu=rh850g3k`	The compiler produces code for the Renesas RH850F1L device.
`-Ospeed`	Optimizes for speed, even if code becomes larger.

Assembler

This table lists the options used for the assembler:

Option (AS_OPTS)	Result/Description
`-cpu=rh850g3k`	The compiler produces code for the Renesas RH850F1L device.

Linker

This table lists the options used for the linker:

Option (LD_OPTS)	Result/Description
`-cpu=rh850g3k`	The compiler produces code for the Renesas RH850F1L device.

Renesas SH-2 (Renesas SH-2A-FPU/SH72513)

Introduction

The evaluation boards that are equipped with Renesas SH-2A-FPU/SH72513 microcontrollers, and are supported by the Target Simulation Module (TSM) are described. In addition, the compilers that can be used for these microcontrollers and are supported by TargetLink are described.

Where to go from here

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Compilers..... 74

Evaluation Boards

Renesas SDK72513

Support information

Note

The Renesas SH72513 evaluation board (SDK72513) is no longer distributed by dSPACE but is still supported for downward compatibility.

Technical characteristics

The Renesas SH72513 evaluation board (SDK72513) has the following characteristics:

Microcontroller unit The board uses the SH72513 microcontroller.

On-Chip Memory	Size
FLASH ROM	2 MB
RAM	128 kB

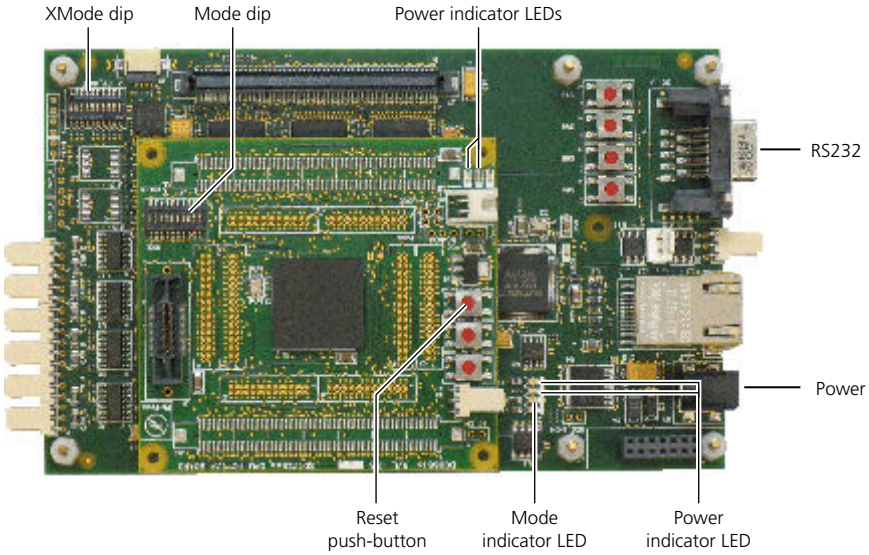
Onboard memory No onboard memory installed.

System clock PIL simulation is performed at 160 MHz.

Interface TargetLink uses the RS232 interface for program download and processor-in-the-loop (PIL) simulation.

Important hardware elements

The following illustration shows the Renesas SH72513 evaluation board (SDK72513). Only components that are relevant for operating the board or simulating in PIL simulation mode are labeled. These are described in more detail below.



LEDs

Power indicator LEDs After you connect the board to the power supply, the red power indicator LEDs light up.

Application indicator LED This LED indicates the following modes:

- When the board is switched on or reset, the boot loader starts automatically. The mode indicator LED flashes slowly when the boot loader is ready.
- After a successful download, the boot loader automatically starts the application. Then the mode indicator LED flashes fast.

Power

Power supply Use the 5 V= power supply delivered with the board. After you connect the board to the power supply, the red power indicator LEDs light up.

Reset push-button Resets the evaluation board.

Jumpers and switches

Note

Do not change the jumper settings. Leave them in their default positions.

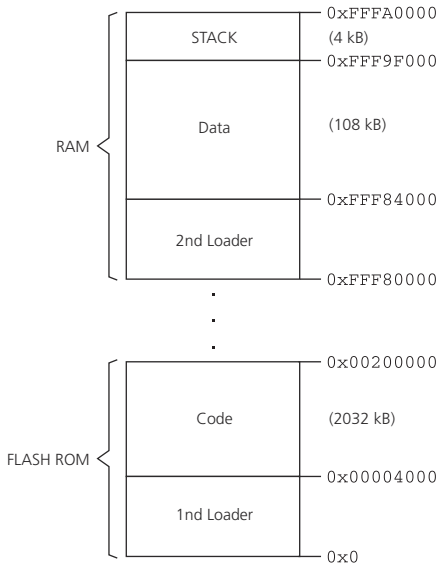
The dip switches must be set as follows.

Dip Switch:	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**
Mode	Off	Off	On	On	On	On	Off	Off	Off	On

Dip Switch:	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**
XMode	Off	Off	Off	Off	Off	Off	Off	Off	On	On

Memory configuration

The following illustration shows the memory configuration in detail:



Download

The power supply of the SDK72513 must be switched on. Resetting or switching on the SDK72513 starts a loader program. The mode indicator LED blinks once the loader is running.

When downloading an application for PIL simulation (PIL application), the loader program of the host PC communicates with the loader program of the SDK72513 via the RS232 interface.

Note

Use a serial extension cable to connect the evaluation board to the host PC.

After the flash memory has successfully been programmed, and the SDK72513 is powered/reset, the SDK72513 sends the following message to the host PC (baud rate of 57,600 bps with 8 data bits, none parity, and one stop bit):

```
TargetLink SDK72513 FlashLoader (57600 Baud) V1.5.1
a) Erase FLASH
b) Program FLASH
c) Execute Program
d) Verify Program
```

Compilers

Renesas SH Series C Compiler

Introduction

The various options for the compiler and assembler that influence the generated code are described. These options are specified in the corresponding makefile.

Compiler versions

The following compiler versions are supported:

Renesas SH72513 System Development Kit	Renesas 9.4

Compiler

This table lists the options used for the compiler. Some options are valid for specific compiler versions only.

Option (CC_OPTS)	Result/Description
`/cp=sh2afpu`	Produces code for SH-2A-FPU processors.
`/Goptimize`	Enables intermodule optimization.
`/m=1`	Save `MACH` and `MACL` registers.
`/op=1`	Enables compiler optimization.
`/speed`	Optimizes for speed.

Assembler

This table lists the options used for the assembler. Some options are valid for specific compiler versions only.

Option (AS_OPTS)	Result/Description
`/cpu=sh2afpu`	Assembles code for SH-2A-FPU processors.

Linker command file

The memory location process of the linker is controlled by the temporary linker command file (`ld.rsp`). This file is created while the makefile is being processed and is deleted automatically after a successful build process.

Renesas SH-2 (Renesas SH-2E/SH7058)

Introduction

The evaluation boards that are equipped with Renesas SH-2/SH7058 microcontrollers, and are supported by the Target Simulation Module (TSM) are described. In addition, the compilers that can be used for these microcontrollers and are supported by TargetLink are described.

Where to go from here

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Evaluation Boards

Renesas EVB7058

Support information

Note

The Renesas SH7058 evaluation board (Renesas EVB7058) is no longer distributed by dSPACE but is still supported for downward compatibility.

Technical characteristics

The Renesas EVB7058 evaluation board has the following characteristics:

Microcontroller unit The board uses the HD64E7058 microcontroller.

On-Chip Memory	Size
RAM	48 kB
FLASH ROM	1024 kB

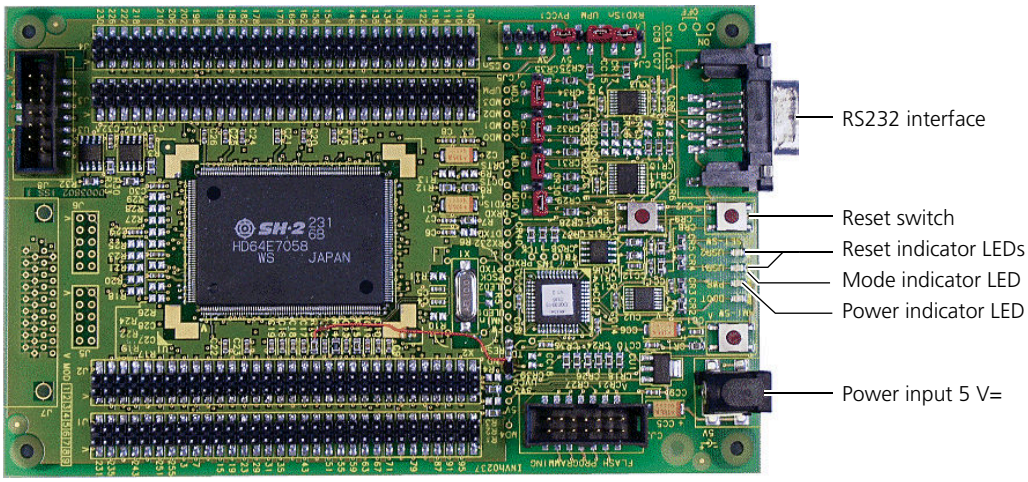
Onboard memory No onboard memory installed.

System clock PIL simulation is performed at 80 MHz.

Interface TargetLink uses the RS232 interface for program download and processor-in-the-loop (PIL) simulation.

Important hardware elements

The following illustration shows the Renesas SH7058 evaluation board . Only components that are relevant for operating the board or simulating in PIL simulation mode are labeled. These are described in more detail below.



Note

Do not change the jumper settings. Leave them in their default positions.

LEDs

Power indicator LED After you connect the board to the power supply, the red power indicator LED lights up.

Mode indicator LED This LED indicates the following modes:

- When the board is switched on or reset, the boot loader starts automatically. The mode indicator LED flashes slowly when the boot loader is ready.
- After a successful download, the boot loader automatically starts the application. Then the mode indicator LED flashes fast.

Reset indicator LEDs As long as the Reset push-button is being pressed the Reset indicator LEDs light.

Power

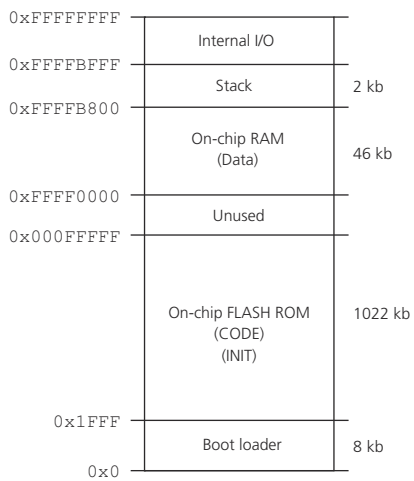
Power supply Connect a stabilized power supply (exactly 5 V=) to the terminals indicated in the photo above.

When you switch on the power supply, you should always push the reset switch once so that the evaluation board inherits a defined status.

Reset switch Resets the evaluation board.

Memory configuration

The following illustration shows the memory configuration in detail:



The PIL application can be placed in the address range `0x00002000 ... 0x000FFFFF`. The address range `0x00000000 ... 0x00001FFF` is reserved for the boot loader.

Download

The power supply of the Renesas EVB7058 must be switched on, indicated by the Power indicator LED lit.

When you download an application for PIL simulation (PIL application), the loader program of the host PC communicates with the loader program of the Renesas EVB7058 via the RS232 interface.

After the flash memory is programmed successfully, the Renesas EVB7058 sends the following message to the host PC (baud rate of 57,600 bps with 8 data bits, none parity, and one stop bit):

```
TargetLink SH7058 Bootloader (57600 Baud) V1.0
a) Erase FLASH
b) Program FLASH
c) Execute Program
```

Note

Use the serial extension cable that is delivered with the Renesas EVB7058 to connect the board to the host PC.

Compilers

Renesas SH Series C Compiler

Introduction

The various options for the compiler and assembler that influence the generated code are described. These options are specified in the corresponding makefile.

Compiler versions

The following compiler versions are supported:

Renesas EVB7058	Renesas 9.3

Compiler

This table lists the options used for the compiler. Some options are valid for specific compiler versions only.

Option (CC_OPTS)	Result/Description
`/cp=sh2e`	Produces code for SH2e processors.
`/pi=0`	Generates position-dependent codes for the program section.
`/nodeb`	Generates no additional debug information.
`/st=d`	Places string data in the data section.
`/Goptimize`	Enables intermodule optimization.
`/m=1`	Saves `MACH` and `MACL`.
`/op=1`	Enables compiler optimization.
`/speed`	Optimizes for speed.
`/noinl`	No automatic inline expansion.
`/c=m` or `/c=a`	Generates machine code or assembly code. A source file parsing process before compilation determines whether machine code (`/c=m`) or assembly code (`/c=a`) is generated. If assembly statements are found, `/c=a` is set.

Assembler

This table lists the options used for the assembler. Some options are valid for specific compiler versions only.

Option (AS_OPTS)	Result/Description
`/cpu=sh2e`	Specifies SH2e processors.
`/nodeb`	No additional debug information.

Linker command file

The memory location process of the linker is controlled by the temporary linker command file (ld.rsp). This file is created while the makefile is being processed and will be deleted automatically after a successful build process. If you want to change TargetLink's default memory settings you have to modify the corresponding lines of the makefile, which define the contents of the linker command file. The most important instructions are listed below. For detailed information, refer to the corresponding linker manual.

This table lists the instructions for defining the contents of the linker command file. Some instructions are valid for specific compiler versions only.

Instruction	Result/Description
`optimize`	Enables intermodule optimization.
`show=symbol`	Outputs a symbol name list to a module.
`INPUT <objectfilename>.objLIB <libfilename>.lib`	Specifies the names of the object (INPUT) and library (LIB) files that have to be linked for the target program.
`PRINT <application name>.mapOUTPUT <application name>.abs`	Generates a MAP file named `<application name>.map` and an output file named `<application name>.abs`.
`entry __startlabel`	Marks the beginning of the assembler start-up code with __startlabel. After download the HDI debugger starts the program at this position.
`rom=D=R start=P,C,D,B,R/<hexaddress1>`	Makes the linker place the different sections in the memory starting at <hexaddress1> and using the given order. Via the <hexaddress1> value, you can place the program in the on-chip or onboard RAM and select the `fast memory` or `big memory` configuration for the SH2eEVB.It also reserves RAM for certain ROM sections (initial values for variables). During startup these ROM sections are copied to the reserved RAM.
`start STACK(<hexaddress2>)`	Makes the stack start at <hexaddress2>. The size is defined in the startup code.

Renesas V850E2 (Renesas V850E2/Fx4-µPD70F4012)

Introduction

The evaluation boards that are equipped with Renesas V850E2/Fx4-µPD70F4012 microcontrollers, and are supported by the Target Simulation Module (TSM) are described. In addition, the compilers that can be used for these microcontrollers and are supported by TargetLink are described.

Where to go from here

Information in this section

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Evaluation Boards

Renesas AB_050_Fx4

Technical characteristics

The Renesas AB_050_Fx4 evaluation board has the following characteristics:

Microcontroller unit The board uses the V850E2/FL4 µPD70F4012 microcontroller.

On-Chip Memory	Size
RAM	144 kB
FLASH ROM	2048 kB

Onboard memory No onboard memory installed.

System clock PIL simulation is performed at 80 MHz.

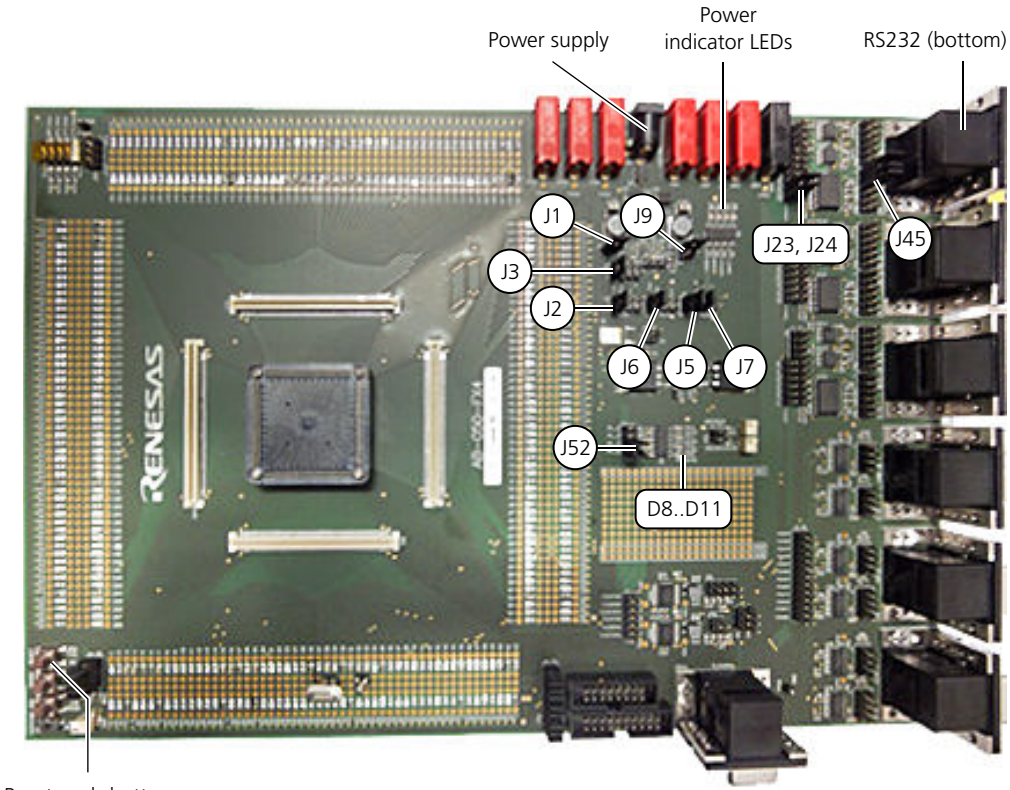
Interface TargetLink uses the RS232 interface for program download and processor-in-the-loop (PIL) simulation.

Note

Use the bottom connector.

Important hardware elements

The following illustration shows the Renesas AB_050_Fx4 evaluation board. Only components that are relevant for operating the board or simulating in PIL simulation mode are labeled. These are described in more detail below.



LEDs

Power indicator LEDs (D4...D7) After you connect the board to the power supply, the power indicator LEDs light up.

Mode indicator LEDs (D8+D9) These LEDs indicate the following modes:

- When the board is switched on or reset, the boot loader starts automatically. The LEDs flash synchronously.
- After a successful download, the boot loader automatically starts the application. The LEDs flash alternately.

Power

Power supply Connect a plug-in power supply unit (12 V=) to the power connector shown above.

Reset push-button Resets the evaluation board.

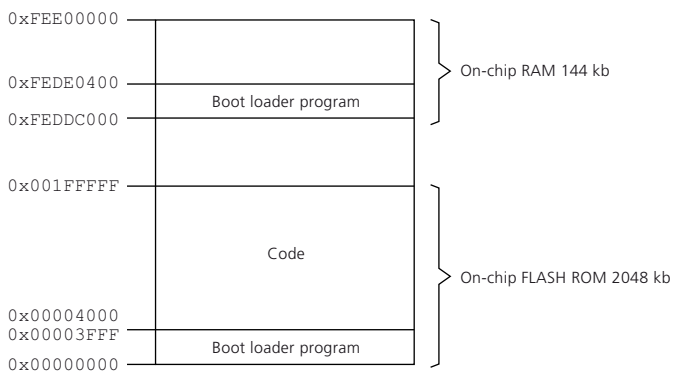
Jumpers and switches

The jumpers and dip switches must be set as follows:

Jumper	Setting
Power supply:	
J1	1-2: On
J2	1-2: On, other: Off
J3	1-2: On, other: Off
J5	1-2: On
J6	1-2: On, other: Off
J7	1-2: On, other: Off
J9	1-2: On, other: Off
RS232 interface:	
J23	1-2: On
J24	1-2: On
J45	1-2: On 3-4: On 5-6: On
LEDs:	
J52	P1_4: On P1_5: On
Oscillator	
16 MHz	Pin 28+29

Memory configuration

The following illustration shows the memory configuration in detail:



The production code application can be placed in the address range 0x00004000-0x001FFFFF. 0x00000000 ... 0x00003FFF and 0xFEDDC000 ... 0xFEDE0400 is reserved for the boot loader program.

Download

Note

Use a serial extension cable to connect the evaluation board to the host PC.

A loader program is located in the on-chip flash memory of the Renesas AB_050_Fx4. After applying power to the board, the loader is automatically started.

To download an application for PIL simulation, a loader of the host PC communicates with the loader of the board. The loader of the host PC sends an executable image of the application to the board. The loader of the board receives the image and saves it into the on-chip Program FLASH of the Renesas AB_050_Fx4. Therefore the unreserved FLASH is erased when the download is being started.

To download programs you have to use a baud rate of 115,200 bps with 8 data bits, no parity, one stop bit and xon/xoff as flow control.

To check whether board and serial interface work correctly, connect the Renesas AB_050_Fx4 to an ASCII terminal. After reset or power-on, the board should send the following message to the host PC (baud rate of 115,200 bps with 8 data bits, none parity, one stop bit, xon/xoff flow control):

```
TargetLink AB_050_Fx4_70F4012 FlashLoader (115200 Baud) V1.5.1
a) Erase FLASH
b) Program FLASH
c) Execute Program
d) Verify Program
```

Compilers

Green Hills V8xx C Compiler

Introduction

The various options for the compiler, assembler, and linker that influence the generated code are described. These options are specified in the corresponding makefile.

Compiler versions

The following compiler versions are supported:

Renesas AB_050_Fx4_70F4012	Green Hills 2019

Compiler

This table lists the options used for the compiler:

Option (CC_OPTS)	Result/Description
`-cpu= v850e2v3`	The compiler produces code for the V850E2 core.
`-sda= 1088`	Enables Small Data Area optimization without size restriction.
`-Ospace`	Enables all the -O optimizations except those which are known to increase code size.

Assembler

This table lists the options used for the assembler:

Option (AS_OPTS)	Result/Description
`-cpu= v850e2v3`	The assembler generates code for the V850E2 core.

Linker

This table lists the options used for the linker:

Option (LD_OPTS)	Result/Description
`-cpu= v850e2v3`	The linker uses libraries for the V850E2 core.

The memory location process of the linker is controlled by the linker command file `linkcmd.lk`. If you want to change TargetLink's default memory settings you have to modify this file. For detailed information, refer to the corresponding linker manual.

ARM Cortex (Texas Instruments TMS570LC43)

Introduction

The evaluation boards that are equipped with Texas Instruments TMS570LC43, an ARM Cortex-R5F derivative, microcontrollers, and are supported by the Target Simulation Module (TSM) are described. In addition, the compilers that can be used for these microcontrollers and are supported by TargetLink are described.

Where to go from here

Information in this section

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Evaluation Boards

Texas Instruments LAUNCHXL2570LC43

Technical characteristics

The LAUNCHXL2570LC43 evaluation board has the following characteristics:

Microcontroller unit The board uses the TMS570LC series microcontroller TMS570LC4357.

On-Chip Memory	Size
FLASH ROM	4 MB
RAM	512 kB

Onboard memory No onboard memory installed.

System clock PIL simulation is performed at 150 MHz.

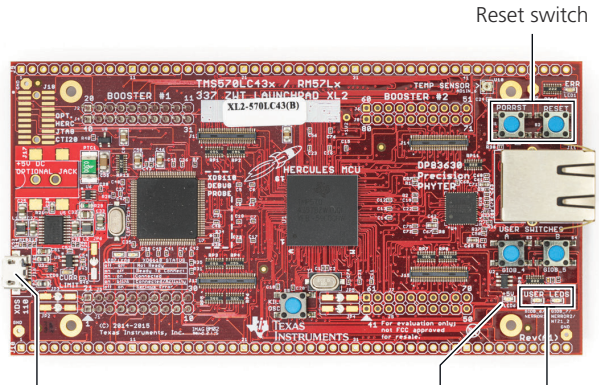
Interface TargetLink uses the USB interface for program download and processor-in-the-loop (PIL) simulation.

Note

A virtual COM port driver (XDS110 Class Application/User UART) is required. It is bundled with the Code Composer Studio or XDS Emulation Software Package.

Important hardware elements

The following illustration shows the LAUNCHXL2570LC43 Evaluation Board. Only components that are relevant for operating the board or simulating in PIL simulation mode are labeled. These are described in more detail below.



LEDs

Power indicator LED After you connect the board to the power supply, the white power indicator LED lights up.

Mode indicator LEDs These LEDs indicate the following modes:

- When the board is switched on or reset, the boot loader starts automatically. The two green mode indicator LEDs (LEDs 2and 3) of the board flash sequentially.
- When the host PC communicates with the board, the two LEDs (LEDs 2 and 3) flash synchronously.
- After a successful download, the boot loader automatically starts the application. Only the green LED 2 flashes.

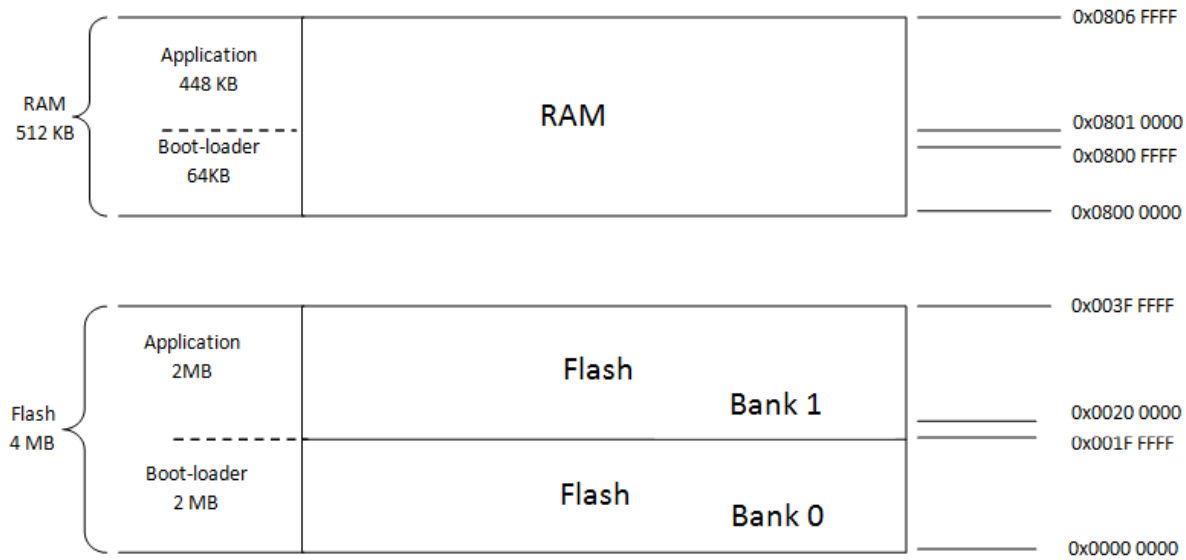
Power

Power supply Draws power from the connected USB port.

Reset push-button Resets the evaluation board.

Memory configuration

The following illustration shows the memory configuration in detail:



Download

When you switch on or reset the LAUNCHXL2570LC43, the boot loader starts automatically. The two green mode indicator LEDs (LEDs 2 and 3) of the board flash sequentially.

When you download an application for PIL simulation (PIL application), the loader program of the host PC communicates with the loader program of the LAUNCHXL2570LC43 via the USB interface.

1. The unreserved flash memory areas are cleared.
2. The loader of the host PC sends an executable image of the application to the unreserved flash memory areas. The two mode indicator LEDs on the left-hand side flash.
3. After a successful download, the board's loader automatically starts the application. The fourth mode indicator LED flashes.

To check whether board and serial interface work correctly, connect the LAUNCHXL2570LC43 to an ASCII terminal. After reset or power-on, the board should send the following message to the host PC (baud rate of 115,200 bps with 8 data bits, none parity, one stop bit):

```
TargetLink LAUNCHXL2570LC43 Flashloader (115200 Baud) V2.0.0 >
```

Compilers

Texas Instruments Code Composer Studio

Introduction

The various options for the compiler, assembler, and linker that influence the generated code are described. These options are specified in the corresponding makefile.

Compiler versions

The following compiler versions are supported:

Texas Instruments LAUNCHXL2570LC43	Texas Instruments Code Composer Studio 7.0

Compiler

This table lists the options used for the compiler:

Option (CC_OPTS)	Result/Description
`-O4`	Sets the optimization level to high.
`--silicon_version=7R5`	Selects the processor variant.
`--float_support=VFPv3D16`	Selects the type of floating-point unit.
`--code_state=32`	Generates 32-bit code.

Assembler

This table lists the options used for the assembler:

Option (AS_OPTS)	Result/Description
`--silicon_version=7R5`	Selects the processor variant.
`--float_support=VFPv3D16`	Selects the type of floating-point unit.
`--code_state=32`	Generates 32-bit code.

Linker

This table lists the options used for the linker:

Option (LD_OPTS)	Result/Description
`--rom_model`	Automatically initializes variables at run time.
`--be32`	Forces the linker to generate BE-32 object code.
`-mv7R5`	Selects the processor version.

Option (LD_OPTS)	Result/Description
`--unused_section_elimination=Off`	Disables the elimination of sections that are not required in the executable module.
--absolute_exe	Produces an absolute executable file.

Virtual Evaluation Boards

Introduction

Virtual evaluation boards are supported for the following microcontroller units. The list is sorted by microcontroller families and shows only boards included in the Target Simulation Module (TSM).

Where to go from here

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ARM Cortex (ARM Cortex-M3)

Introduction

The virtual evaluation boards, that are implemented with an instruction set simulator and simulate ARM Cortex-M3 microcontrollers, and are supported by the Target Simulation Module (TSM) are described. In addition, the compilers that can be used for these simulated microcontrollers and are supported by TargetLink are described.

TargetLink offers support for physical evaluation boards for this microcontroller family. For more information, refer to ARM Cortex (STMicroelectronics STM32F107) on page 13.

Where to go from here

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Evaluation Boards

Lauterbach TRACE32 Simulator for ARM Cortex-M3

Technical characteristics

The Lauterbach TRACE32 Simulator for the virtual ARM evaluation board (LBSIM_ARM) has the following characteristics:

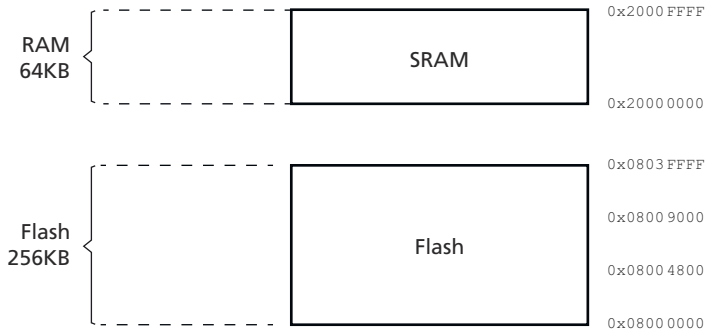
Microcontroller unit It simulates the Cortex-M3 microcontroller.

On-Chip Memory	Size
FLASH ROM	256 kB
RAM	64 kB

Interface TargetLink uses interprocess communication for processor-in-the-loop (PIL) simulation.

Memory configuration

The following illustration shows the memory configuration in detail:



Download

When downloading an application for PIL simulation, the Simulator will be started and the binary will be executed.

Physical evaluation board

TargetLink offers you support for a physical counterpart of this virtual evaluation board. For more information, refer to Emerge-Engineering ARM MEDKit on page 13.

Compilers

Keil Compiler

Introduction

The various options for the compiler, assembler, and linker that influence the generated code are described. These options are specified in the corresponding makefile.

Compiler versions

The following compiler versions are supported:

Lauterbach Simulator for ARM CortexM3	Keil 5.2

Compiler

This table lists the options used for the compiler:

Option (CC_OPTS)	Result/Description
`--cpu Cortex-M3`	Enables code generation for the selected ARM processor or architecture.

Option (CC_OPTS)	Result/Description
`--fpu=softvfp`	Specifies the target FPU architecture.
`-Ospace`	Instructs the compiler to perform optimizations to reduce image size at the expense of a possible increase in execution time.
`-Onum`	Specifies the level of optimization to be used when compiling source files.

Assembler

This table lists the options used for the assembler:

Option (AS_OPTS)	Result/Description
`--cpu Cortex-M3`	Specifies the target CPU.

Linker

This table lists the options used for the linker:

Option (LD_OPTS)	Result/Description
`--cpu Cortex-M3`	Enables the linker to determine the target ARM processor or architecture.
`--fpu=softvfp`	Specifies the target FPU architecture.

Infineon TriCore (Infineon TC275)

Introduction

The virtual evaluation boards, that are implemented with an instruction set simulator and simulate Infineon TriCore TC275 microcontrollers, and are supported by the Target Simulation Module (TSM) are described. In addition, the compilers that can be used for these simulated microcontrollers and are supported by TargetLink are described.

TargetLink offers support for physical evaluation boards for this microcontroller family. For more information, refer to Infineon TriCore (Infineon TC275) on page 56.

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Evaluation Boards

Lauterbach TRACE32 Simulator for Infineon TC 275

Technical characteristics

The Lauterbach TRACE32 Simulator for the virtual Infineon TBTC275 evaluation board has the following characteristics:

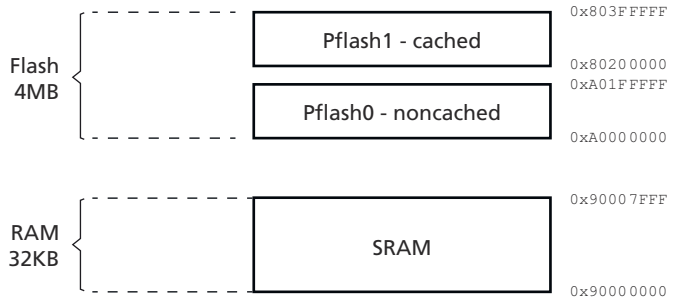
Microcontroller unit It simulates the TC275 microcontroller.

On-Chip Memory	Size
FLASH ROM	4 MB
RAM	32 kB

Interface TargetLink uses interprocess communication for processor-in-the-loop (PIL) simulation.

Memory configuration

The following illustration shows the memory configuration in detail:



Download

When downloading an application for PIL simulation , the Simulator will be started and the binary will be executed.

Physical evaluation board

TargetLink offers you support for a physical counterpart of this virtual evaluation board. For more information, refer to Infineon TBTC275 on page 56.

Compilers

Altium Tasking TriCore C Cross-Compiler

Introduction

The various options that are used for the compiler, and influence the generated code are described. These options are specified in the corresponding makefile.

Compiler versions

The following compiler versions are supported:

Lauterbach Simulator for TriCore 275	Altium TASKING TriCore VX-Toolset 4.2

Compiler

The following options are used for the compiler.

Option (CC_OPTS)	Result/Description
`--optimize=3`	Sets the optimization level as high.
`--tradeoff=4`	Sets the tradeoff between speed and size.

Option (CC_OPTS)	Result/Description
`--core=tc1.6.x`	Specifies the core used by controller.
`--align=4`	32-bit alignment of objects of four bytes or larger

Assembler

The following options are used for the assembler.

Option (AS_OPTS)	Result/Description
`--core=tc1.6.x`	Specifies the core used by controller.

Linker

The following options are used for the linker.

Option (LD_OPTS)	Result/Description
`-cpu=tc27x`	Specifies the CPU of the controller.

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