RTI FPGA Programming Blockset

Processor Interface Reference

For RTI FPGA Programming Blockset 3.11

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dSPACE

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Important Notice

Contents

About This Reference

Content

This RTI Reference is a complete description of the Real-Time Interface (RTI) blocks provided by the Processor Interface sublibrary of the RTI FPGA Programming Blockset and the FPGA specific dialog pages of the Model Interface Package for Simulink. You can use these RTI blocks to implement the data access between the processor model and the FPGA model.

Note on the license

Note

The Processor Interface sublibrary of the RTI FPGA Programming Blockset does not require the full license for the RTI FPGA Programming Blockset. It is sufficient to include existing FPGA applications to your dSPACE system.

Symbols

dSPACE user documentation uses the following symbols:

Symbol	Description
⚠ DANGER	Indicates a hazardous situation that, if not avoided, will result in death or serious injury.
⚠ WARNING	Indicates a hazardous situation that, if not avoided, could result in death or serious injury.
⚠ CAUTION	Indicates a hazardous situation that, if not avoided, could result in minor or moderate injury.
NOTICE	Indicates a hazard that, if not avoided, could result in property damage.
Note	Indicates important information that you should take into account to avoid malfunctions.
Tip	Indicates tips that can make your work easier.
	Indicates a link that refers to a definition in the glossary, which you can find at the end of the document unless stated otherwise.

Symbol	Description
🕮	Precedes the document title in a link that refers to another document.

Naming conventions

dSPACE user documentation uses the following naming conventions:

%name% Names enclosed in percent signs refer to environment variables for file and path names.

< > Angle brackets contain wildcard characters or placeholders for variable file and path names, etc.

Examples:

- Where you find terms such as `rti<XXXX>` replace them by the RTI platform support you are using, for example, `rti1007`.
- Where you find terms such as `<model>` or `<submodel>` in this document, replace them by the actual name of your model or submodel. For example, if the name of your Simulink model is `smd_1007_sl.slx` and you are asked to edit the `<model>_usr.c` file, you actually have to edit the `smd_1007_sl_usr.c` file.

RTI block name conventions All I/O blocks have default names based on dSPACE's board naming conventions:

- Most RTI block names start with the board name.
- A short description of functionality is added.
- Most RTI block names also have a suffix.

Suffix	Meaning
B	Board number (for PHS-bus-based systems)
M	Module number (for MicroAutoBox II)
C	Channel number
G	Group number
CON	Converter number
BL	Block number
P	Port number
I	Interrupt number

A suffix is followed by the appropriate number. For example, DS2201IN_B2_C14 represents a digital input block located on a DS2201 board. The suffix indicates board number 2 and channel number 14 of the block. For more general block naming, the numbers are replaced by variables (for example, DS2201IN_Bx_Cy).

Special folders

Some software products use the following special folders:

Common Program Data folder A standard folder for application-specific configuration data that is used by all users.

`%PROGRAMDATA%\dSPACE\<InstallationGUID>\<ProductName>`

or

`%PROGRAMDATA%\dSPACE\<ProductName>\<VersionNumber>`

Documents folder A standard folder for user-specific documents.

`%USERPROFILE%\Documents\dSPACE\<ProductName>\<VersionNumber>`

Local Program Data folder A standard folder for application-specific configuration data that is used by the current, non-roaming user.

`%USERPROFILE%\AppData\Local\dSPACE\<InstallationGUID>\<ProductName>`

Accessing dSPACE Help and PDF Files

After you install and decrypt dSPACE software, the documentation for the installed products is available in dSPACE Help and as PDF files.

dSPACE Help (local) You can open your local installation of dSPACE Help:

- On its home page via Windows Start Menu
- On specific content using context-sensitive help via **F1**

dSPACE Help (Web) You can access the Web version of dSPACE Help at www.dspace.com/go/help.

To access the Web version, you must have a *mydSPACE* account.

PDF files You can access PDF files via the icon in dSPACE Help. The PDF opens on the first page.

General Information on the Processor Interface

Introduction

To provide basic information on the processor interface.

Where to go from here

Information in this section

Overview of the RTI FPGA Programming Blockset

RTI FPGA Programming Blockset

The RTI FPGA Programming Blockset is a Simulink® blockset for using an FPGA model with a dSPACE system.

The blockset provides RTI blocks for implementing and simulating the interface between the FPGA mounted on a dSPACE I/O board and the board's I/O, and the interface between the dSPACE I/O board and its processor board. The following table shows the supported FPGA hardware.

Platform	Supported Hardware	Framework	Notes
MicroLabBox	MicroLabBox	*DS1202 FPGA I/O Type 1*	Remaining I/O channels cannot be used by RTI/RTLib.
		DS1202 FPGA I/O Type 1 (Flexible I/O)	Can be used together with the RTI1202 and the RTI Electric Motor (EMC) blocksets.
MicroAutoBox II	▪ MicroAutoBox II 1401/1511/1514 ▪ MicroAutoBox II 1401/1513/1514	*FPGA1401Tp1 (7K325) with Multi-I/O Module (DS1552)*	Supports the DS1552 Multi-I/O Module.
		FPGA1401Tp1 (7K325) with Multi-I/O Module (DS1552B1)	Supports the DS1552B1 Multi-I/O Module.
		FPGA1401Tp1 (7K325) with Engine Control I/O Module (DS1554)	Supports the DS1554 Engine Control I/O Module.
MicroAutoBox III	DS1514 FPGA Base Board	FPGA1403Tp1 (7K325) with Multi-I/O Module (DS1552)	Supports the DS1552 Multi-I/O Module.
		FPGA1403Tp1 (7K325) with Multi-I/O Module (DS1552B1)	Supports the DS1552B1 Multi-I/O Module.
		FPGA1403Tp1 (7K325) with Engine Control Module (DS1554)	Supports the DS1554 Engine Control I/O Module.
SCALEXIO	DS2655 FPGA Base Board (7K160)	*DS2655 (7K160) FPGA Base Board*	The SCALEXIO FPGA base boards provide 5 slots to extend the I/O capability with DS2655M1 Multi-I/O Modules, DS2655M2 Digital I/O Modules, and DS6551 Multi-I/O Modules. The assembly has no slot dependencies. With the *Inter-FPGA Interface* framework, you can use I/O module slots of the SCALEXIO FPGA base boards as inter-FPGA interfaces.
	DS2655 FPGA Base Board (7K410)	*DS2655 (7K410) FPGA Base Board*	
	DS6601 FPGA Base Board	*DS6601 (KU035) FPGA Base Board*	
	DS6602 FPGA Base Board	*DS6602 (KU15P) FPGA Base Board*	
	DS2655M1 Multi-I/O Module	*DS2655M1 I/O Module*	Can be used after you load one of the SCALEXIO FPGA base board frameworks.
	DS2655M2 Digital I/O Module	*DS2655M2 I/O Module*	
	DS6651 Multi-I/O Module	*DS6651 Multi-I/O Module*	
	Inter-FPGA connection	*Inter-FPGA Interface*	
	MGT communication bus	*DS660X_MGT*	An MGT module can be plugged into the DS6601 and DS6602 FPGA base boards.

Platform	Supported Hardware	Framework	Notes
PHS-bus-based system	DS5203 FPGA Board (7K325)	*DS5203 (7K325) with onboard I/O*	Supports the FPGA board, but no I/O modules.
		DS5203 (7K325) with Multi-I/O Module (DS5203M1)	Supports the FPGA board and the DS5203M1 Multi-I/O Module.
	DS5203 FPGA Board (7K410) without I/O Module	*DS5203 (7K410) with onboard I/O*	Supports the FPGA board, but no I/O modules.
		DS5203 (7K410) with Multi-I/O Module (DS5203M1)	Supports the FPGA board and the DS5203M1 Multi-I/O Module.

Library access

To open the library, execute one of the following methods:

- In the MATLAB Command Window, enter `rtifpga`.
- To access the RTI blocks of the library separately:

  In the Simulink Library Browser, navigate to the dSPACE RTI FPGA Programming Blockset folder.
- For MicroAutoBox II:

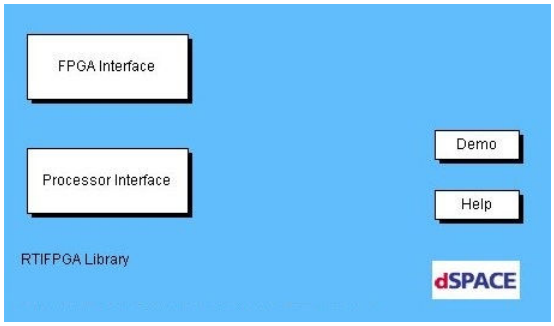
  In the RTI1401 Blockset, click one of the following blocksets:
  - MicroAutoBox II DS1511/DS1514
  - MicroAutoBox II DS1513/DS1514

  Then click FPGA Type 1.
- For MicroLabBox:

  In the DS1202 MicroLabBox FPGA I/O Type 1 blockset, Click FPGA Class 1.
- For PHS-bus-based systems:

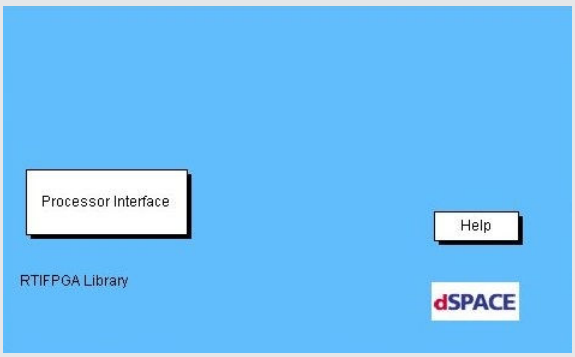
  In the DS1006 or DS1007 Blockset, click Blocksets - RTI FPGA Pr. Blockset.

If you open the block library, the blockset is displayed.



Note

The FPGA Interface library and the Demo model are only available, if you have the full license for the RTI FPGA Programming Blockset.
If you have the standard RTI license only, the blockset looks like this:



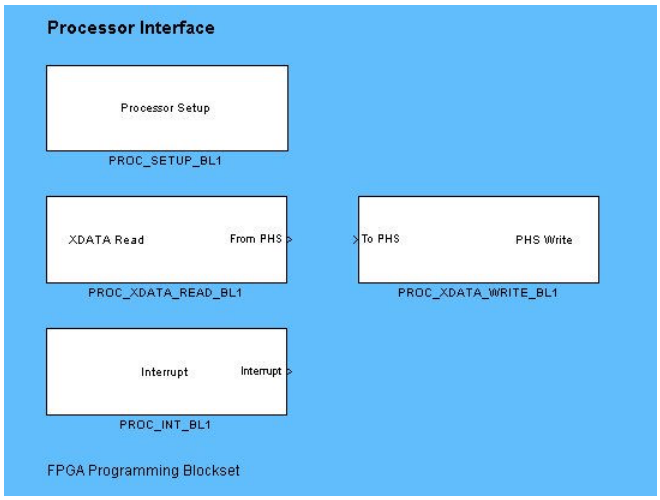
Library components

The following components are available in the RTI FPGA Programming Blockset:

FPGA Interface The RTI blocks of the FPGA INTERFACE sublibrary are used on the dSPACE I/O board that provides an FPGA, for example, the DS5203 FPGA Board. They let you configure the interface to external I/O and to a processor board, for example, a DS1007 PPC Processor Board.

For further information, refer to RTI FPGA Programming Blockset - FPGA Interface Reference 🕮.

Processor Interface The RTI blocks of the Processor Interface library are used on the dSPACE processor board to implement communication on its board-specific bus. The model on the I/O board that you want to access, for example, the DS5203 FPGA Board, must contain the related FPGA interface RTI blocks.



The Processor Interface library provides the following RTI blocks:

- Setup
  - PROC_SETUP_BL on page 20
- I/O board access via the board's internal bus (PHS bus, intermodule bus or local bus)
  - PROC_XDATA_READ_BL on page 27
  - PROC_XDATA_WRITE_BL on page 32
  - PROC_INT_BL on page 37

Note

If you use a MicroAutoBox III or a SCALEXIO system, the processor interface is implemented within the behavior model using the Model Interface Blockset for Simulink.

Demo model

If you have the full license for the RTI FPGA Programming Blockset, Simulink models are available that show how to use the RTI blocks of the RTI FPGA Programming Blockset. Double-click the **Demos** button in the blockset to open the library containing the demo models. In the next step you have to choose the demo model for the framework which you have in use. A demo model prepared for a different framework will not work. You can also find the model files at `<RCP_HIL_InstallationPath>\Demos\RTIFPGA`.

Related topics

References

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Features of the Processor Interface of the RTI FPGA Programming Blockset

Introduction

The processor interface of the RTI FPGA Programming Blockset allows you to implement the internal bus communication in the processor model.

Supported platforms

The processor interface of the RTI FPGA Programming Blockset supports the following platforms:

- MicroLabBox
- MicroAutoBox II
- PHS-bus-based systems

Main features

Specific dSPACE hardware provides a Xilinx® FPGA for which you can implement an application. The RTI FPGA Programming Blockset allows you to integrate such an FPGA model in a Simulink model that can be built to run on dSPACE hardware.

The RTI FPGA Programming Blockset is providing the **Processor Interface** sublibrary and the **FPGA Interface** sublibrary if you have the full license for the RTI FPGA Programming Blockset. Otherwise the **Processor Interface** library can be used only.

The main features of the processor interface are:

- Communication between processor board and I/O board

  You can connect the FPGA model with the processor model running on the computation node. Data exchange between the I/O board and the processor board runs via a board-specific bus.

  - DS1006/DS1007 Processor Board: **PHS bus**
  - MicroAutoBox II: **Intermodule bus**
  - MicroLabBox: **Local bus**

  You must have an FPGA_XDATA_READ_BL or FPGA_XDATA_WRITE_BL block in the FPGA model and a corresponding PROC_XDATA_WRITE_BL or PROC_XDATA_READ_BL block in the processor model to implement a communication line.
- Asynchronous tasks

  With the interrupt blocks from the FPGA interface (FPGA_INT_BL) and the processor interface, you can implement interrupt-driven tasks in the processor model triggered from the FPGA model.

Managing FPGA and processor application

The setup block of the processor interface (PROC_SETUP_BL) provides commands to manage the FPGA application and the processor application:

- Starting the build process for the FPGA model.
- Programming the generated FPGA code to the flash of the FPGA board or the RAM of the FPGA.
- Starting the build process for the processor application.
- Creating a separate burn application to explicitly program the FPGA.
- Integrating the FPGA application into the processor application to automatically program the FPGA at startup.

INI files used with the RTI FPGA Programming Blockset

There are two kinds of initialization files:

- Framework INI file

  A framework INI file contains the interface definitions for the FPGA, the FPGA board's I/O and the processor. It also contains the function-specific settings that are displayed in the dialogs of the FPGA Interface RTI blocks according to the specified function. It is therefore mainly used for configuring the FPGA Interface RTI blocks.

- FPGA model INI file

  An FPGA model INI file is created when you build an FPGA application. It allows you to include built FPGA applications in your processor application without specifying the corresponding FPGA model. For example, in the setup block for the processor model, you can specify either an FPGA subsystem or an FPGA model INI file for further actions.

Details on the access types

The FPGA framework contains the definition of the data storage areas. It specifies one data storage type as register (implemented as Flip-Flop) and one data storage type as buffer (implemented in the FPGA RAM). With the access type, you can choose the data storage that you want to use for the data exchange.

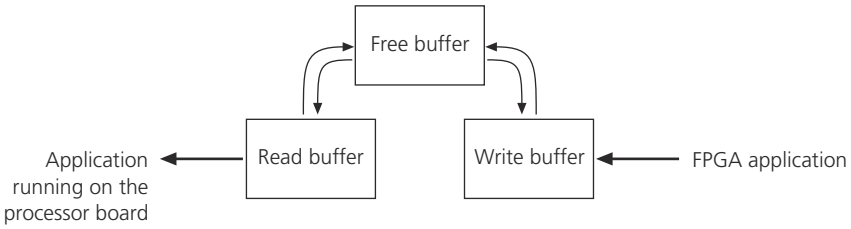
Register access Register access lets you access a scalar value in the register. The data is identified by the specified channel number. The values are transmitted element by element.

Register group access You can group registers to a register group via a common Register Group ID. All the values that belong to the same Register Group ID are synchronously updated in the FPGA subsystem.

For read access, the registers of a register group are read from the board-specific bus sequentially and then provided to the FPGA application simultaneously. For write access, the registers of a register group are sampled simultaneously in the FPGA application. These values form a consistent data group that is written to the board-specific bus.

Buffer access Buffer access lets you access a vector value in the data buffer. One specific value of the data is identified by the specified channel number and the position within the buffer.

Data exchange is implemented via a FIFO buffer that works as a swinging buffer. This means that there are two separate buffers for reading and writing, and one buffer that switches between reading and writing. Only the pointer has to be changed to switch the buffer so that no buffer has to be copied from one position to another.



Related topics

References

Processor Interface RTI Blocks (MicroAutoBox II, MicroLabBox, PHS-Bus-Based System)..... 19

Features of the Processor Interface of the Model Interface Package for Simulink

Introduction

The processor interface of the Model Interface Package for Simulink allows you to implement the internal bus communication in the processor model.

The dialogs of the model port blocks provide FPGA-specific pages that are displayed if you use the model port blocks with the RTI FPGA Programming Blockset. For instructions, refer to How to Generate a Processor Interface (RTI FPGA Programming Blockset Guide 🕮).

Supported platforms

The Model Interface Package for Simulink supports the following FPGA platforms:

- MicroAutoBox III
- SCALEXIO

Main features

Specific dSPACE hardware provides a Xilinx® FPGA for which you can implement an application. The Model Interface Package for Simulink allows you to implement the communication between the FPGA application and the processor application.

The main features of the processor interface are:

- Communication between processor board and FPGA board

  You must have an FPGA_XDATA_READ_BL or FPGA_XDATA_WRITE_BL block in the FPGA model and a corresponding model port block in the processor model to implement a communication line.
- Asynchronous tasks

  With the interrupt blocks from the FPGA interface (FPGA_INT_BL) and the processor interface, you can implement interrupt-driven tasks in the processor model triggered from the FPGA model.

For more information, refer to Introduction to the Model Interface Package for Simulink (Model Interface Package for Simulink - Modeling Guide 🕮)

Details on the access types

The FPGA framework contains the definition of the data storage areas. It specifies one data storage type as register (implemented as Flip-Flop) and one data storage type as buffer (implemented in the FPGA RAM). With the access type, you can choose the data storage that you want to use for the data exchange.

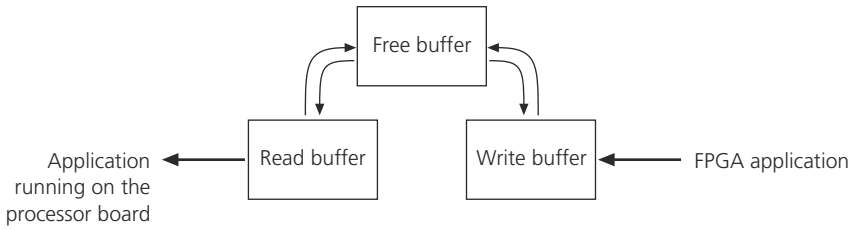
Register access Register access lets you access a scalar value in the register. The data is identified by the specified channel number. The values are transmitted element by element.

Register group access You can group registers to a register group via a common **Register Group ID**. All the values that belong to the same **Register Group ID** are synchronously updated in the FPGA subsystem.

For read access, the registers of a register group are read from the board-specific bus sequentially and then provided to the FPGA application simultaneously. For write access, the registers of a register group are sampled simultaneously in the FPGA application. These values form a consistent data group that is written to the board-specific bus.

Buffer access Buffer access lets you access a vector value in the data buffer. One specific value of the data is identified by the specified channel number and the position within the buffer.

Data exchange is implemented via a FIFO buffer that works as a swinging buffer. This means that there are two separate buffers for reading and writing, and one buffer that switches between reading and writing. Only the pointer has to be changed to switch the buffer so that no buffer has to be copied from one position to another.



Related topics

HowTos

How to Generate a Processor Interface (RTI FPGA Programming Blockset Guide 🕮)

References

Processor Interface Blocks (MicroAutoBox III, SCALEXIO)..... 41

Processor Interface RTI Blocks (MicroAutoBox II, MicroLabBox, PHS-Bus-Based System)

Introduction

The Processor Interface library provides RTI blocks that you use in the processor model of a MicroAutoBox II, MicroLabBox, or PHS-Bus-Based System to implement access to the FPGA model.

Where to go from here

Information in this section

PROC_SETUP_BL

Purpose

To manage all the FPGA subsystems in the processor model.

Where to go from here

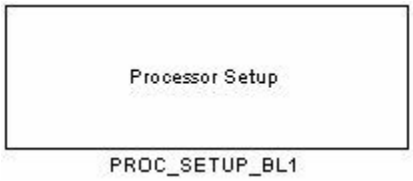
Information in this section

Information in other sections

Block Description (PROC_SETUP_BL)

Block appearance

The figure below shows the block if it is in the library.



Purpose

To manage all the FPGA subsystems of non-RTI systems in the processor model.

Supported Platforms

The PROC_SETUP_BL block supports the following platforms:

- MicroAutoBox II
- MicroLabBox
- PHS-bus-based systems

FPGA subsystems of MicroAutoBox III devices or SCALEXIO systems are managed in ConfigurationDesk.

Description

A processor model can contain several FPGA subsystems. These can be centrally managed by this block. It allows you to map an FPGA subsystem or an FPGA model INI file to one of the available FPGA boards. The assigned board numbers are displayed on the Unit pages of the corresponding FPGA RTI blocks. You can start the build process for the selected FPGA models and download them to the connected FPGA boards. You can generate the RTI blocks required for exchanging data between the processor model and an FPGA subsystem.

Related RTLib functions

This RTI block is implemented by using the following RTLib functions. You can find the descriptions of these functions in the *RTLib Reference* of the hardware used.

MicroAutoBox II

- fpga_tp1_init
- fpga_tp1_program

MicroLabBox

- IoFpga_init

  FPGA programming is done by the MicroLabBox RTLib itself to handle shared FPGA use of multicore applications correctly.

DS5203 FPGA Board

- ds5203_init
- ds5203_program

Related topics

References

Unit Page (PROC_SETUP_BL)

Purpose

To assign FPGA subsystems or FPGA model INI files to FPGA boards and to build and download the FPGA applications.

Dialog settings

Number of FPGA boards used Lets you select the number of FPGA boards you want to use with your processor application. Up to 16 FPGA boards can be connected via PHS bus or intermodule bus. The assignment of an FPGA subsystem to an FPGA board number is also displayed in the related RTI blocks added to your FPGA model.

Note

- If you use a PHS-bus-based system, this setting can be specified to the number of the available DS5203 FPGA Boards in the range 1 … 16. The board number then specifies one specific board.
  The board numbers are ordered by the PHS-bus addresses of the boards. The board with the lowest PHS-bus address gets number 1.
- If you use MicroAutoBox II/III or MicroLabBox, only one FPGA unit is available. The board number has to be set to 1.
- If you use a SCALEXIO system, the number of the available SCALEXIO FPGA base boards is in the range 1 … 16. The board number is used to distinguish between multiple FPGA boards during modeling, but you assign specific FPGA boards in ConfigurationDesk via the hardware resource assignment.

Note

If you reduce the number of FPGA boards later on, the entries of the disabled settings are cleared.

FPGA board number Displays all the possible board numbers from 1 to 16.

FPGA subsystem / INI file Lets you select the FPGA subsystem or FPGA model INI file that you want to assign to a specific FPGA board. The selection provides all the subsystems that are contained in your processor model, and all the FPGA model INI files which you specified on the Advanced page of this

block. You can select a subsystem only once, an FPGA model INI file multiple times. The specified number of FPGA boards used defines how many items are enabled for this setting.

Note

You can select an FPGA subsystem only in the **FPGA-Build/Offline simulation** model mode. An FPGA model INI file can be also assigned in the **Processor-Build** model mode. For further information on the model modes, refer to Model Configuration Page (PROC_SETUP_BL) on page 24.

Programming option Lets you select the download behavior. You can decide whether the built FPGA application is embedded into the processor application during a processor build. The processor application can be used to download the FPGA application in its initialization phase, before the processor application starts its simulation.

If you do not specify a programming option, the FPGA application will not be embedded into the processor application and not downloaded to the FPGA. If you specify that the application is to be downloaded to flash, the FPGA application starts running immediately when the hardware is powered up the next time. If you specify that the application is to be downloaded to RAM, the FPGA application must be downloaded again after each power down of the hardware.

FPGA build Lets you decide which of the FPGA subsystems are to be built or rebuilt when you click **Build**. The **Build** button is enabled if at least one FPGA build is specified and the model mode in the Model Configuration page is set to **FPGA-Build/Offline simulation**.

If FPGA build results exist for all assigned subsystems, you can switch the model mode in the Model Configuration page to **Processor-Build** to enable the **Create burn application** button. The burn application can be used to download only the FPGA applications to the associated FPGAs according to the specified programming options.

Related topics

References

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Block Description (PROC_SETUP_BL)....21
Interface Page (PROC_SETUP_BL)....24
Model Configuration Page (PROC_SETUP_BL)....24
PROC_SETUP_BL....20

Interface Page (PROC_SETUP_BL)

Purpose

To specify the processor interface model.

Dialog settings

FPGA board number Displays all the possible board numbers from 1 to 16.

FPGA model INI file Displays the FPGA subsystems and FPGA model INI files that you specified on the Unit page.

The **Generate** and **Adapt** commands are enabled for each item selected.

- If you click **Generate**, the related FPGA model is analyzed and a corresponding processor interface model is created with the blocks of the Processor Interface library.

  The PROC_XDATA blocks are automatically configured with the corresponding channel numbers, channel names, access type and format parameters.

  After you copy the generated processor model interface blocks to the processor model, you can close the generated interface model without saving.
- If you click **Adapt**, a standard Browse dialog opens for you to select an existing processor interface model to check against the associated FPGA model and update to the assigned board number.

  A pair of related blocks is recognized by all of their settings. If there is no correlation, a message is displayed to show the incompatibility of the interfaces.

  The **Adapt** command is used to update a processor interface after you specify a different FPGA board for the associated FPGA subsystem or FPGA model INI file. Only the board number is changed. If the command recognizes incompatible blocks, the board number is not changed for these blocks. The settings that define the interface (these are the channel number and the access type) are displayed in an error message, if they are not identical for the corresponding interface blocks.

Related topics

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PROC_SETUP_BL 20

Model Configuration Page (PROC_SETUP_BL)

Purpose

To configure a model containing FPGA subsystems or FPGA model INI files for RTI build actions.

Dialog settings

Model mode Lets you select the model mode:

- FPGA-Build / Offline simulation

  In this mode, you can execute the build process for the specified FPGA subsystems or FPGA model INI files and start an offline simulation. The processor model contains the FPGA subsystems or FPGA model INI files. You cannot therefore execute a build process for the processor model.

- Processor-Build

  In this mode, the FPGA subsystems or FPGA model INI files are separated from the processor model. You can execute a build process for the processor model using the Simulink Coder.

  The model is copied to a new model called `<ModelName>_rtiFPGASeparationFile.mdl` before the separation. If you reswitch to the FPGA-Build / Offline simulation model mode, this copy is used to restore the previously separated FPGA subsystems or FPGA model INI files.

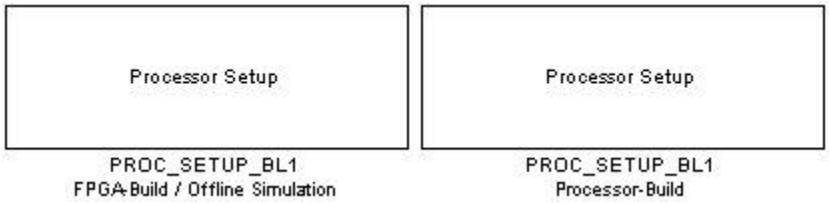
  Note

  If you want to exchange the model with other users, you must provide all the separated files or the model that is stored in the FPGA-Build / Offline Simulation model mode.

After selecting the model mode, you must activate it by clicking Switch model mode.

The default is the FPGA-Build / Offline simulation mode.

The specified model mode is displayed in the block.



Related topics

References

Advanced Page (PROC_SETUP_BL)

Purpose

To specify the FPGA model INI files used instead of FPGA subsystems.

Dialog settings

Current path Displays the folder where your current Simulink model is stored.

FPGA model INI files You can add an entry to the FPGA model INI file list by clicking **Add** and browsing for an FPGA model INI file using the opened standard file browser.

A description of the FPGA model can be available in the FPGA model INI file. To display this description, select a FPGA model ini file and click **Information**. For details on entering a FPGA model description, refer to Parameters Page (FPGA_SETUP_BL) (RTI FPGA Programming Blockset - FPGA Interface Reference 🕮).

You can delete one single entry by selecting it and then clicking **Remove**. You can delete all entries in the list by clicking **Remove all**. If you want to remove an entry that is assigned to an FPGA board, you must confirm that you want to delete it.

The added FPGA model INI files are selectable on the **Unit** page of the PROC_SETUP block to assign them to an FPGA board.

Related topics

References

PROC_XDATA_READ_BL

Purpose

To read data in the processor model that comes from the FPGA model via the board-specific bus.

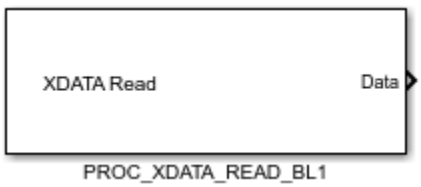
Where to go from here

Information in this section

Information in other sections

Block Description (PROC_XDATA_READ_BL)

Block appearance



Purpose

To read data in the processor model that comes from the FPGA model via the board-specific bus.

Description

This block is the counterpart to an FPGA_XDATA_WRITE_BL block in the associated FPGA subsystem. The data that the FPGA block writes to a storage can be read by the PROC_XDATA_READ_BL block.

If you have generated the block, the block settings are automatically adapted to the corresponding block in the FPGA model. If you want to configure the block manually, you must specify the same values for the board number, the access type (register or buffer) and the channel number as its counterpart in the FPGA model.

I/O characteristics

The following table describes the ports of the block in initial state:

Port	Description
Output	
Data	Outputs the data you want to read from the FPGA model via the board-specific bus. The characteristics depend on the specified bus access type.

Related RTLib functions

This RTI block is implemented by using the following RTLib functions. You can find the descriptions of these functions in the *RTLib Reference* of the hardware used.

DS5203 FPGA Board

- ds5203_read_reg
- ds5203_read_reg_grp
- ds5203_read_buf

MicroAutoBox II

- fpga_tp1_read_reg
- fpga_tp1_read_reg_grp
- fpga_tp1_read_buf

MicroLabBox

- loFpga_read_reg
- loFpga_read_reg64
- loFpga_read_reg_grp
- loFpga_read_reg_grp_mixed
- loFpga_read_buf
- loFpga_read_buf64

Related topics

References

Unit Page (PROC_XDATA_READ_BL)

Purpose

To configure read access to the FPGA model in the processor model via a board-specific bus.

Dialog settings

If the model interface has been generated using the PROC_SETUP_BL block, all the relevant parameters are automatically specified, for example, the access type and the channel number.

Blocks in the processor model and the FPGA subsystem that belong together are recognized by the identical values for the board number, the access type and the channel number.

Board number Lets you select a board number in the range 1 … 16. The specified board number must correspond to the board number of the related RTI block in the FPGA subsystem. If your system contains several boards of the same type, RTI uses the board number to distinguish between them. For further information, refer to Unit Page (PROC_SETUP_BL) on page 22.

Access type Lets you specify the storage you want to read from. The value must correspond to the associated block in the FPGA subsystem.

Channel number Lets you specify a channel number that corresponds to the storage. The range depends on the specified access type. The value must correspond to the associated block in the FPGA subsystem.

Enable multiple access Lets you allow the same channel to be specified for data exchange in several blocks of the processor model. For example, this allows you to access the same channel from different tasks.

Register In description

If you select Register or Register64 as the access type, the data is read from a register. The register features, for example, the channel number range, depend on the framework used. For further information, refer to the framework-specific block settings of the corresponding FPGA_XDATA_WRITE block.

I/O characteristics The following table describes the ports of the block when used in register access mode:

Port	Description
Output	
Data	Outputs the data you want to read from the FPGA model via the board-specific bus. Data type: Double Data width: 1

Buffer In description

If you select Buffer or Buffer64 as the access type, the data is read from a buffer. The buffer features, for example, the channel number range, depend on the framework used. For further information, refer to the framework-specific block settings of the corresponding FPGA_XDATA_WRITE block.

I/O characteristics The following table describes the ports of the block when used in buffer access mode:

Port	Description
Output	
Data	Outputs the data you want to read from the FPGA model via the board-specific. Data type: Double Data width: 1 … 32765 The data width is the specified buffer size and not the number of read values.
Status	Represents the current status of the output. Data type: UInt32 Data width: 3 ▪ Status[0]: Indicates the data length read from the buffer. This is the number of valid elements in the Data vector. ▪ Status[1]: Indicates whether the data in the buffer is new. 1 means that the data in the buffer is new, 0 means that the data in the buffer is old. ▪ Status[2]: Indicates whether a buffer overflow occurred. 1 means that an overflow occurred, 0 means that no overflow occurred.

Related topics

References

Parameters Page (PROC_XDATA_READ_BL)

Purpose

To display the data configuration of the related RTI block in the FPGA model.

Dialog settings

After generating the model interface using the PROC_SETUP_BL block, all the relevant parameters of the corresponding blocks in the FPGA model are automatically specified, for example, the binary point position and the data format.

Binary point position Displays the fixed- or floating-point format that is specified for the Data outport of the corresponding block in the FPGA model.

Format Displays the data format that is specified for the Data outport of the corresponding block in the FPGA model.

Register group ID Only valid for Register access type.

Displays the register group ID for the Data outport of the corresponding block in the FPGA model.

Buffer size Only valid for Buffer access type.

Displays the buffer size that is specified for the Data outport of the corresponding block in the FPGA model.

Related topics

References

PROC_XDATA_WRITE_BL

Purpose

To write data from the processor model to the FPGA model via the board-specific bus.

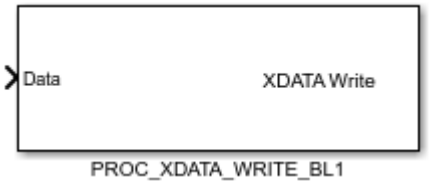
Where to go from here

Information in this section

Information in other sections

Block Description (PROC_XDATA_WRITE_BL)

Block appearance



Purpose

To write data from the processor model to the FPGA model via the board-specific bus.

Description

This block is the counterpart to an FPGA_XDATA_READ_BL block in the associated FPGA subsystem. The data that the corresponding FPGA block reads from the storage can be written by the PROC_XDATA_WRITE_BL block.

If you have generated the block, the block settings are automatically adapted to the corresponding block in the FPGA model. If you want to configure the block manually, you must specify the same values for the board number, the access type (register or buffer) and the channel number as its counterpart in the FPGA model.

I/O characteristics

The following table describes the ports of the block in its initial state:

Port	Description
Input	
Data	Lets you input the data you want to write to the FPGA model via the board-specific bus.

Related RTLib functions

This RTI block is implemented by using the following RTLib functions. You can find the descriptions of these functions in the *RTLib Reference* of the hardware used.

DS5203 FPGA Board

- ds5203_write_reg
- ds5203_write_reg_grp
- ds5203_write_buf

MicroAutoBox II

- fpga_tp1_write_reg
- fpga_tp1_write_reg_grp
- fpga_tp1_write_buf

MicroLabBox

- loFpga_write_reg
- loFpga_write_reg64
- loFpga_write_reg_grp
- loFpga_write_reg_grp_mixed
- loFpga_write_buf
- loFpga_write_buf64

Related topics

References

Unit Page (PROC_XDATA_WRITE_BL)

Purpose

To configure write access to the FPGA model in the processor model via the board-specific bus.

Dialog settings

If the model interface has been generated, all the relevant parameters are automatically specified, for example, the access type and the channel number.

Board number Lets you select a board number in the range 1 … 16. The specified board number must correspond to the board number of the related RTI block in the FPGA subsystem. If your system contains several boards of the same type, RTI uses the board number to distinguish between them. For further information, refer to Unit Page (PROC_SETUP_BL) on page 22.

Access type Lets you specify the storage you want to write to. The value must correspond to the associated block in the FPGA subsystem.

Channel number Lets you specify a channel number that corresponds to the storage. The range depends on the specified access type. The value must correspond to the associated block in the FPGA subsystem.

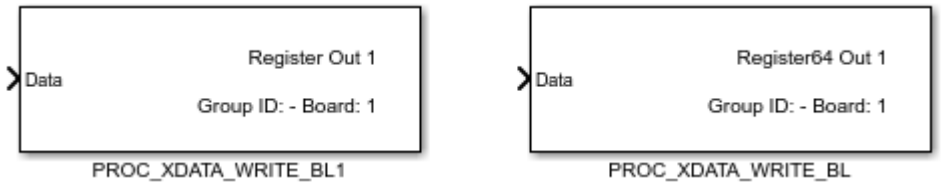
Initialization only The block inport disappears if Initialization only is set. The associated communication channel is written only during the initialization phase.

Initial value Lets you specify the initial value that is written at the initialization phase.

Enable multiple access Lets you allow the same channel to be specified for data exchange in several blocks of the processor model. For example, this allows you to access the same channel from different tasks.

Register Out description

If you select Register or Register64 as the access type, the data is written to a register. The register features, for example, the channel number range, depend on the framework used. For further information, refer to the framework-specific block settings of the corresponding FPGA_XDATA_READ block.



I/O characteristics The following table describes the ports of the block when used in register access mode:

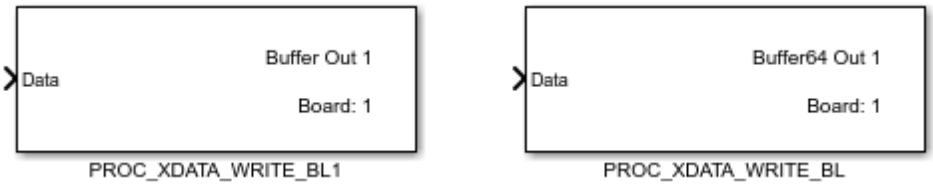
Port	Description
Input	
Data	Lets you input the data you want to write to the FPGA model via the board-specific bus. Data type: Double Data width: 1

Note

The data must be convertible to the data format specified in the corresponding FPGA_XDATA_READ_BLx block in the FPGA subsystem.

Buffer Out description

If you select Buffer or Buffer64 as the access type, the data is written to a buffer. The buffer features, for example, the channel number range, depend on the framework used. For further information, refer to the framework-specific block settings of the corresponding FPGA_XDATA_READ block.



I/O characteristics The following table describes the ports of the block when used in buffer access mode:

Port	Description
Input	
Data	Lets you input the data you want to write to the FPGA model via the board-specific bus. Data type: Double Data width: 1 ... Buffer size, according to the corresponding block in the FPGA subsystem.

Note

The data must be convertible to the data format specified in the corresponding FPGA_XDATA_READ_BLx block in the FPGA subsystem.

Related topics

References

Block Description (PROC_XDATA_WRITE_BL)....32
Parameters Page (PROC_XDATA_WRITE_BL)....36
PROC_XDATA_WRITE_BL....32

Parameters Page (PROC_XDATA_WRITE_BL)

Purpose

To display the data configuration of the related RTI block in the FPGA model.

Dialog settings

After generating the model interface using the PROC_SETUP_BL block, all the relevant parameters of the corresponding blocks in the FPGA model are automatically specified, for example, the binary point position and the data format.

Binary point position Displays the fixed- or floating-point format that is specified for the Data outport of the corresponding block in the FPGA model.

Format Displays the data format that is specified for the Data outport of the corresponding block in the FPGA model.

Register group ID Only valid for Register access type.

Displays the register group ID for the Data outport of the corresponding block in the FPGA model.

Buffer size Only valid for Buffer access type.

Displays the buffer size that is specified for the Data outport of the corresponding block in the FPGA model.

Related topics

References

Block Description (PROC_XDATA_WRITE_BL)....32
PROC_XDATA_WRITE_BL....32
Unit Page (PROC_XDATA_WRITE_BL)....34

PROC_INT_BL

Purpose

To receive an interrupt from the FPGA model to trigger an asynchronous task in the processor model.

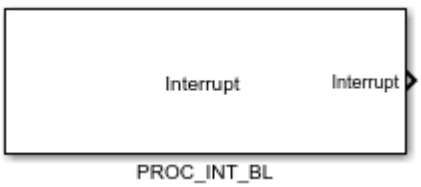
Where to go from here

Information in this section

Information in other sections

Block Description (PROC_INT_BL)

Block appearance



Purpose

To receive an interrupt from the FPGA model to trigger an asynchronous task in the processor model.

Description

An interrupt that is provided by the FPGA_INT_BL block in the FPGA model must be received by a PROC_INT_BL block in the processor model. The interrupt is transmitted via the board-specific bus.

I/O characteristics

The following table describes the ports of the block in its initial state:

Port	Description
Output	
Interrupt	Outputs an interrupt on the specified channel by performing a function call to enable a function-call subsystem. Data type: Function call

Related RTLib functions

This RTI block is implemented by using the following RTLib functions. You can find the descriptions of these functions in the *RTLib Reference* of the hardware used.

DS5203 FPGA Board

- Interrupt Functions

MicroAutoBox II

- Interrupt Functions

MicroLabBox

- Interrupt Functions

Related topics

References

PROC_INT_BL 37
Unit Page (PROC_INT_BL) 39

Unit Page (PROC_INT_BL)

Purpose

To configure the interrupt in the processor model.

Dialog settings

If the model interface has been generated using the PROC_SETUP_BL block, all the relevant parameters are automatically specified, for example, the channel number.

Board number Lets you select a board number in the range 1 … 16. The specified board number must correspond to the board number of the related RTI block in the FPGA subsystem. If your system contains several boards of the same type, RTI uses the board number to distinguish between them. For further information, refer to Unit Page (PROC_SETUP_BL) on page 22.

Channel number Lets you select a channel number. The range of the selectable interrupt channels depend on the specified framework or piggyback module. The value must correspond to the associated block in the FPGA subsystem.

Channels that were already assigned to other blocks are not displayed in the list.

Related topics

References

Processor Interface Blocks (MicroAutoBox III, SCALEXIO)

Introduction

The Model Interface Package for Simulink provides model port blocks that you use in the behavior model to implement access to the FPGA custom function block in ConfigurationDesk.

If you use the RTI FPGA Programming Blockset, the model port blocks provide FPGA-specific functionalities.

Where to go from here

Information in this section

Information in other sections

For reference information on the common functionalities of the Model Interface Package for Simulink, refer to the following topic.

Model Interface Blockset (Model Interface Package for Simulink Reference 🕮)

Data Inport Block

Purpose

Data Inport blocks receive data from function ports of an FPGA custom function in ConfigurationDesk.

Where to go from here

Information in this section

Block Description (Data Inport Block)

Block display

Purpose

To prepare the behavior model for receiving data from a FPGA custom function in ConfigurationDesk.

Dialog pages

The dialog of the Data Inport block provides the following pages:

- The ConfigurationDesk page lets you view information about the Data Inport block in the related ConfigurationDesk project and application.

  For more information, refer to ConfigurationDesk Page (Data Inport Block) (Model Interface Package for Simulink Reference 🕮).
- The Signal Configuration page lets you view and change the available ports and their configurations.

  For more information, refer to Signal Configuration Page (Data Inport Block) (Model Interface Package for Simulink Reference 🕮).
- The Block Configuration page lets you view and change the block configuration.

  For more information, refer to Block Configuration Page (Data Inport Block) (Model Interface Package for Simulink Reference 🕮).

- The Block Connections page lets you configure data connections between model port blocks and XDATA_WRITE_BL blocks from the RTI FPGA Programming Blockset.

Block Connections Page (Data Inport Block)

Purpose

To configure data connections between model port blocks and XDATA_WRITE_BL blocks from the RTI FPGA Programming Blockset.

Page access

This page is displayed only if the model port block is used with the RTI FPGA Programming Blockset.

Configuration

Enable Block Connections Lets you enable/disable the block connection properties on the Block Connections page.

Board number (1 .. 256) Lets you select a board number in the range 1 … 256.

Type Lets you specify an access type. The following access types are available:

- Buffer
- Register
- Buffer64
- Register64

Channel number (1 .. 256) Lets you specify a channel number in the range of 1 … 256.

Subchannel number (1 .. 256) Lets you specify a subchannel to use Simulink buses for data exchange. Up to 256 subchannels can be used for each channel. Subchannel number 1 of a buffer channel must always be used, the other subchannels can be used in any order.

For more information on subchannels, refer to Using Subchannels for Data Exchange (RTI FPGA Programming Blockset Guide 🕮).

If no Simulink bus is used, leave this parameter at the default value 1.

Corresponding FPGA Blocks Displays a list of links to the blocks from the RTI FPGA Programming Blockset whose Goto tag corresponds to that of the model port block. The list is empty by default. You must press the  button to refresh the list.

 Refreshes the Corresponding FPGA Blocks list.

Related topics

References

Block Configuration Page (Data Inport Block) (Model Interface Package for Simulink Reference 🕮)
ConfigurationDesk Page (Data Inport Block) (Model Interface Package for Simulink Reference 🕮)
Signal Configuration Page (Data Inport Block) (Model Interface Package for Simulink Reference 🕮)

Data Outport Block

Purpose

Data Outport blocks send data to function ports of an FPGA custom function in ConfigurationDesk.

Where to go from here

Information in this section

Block Description (Data Outport Block)

Block display

Purpose

To prepare the behavior model for sending data to an FPGA custom function in ConfigurationDesk.

Dialog pages

The dialog of the Data Outport block provides the following pages:

- The ConfigurationDesk page lets you view information about the Data Outport block in the related ConfigurationDesk project and application.

  For more information, refer to ConfigurationDesk Page (Data Outport Block) (Model Interface Package for Simulink Reference 🕮).
- The Signal Configuration page lets you view and change the available ports and their configurations.

  For more information, refer to Signal Configuration Page (Data Outport Block) (Model Interface Package for Simulink Reference 🕮).
- The Block Configuration page lets you view and change the block configuration.

  For more information, refer to Block Configuration Page (Data Outport Block) (Model Interface Package for Simulink Reference 🕮).

- The Block Connections page lets you configure data connections between model port blocks and XDATA_READ_BL blocks from the RTI FPGA Programming Blockset.

Block Connections Page (Data Outport Block)

Purpose

To configure data connections between model port blocks and XDATA_READ_BL blocks from the RTI FPGA Programming Blockset.

Page access

This page is displayed only if the model port block is used with the RTI FPGA Programming Blockset.

Configuration

Enable Block Connections Lets you enable/disable the block connection properties on the Block Connections page.

Board number (1 .. 256) Lets you select a board number in the range 1 … 256.

Type Lets you specify an access type. The following access types are available:

- Buffer
- Register
- Buffer64
- Register64

Channel number (1 .. 256) Lets you specify a channel number in the range of 1 … 256.

Subchannel number (1 .. 256) Lets you specify a subchannel to use Simulink buses for data exchange. Up to 256 subchannels can be used for each channel. Subchannel number 1 of a buffer channel must always be used, the other subchannels can be used in any order.

For more information on subchannels, refer to Using Subchannels for Data Exchange (RTI FPGA Programming Blockset Guide 🕮).

If no Simulink bus is used, leave this parameter at the default value 1.

Corresponding FPGA Blocks Displays a list of links to the blocks from the RTI FPGA Programming Blockset whose Goto tag corresponds to that of the model port block. The list is empty by default. You must press the  button to refresh the list.

 Refreshes the Corresponding FPGA Blocks list.

Related topics

References

Block Configuration Page (Data Outport Block) (Model Interface Package for Simulink Reference 🕮)
ConfigurationDesk Page (Data Outport Block) (Model Interface Package for Simulink Reference 🕮)
Signal Configuration Page (Data Outport Block) (Model Interface Package for Simulink Reference 🕮)

Hardware-Triggered Runnable Function Block

Purpose

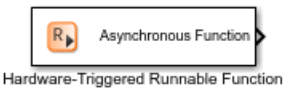
Hardware-Triggered Runnable Function blocks let you execute parts of a model asynchronously triggered by an event of an FPGA custom function block. For this purpose, a **Hardware-Triggered Runnable Function** block exports a function-call subsystem as a runnable function. In ConfigurationDesk, you can then create a task from the runnable function and an asynchronous event.

Where to go from here

Information in this section

Block Description (Hardware-Triggered Runnable Function Block)

Block display



Purpose

To model asynchronous tasks in ConfigurationDesk that are triggered by an FPGA custom function block.

Dialog pages

The dialog of the **Hardware-Triggered Runnable Function** block provides the following pages:

- The **ConfigurationDesk** page lets you view information about the **Hardware-Triggered Runnable Function** block in the related ConfigurationDesk project and application.

  For more information, refer to ConfigurationDesk Page (Hardware-Triggered Runnable Function Block) (Model Interface Package for Simulink Reference 🕮).
- The **Runnable Function** page lets you view and change the runnable function configuration.

For more information, refer to Runnable Function Page (Hardware-Triggered Runnable Function Block) (Model Interface Package for Simulink Reference 🕮).

- The **Block Configuration** page lets you view and change the block configuration.

  For more information, refer to Block Configuration Page (Hardware-Triggered Runnable Function Block) (Model Interface Package for Simulink Reference 🕮).
- The **Block Connections** page lets you configure data connections between model port blocks and **FPGA_INT_BL** blocks from the RTI FPGA Programming Blockset.

Block Connections Page (Hardware-Triggered Runnable Function Block)

Purpose

To configure data connections between model port blocks and **FPGA_INT_BL** blocks from the RTI FPGA Programming Blockset.

Page access

This page is displayed only if the model port block is used with the RTI FPGA Programming Blockset.

Configuration

Enable Block Connections Lets you enable/disable the block connection properties on the **Block Connections** page.

Board number (1 .. 256) Lets you select a board number in the range 1 … 256.

Type Displays the access type. For **Hardware-Triggered Runnable Function** blocks, the access type is always *Interrupt*.

Channel number (1 .. 256) Lets you specify a channel number in the range of 1 … 256.

The valid value range depends on the used FPGA base board:

- DS2655: 1 … 8
- DS6601: 1 … 16
- DS6602: 1 … 16
- MicroAutoBox III: 1 … 8

Corresponding FPGA Blocks Displays a list of links to the blocks from the RTI FPGA Programming Blockset whose Goto tag corresponds to that of the model port block. The list is empty by default. You must press the button to refresh the list.

 Refreshes the **Corresponding FPGA Blocks** list.

Related topics

References

Block Configuration Page (Hardware-Triggered Runnable Function Block) (Model Interface Package for Simulink Reference 🕮)
ConfigurationDesk Page (Hardware-Triggered Runnable Function Block) (Model Interface Package for Simulink Reference 🕮)
Runnable Function Page (Hardware-Triggered Runnable Function Block) (Model Interface Package for Simulink Reference 🕮)