DS1104 R&D Controller Board

Features

Release 2021-A – May 2021

dSPACE

How to Contact dSPACE

Mail:	dSPACE GmbH Rathenaustraße 26 33102 Paderborn Germany
Tel.:	+49 5251 1638-0
Fax:	+49 5251 16198-0
E-mail:	info@dspace.de
Web:	http://www.dspace.com

How to Contact dSPACE Support

If you encounter a problem when using dSPACE products, contact your local dSPACE representative:

- Local dSPACE companies and distributors: http://www.dspace.com/go/locations
- For countries not listed, contact dSPACE GmbH in Paderborn, Germany.
  Tel.: +49 5251 1638-941 or e-mail: support@dspace.de

You can also use the support request form: http://www.dspace.com/go/supportrequest. If you are logged on to mydSPACE, you are automatically identified and do not need to add your contact details manually.

If possible, always provide the relevant dSPACE License ID or the serial number of the CmContainer in your support request.

Software Updates and Patches

dSPACE strongly recommends that you download and install the most recent patches for your current dSPACE installation. Visit http://www.dspace.com/go/patches for software updates and patches.

Important Notice

This publication contains proprietary information that is protected by copyright. All rights are reserved. The publication may be printed for personal or internal use provided all the proprietary markings are retained on all printed copies. In all other cases, the publication must not be copied, photocopied, reproduced, translated, or reduced to any electronic medium or machine-readable form, in whole or in part, without the prior written consent of dSPACE GmbH.

© 2001 - 2021 by:
dSPACE GmbH
Rathenaustraße 26
33102 Paderborn
Germany

This publication and the contents hereof are subject to change without notice.

AUTERA, ConfigurationDesk, ControlDesk, MicroAutoBox, MicroLabBox, SCALEXIO, SIMPHERA, SYNECT, SystemDesk, TargetLink and VEOS are registered trademarks of dSPACE GmbH in the United States or other countries, or both. Other brand names or product names are trademarks or registered trademarks of their respective companies or organizations.

Contents

About This Document

Content

This document provides feature-oriented access to the information you need to implement your control models on the DS1104.

Symbols

dSPACE user documentation uses the following symbols:

Symbol	Description
DANGER	Indicates a hazardous situation that, if not avoided, will result in death or serious injury.
WARNING	Indicates a hazardous situation that, if not avoided, could result in death or serious injury.
CAUTION	Indicates a hazardous situation that, if not avoided, could result in minor or moderate injury.
NOTICE	Indicates a hazard that, if not avoided, could result in property damage.
Note	Indicates important information that you should take into account to avoid malfunctions.
Tip	Indicates tips that can make your work easier.
	Indicates a link that refers to a definition in the glossary, which you can find at the end of the document unless stated otherwise.
	Precedes the document title in a link that refers to another document.

Naming conventions

dSPACE user documentation uses the following naming conventions:

%name% Names enclosed in percent signs refer to environment variables for file and path names.

< > Angle brackets contain wildcard characters or placeholders for variable file and path names, etc.

Special folders

Some software products use the following special folders:

Common Program Data folder A standard folder for application-specific configuration data that is used by all users.

`%PROGRAMDATA%\dSPACE\<InstallationGUID>\<ProductName>`

or

`%PROGRAMDATA%\dSPACE\<ProductName>\<VersionNumber>`

Documents folder A standard folder for user-specific documents.

`%USERPROFILE%\Documents\dSPACE\<ProductName>\<VersionNumber>`

Local Program Data folder A standard folder for application-specific configuration data that is used by the current, non-roaming user.

`%USERPROFILE%\AppData\Local\dSPACE\<InstallationGUID>\<ProductName>`

Accessing dSPACE Help and PDF Files

After you install and decrypt dSPACE software, the documentation for the installed products is available in dSPACE Help and as PDF files.

dSPACE Help (local) You can open your local installation of dSPACE Help:

- On its home page via Windows Start Menu
- On specific content using context-sensitive help via **F1**

dSPACE Help (Web) You can access the Web version of dSPACE Help at www.dspace.com.

To access the Web version, you must have a *mydSPACE* account.

PDF files You can access PDF files via the icon in dSPACE Help. The PDF opens on the first page.

Introduction to the Features of the DS1104

Introduction

The *DS1104 R&D Controller Board* upgrades your PC to a development system for rapid control prototyping (RCP).

The real-time hardware – based on a PowerPC microprocessor – and its I/O interfaces make the board ideally suited for developing controllers in various fields – in both industry and university.

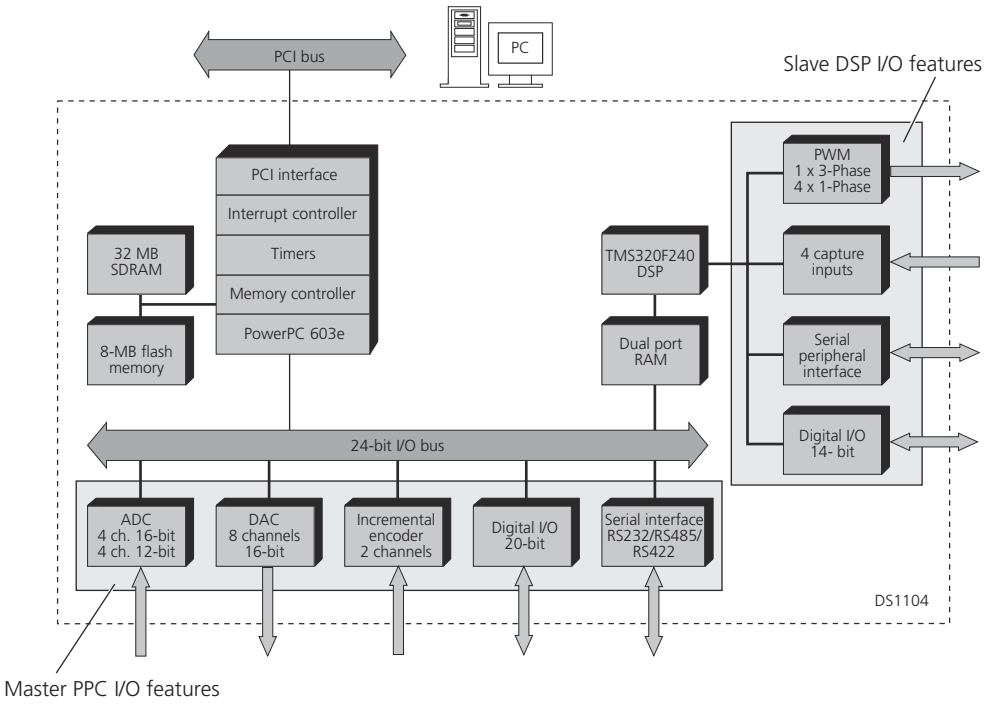
Where to go from here

Information in this section

Board Architecture

System overview

The following illustration gives an overview of the architecture and the functional units of the DS1104:



Connection to External Devices

Details on connectors

There are three different ways to connect external devices to the DS1104. To access the I/O units of the master PPC and the slave DSP, connect external devices

- to the 100-pin I/O connector P1 of the DS1104, or
- to the adapter cable with two 50-pin Sub-D connectors P1A and P1B, that are included in the DS1104 hardware package, or
- to the optional connector panel CP1104 or the optional combined connector/LED panel CLP1104, which provides an additional array of LEDs indicating the states of the digital signals.

Memory Features

Memory sections

The DS1104 is equipped with two memory sections:

- Global memory
  - 32-MByte synchronous DRAM (SDRAM) for applications and data
  - Fully cached (L1 cache)
- Flash memory
  - 8 MByte, divided into 4 blocks of 2 MByte each
  - 6.5 MByte can be used for a user-specific application
  - 1.5 MByte are reserved for the boot firmware
  - 8-bit read / write access by master PPC
  - At least 100,000 erase cycles possible

Tip

An application loaded to the flash memory will be started automatically after reboot. Loading an application to the flash memory therefore avoids having to load the application manually whenever you reboot your host PC. For more information, refer to Handling Real-Time Applications with ControlDesk (DS100x, DS110x, MicroAutoBox II, MicroLabBox – Software Getting Started 🕮).

Memory map

The memory map of the DS1104 is shown in the following table:

Address Range	Description
0000 0000H … 1FF FFFFH	32-MByte cached global memory area
FF80 0000H … FF9F FFFFH	8-MByte flash memory (4 blocks of 2 MByte each at the same address)
FF90 0100H	Boot vector

Timer Features

Timer characteristics

The DS1104 board is equipped with 6 timer devices. The timers are driven by the bus clock, whose frequency is referred to as BCLK.

Using ControlDesk, you can get the current BCLK value via the Properties controlbar; refer to Board Details Properties (ControlDesk Platform Management 🕮).

The timers have the following characteristics:

- Time Base Counter
  - Free-running 64-bit up counter driven by BCLK/4
  - Used for measurement of relative and absolute times
  - Used for time-stamping
- Timers 0 … 3
  - 32-bit down counters driven by BCLK/8
  - Used as trigger source for periodic tasks
  - When the counter reaches 0, the timer generates an interrupt and the counter is reloaded with the value of the period register.
- Decrementer
  - 32-bit down counter driven by BCLK/4
  - Used as trigger source for periodic tasks
  - When the counter reaches 0 the timer generates an interrupt. A new counter value is set by software in the timer interrupt service routine.

Timer names

The names of the timers listed above are the names of the hardware timer devices used by RTLib. They differ from the names used by RTI Timer Interrupt block:

Timer Device Name Used by RTLib	Timer Interrupt Name Used by RTI
Timer 0	Timer A interrupt
Timer 1	Timer B interrupt
Timer 2	– (not supported by RTI)
Timer 3	– (not supported by RTI)
Decrementer	Timer C interrupt

Timer interrupts for periodic events

Timers 0 … 3 and the Decrementer provide timer interrupts that you can use to trigger periodic events in a real-time application. These 32-bit down counters generate an interrupt whenever they reach 0. Then the timer is automatically reloaded.

For information on the interrupt handling, see Interrupts Provided by the DS1104 on page 61. For details on using the timers as interrupt sources in a model, see Timer Interrupt Block (RTI and RTI-MP Implementation Reference 🕮).

Note

With RTI, only Timer 0, Timer 1 and the Decrementer can be used as timer interrupt sources in a model. In timer-driven models, RTI automatically uses Timer 0 as the default sample rate timer. In this case, only Timer 1 and the Decrementer can be used as additional timer interrupt sources.

Measurement of absolute times

The Time Base Counter can be used to measure both relative and absolute execution times in handcoded applications. This allows you to get profiling information (execution times), or to implement time delays. For details, refer to Time Interval Measurement (DS1104 RTLib Reference 🕮).

The Time Base Counter also performs the turnaround time measurement of the tasks in RTI models.

Time-stamping

The Time Base Counter provides the time base for time-stamping. Time-stamping supplements data points with their time values. This means that the plots are not distorted even if data points are sampled at irregular intervals, for example, when asynchronous tasks are simulated. For details on the time-stamping feature, see:

- Time-Stamping and Data Acquisition (RTI and RTI-MP Implementation Guide 🕮)
- Time-Stamping (DS1104 RTLib Reference 🕮)

Host Interface

Characteristics

The DS1104 provides a PCI interface requiring a single 5 V PCI slot. The interface has the following characteristics:

- Access from/to the host PC via 33 MHz-PCI interface

  The interface serves the board setup, program downloads and runtime data transfers from/to the host PC.

  Note

  For PCI interfaces, 33 MHz is the standard frequency. The host interface of the DS1104 is therefore designed to handle frequencies in the range 33 MHz ±5%. To indicate whether this range is exceeded, the DS1104 is equipped with a status LED that is lit whenever the host PC's PCI bus used for the DS1104 runs at a clock rate lower than 5 MHz or higher than 35 MHz.

- Interrupt line

  The host interface provides a bidirectional interrupt line: Via this line, the host PC can send interrupt requests to the master PPC and vice versa. Both the host PC and the master PPC can monitor the state of the interrupt line to detect when the corresponding interrupt service is finished.

Autobooting Real-Time Applications on dSPACE Hardware

Introduction

Some dSPACE real-time systems support autobooting a real-time application. Autobooting allows you to use such a system as a stand-alone system without a connection to the host PC.

Basics on autobooting dSPACE hardware

You can enable dSPACE hardware to start an application from flash memory or from a USB mass storage device, for example. On power-up or restart of the hardware, this application is automatically downloaded to the hardware and started on it.

After a real-time application autoboots on dSPACE hardware, you can connect ControlDesk to the hardware. ControlDesk then detects the running real-time application. ControlDesk therefore does not unload the application when online calibration is started.

Autobooting an application on DS1104

The board provides flash memory and thus supports autobooting. To prepare autobooting, you must load the application to the flash memory. For instructions, refer to How to Load an Application to the Flash Memory of dSPACE Real-Time Hardware (ControlDesk Platform Management 🕮).

Related topics

HowTos

How to Load an Application to the Flash Memory of dSPACE Real-Time Hardware (ControlDesk Platform Management 🕮)

Features Provided by the Master PPC

Where to go from here

Information in this section

Master PPC Features

Basics on the Master PPC Features

Hardware features

The DS1104's main processing unit, MPC8240, consists of

- A PowerPC 603e microprocessor (master PPC) on which your control models will be implemented
  - Running at 250 MHz (CPU clock)
  - Containing a 16-KByte L1 data cache
  - Containing a 16-KByte L1 instruction cache
- An interrupt controller (see Interrupts Provided by the DS1104 on page 61)
- A synchronous DRAM controller
- Several timers
- A PCI interface (5 V, 32 bit, 33 MHz)

I/O features of the master PPC

The master PPC controls the following I/O features of the DS1104:

- ADC Unit on page 15
- DAC Unit on page 16
- Bit I/O Unit on page 18
- Incremental Encoder Interface on page 20
- Serial Interface on page 26

These features can be fully programmed from RTI and RTLib.

Standard I/O

Where to go from here

Information in this section

ADC Unit

Characteristics

The master PPC on the DS1104 controls an ADC unit featuring two different types of A/D converters:

- 1 A/D converter (ADC1) multiplexed to four channels (signals ADCH1 … ADCH4).The input signals of the converter are selected by a 4:1 input multiplexer. The A/D converters have the following characteristics:
  - 16-bit resolution
  - ±10 V input voltage range
  - ± 5 mV offset error
  - ± 0.25% gain error
  - > 80 dB (at 10 kHz) signal-to-noise ratio (SNR)
- 4 parallel A/D converters (ADC2 … ADC5) with one channel each (signals ADCH5 … ADCH8). The A/D converters have the following characteristics:
  - 12-bit resolution
  - ±10 V input voltage range
  - ± 5 mV offset error
  - ± 0.5% gain error
  - > 70 dB signal-to-noise ratio (SNR)

Read modes

The A/D converters can be used in polling and in non-polling mode. In polling mode, the conversion values can be read if the end-of-conversion flag in the ADC control register is set to 1. In non-polling mode, the conversion values are read immediately without waiting on the completion of the conversion. The non-polling functions are ds1104_adc_read_ch_immediately (DS1104 RTLib Reference 🕮) and ds1104_adc_read_conv_immediately (DS1104 RTLib Reference 🕮).

Interrupt on end of conversion

The converters ADC1 … ADC5 provide an interrupt at the end of A/D conversion. For information on interrupt handling, see Interrupts Provided by the DS1104 on page 61.

Synchronization with ST1PWM signal

Starting AD conversion can be synchronized with PWM signal generation or an external trigger source. For details, see Synchronizing I/O Features of the Master PPC on page 32.

RTI/RTLib support

You can access the master PPC's ADC unit via RTI1104 and RTLib1104. For details, see

- ADC Unit in the *DS1104 RTI Reference*
- ADC Unit in the *DS1104 RTLib Reference*

Connecting external devices

For a circuit diagram and information on the electrical characteristics and signal conditioning of the ADC unit, see Connecting External Devices to the dSPACE System (DS1104 Hardware Installation and Configuration 🕮).

I/O mapping

The following table shows the mapping between the RTI blocks and RTLib functions and the corresponding pins used by the ADC unit.

Related RTI Blocks	Channel (RTI)	Related RTLib Functions	Channel (RTLib)	Conn. Pin	Sub-D Pin	Pin on CP/CLP	Signal
DS1104MUX_ADC	Ch 1	See ADC Unit (DS1104 RTLib Reference 🕮)	Ch 1	P1 100	P1A 50	CP1	ADCH1
	Ch 2		Ch 2	P1 99	P1B 50	CP2	ADCH2
	Ch 3		Ch 3	P1 96	P1A 33	CP3	ADCH3
	Ch 4		Ch 4	P1 95	P1B 33	CP4	ADCH4
DS1104ADC_Cx	Ch 5		Ch 5	P1 92	P1A 16	CP5	ADCH5
	Ch 6		Ch 6	P1 91	P1B 16	CP6	ADCH6
	Ch 7		Ch 7	P1 88	P1A 48	CP7	ADCH7
	Ch 8		Ch 8	P1 87	P1B 48	CP8	ADCH8

DAC Unit

Characteristics

The master PPC on the DS1104 controls a D/A converter. It has the following characteristics:

- 8 parallel DAC channels (signals DACH1 … DACH8)
- 16-bit resolution
- ±10 V output voltage range

- ± 1 mV offset error, 10 µV/K offset drift
- ± 0.1% gain error, 25 ppm/K gain drift
- > 80 dB (at 10 kHz) signal-to-noise ratio (SNR)
- Transparent and latched mode

Transparent and latched mode

The DAC unit of the master PPC can be driven in two operating modes:

- In the *transparent mode*, the converted value is output immediately.
- In the *latched mode*, the converted value is output after a strobe signal. This allows you to write output values to more than one channel, and output the values simultaneously.

Synchronization with ST1PWM signal

Updating DAC outputs can be synchronized with PWM signal generation or an external trigger source. Refer to Synchronizing I/O Features of the Master PPC on page 32.

Power-up state

On power-up of the DS1104, each output channel of the DAC unit is set to 0 V.

RTI/RTLib support

You can access the master PPC's DAC unit via RTI1104 and RTLib1104. For details, see

- DAC Unit in the *DS1104 RTI Reference*
- DAC Unit in the *DS1104 RTLib Reference*

Connecting external devices

For a circuit diagram and information on the electrical characteristics and signal conditioning of the DAC unit, see Connecting External Devices to the dSPACE System (DS1104 Hardware Installation and Configuration 🕮).

I/O mapping

The following table shows the mapping between the RTI block and RTLib functions and the corresponding pins used by the DAC unit.

Related RTI Block	Related RTLib Functions	Channel	Conn. Pin	Sub-D Pin	Pin on CP/CLP	Signal
DS1104DAC_Cx	See DAC Unit (DS1104 RTLib Reference 🕮)	Ch 1	P1 84	P1A 31	CP9	DACH1
		Ch 2	P1 83	P1B 31	CP10	DACH2
		Ch 3	P1 80	P1A 14	CP11	DACH3
		Ch 4	P1 79	P1B 14	CP12	DACH4
		Ch 5	P1 76	P1A 46	CP13	DACH5
		Ch 6	P1 75	P1B 46	CP14	DACH6
		Ch 7	P1 72	P1A 29	CP15	DACH7
		Ch 8	P1 71	P1B 29	CP16	DACH8

Bit I/O Unit

Characteristics

The master PPC on the DS1104 controls a bit I/O unit with the following characteristics:

- 20-bit digital I/O
- Direction selectable for each channel individually
- ±5 mA maximum output current
- TTL voltage range for input and output

Tip

You can also use the bit I/O unit provided by the slave DSP, which contains 14-bit digital I/O. For details, see Slave DSP Bit I/O Unit on page 37.

Power-up state

On power-up of the DS1104, all digital I/O lines – each having a pull-up resistor to +5 V – are in input mode.

RTI/RTLib support

You can access the master PPC's bit I/O unit via RTI1104 and RTLib1104. For details, see

- Bit I/O Unit in the *DS1104 RTI Reference*
- Bit I/O Unit in the *DS1104 RTLib Reference*

Connecting external devices

For a circuit diagram and information on the electrical characteristics and signal conditioning of the bit I/O unit, see Bit I/O (DS1104 Hardware Installation and Configuration 🕮).

I/O mapping

The following table shows the mapping between the RTI blocks and RTLib functions and the corresponding pins used by the Bit I/O unit.

Related RTI Blocks	Related RTLib Functions	Bit	Conn. Pin	Sub-D Pin	Pin on CP/CLP	Signal
DS1104BIT_IN_Cx/ DS1104BIT_OUT_Cx	See Bit I/O Unit (DS1104 RTLib Reference 🕮)	Bit 0	P1 68	P1A 12	CP17 20	IO0
		Bit 1	P1 67	P1B 12	CP17 2	IO1
		Bit 2	P1 66	P1A 28	CP17 21	IO2
		Bit 3	P1 65	P1B 28	CP17 3	IO3
		Bit 4	P1 64	P1A 44	CP17 23	IO4
		Bit 5	P1 63	P1B 44	CP17 5	IO5
		Bit 6	P1 62	P1A 11	CP17 24	IO6
		Bit 7	P1 61	P1B 11	CP17 6	IO7
		Bit 8	P1 60	P1A 27	CP17 26	IO8
		Bit 9	P1 59	P1B 27	CP17 8	IO9
		Bit 10	P1 58	P1A 43	CP17 27	IO10
		Bit 11	P1 57	P1B 43	CP17 9	IO11
		Bit 12	P1 56	P1A 10	CP17 29	IO12
		Bit 13	P1 55	P1B 10	CP17 11	IO13
		Bit 14	P1 54	P1A 26	CP17 30	IO14
		Bit 15	P1 53	P1B 26	CP17 12	IO15
		Bit 16	P1 52	P1A 42	CP17 32	IO16
		Bit 17	P1 51	P1B 42	CP17 14	IO17
		Bit 18	P1 50	P1A 9	CP17 33	IO18
		Bit 19	P1 49	P1B 9	CP17 15	IO19

Incremental Encoder Interface

Where to go from here

Information in this section

Basics on the Incremental Encoder Interface

Characteristics

The master PPC on the DS1104 controls an incremental encoder interface. It has the following characteristics:

- Input channels for two digital incremental encoders
- Support of single-ended TTL and differential RS422 signals
- 24-bit position counter
- 1.65 MHz maximum encoder line count frequency.

  For details on the encoder signal level and shape, as well as on the available encoder line range, see Encoder Signals and Line Count on page 21.
- Line termination for differential inputs
- Power supply for incremental encoders (5V and 0.1A)

  For details, see Line Termination and Power Supply on page 24.

Synchronization with ST1PWM signal

The incremental encoder position strobe can be synchronized with PWM signal generation or an external trigger source. Refer to Synchronizing I/O Features of the Master PPC on page 32.

Reaction on index found

When the index is found, both incremental encoder interface channels provide an interrupt. For information on the interrupt handling, see Encoder Interrupts on page 64.

The encoder position can automatically be reset when the index is found.

RTI/RTLib support

You can access the master PPC's incremental encoder interface via RTI1104 and RTLib1104. For details, see

- Incremental Encoder Interface in the *DS1104 RTI Reference*
- Incremental Encoder Interface in the *DS1104 RTLib Reference*

Execution times

The execution times required by the RTLib functions have been measured. For details on the results and the corresponding measurement setup, refer to Function Execution Times (DS1104 RTLib Reference 🕮).

Connecting external devices

For a circuit diagram and information on the electrical characteristics and signal conditioning of the incremental encoder unit, see Connecting External Devices to the dSPACE System (DS1104 Hardware Installation and Configuration 🕮).

I/O mapping

The following table shows the mapping between the RTI blocks and RTLib functions and the corresponding pins used by the incremental encoder interface:

Related RTI Blocks	Related RTLib Functions	Channel/Bit	Conn. Pin	Sub-D Pin	Pin on CP/CLP	Signal
DS1104ENC_POS_Cx/ DS1104ENC_SET_POS_Cx	See Incremental Encoder Interface (DS1104 RTLib Reference 🕮)	Ch 1	P1 46	P1A 41	CP19 2	PHI0(1)
			P1 44	P1A 8	CP19 3	/PHI0(1)
			P1 42	P1A 24	CP19 4	PHI90(1)
			P1 40	P1A 40	CP19 5	/PHI90(1)
		Ch 2	P1 45	P1B 41	CP20 2	PHI0(2)
			P1 43	P1B 8	CP20 3	/PHI0(2)
			P1 41	P1B 24	CP20 4	PHI90(2)
			P1 39	P1B 40	CP20 5	/PHI90(2)
DS1104ENC_HW_INDEX_Cx/ DS1104ENC_SW_INDEX_Cx	See Incremental Encoder Interface (DS1104 RTLib Reference 🕮)	Ch 1	P1 38	P1A 7	CP19 6	IDX(1)
			P1 36	P1A 23	CP19 7	/IDX(1)
		Ch 2	P1 37	P1B 7	CP20 6	IDX(2)
			P1 35	P1B 23	CP20 7	/IDX(2)

Encoder Signals and Line Count

Introduction

Incremental encoders provide the two encoder signals PHI0 and PHI90 and the index signal IDX. The encoder signal pair PHI0 <-> PHI90 has a phase shift of 90°. In addition, most encoders also provide the inverted signals /PHI0, /PHI90 and /IDX.

Note

Some encoder manufacturers use the specifications A and B instead of PHI0 and PHI90.

Basic terms

These are the basic terms used in connection with incremental encoders.

Encoder type Sensor signal type of the incremental encoder, either analog (sinusoidal 1 V_{pp} or 11 μA_{pp}) or digital (RS422 / differential or single-ended TTL).

Encoder lines Number of physical encoder lines of the incremental encoder. Refer to your encoder user documentation for the correct value.

Line subdivision Number of subdivisions measured from one physical encoder line. A higher line subdivision results in a more accurate position measurement.

Increment Size of the fraction for the position value. It is the reciprocal of the line subdivision.

Position value For all block outputs and dialog entries the position value is interpreted as the number of encoder lines counted. The result of the line subdivision is added as a fraction.

Delta position value The difference of the position value from the last to the current sample step, measured in encoder lines. To compute the velocity from this value you need to divide the delta position value by the sample time that the RTI block is executed with.

Position range Number of physical encoder lines to be counted without wrap around of the position value.

Wrap around If the position range is exceeded, the position value wraps around from the positive to the negative limit range, or vice versa. The delta position value is not affected by one wrap around of the position value when the position range is exceeded.

Differential versus single-ended signals

The signal, together with the corresponding inverted signal, represents the *differential input*. For example, PHI0 and /PHI0 represent a differential input signal. Using differential inputs improves signal integrity, noise immunity and thus system reliability. Nevertheless, if your encoder does not provide the inverted signals /PHI0, /PHI90 and /IDX, the DS1104 can also handle single-ended TTL signals. In that case, the corresponding pins for /PHI0, /PHI90 and /IDX must be left unconnected. For details on how to connect incremental encoders to the DS1104, see Connecting External Devices to the dSPACE System (DS1104 Hardware Installation and Configuration 🕮).

Level of the digital input signals

Differential RS422 signals The input for differential RS422 signals requires the following signal levels:

Logic Level	Voltage Difference of Differential Inputs	Voltage Range
Low (logical 0)	< – 0.2 V	0.0 … 5.0 V
High (logical 1)	> + 0.2 V	0.0 … 5.0 V

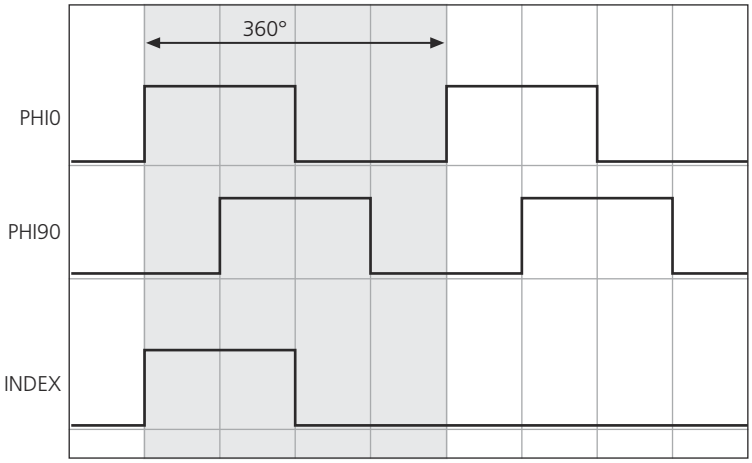
Single-ended TTL signals The input for single-ended TTL signals requires the following signal levels:

Logic Level	Required Voltage Range
Low (logical 0)	0 … 0.8 V
High (logical 1)	2.0 … 5.0 V

Shape of digital input signals

The following illustration shows the shape of the PHI0 and PHI90 digital signals together with the index signal. The gray-shaded area represents one encoder line (360° means one period). For the number of encoder lines per rotation, refer to the encoder user documentation.

The DS1104 lets you discriminate up to 4 positions per encoder line (4-fold subdivision).



Index signal

Each encoder channel provides an IDX input. The input is connected to the DS1104 interrupt control unit. You can poll the index signal and write the position information to the position counters immediately when an index is found, for example.

The index signal can automatically trigger a reset of the encoder line counter. You can specify:

- *never*- no reset
- *once*- the counter is reset only after the first index detection
- *always*- the counter is reset after each index detection

Specifics on encoder line count

- Both digital encoder input channels of the DS1104 can handle encoder signal frequencies of up to 1.65 MHz: Up to 1,650,000 encoder lines can be measured per second.

- The DS1104 is equipped with a 24-bit position counter. Due to the 4-fold subdivision of each encoder line, the counter allows you to measure up to 2^{22} encoder lines in the range -2^{21} … $+2^{21} - 1$. This is the integer representation of the encoder lines, which can be enlarged by the 4-fold subdivision increments up to $+2^{21}$ - 0.25.
- The count direction depends on the encoder's rotation direction.

Related topics

Basics

Incremental Encoder Interface 20
Line Termination and Power Supply 24

Line Termination and Power Supply

Introduction

The differential input channels of the DS1104 also provide a line terminator to avoid reflections of encoder input signals and thus optimize their signal integrity.

Encoder interface terminatorLine termination

The terminator – a resistor (150 Ω) and a capacitor (4.7 nF) connected in series – internally connects the non-inverted to the corresponding inverted encoder input signals. For a circuit diagram, see Connecting External Devices to the dSPACE System (DS1104 Hardware Installation and Configuration 🕮).

Note

If you use single-ended TTL signals, the pins for the inverted signals /PHI0, /PHI90 and /IDX must be left unconnected.

Power supply for incremental encoder

Via the VCC pins, the DS1104 offers a 5 V supply voltage for incremental encoders. These voltage outputs are internally connected to the 5 V power supply of the host PC via multifuse.

Note

- For the VCC pins on the DS1104, the Sub-D connectors as well as on the CP1104, the total load is 500 mA. For the VCC pins on the CLP1104, the total load is 400 mA.
- To reduce the current flowing over the two available VCC pins, you should use both VCC pins even if you connect only one encoder. This does not apply if you use connector panels to connect your encoder(s) to the board since the VCC pins are internally connected at the connector panels.

As an alternative, you can use an external supply voltage for your encoders. In this case,

- Make sure that no input voltages are fed to the DS1104 while it is switched off.
- Connect the ground line of the encoders to a GND pin of the DS1104.

Related topics

Basics

Encoder Signals and Line Count 21
Incremental Encoder Interface 20

Serial Interface

Where to go from here

Information in this section

Basics on the Serial Interface

UART

The board contains a universal asynchronous receiver and transmitter (UART) for performing serial asynchronous communication with external devices.

The UART interface is based on a 16C550C-compatible communication element (TL16C550C from Texas Instruments). It is driven by a 16 MHz oscillator. For more information on the TL16C550C, refer to http://www.ti.com. The UART can be used in the RS232, RS422 or RS485 transceiver mode with the following characteristics:

- Selectable transceiver mode (RS232, RS422, RS485). Depending on the selected transceiver mode, the I/O board can be connected to only one external serial communication device, or to a network of devices. For details, see Comparing RS232, RS422 and RS485 on page 28.
- Baud rates of up to
  - 115.2 kBd (RS232)
  - 1 MBd (RS422/ RS485)

  For details, see Specifying the Baud Rate of the Serial Interface on page 30.
- Selectable number of data bits, parity bit and stop bits
- Software FIFO buffer of selectable size. For details, see Software FIFO Buffer on page 30.

Serial data transfer

Data transfer is initiated by a start bit. Starting with the least significant bit (LSB), a selectable number of data bits (5 … 8) is transferred, followed by an optional parity bit. You can select between different parity modes (no, even, odd parity, and parity bit forced to a logical 0 or 1). 1, 1.5 or 2 stop bits follow. To avoid overflows, data transfer can be controlled by hardware or software handshaking.

UART interrupt

The UART provides one hardware interrupt. Using RTI, this interrupt is extended to the following 4 subinterrupts:

- Interrupt triggered when the number of bytes in the receive buffer reaches a specified threshold
- Interrupt triggered when the transmit buffer is empty
- Line status interrupt
- Modem status interrupt

For information on the interrupt handling, see Interrupts Provided by the DS1104 on page 61.

RTI/RTLib support

You can access the serial interface via RTI and RTLib. For details, see

- RTI: Serial Interface (DS1104 RTI Reference 🕮)
- RTLib: Serial Interface Communication (DS1104 RTLib Reference 🕮)

Connecting external devices

For a circuit diagram and information on the electrical characteristics and signal conditioning of the serial interface, see Connecting External Devices to the dSPACE System (DS1104 Hardware Installation and Configuration 🕮).

I/O mapping

The following table shows the mapping between the RTI blocks and RTLib functions and the corresponding pins used by the serial interface.

Related RTI Blocks	Related RTLib Functions	Conn. Pin	Sub-D Pin	Pin on CP/CLP	Signal
RS232 mode					
DS1104SER_SETUP/ DS1104SER_STAT/ DS1104SER_TX/ DS1104SER_RX/ DS1104SER_INT_Iy/ DS1104SER_INT_REC_LEV	See Serial Interface Communication (DS1104 RTLib Reference 🕮)	P1 3 P1 5 P1 6 P1 7 P1 8 P1 9 P1 10	P1B 34 P1B 18 P1A 18 P1B 2 P1A 2 P1B 35 P1A 35	CP21 1 CP21 8 CP21 7 CP21 6 CP21 4 CP21 2 CP21 3	DCD CTS RTS DSR DTR RXD TXD
RS422/RS485 mode					
DS1104SER_SETUP/ DS1104SER_STAT/ DS1104SER_TX/ DS1104SER_RX/	See Serial Interface Communication (DS1104 RTLib Reference 🕮)	P1 3 P1 4 P1 5 P1 6	P1B 34 P1A 34 P1B 18 P1A 18	CP22 8 CP22 7 CP22 9 CP22 6	CTS RTS $\overline{\text{CTS}}$ $\overline{\text{RTS}}$

Related RTI Blocks	Related RTLib Functions	Conn. Pin	Sub-D Pin	Pin on CP/CLP	Signal
DS1104SER_INT_ly/ DS1104SER_INT_REC_LEV		P1 7	P1B 2	CP22 3	RXD
		P1 8	P1A 2	CP22 2	TXD
		P1 9	P1B 35	CP22 4	$\overline{\text{RXD}}$
		P1 10	P1A 35	CP22 1	$\overline{\text{TXD}}$

Note

The board provides only one serial interface. You can choose between RS232 and RS422/485 only.

Comparing RS232, RS422 and RS485

Introduction

The DS1104 allows you to use the RS232, RS422 or RS485 transceiver mode.

RS232 transceiver mode

In RS232 transceiver mode, one transmitter and one receiver are supported at each data transmission line (point-to-point connection). The RS232 transceiver mode is a single-ended data transfer mode: Signals are represented by voltage levels with respect to ground. There is one wire for each signal.

Data signals and control signals In RS232 transceiver mode, the TXD signal provides the data to be transmitted. The RXD signal provides the received data. The RS232 transceiver mode provides optional control signals – DCD, DTR, DSR, RTS, and CTS – for handshaking. You can use the control signals to avoid overflows.

Cable length and baud rate Due to the single-ended mode, noise signals strongly affect data transfer in an RS232 network. The maximum distance and baud rate between transmitter and receiver are therefore limited. The cable length also limits the maximum baud rate (meets EIA-232-E and V.28 specifications).

RS422 and RS485 transceiver mode

The RS422 and RS485 transceiver modes are balanced differential data transfer modes: Each signal is transmitted together with the corresponding inverted signal. For example, the data transmission signals TXD and $\overline{\text{TXD}}$ represent a pair of balanced differential inputs.

Data signals and control signals In RS422 and RS485 transceiver mode, the TXD and $\overline{\text{TXD}}$ signals provide the data to be transmitted. The RXD and $\overline{\text{RXD}}$ signals provide the received data.

The RS422 and RS485 transceiver modes provide optional control signals – RTS, CTS, and the inverted signals $\overline{\text{RTS}}$ and $\overline{\text{CTS}}$ – for hardware handshaking. You can use the control signals to avoid overflows.

Cable length and baud rate Since the RS422 and RS485 transceiver mode use differential signals, the effects of induced noise signals that appear as common mode voltages on a network are reduced. Compared to the RS232 transceiver mode, higher baud rates between transmitters and receivers are therefore possible. However, the cable length limits the maximum baud rate: As a rule of thumb, the baud rate (in baud) multiplied by the cable length (in meters) should not exceed 10^8.

RS422 networks In RS422 networks, data is sent by one transmitter and received by up to 10 receivers. Two twisted pair cables – each providing two transmission lines – are usually used (unidirectional connections) for transmission and reception of data: one twisted pair cable for the transmitted data (TXD and $\overline{\text{TXD}}$), the other for the received data (RXD and $\overline{\text{RXD}}$).

RS485 networks Up to 32 nodes can participate in RS485 networks. However, only one node is allowed to control the lines at a time. The twisted pair cable is used for transmitting and receiving data (bidirectional connections) – one for the signals TXD and RXD, the other for the inverted signals $\overline{\text{TXD}}$ and $\overline{\text{RXD}}$. The control signals RTS and CTS can also be used to select the transmitting node.

Tip

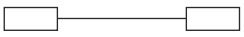
The RS485 transceiver mode is electrically compatible with the RS422 transceiver mode. For this reason, transmitters and receivers that comply with the RS485 transceiver mode can also be used in the RS422 transceiver mode.

Line termination for RS422 and RS485 The network you connect to the serial interface has to contain a line termination that is suitable for the respective receiver. For details, see Connecting RS422/RS485 Devices (DS1104 Hardware Installation and Configuration 🕮).

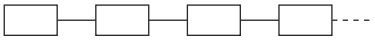
Avoiding undefined conditions (RS485) If no transmitter is currently active in an RS485 network, undefined conditions may occur. An open-line fail-safe termination is mandatory to avoid these conditions. You must provide a pull-up and a pull-down resistor – 1 kΩ each. The pull-up resistor has to be connected between +5 V and the TXD signal line. The pull-down resistor has to be connected between GND and the $\overline{\text{TXD}}$ signal line. For details, see Connecting RS422/RS485 Devices (DS1104 Hardware Installation and Configuration 🕮).

Topologies of RS422 and RS485 networks In RS422 and RS485 networks, you can implement different topologies such as

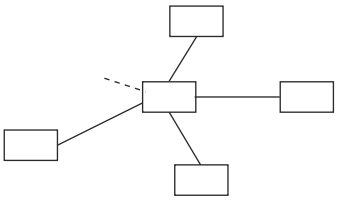
- Simple point-to-point connections



- Daisy-chain connections



- Backbone connections



Related topics

Basics

Specifying the Baud Rate of the Serial Interface

Oscillator frequency

The serial interface of the DS1104 is driven by an oscillator with a frequency f_{osc} = 16 MHz.

Baud rate range

Depending on the selected transceiver mode, you can specify the baud rate for serial communication with the DS1104 in the following range:

Mode	Baud Rate Range
RS232	300 … 115,200 baud
RS422	300 … 1,000,000 baud
RS485	300 … 1,000,000 baud

Available baud rates

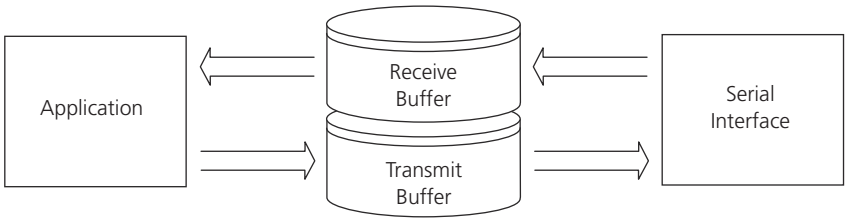
Using RTI and RTLib, you can specify any baud rate in the range listed above. However, the baud rate used by the DS1104 differs slightly from the baud rate you specify. The maximum deviation is ±0.4%.

Software FIFO Buffer

Introduction

The serial interface features a memory section (software FIFO buffer) of selectable size providing the UART with additional space for data storage. The buffer stores data that will be written to (transmit buffer) or was read by (receive buffer) the UART.

The following illustration shows the buffer principle:



Transmit buffer

Data to be transmitted usually is sent immediately.

Data that cannot be transmitted immediately is buffered in the transmit buffer (TX SW FIFO). The buffer cannot be overwritten: If an overflow of TX SW FIFO occurs, you can specify either to discard all new data, or to write as much data as possible to the buffer.

Receive buffer

Data that is received via the serial interface is first copied to the UART FIFO buffer. When the specified number of bytes is received:

- The UART generates an interrupt.
- The bytes are moved to the receive buffer (RX SW FIFO).

If an overflow of the RX SW FIFO occurs, either old data can be overwritten, or new data discarded.

Related topics

Basics

Comparing RS232, RS422 and RS485 28

Synchronizing I/O Features of the Master PPC

Basics of Synchronizing I/O Features

Introduction

Drives control applications, for example, require accurate timing for the control of analog inputs, outputs or incremental encoder position readouts. These actions usually need to be synchronized with a PWM signal, or with another application-specific hardware signal.

Synchronizable actions

On the DS1104, the following actions can be synchronized with a hardware signal:

- Starting A/D conversion (see ADC Unit on page 15)

Note

When using the synchronous I/O trigger with the multiplexed A/D converter (ADCH1... 4), it is only possible to trigger the channel currently selected by the multiplexer. As the trigger signal is usually unsynchronized to the switching of the multiplexer, you can use only one channel per A/D converter when synchronous I/O triggering is desired.

Note

If you enable synchronous triggering of an ADC channel, you cannot use software triggering for the other ADC channels. You cannot mix the trigger modes.

- Strobing the DAC outputs (see DAC Unit on page 16) and
- Reading the incremental encoder position (see Incremental Encoder Interface on page 20)

Synchronization signal

The ST1PWM signal line of the DS1104 is used for synchronization. In this case, it acts as an on-board start of A/D conversion triggering, for example. You can specify to trigger the actions above synchronously with a rising or falling edge of the ST1PWM signal.

Depending on the configuration of the ST1PWM signal line, it provides one of the following signals:

Slave DSP PWM interrupt If you perform PWM3 or PWMSV generation, you can let the slave DSP generate an interrupt at the beginning or in the middle of each PWM period. The interrupt is provided by the ST1PWM signal line. For a detailed description on PWM interrupts, refer to Slave DSP PWM Interrupt on page 65. The I/O components are triggered synchronously with the PWM

interrupt. For example, often voltage measurement within the middle of a PWM high period is required.

Slave DSP bit I/O unit You can use the ST1PWM signal for the slave DSP bit I/O unit. If you configure the signal for output, you can use it as the trigger signal. Refer to Slave DSP Bit I/O Unit on page 37.

External trigger signal If you configure the ST1PWM signal as trigger input, you can synchronize the above actions with external events. The external signal can be fed in or picked up at connector P1 or at connector panel CP1104, refer to the I/O mapping below.

Limitations when using external trigger

- With the `SYNCIN` and `SYNCOUT` parameters you can specify the trigger on the rising or falling edge of the signal. For example, you define an PWM interrupt at position 0.25 and you want to read an ADC signal. If the corresponding `SYNCIN` signal is set to "rising edge", the PWM interrupt and the A/D's converter start are not synchronized, because the interrupt is triggered on the falling edge.
- If the external trigger is initialized, the pins of group 2 of the Slave-DSP digital I/O are no longer available for digital I/O:

RTI	RTLib	Signal
Bit 0	Group 2 bit 0	SPWM7
Bit 1	Group 2 bit 1	SPWM8
Bit 2	Group 2 bit 2	SPWM9
Bit 3	Group 2 bit 3	ST1PWM
Bit 4	Group 2 bit 4	ST2PWM
Bit 5	Group 2 bit 5	ST3PWM

For the electrical characteristics of the external trigger signal, refer to I/O Circuit and Electrical Characteristics (DS1104 Hardware Installation and Configuration 🕮).

RTI/RTLib support

For information on how to access the synchronous I/O trigger, see

- DS1104SYNC_IO_SETUP in the *DS1104 RTI Reference*
- Synchronous I/O Trigger in the *DS1104 RTLib Reference*

Connecting external devices

For a circuit diagram and information on the electrical characteristics and signal conditioning of the digital I/O, see Signal Connection to External Devices (DS1104 Hardware Installation and Configuration 🕮).

I/O mapping

The I/O features of the DS1104 conflict with each other. In the table below, the corresponding signals are marked with a "*". For details, see Conflicting I/O Features on page 73.

Related RTI Block	Related RTLib Functions	Conn. Pin	Sub-D Pin	Pin on CP/CLP	Signal
DS1104SLAVE_PWMINT	See Synchronous I/O Trigger	P1 25	P1B 5	CP18 23	ST1PWM *

Features Provided by the Slave DSP

Where to go from here

Information in this section

Slave DSP Features

Basics on the Slave DSP Features

Hardware features

The DS1104's slave DSP subsystem consists of

- A Texas Instruments TMS320F240 DSP
  - Running at 20 MHz
  - 4Kx16 bit dual-port memory (DPMEM) used for communication with the master PPC

I/O features of the slave DSP

The slave DSP provides the following I/O features of the DS1104:

- Slave DSP Bit I/O Unit on page 37
- Slave DSP Timing I/O Unit on page 39
- Slave DSP Serial Peripheral Interface (SPI) on page 58

Except for the latter, these features can be fully programmed from RTI and RTLib. The Slave DSP Serial Peripheral Interface can be programmed from RTLib1104 only.

Slave DSP Standard I/O

Slave DSP Bit I/O Unit

Characteristics

The slave DSP on the DS1104 provides a bit I/O unit with the following characteristics:

- 14-bit digital I/O
- Direction selectable for each channel individually
- ±13 mA maximum output current
- TTL voltage range for input and output

Tip

The master PPC also provides a bit I/O unit with 20-bit digital I/O. For details, see Bit I/O Unit on page 18.

Power-up state

On power-up of the DS1104, all digital I/O lines – each having a pull-up resistor to +5 V – are in input mode.

RTI/RTLib support

You can access the slave DSP's bit I/O unit via RTI1104 and RTLib1104.

For details, see:

- Slave DSP Bit I/O Unit in the *DS1104 RTI Reference*
- Slave DSP Bit I/O Unit in the *DS1104 RTLib Reference*

Connecting external devices

For a circuit diagram and information on the electrical characteristics and signal conditioning of the slave DSP bit I/O unit, see Slave DSP Digital I/O (DS1104 Hardware Installation and Configuration 🕮).

I/O mapping

The following table shows the mapping between the RTI blocks and RTLib functions and the corresponding pins used by the slave DSP bit I/O unit.

Related RTI Blocks	Bit (RTI)	Related RTLib Functions	Bit (RTLib)	Conn. Pin	Sub-D Pin	Pin on CP/CLP	Signal
DS1104SL_DSP_BIT_IN_Cx/ DS1104SL_DSP_BIT_OUT_Cx	Bit 0	See Slave DSP Bit I/O Unit (DS1104 RTLib Reference 🕮)	Group 2 bit 0	P1 31	P1B 6	CP18 10	SPWM7
	Bit 1		Group 2 bit 1	P1 29	P1B 22	CP18 29	SPWM8
	Bit 2		Group 2	P1 27	P1B 38	CP18 11	SPWM9

Related RTI Blocks	Bit (RTI)	Related RTLib Functions	Bit (RTLib)	Conn. Pin	Sub-D Pin	Pin on CP/CLP	Signal
			bit 2				
	Bit 3		Group 2 bit 3	P1 25	P1B 5	CP18 23	ST1PWM
	Bit 4		Group 2 bit 4	P1 23	P1B 21	CP18 5	ST2PWM
	Bit 5		Group 2 bit 5	P1 21	P1B 37	CP18 24	ST3PWM
	Bit 6		Group 3 bit 4	P1 18	P1A 20	CP18 2	SCAP1
	Bit 7		Group 3 bit 5	P1 16	P1A 36	CP18 21	SCAP2
	Bit 8		Group 3 bit 6	P1 14	P1A 3	CP18 3	SCAP3
	Bit 9		Group 3 bit 7	P1 12	P1A 19	CP18 22	SCAP4
	Bit 10		Group 4 bit 0	P1 17	P1B 20	CP18 17	SCLK
	Bit 11		Group 4 bit 1	P1 15	P1B 36	CP18 35	SSTE
	Bit 12		Group 4 bit 2	P1 13	P1B 3	CP18 16	SSIMO
	Bit 13		Group 4 bit 3	P1 11	P1B 19	CP18 34	SSOMI

Note

Due to the board's limited number of I/O pins, the pins used to provide the bit I/O signals of the slave DSP are shared with other I/O signals of the slave DSP. For details, see Conflicting I/O Features on page 73.

Slave DSP Timing I/O Unit

Introduction

The slave DSP on the DS1104 provides a timing I/O unit that you can use to generate and measure pulse-width modulated (PWM) and square-wave signals.

Where to go from here

Information in this section

Basics on the Slave DSP Timing I/O Unit

PWM signal generation

The PWM signal generation has the following characteristics:

- Outputs for the generation of up to four 1-phase PWM signals with variable
  - Duty cycles (T/T_p ratio)
  - PWM frequencies
  - Polarity
  - Symmetric or asymmetric PWM mode

  For details, see 1-Phase PWM Signal Generation (PWM) on page 43.
- Non-inverted and inverted outputs for 3-phase PWM signal generation (PWM3) with variable
  - Duty cycles (T/T_p ratio)
  - PWM frequencies
  - Deadband

  For details, see 3-Phase PWM Signal Generation (PWM3) on page 46.
- Non-inverted and inverted outputs for the generation of 3-phase space vector PWM signals (PWMSV) with variable
  - Values T_1 and T_2 of the space vector
  - Sector of the space vector

- PWM frequencies
- Deadband

For details, see Space Vector PWM Signal Generation (PWMSV) on page 49.

Square-wave signal generation (D2F)

The square-wave signal generation (D2F) provides outputs for the generation of up to four square-wave signals with variable frequencies. For details, see Slave DSP Square-Wave Signal Generation (D2F) on page 52.

PWM signal measurement (PWM2D)

The PWM signal measurement (PWM2D) provides inputs for the measurement of the duty cycle and frequency of up to four PWM signals. For details, see Slave DSP PWM Signal Measurement (PWM2D) on page 54.

Square-wave signal measurement (F2D)

The square-wave signal measurement (F2D) provides inputs for the measurement of up to four square-wave signals. For details, see Slave DSP Square-Wave Signal Measurement (F2D) on page 56.

Limitations

There are some limitations when you work with the slave DSP timing I/O unit. Refer to Limitations on page 69.

Basics of Slave DSP PWM Signal Generation

Introduction

The slave DSP of the DS1104 provides outputs for PWM signal generation. Each PWM pulse is centered around the middle of the corresponding PWM period (symmetric PWM generation mode). For 1-phase PWM signals, an asymmetric PWM generation mode also is available: see 1-Phase PWM Signal Generation (PWM) on page 43 for details.

PWM signals

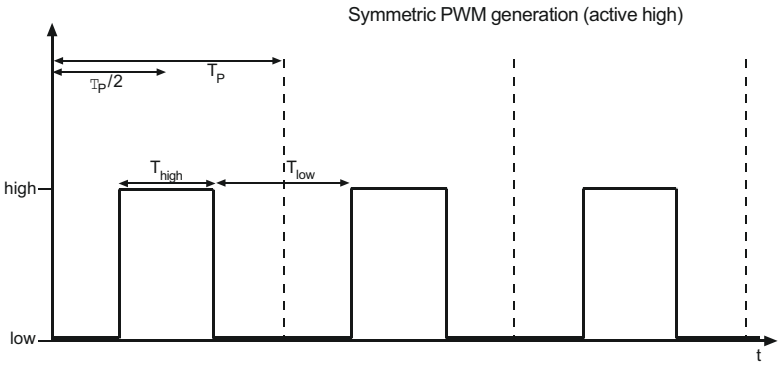
PWM signal generation is crucial to many motor and motion control applications. PWM signals are pulse trains with fixed frequency and magnitude and variable pulse width. There is one pulse of fixed magnitude in every PWM period.

However, the width of the pulses changes from period to period according to a modulating signal. When a PWM signal is applied to the gate of a power transistor, it causes the turn-on/turn-off intervals of the transistor to change from one PWM period to another, according to the same modulating signal. The frequency of a PWM signal is usually much higher than that of the modulating signal, or the fundamental frequency, so that the energy delivered to the motor and its load depends mainly on the modulating signal.

PWM period, duty cycle and resolution

For PWM signals, you can specify the PWM period T_P (= T_{high}+ T_{low}) in the range 200 ns … 819.2 ms. For PWM3 and PWMSV signals, the PWM period T_P applies to each of the 3 phases. For 1-phase PWM signals, the PWM period T_P applies to each of the four PWM output channels. If you perform 3-phase and 1-phase PWM signal generation at the same time, you can specify different PWM periods for the 3-phase and 1-phase PWM signals.

You can also specify the duty cycle. The following illustration shows how the duty cycle d (= T_{high}/ T_P) is defined. The available duty cycle range is 0 … 1 (0 … 100 %).

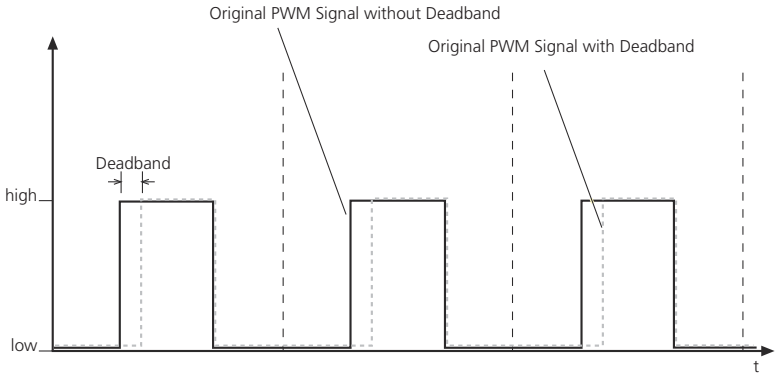


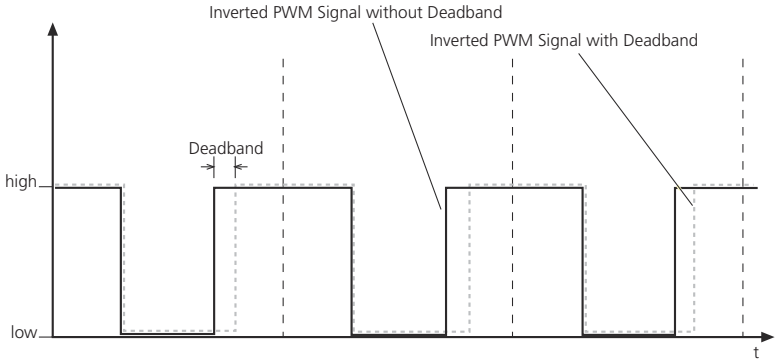
Depending on the selected PWM period, the following resolutions are given. They apply to symmetric PWM signals. For the resolution in asymmetric PWM generation mode, see 1-Phase PWM Signal Generation (PWM) on page 43.

Period T_p	Resolution
< 6.4 ms	100 ns
< 12.8 ms	200 ns
< 25.6 ms	400 ns
< 51.2 ms	800 ns
< 102.4 ms	1.6 µs
< 204.8 ms	3.2 µs
< 409.6 ms	6.4 µs
< 819.2 ms	12.8 µs

Deadband

For the three PWM duty cycles of PWM3 and PWMSV, you can specify one deadband value. This is the time gap between the rising and falling edges of the non-inverted and inverted PWM signals. The deadband introduces a time delay that allows complete turning off of one power transistor before the turning on of the other power transistor.





Note

The maximum deadband value is 100 µs. However, it should not be greater than $T_p/2$.

For details on PWM signal generation, see:

- 1-Phase PWM Signal Generation (PWM) on page 43,
- 3-Phase PWM Signal Generation (PWM3) on page 46,
- Space Vector PWM Signal Generation (PWMSV) on page 49, and
- Slave DSP Square-Wave Signal Generation (D2F) on page 52.

PWM outputs

For each of the PWM generation modes (1-phase, 3-phase and space vector), the PWM outputs can be specified. The running PWM generation can be suspended and the corresponding channels can be set to a specified TTL level (high or low). Only the output of the PWM signal is disabled. Signal calculation is still running and if you enable PWM generation, the currently calculated signal is output, and not the defined initialization or termination value. The PWM outputs can be specified for the two simulation phases (RTI):

- During the initialization phase, you can disable the PWM generation of selected channels (channel pairs for PWM3 and PWMSV) and set each output (pair) to a defined TTL level (high or low). No signal is generated during the initialization.

- During run time, you can stop PWM generation and set the outputs to a defined TTL level (high or low). At any time you can resume in generating the PWM signal. If the simulation terminates the outputs can be set to defined TTL levels.

If the PWM stop feature is disabled, the normal initialization and termination routines are executed. That means the specified duty cycles for initialization and termination are used.

For detailed information, see Slave DSP Timing I/O Unit.

Related topics

Basics

Slave DSP PWM Signal Measurement (PWM2D) 54
Slave DSP Timing I/O Unit 39

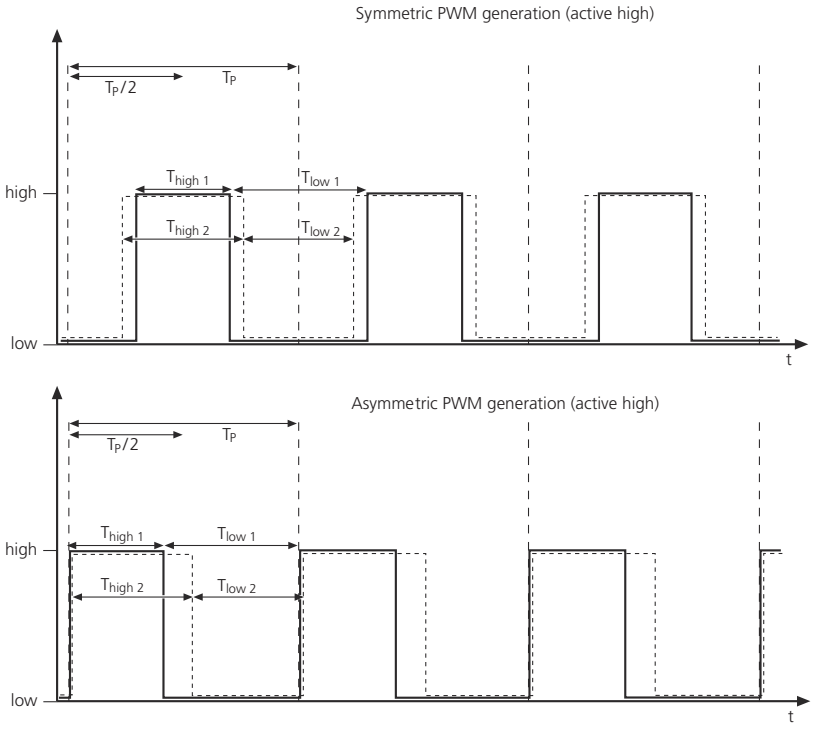
1-Phase PWM Signal Generation (PWM)

Introduction

The slave DSP provides four output channels for 1-phase PWM signal generation.

Asymmetric PWM mode

As an alternative to the symmetric PWM generation mode, you can also let each PWM pulse start at the beginning of the corresponding PWM period *(asymmetric PWM mode)*. Switching between symmetric and asymmetric PWM mode applies to all of the four 1-phase PWM output channels. The following illustration shows two active high symmetric and asymmetric 1-phase PWM signals.



PWM period and resolution in asymmetric mode

In the asymmetric mode, the PWM period T_P must be in the range 200 ns … 409.6 ms. Depending on the period, the following resolutions are given:

Period T_p	Resolution
< 3.2 ms	50 ns
< 6.4 ms	100 ns
< 12.8 ms	200 ns
< 25.6 ms	400 ns
< 51.2 ms	800 ns
< 102.4 ms	1.6 µs
< 204.8 ms	3.2 µs
< 409.6 ms	6.4 µs

For the resolution in symmetric mode, see Basics of Slave DSP PWM Signal Generation on page 40.

Note

Due to quantization effects, you will encounter considerable deviations between the desired PWM period T_P and the generated PWM period, especially for higher PWM frequencies. Refer to Limitations on page 69.

Polarity of PWM signals

For each of the four 1-phase PWM channels, you can specify separately whether to generate active high or active low PWM signals.

PWM output

Via RTI you can specify separately for each of the four 1-phase PWM channels, whether or not to generate PWM signals. In case of PWM stop, the output of each channel can be set to TTL high or low.

RTI/RTLib support

You can perform 1-phase PWM signal generation on the slave DSP via RTI1104 and RTLib1104.

For details, see:

- DS1104SL_DSP_PWM in the *DS1104 RTI Reference*.
- Slave DSP PWM Generation in the *DS1104 RTLib Reference*.

Connecting external devices

For a circuit diagram and information on the electrical characteristics and signal conditioning of the timing I/O unit, see Signal Connection to External Devices (DS1104 Hardware Installation and Configuration 🕮).

I/O mapping

The following table shows the mapping between the RTI block and RTLib functions and the corresponding pins used to provide 1-phase PWM signals.

Related RTI Block	Related RTLib Functions	Channel	Conn. Pin	Sub-D Pin	Pin on CP/CLP	Signal
DS1104SL_DSP_PWM	See Slave DSP PWM Generation (DS1104 RTLib Reference 🕮)	Ch 1	P1 23	P1B 21	CP18 5	ST2PWM
		Ch 2	P1 31	P1B 6	CP18 10	SPWM7
		Ch 3	P1 29	P1B 22	CP18 29	SPWM8
		Ch 4	P1 27	P1B 38	CP18 11	SPWM9

Note

Due to the board's limited number of I/O pins, the pins used to provide the PWM signals are shared with other I/O signals of the slave DSP. For details, see Conflicting I/O Features on page 73.

Related topics

Basics

3-Phase PWM Signal Generation (PWM3)....46
Basics of Slave DSP PWM Signal Generation....40
Slave DSP Square-Wave Signal Generation (D2F)....52
Space Vector PWM Signal Generation (PWMSV)....49

3-Phase PWM Signal Generation (PWM3)

Introduction

The slave DSP provides 3 output channels (phases) for 3-phase PWM signal generation (PWM3) in the frequency range 1.25 Hz … 5 MHz. For PWM3, the DS1104 (and the optional connector panels CP1104 / CLP1104) provides the signals for both the non-inverted and the inverted PWM3 phases:

PWM3 Phase	Signal Name of Non-Inverted PWM3 Phase	Signal Name of Corresponding Inverted PWM3 Phase
1	SPWM1	SPWM2
2	SPWM3	SPWM4
3	SPWM5	SPWM6

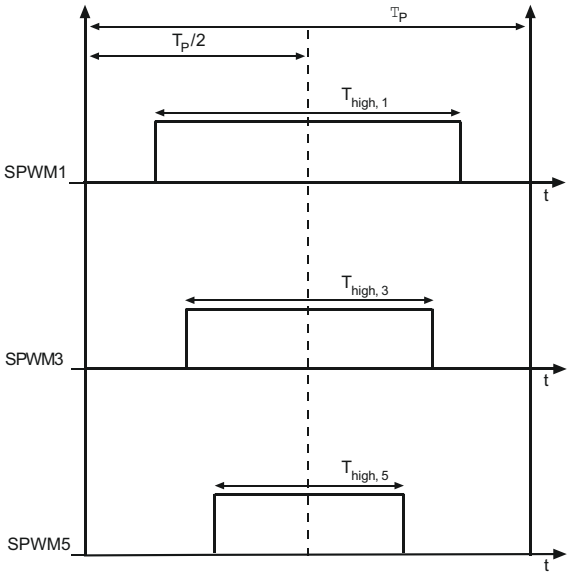
PWM3 signals are centered around the middle of the PWM period (symmetric mode). The polarity of the non-inverted PWM3 signals is active high.

Duty cycle and pulse pattern

For each of the three phases, you can specify the duty cycle d_x (x = 1, 3, 5) individually. The duty cycle is defined as follows:

$d_x = T_{high,x} / T_P$, where T_P is the PWM period.

In PWM3 generation mode, the pulse pattern for the three non-inverted PWM signals SPWM1, SPWM3 and SPWM5 may look like this:



Note

Due to quantization effects, you will encounter considerable deviations between the desired PWM period T_P and the generated PWM period, especially for higher PWM frequencies.

PWM interrupt

When you perform 3-phase PWM signal generation, an interrupt is generated that can be shifted nearly over the whole PWM period by specifying the interrupt alignment.

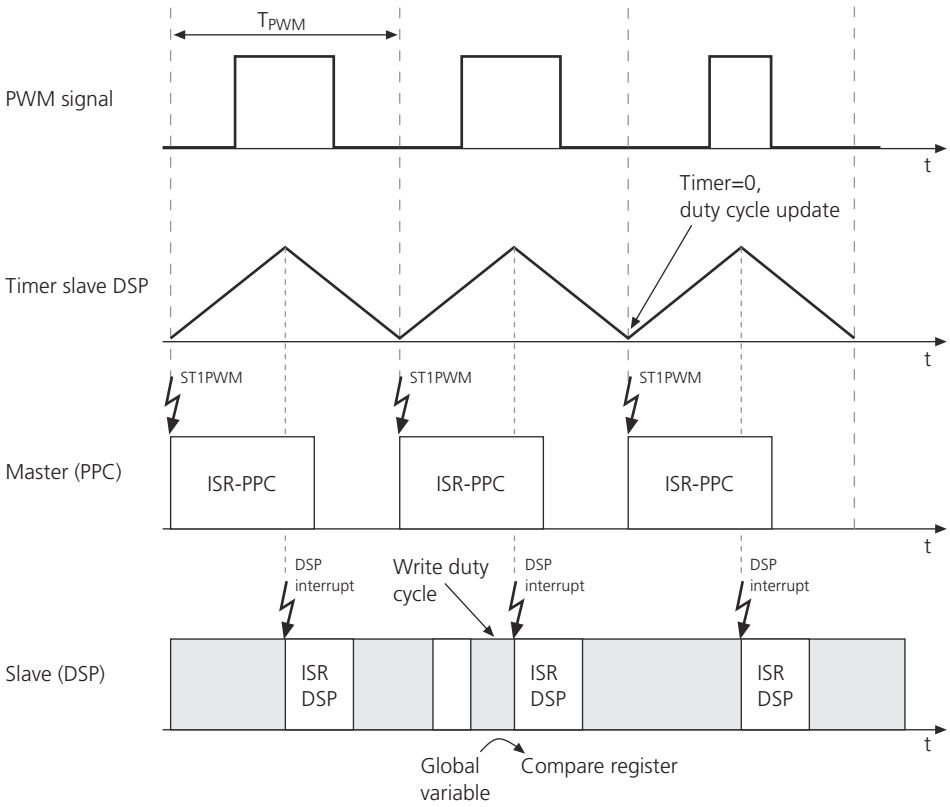
The PWM interrupt can be used to synchronize the generation of the PWM signals on the slave DSP with, for example, the input of the A/D converters of the master PPC. For information on the interrupt handling, see Interrupts Provided by the DS1104 on page 61.

Duty cycle update

You can calculate the new values for the duty cycles within an interrupt service routine on the master PPC (ISR-PPC). The interrupt service routine is triggered by the PWM interrupt (ST1PWM signal). The PPC transfers the values to the slave DSP, that stores them in global variables. In the middle of the period, an interrupt is triggered on the slave DSP that starts a routine (ISR-DSP) for copying the calculated values from the global variables to the compare registers of the PWM unit. The duty cycle is updated with the values from the compare register, if the timer has reached the next zero point.

Note

The duty cycle is updated for the next PWM period, if the new values are stored on the slave DSP *before* the slave DSP interrupt has been triggered. To guarantee this, you must consider a transfer time of the values between PPC and slave DSP of 15 to 20 µs. Otherwise, the duty cycles are updated with the second new PWM period. You must note this especially, if you have specified a shifted PWM interrupt.



PWM output

For 3-phase PWM generation, you can specify via RTI whether or not to generate PWM signals. In case of PWM stop, the output of each channel can be set to TTL high or low.

RTI/RTLib support

You can perform 3-phase PWM signal generation on the slave DSP via RTI1104 and RTLib1104.

For details, see:

- DS1104SL_DSP_PWM3 in the *DS1104 RTI Reference*
- Slave DSP PWM3 Generation in the *DS1104 RTLib Reference*

Connecting external devices

For a circuit diagram and information on the electrical characteristics and signal conditioning of the timing I/O unit, see Signal Connection to External Devices (DS1104 Hardware Installation and Configuration 🕮).

I/O mapping

The following table shows the mapping between the RTI block and RTLib functions and the corresponding pins used to provide PWM3 signals.

Related RTI Block	Related RTLib Functions	Phase	Conn. Pin	Sub-D Pin	Pin on CP/CLP	Signal
DS1104SL_DSP_PWM3	See Slave DSP PWM3 Generation (DS1104 RTLib Reference 🕮)	Phase 1	P1 32	P1A 6	CP18 7	SPWM1
		Phase 2	P1 28	P1A 38	CP18 8	SPWM3
		Phase 3	P1 24	P1A 21	CP18 9	SPWM5
		Phase 1 (inverted)	P1 30	P1A 22	CP18 26	SPWM2
		Phase 2 (inverted)	P1 26	P1A 5	CP18 27	SPWM4
		Phase 3 (inverted)	P1 22	P1A 37	CP18 28	SPWM6

For information on the connectors, refer to Connector Pinouts and LEDs (DS1104 Hardware Installation and Configuration 🕮).

Note

Due to the board's limited number of I/O pins, the pins used to provide the PWM3 signals are shared with other I/O signals of the slave DSP. For details, see Conflicting I/O Features on page 73.

Related topics

Basics

Space Vector PWM Signal Generation (PWMSV)

Introduction

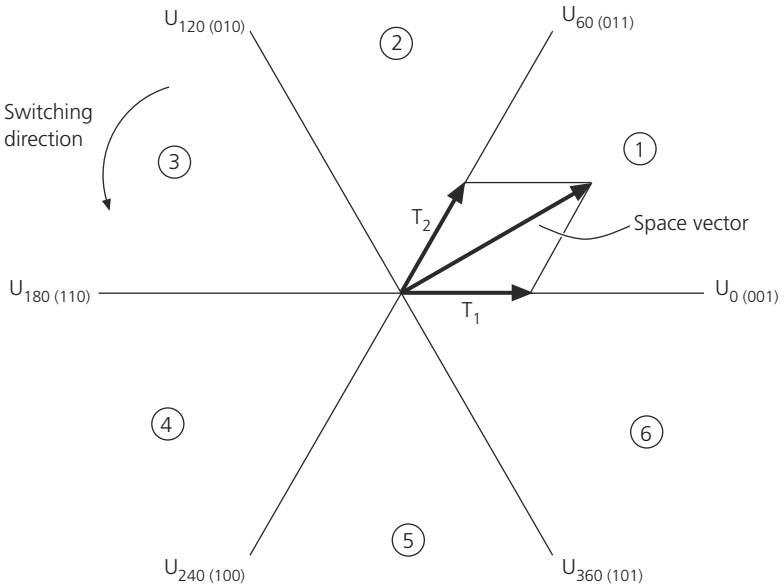
The slave DSP provides 3 output channels (phases) for 3-phase space vector PWM signal generation (PWMSV) in the frequency range 1.25 Hz … 5 MHz. For PWMSV, the DS1104 (and the optional connector panels CP1104 / CLP1104) provide the signals for both the non-inverted and the inverted PWMSV phases:

PWMSV Phase	Signal Name of Non-Inverted PWMSV Phase	Signal Name of Corresponding Inverted PWMSV Phase
1	SPWM1	SPWM2
2	SPWM3	SPWM4
3	SPWM5	SPWM6

PWMSV signals are centered around the middle of the PWM period (symmetric mode). The polarity of the non-inverted PWMSV signals is active high.

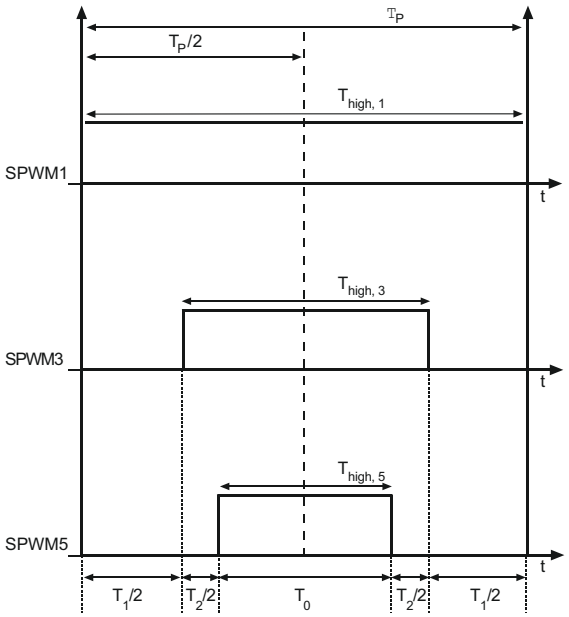
Control of electrical drives

Typically, space vector PWM signals are used to control electrical drives. The *space vector* determines the sector and the values T_1 and T_2 of the corresponding right (T_1) and left (T_2) vectors. T_1/T_P denotes the duty cycle of the right vector in the corresponding sector, while T_2/T_P denotes the duty cycle of the left vector. The sector, which is in the range 1 … 6, is determined by projecting the rotating space vector onto the plane defined by the *basic space vectors* $U_{0(001)}$, $U_{60(011)}$, $U_{120(010)}$, $U_{180(110)}$, $U_{240(100)}$ and $U_{300(101)}$. The values T_1 and T_2 are determined by the projection of the space vector onto the two adjacent basic space vectors. The following illustration shows the plane defined by the basic space vectors, and the projection of a space vector onto the first sector.



Duty cycle and pulse pattern

The duty cycles $d_x = T_{high,x} / T_P$ (x = 1, 3, 5) of the three non-inverted PWMSV signals depend on the projections T_1 and T_2 (see previous diagram). For a space vector in the first sector, the pulse pattern for the three non-inverted PWM signals SPWM1, SPWM3 and SPWM5 generated by the slave DSP looks like this:



The value T_0 is defined as $T_0 = T_P - T_1 - T_2$. Since $T_0 \geq 0$, the following restriction applies to T_1 and T_2:

$T_1 + T_2 \leq T_p$.

Note

Due to quantization effects, you will encounter considerable deviations between the desired PWM period T_P and the generated PWM period, especially for higher PWM frequencies.

For further information on duty cycle update, refer to 3-Phase PWM Signal Generation (PWM3) on page 46.

PWM interrupt

When you perform space vector PWM signal generation, an interrupt is generated that can be shifted nearly over the whole PWM period. For information on the interrupt handling, see Basics of Slave DSP PWM Signal Generation on page 40 and Interrupts Provided by the DS1104 on page 61.

PWM output

For space vector PWM generation, you can specify via RTI whether or not to generate PWM signals. In case of PWM stop, the output of each channel can be set to TTL high or low.

RTI/RTLib support

You can perform space vector PWM signal generation on the slave DSP via RTI1104 and RTLib1104.

For details, see:

- DS1104SL_DSP_PWMSV in the *DS1104 RTI Reference*
- Slave DSP PWMSV Generation in the *DS1104 RTLib Reference*

Connecting external devices

For a circuit diagram and information on the electrical characteristics and signal conditioning of the timing I/O unit, see Signal Connection to External Devices (DS1104 Hardware Installation and Configuration 🕮).

I/O mapping

The following table shows the mapping between the RTI block and RTLib functions and the corresponding pins used to provide PWMSV signals.

Related RTI Block	Related RTLib Functions	Phase	Conn. Pin	Sub-D Pin	Pin on CP/CLP	Signal
DS1104SL_DSP_PWMSV	See Slave DSP PWMSV Generation (DS1104 RTLib Reference 🕮)	Phase 1	P1 32	P1A 6	CP18 7	SPWM1
		Phase 2	P1 28	P1A 38	CP18 8	SPWM3
		Phase 3	P1 24	P1A 21	CP18 9	SPWM5
		Phase 1 (inverted)	P1 30	P1A 22	CP18 26	SPWM2
		Phase 2 (inverted)	P1 26	P1A 5	CP18 27	SPWM4
		Phase 3 (inverted)	P1 22	P1A 37	CP18 28	SPWM6

For information on the connectors, refer to Connector Pinouts and LEDs (DS1104 Hardware Installation and Configuration 🕮).

Note

Due to the board's limited number of I/O pins, the pins used to provide the PWMSV signals are shared with other I/O signals of the slave DSP. For details, see Conflicting I/O Features on page 73.

Related topics

Basics

Slave DSP Square-Wave Signal Generation (D2F)

Introduction

The slave DSP provides four output channels for square-wave signal generation.

Frequency range and resolution

For the available D2F channels, you have to specify the desired frequency range. The selected frequency range determines the signal resolution.

Range	Frequency Range (Channels 1 … 3)	Frequency Range (Channel 4)	Resolution
1	320 Hz … 35 kHz	320 Hz … 4.8 MHz	100 ns
2	160 Hz … 35 kHz	160 Hz … 2.4 MHz	200 ns
3	80 Hz … 35 kHz	80 Hz … 1.2 MHz	400 ns
4	40 Hz … 35 kHz	40 Hz … 600 kHz	800 ns
5	20 Hz … 35 kHz	20 Hz … 300 kHz	1.6 µs
6	10 Hz … 35 kHz	10 Hz … 150 kHz	3.2 µs
7	5 Hz … 35 kHz	5 Hz … 75 kHz	6.4 µs
8	2.5 Hz … 35 kHz	(not available)	12.8 µs

Note

Due to quantization effects, you will encounter considerable deviations between the desired frequency and the generated frequency, especially for higher frequencies. You should therefore select the range with the best possible resolution.

RTI/RTLib support

You can perform square-wave signal generation on the slave DSP via RTI1104 and RTLib1104.

For details, see:

- DS1104SL_DSP_D2F in the *DS1104 RTI Reference*
- Square Wave Signal Generation (D2F) in the *DS1104 RTLib Reference*

Connecting external devices

For a circuit diagram and information on the electrical characteristics and signal conditioning of the timing I/O unit, see Signal Connection to External Devices (DS1104 Hardware Installation and Configuration 🕮).

I/O mapping

The following table shows the mapping between the RTI block and RTLib functions and the corresponding pins used to provide D2F signals.

Related RTI Block	Related RTLib Functions	Channel	Conn. Pin	Sub-D Pin	Pin on CP/CLP	Signal
DS1104SL_DSP_D2F	See Square Wave Signal Generation (D2F) (DS1104 RTLib Reference 🕮)	Ch 1	P1 32	P1A 6	CP18 7	SPWM1
		Ch 2	P1 28	P1A 38	CP18 8	SPWM3
		Ch 3	P1 24	P1A 21	CP18 9	SPWM5
		Ch 4	P1 23	P1B 21	CP18 5	ST2PWM

Note

Due to the board's limited number of I/O pins, the pins used to provide the D2F signals are shared with other I/O signals of the slave DSP. For details, see Conflicting I/O Features on page 73.

Related topics

Basics

Slave DSP PWM Signal Measurement (PWM2D)

Introduction

The slave DSP provides input channels for the measurement of the duty cycles and PWM periods T_p of up to four PWM signals.

Possible PWM period and resolution

The PWM period length T_p that can be measured depend on the number of channels used for PWM2D:

Number of Channels Used for PWM2D	Possible PWM Period Length	Resolution
1	35 µs … 200 s	50 ns
2	70 µs … 200 s	50 ns
3	100 µs … 200 s	50 ns
4	140 µs … 200 s	50 ns

Note

If the input PWM period length exceeds these ranges, the measurement will be faulty.

Possible duty cycle

The duty cycles that can be measured greatly depend on the number of channels used for PWM2D, and on T_p. As an example, the following table shows the available ranges for two values of T_p.

Number of Channels Used for PWM2D	Possible Duty Cycle Range (T_p = 1 ms)	Possible Duty Cycle Range (T_p = 100 µs)
1	0.02 … 0.99	0.13 … 0.91
2	0.04 … 0.97	0.33 … 0.75
3	0.05 … 0.96	0.48 … 0.64
4	0.07 … 0.95	–

Note

- Due to quantization effects, you will encounter deviations between the input frequency and the measured frequency value, especially for higher PWM frequencies.
- If you perform 3-phase PWM or PWMSV generation at the same time, there may be measurement faults for PWM2D, even in lower frequency ranges.

Measuring symmetric PWM signals

The measurement algorithm used is accurate if the PWM period starts with the falling or rising edge of the corresponding PWM signal (asymmetric signal).

The DS1104 can also be used to measure PWM signals that are centered around the middle of the PWM period (symmetric signals). However, the measurement of the PWM frequency of symmetric PWM signals is faulty if the duty cycle of the PWM signal changes during measurement. For details, refer to Limitation for the Measurement of Symmetric PWM Signals on page 70.

RTI/RTLib support

You can perform PWM measurement on the slave DSP via RTI1104 and RTLib1104.

For details, see:

- DS1104SL_DSP_PWM2D in the *DS1104 RTI Reference*
- Slave DSP PWM Measurement (PWM2D) in the *DS1104 RTLib Reference*

Connecting external devices

For a circuit diagram and information on the electrical characteristics and signal conditioning of the timing I/O unit, see Signal Connection to External Devices (DS1104 Hardware Installation and Configuration 🕮).

I/O mapping

The following table shows the mapping between the RTI block and RTLib functions and the corresponding pins used for PWM measurement.

Related RTI Block	Related RTLib Functions	Ch (RTLib)	Conn. Pin	Sub-D Pin	Pin on CP/CLP	Signal
DS1104SL_DSP_PWM2D	See Slave DSP PWM Measurement (PWM2D) (DS1104 RTLib Reference 🕮)	Ch 1	P1 18	P1A 20	CP18 2	SCAP1
		Ch 2	P1 16	P1A 36	CP18 21	SCAP2
		Ch 3	P1 14	P1A 3	CP18 3	SCAP3
		Ch 4	P1 12	P1A 19	CP18 22	SCAP4

Note

Due to the board's limited number of I/O pins, the pins used for PWM measurement are shared with other I/O signals of the slave DSP. For details, see Conflicting I/O Features on page 73.

Related topics

Basics

Slave DSP Square-Wave Signal Measurement (F2D)

Introduction

The slave DSP provides input channels for the measurement of the frequencies of up to four square-wave signals.

Minimum frequency

For each of the four input channels, you can specify a minimum frequency in the range 5 mHz … 150 Hz. If the frequency of the corresponding input channel is smaller than the minimum frequency, the square-wave signal measurement will return a value of 0 Hz.

Maximum frequency and resolution

The maximum frequency that can be measured depends on the number of channels used for F2D:

Number of Channels	Maximum Frequency	Resolution
1	80 kHz	50 ns
2	40 kHz	50 ns
3	25 kHz	50 ns
4	20 kHz	50 ns

Note

- Due to quantization effects, you will encounter deviations between the input frequency and the measured frequency value, especially for higher input frequencies.
- If the input frequency exceeds these ranges, the measurement will be faulty.
- If you perform 3-phase PWM or PWMSV generation at the same time, there may be measurement faults for F2D, even in lower frequency ranges.

RTI/RTLib support

You can perform square-wave signal measurement on the slave DSP via RTI1104 and RTLib1104.

For details, see:

- DS1104SL_DSP_F2D in the *DS1104 RTI Reference*
- Square Wave Signal Measurement (F2D) in the *DS1104 RTLib Reference*

Connecting external devices

For a circuit diagram and information on the electrical characteristics and signal conditioning of the timing I/O unit, see Signal Connection to External Devices (DS1104 Hardware Installation and Configuration 🕮).

I/O mapping

The following table shows the mapping between the RTI block and RTLib functions and the corresponding pins used for square-wave signal measurement.

Related RTI Block	Related RTLib Functions	Channel	Conn. Pin	Sub-D Pin	Pin on CP/CLP	Signal
DS1104SL_DSP_F2D	See Square Wave Signal Generation (D2F) (DS1104 RTLib Reference 🕮)	Ch 1	P1 18	P1A 20	CP18 2	SCAP1
		Ch 2	P1 16	P1A 36	CP18 21	SCAP2
		Ch 3	P1 14	P1A 3	CP18 3	SCAP3
		Ch 4	P1 12	P1A 19	CP18 22	SCAP4

Note

Due to the board's limited number of I/O pins, the pins used for square-wave signal measurement are shared with other I/O signals of the slave DSP. For details, see Conflicting I/O Features on page 73.

Related topics

Basics

Slave DSP PWM Signal Measurement (PWM2D) 54

Slave DSP Serial Interface

Slave DSP Serial Peripheral Interface (SPI)

Introduction

The slave DSP of the DS1104 features a serial peripheral interface (SPI). The SPI can be used to perform high-speed synchronous communication with devices connected to the DS1104, such as an A/D converter.

SPI communication

The SPI transfers serial bit streams of selectable length (1 … 8 bits) and transfer rate (78,125 Baud … 1.25 MBaud (slave mode) or 2.5 MBaud (master mode)) from and to external devices. Received data can be stored in a communication buffer. For further processing, this data is transferred to the master PPC. The transfer rate for serial data transmission is defined via the SCLK signal. This triggers the data transfer from the SPI and a connected external device. Data can be transferred on either the rising or falling edge, with or without delay. The SPI is used with a frequency of 10 MHz, the maximum baudrate is therefore 2.5 MBaud.

Master and slave mode

The SPI of the slave DSP can be driven in two operating modes:

- In the *master mode*, the SPI defines the transfer rate (SCLK signal). The data to be transferred from the SPI to the external device – the most significant bit (MSB) first – is provided by the SSIMO signal. To provide the "chip enable" signal, the SSTE pin is used: Before data is transmitted from the SPI to an external device, the SSTE pin is set low. After transmission, it is set high.

  Data received from an external device (SSOMI signal) is latched on the SPI: The bits of the SSOMI signal are shifted into the least significant bit (LSB) of the master's input register until the selected number of bits are received. Then the data of the input register is transferred – MSB first – to the slave DSP's CPU.
- In the *slave mode*, an external device supplies the clock for serial data transmission (SCLK signal). Via the SSOMI signal, data from the SPI is transmitted to the connected external device. The data to be transferred from the external device to the SPI is provided at the SSIMO pin (MSB first). An active low signal on the SSTE pin allows the SPI to transfer data to the external device. A high signal at the SSTE pin puts the SPI's output pin (SSOMI) into the high-impedance state.

Note

The input frequency applied to the SCLK signal of the slave DSP's SPI should not exceed 2.5 MHz (1.25 MHz in slave mode).

Transmission to the master PPC

Data received by the SPI cannot be transferred directly to the master PPC, but has to be stored temporarily in the 16-byte communication buffer (FIFO queue) of the slave DSP. Buffer overflows are indicated by a status bit, and cause old data to be overwritten.

Tip

For further information on the TMS320F240 DSP's serial peripheral interface, refer to the DSP's technical documentation provided at http://www.ti.com.

RTI/RTLib support

You have access to the slave DSP's serial peripheral interface via RTLib1104.

For details, see:

- Slave DSP Serial Peripheral Interface in the *DS1104 RTLib Reference*

Note

RTI1104 currently does not support the SPI.

Connecting external devices

For a circuit diagram and information on the electrical characteristics and signal conditioning of the serial peripheral interface, see Slave DSP Digital I/O (DS1104 Hardware Installation and Configuration 🕮).

I/O mapping

The following table shows the mapping between the RTLib functions and the corresponding pins used by the SPI.

Related RTLib Functions	Conn. Pin	Sub-D Pin	Pin on CP/CLP	Signal
See Slave DSP Serial Peripheral Interface (DS1104 RTLib Reference 🕮)	P1 11	P1B 19	CP18 34	SSOMI
	P1 13	P1B 3	CP18 16	SSIMO
	P1 15	P1B 36	CP18 35	SSTE
	P1 17	P1B 20	CP18 17	SSCLK

Note

Due to the board's limited number of I/O pins, the pins used to provide the SPI signals are shared with other I/O signals of the slave DSP. For details, see Conflicting I/O Features on page 73.

Interrupts Provided by the DS1104

Where to go from here

Information in this section

Basics on Interrupts

Overview

The DS1104 provides access to various hardware interrupts – originating either from on-board devices such as timers, or from external devices connected to the board. The interrupt controller of the master PPC samples the interrupts originating from outside the master PPC at a frequency of BCLK/ 64.

The following interrupts are available:

Interrupt Type	Description	See Also
ADC1 … 5 end of conversion	Interrupt on end of A/D conversion (multiplexed converter ADC1)	ADC Unit on page 15
Encoder index channels 1 … 2	Interrupt on index found (incremental encoder channel 1)	Encoder Interrupts on page 64
Host interrupt	Interrupt from the host PC	Host Interface on page 11
User interrupts 1 … 4	Interrupt from external device	User Interrupts on page 62

Interrupt Type	Description	See Also
Timers 0 … 3 and Decrementer interrupt	Interrupt when timers reach 0	Timer Features on page 9
UART interrupt	Interrupt of the serial interface	Serial Interface on page 26
Slave DSP interrupt	Interrupt of the slave DSP to the master PPC	Slave DSP Interrupt on page 64
Slave DSP PWM interrupt	PWM interrupt of the slave DSP	Slave DSP PWM Interrupt on page 65

Note

With RTI, Timer 2 and Timer 3 cannot be used as timer interrupt sources.

RTI/RTLib support

With RTI, you can easily implement interrupt-driven subsystems by means of specific interrupt blocks provided by RTI1104. For handcoded applications, you can use RTLib functions to handle interrupts.

- For details on accessing the interrupts via RTI, see in the *DS1104 RTI Reference*:
  - Interrupts (interrupts provided by the master PPC)
  - DS1104SER_INT_ly (UART interrupt)
  - Slave DSP Interrupts (interrupts provided by the slave DSP)
- For details to access the interrupts via RTLib, see in the *DS1104 RTLib Reference*:
  - Interrupt Handling
  - Synchronous I/O Trigger

User Interrupts

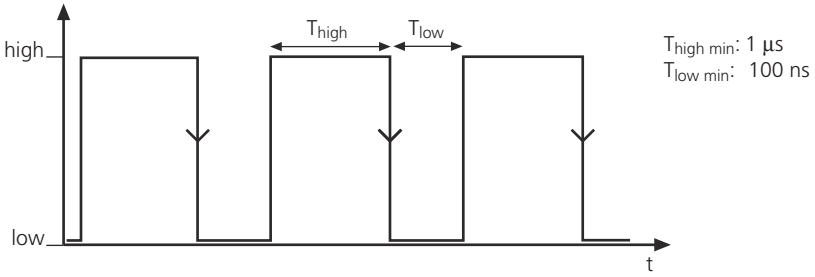
Introduction

The master PPC of the DS1104 also provides four user interrupts that you can use as trigger sources in a real-time application. The user interrupt sources have to be connected externally to the DS1104.

Timing requirements

User interrupts are triggered at the falling edge of the corresponding external signal. To allow the interrupt controller to recognize all incoming user interrupts, the input must be kept high for at least 1 µs. But this is just the time the hardware needs to recognize interrupts. In addition, a restriction caused by the software must be considered, $T_{high} + T_{low} > T_{interrupt\_period\_min}$. The interrupt service routine needs at least $T_{interrupt\_period\_min}$ to execute an interrupt. Thus, the minimal interrupt time strongly depends on the used application and is much longer than that time needed for hardware detection.

To let the hardware recognize the interrupt, the low-active pulse must be at least 100 ns and then the signal must have high level for at least 1 µs.



RTI/RTLib support

For information on how to access the user interrupts, see:

- Interrupts in the *DS1104 RTI Reference*
- Interrupt Handling in the *DS1104 RTLib Reference*

Circuit diagram

For a circuit diagram, see Bit I/O (DS1104 Hardware Installation and Configuration 🕮).

I/O mapping

The following table shows the mapping between the RTI block and RTLib functions and the corresponding pins used by the user interrupts.

Related RTI Block	Int # (RTI)	Related RTLib Functions	Int # (RTLib)	Conn. Pin	Sub-D Pin	Pin on CP/CLP	Signal
DS1104MASTER_HWINT_Ix	User int 1	See Interrupt Handling (DS1104 RTLib Reference 🕮)	Ext. int 0	P1 52	P1A 42	CP17 32	IO16
	User int 2		Ext. int 1	P1 51	P1B 42	CP17 14	IO17
	User int 3		Ext. int 2	P1 50	P1A 9	CP17 33	IO18
	User int 4		Ext. int 3	P1 49	P1B 9	CP17 15	IO19

Note

Due to the board's limited number of I/O pins, the pins used to provide user interrupt sources are shared by the pins used for bits 16 … 19 (signals IO16 … IO19) of the master PPC's bit I/O unit. For details, see Conflicting I/O Features on page 73.

Related topics

Basics

Interrupts Provided by the DS1104 61

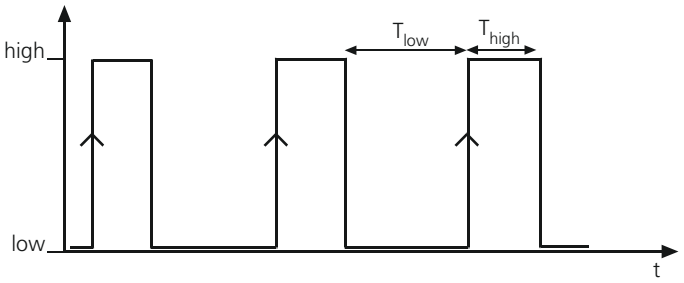
Encoder Interrupts

Introduction

The master PPC provides interrupts on the encoder index channels 1 … 2. The interrupts automatically trigger a reset of the encoder position.

Timing requirements

The timing behavior of encoder interrupts and user interrupts is the same, but the signal characteristic is inverted as the interrupt is triggered on the rising edge of the high-active signal, see the illustration below.



For detailed information, see User Interrupts on page 62.

RTI/RTLib support

You can access the master PPC's incremental encoder interface via RTI1104 and RTLib1104.

For details, see:

- Incremental Encoder Interface in the *DS1104 RTI Reference*
- Incremental Encoder Interface in the *DS1104 RTLib Reference*

Related topics

Basics

Interrupts Provided by the DS1104 61

Slave DSP Interrupt

Introduction

The DS1104 provides a physical line for an interrupt from the slave DSP to the master PPC. Within user applications running on the slave DSP, you can extend this interrupt to several subinterrupts that are identified by specific subinterrupt numbers.

RTI/RTLib support

For information on how to access the slave DSP interrupt, see:

- DS1104SLAVE_DSPINT_Ix in the *DS1104 RTI Reference*
- Interrupt Handling in the *DS1104 RTLib Reference*

Related topics

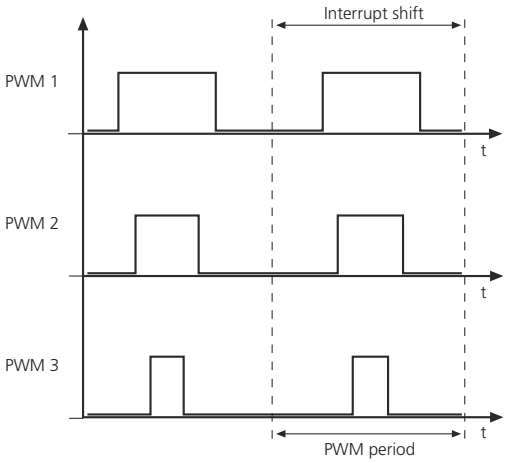
Basics

Interrupts Provided by the DS1104 61

Slave DSP PWM Interrupt

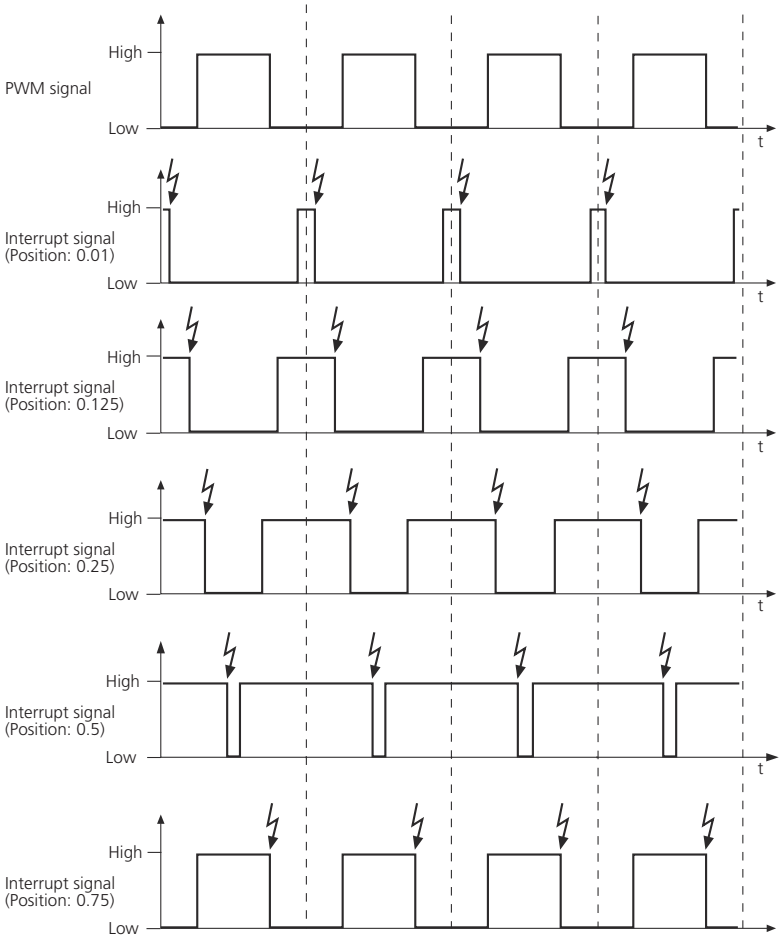
Introduction

If you perform PWM3 or PWMSV generation, you can let the slave DSP generate an interrupt nearly over the whole PWM period. The position (interrupt alignment) of the generated interrupt must be within the range 0< … 1. An alignment value of 0 would disable the interrupt and is therefore not supported. See the following illustration.



The PWM interrupt (from slave to master) is triggered by the falling edge of the active-low synchronization interrupt signal. The following illustrations show the interrupt signal in dependency with the interrupt position (alignment).

The bigger the value is, the more the falling edge is shifted to the right end of the PWM signal. For interrupt positions in the range 0.5 … 1, the interrupt signal is inverted.



The slave DSP PWM interrupt is also available externally via the ST1PWM signal line.

Synchronizing with ST1PWM signal

The slave DSP interrupt can be used to synchronize PWM3 or PWMSV signal generation with other I/O features of the DS1104. If the synchronous I/O trigger is enabled you can synchronize starting of A/D conversion, strobing the DAC outputs and strobing the incremental encoder interface. Refer to 3-Phase PWM Signal Generation (PWM3) on page 46 and Space Vector PWM Signal Generation (PWMSV) on page 49.

RTI/RTLib support

For information on how to access the slave DSP PWM interrupt, see:

- DS1104SLAVE_PWMINT in the *DS1104 RTI Reference*
- Interrupt Handling in the *DS1104 RTLib Reference*

I/O mapping

The following table shows the mapping between the RTI block and RTLib functions and the corresponding pins used by the user interrupts.

Related RTI Block	Related RTLib Functions	Conn. Pin	Sub-D Pin	Pin on CP/CLP	Signal
DS1104SLAVE_PWMINT	ds1104_slave_dsp_pwm3_int_init	P1 25	P1B 5	CP18 23	ST1PWM

For information on the connectors, refer to Connector Pinouts and LEDs (DS1104 Hardware Installation and Configuration 🕮).

Note

Due to the board's limited number of I/O pins, the pin used to provide the slave DSP PWM interrupt is shared with other I/O signals of the slave DSP. For details, see Conflicting I/O Features on page 73.

Related topics

Basics

Interrupts Provided by the DS1104 61

Limitations

Introduction

There are some limitations you have to take into account when working with the DS1104.

Where to go from here

Information in this section

Quantization Effects

Introduction

Signal generation and measurement are only feasible within the limits of the resolution of the timing I/O unit. The limited resolution causes quantization errors that increase with increasing frequencies.

When performing square-wave signal generation (D2F), for example, you will encounter considerable deviations between the desired frequency and the generated frequency, especially for higher frequencies. The (quantized) generated signal frequencies can be calculated according to the following equation:

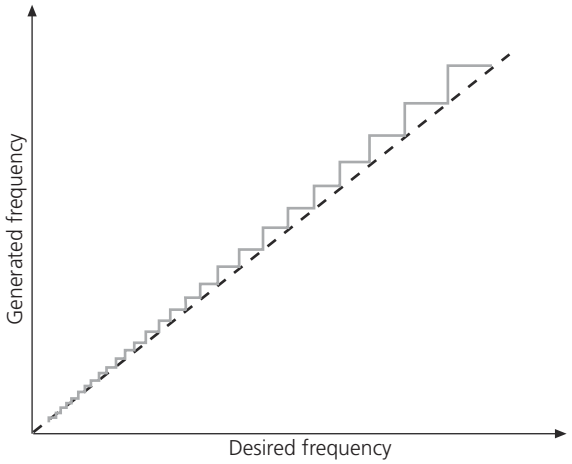
$$f = \frac{1}{n \cdot R}$$

where R is the resolution (in s), and n is a positive integer.

Example

For example, if you select range 6 on D2F channel 1, a signal with a frequency of 34.73 kHz is generated, even for a desired frequency of 31.5 kHz. Refer to Slave DSP Square-Wave Signal Generation (D2F) on page 52.

The following illustration shows the increasing quantization effects for increasing desired frequencies:

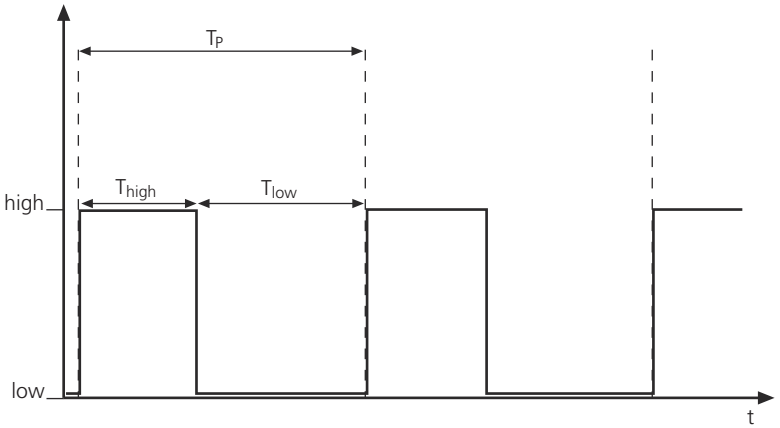


You should therefore select the range with the best possible resolution.

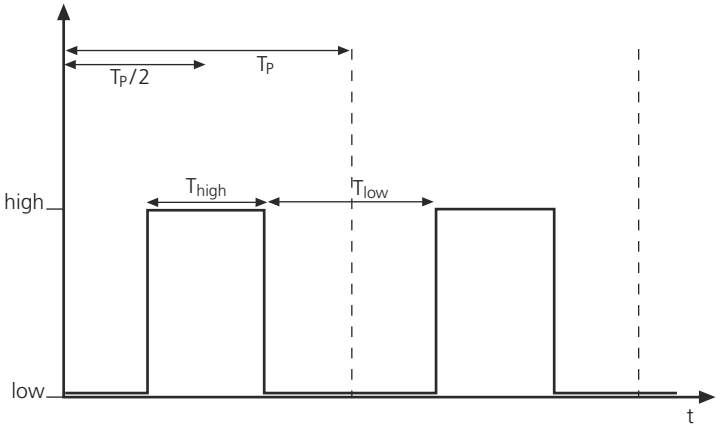
Limitation for the Measurement of Symmetric PWM Signals

Asymmetric and symmetric PWM signals

PWM measurement is accurate if the PWM period starts with the falling or rising edge of the corresponding PWM signal (asymmetric signal). For example, in the illustration below, each PWM period starts with a rising edge of the asymmetric PWM signal:



The DS1104 can also measure PWM signals that are centered around the middle of the PWM period (symmetric signals):



However, the evaluation of the PWM frequency f_p of symmetric PWM signals is faulty if the duty cycle of the PWM signal changes during measurement.

PWM frequency evaluation algorithm

The PWM frequency f_p is evaluated according to the following equation:

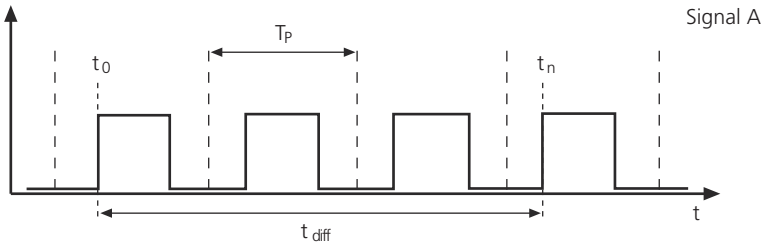
$$f_p = \frac{n}{t_{diff}}$$

Where

t_{diff} is the interval between the first and the last detected rising edge

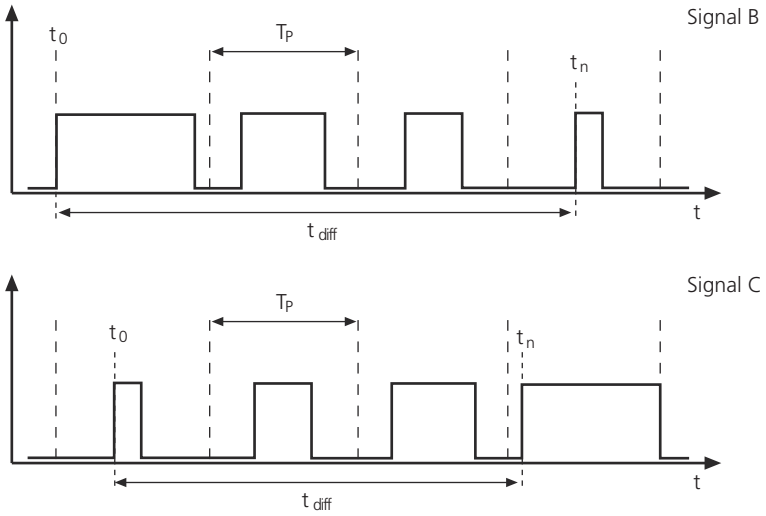
n is the number of PWM periods used to evaluate f_p.

The following illustration shows how f_p is evaluated for a symmetric PWM signal (signal A) without duty cycle changes during measurement; $n = 3$:



Measurement error due to duty cycle changes

PWM frequency measurement of a symmetric PWM signal is faulty if the duty cycle of the signal changes during measurement. The illustration below shows two PWM signals (signals B and C) with duty cycle changes: The duty cycle of signal B decreases whereas the duty cycle of signal C increases during measurement.



According to the illustration above, duty cycle changes during run time have an effect on the measured interval t_{diff}. As a result, the f_p values evaluated for the signals B and C are faulty, since t_{diff} is used to evaluate the PWM frequency f_p.

Estimating the measurement error

The difference between the correct frequency value and the one evaluated cannot be calculated exactly since it depends on the speed of the duty cycle change. However, the maximum deviation from the correct frequency value f_p can be calculated according to the following equation:

$$f_{deviation} = \pm \frac{f_p}{(2 \cdot \pi - 1)}$$

The evaluated frequency value therefore is in the range

$$f_{p,\ evaluated} = f_p \pm \frac{f_p}{(2 \cdot \pi - 1)}$$

$$f_{p,\ evaluated} = f_p \cdot \left(1 \pm \frac{1}{(2 \cdot \pi - 1)}\right)$$

Tip

To decrease the measurement error, specify a large value for n, which is the number of PWM periods used to evaluate f_p.

Related topics

Basics

Limitations.....69

Conflicting I/O Features

Types of I/O conflicts

There are I/O features that share the same board resources.

Conflicts concerning single I/O channels There are conflicts that concern single channels of an I/O feature. The dSPACE board provides only a limited number of I/O pins. The same pins can be shared by different I/O features. However, a pin can serve as the I/O channel for only one feature at a time.

Conflicts concerning an I/O feature as a whole There are conflicts that concern the use of an I/O feature as a whole. Suppose two I/O features of the dSPACE board use the same on-board timer device. In this case, only one of the two I/O features can be used at a time. The other feature is completely blocked.

Conflicts for the DS1104

The following I/O features of the DS1104 conflict with other I/O features:

- Conflicts for the Bit I/O Unit on page 73
- Conflicts for the Serial Interface on page 74
- Conflicts for External Triggering on page 74
- Conflicts for the Slave DSP Bit I/O Unit on page 74
- Conflicts for Slave DSP 1-Phase PWM Signal Generation (PWM) on page 75
- Conflicts for Slave DSP 3-Phase PWM Signal Generation (PWM3) on page 76
- Conflicts for Slave DSP Space Vector PWM Signal Generation (PWMSV) on page 76
- Conflicts for Slave DSP Square-Wave Signal Generation (D2F) on page 77
- Conflicts for Slave DSP PWM Signal Measurement (PWM2D) on page 78
- Conflicts for Slave DSP Square-Wave Signal Measurement (F2D) on page 78
- Conflicts for the Slave DSP Serial Peripheral Interface (SPI) on page 79

Conflicts for the Bit I/O Unit

The following I/O features of the DS1104 conflict with the Bit I/O unit:

Bit I/O Unit *)		**Signal**	**Conflicting I/O Feature **)**		
Bit (RTI)	**Bit (RTLib)**			**Ch (RTI)**	**Ch (RTLib)**
Conflicts Concerning Single Bits					
Bit 16	Bit 16	IO16	User interrupt	User Int 1	Ext Int 0
Bit 17	Bit 17	IO17	User interrupt	User Int 2	Ext Int 1
Bit 18	Bit 18	IO18	User interrupt	User Int 3	Ext Int 2
Bit 19	Bit 19	IO19	User interrupt	User Int 4	Ext Int 3
*) Related RTI blocks and RTLib functions: ▪ DS1104BIT_IN_Cx DS1104BIT_OUT_Cx ▪ See Bit I/O Unit (DS1104 RTLib Reference 🕮)			**) Related RTI blocks and RTLib functions: ▪ DS1104MASTER_HWINT_Ix ▪ See Interrupt Handling (DS1104 RTLib Reference 🕮)		

Conflicts for the Serial Interface

The master PPC of the DS1104 supports only one serial interface. It can be configured as either RS232 or RS422/RS485 transceiver.

Conflicts for External Triggering

Enabling the external trigger conflicts with the slave DSP bit I/O unit. You cannot use the following bits for digital I/O purposes at the same time:

External Trigger Signal		Signal	Conflicting I/O Feature **)		
Bit (RTI)	**Bit (RTLib)**			**Ch (RTI)**	**Ch (RTLib)**
Conflicts Concerning External Triggering					
External Trigger			SPWM7	Bit 0	Group 2 bit 0
			SPWM8	Bit 1	Group 2 bit 1
			SPWM9	Bit 2	Group 2 bit 2
			ST1PWM (used for triggering)	Bit 3	Group 2 bit 3
			ST2PWM	Bit 4	Group 2 bit 4
			ST3PWM	Bit 5	Group 2 bit 5
*) Related RTI blocks and RTLib functions: ▪ DS1104SYNC_IO_SETUP ▪ See Synchronous I/O Trigger			**) Related RTI blocks and RTLib functions: ▪ DS1104SL_DSP_BIT_IN_Cx DS1104SL_DSP_BIT_OUT_Cx ▪ See Slave DSP Bit I/O Unit (DS1104 RTLib Reference 🕮)		

Conflicts for the Slave DSP Bit I/O Unit

The following I/O features of the DS1104 conflict with the Slave DSP Bit I/O unit:

Slave DSP Bit I/O Unit *)		Signal	Conflicting I/O Feature **)		
Bit (RTI)	**Bit (RTLib)**			**Ch (RTI)**	**Ch (RTLib)**
Conflicts Concerning Single Bits					
Bit 0	Group 2, bit 0	SPWM7	▪ PWM ▪ External Trigger	Ch 2	Ch 2
Bit 1	Group 2, bit 1	SPWM8	▪ PWM ▪ External Trigger	Ch 3	Ch 3
Bit 2	Group 2, bit 2	SPWM9	▪ PWM ▪ External Trigger	Ch 4	Ch 4
Bit 3	Group 2, bit 3	ST1PWM	▪ Slave DSP PWM int ▪ External Trigger		
Bit 4	Group 2, bit 4	ST2PWM	▪ PWM ▪ D2F ▪ External Trigger	▪ Ch 1 ▪ Ch 4	▪ Ch 1 ▪ Ch 4
Bit 5	Group 2, bit 5	ST3PWM	External Trigger		
Bit 6	Group 3, bit 4	SCAP1	PWM2D/F2D	Ch 1	Ch 1

Slave DSP Bit I/O Unit *)		Signal	Conflicting I/O Feature **)		
Bit (RTI)	**Bit (RTLib)**			**Ch (RTI)**	**Ch (RTLib)**
Bit 7	Group 3, bit 5	SCAP2	PWM2D/F2D	Ch 2	Ch 2
Bit 8	Group 3, bit 6	SCAP3	PWM2D/F2D	Ch 3	Ch 3
Bit 9	Group 3, bit 7	SCAP4	PWM2D/F2D	Ch 4	Ch 4
Bit 10	Group 4, bit 0	SCLK	SPI	–	
Bit 11	Group 4, bit 1	SSTE	SPI	–	
Bit 12	Group 4, bit 2	SSIMO	SPI	–	
Bit 13	Group 4, bit 3	SSOMI	SPI	–	
*) Related RTI blocks and RTLib functions: ▪ DS1104SL_DSP_BIT_IN_Cx DS1104SL_DSP_BIT_OUT_Cx ▪ See Slave DSP Bit I/O Unit (DS1104 RTLib Reference 🕮)			**) Related RTI blocks and RTLib functions: PWM: ▪ DS1104SL_DSP_PWM ▪ See Slave DSP PWM Generation (DS1104 RTLib Reference 🕮) Slave DSP PWM int: ▪ DS1104SLAVE_PWMINT ▪ See ds1104_slave_dsp_pwm3_int_init (DS1104 RTLib Reference 🕮) D2F: ▪ DS1104SL_DSP_D2F ▪ See Square Wave Signal Generation (D2F) (DS1104 RTLib Reference 🕮) PWM2D/F2D: ▪ DS1104SL_DSP_PWM2D DS1104SL_DSP_F2D ▪ See Slave DSP PWM Measurement (PWM2D)/Square Wave Signal Generation (D2F) (DS1104 RTLib Reference 🕮) SPI: ▪ See Slave DSP Serial Peripheral Interface (DS1104 RTLib Reference 🕮)		

Conflicts for Slave DSP 1-Phase PWM Signal Generation (PWM)

The following I/O features of the DS1104 conflict with Slave DSP 1-Phase PWM Signal Generation:

Slave DSP 1-Phase PWM Signal Generation (PWM) *)		Signal	Conflicting I/O Feature **)		
Ch (RTI)	**Ch (RTLib)**			**Ch (RTI)**	**Ch (RTLib)**
Conflicts Concerning Slave DSP 1-Phase PWM Signal Generation as a Whole					
▪ If you use channel 4 of D2F, you cannot generate 1-phase PWM signals at the same time.					
Conflicts Concerning Single Channels					
Ch 1	Ch 1	ST2PWM	Slave DSP Bit I/O unit	Bit 4	Group 2, bit 4
Ch 2	Ch 2	SPWM7	Slave DSP Bit I/O unit	Bit 0	Group 2, bit 0
Ch 3	Ch 3	SPWM8	Slave DSP Bit I/O unit	Bit 1	Group 2, bit 1
Ch 4	Ch 4	SPWM9	Slave DSP Bit I/O unit	Bit 2	Group 2, bit 2
*) Related RTI blocks and RTLib functions: ▪ DS1104SL_DSP_PWM			**) Related RTI blocks and RTLib functions: D2F: ▪ DS1104SL_DSP_D2F		

Slave DSP 1-Phase PWM Signal Generation (PWM) *)		Signal	Conflicting I/O Feature **)		
Ch (RTI)	**Ch (RTLib)**			**Ch (RTI)**	**Ch (RTLib)**
▪ See Slave DSP PWM Generation (DS1104 RTLib Reference 🕮)			▪ See Square Wave Signal Generation (D2F) (DS1104 RTLib Reference 🕮) Slave DSP Bit I/O Unit: ▪ DS1104SL_DSP_BIT_IN_Cx DS1104SL_DSP_BIT_OUT_Cx ▪ See Slave DSP Bit I/O Unit (DS1104 RTLib Reference 🕮)		

Conflicts for Slave DSP 3-Phase PWM Signal Generation (PWM3)

The following I/O features of the DS1104 conflict with Slave DSP 3-Phase PWM Signal Generation:

Slave DSP 3-Phase PWM Signal Generation (PWM3) *)		Signal	Conflicting I/O Feature **)		
Ch (RTI)	**Ch (RTLib)**			**Ch (RTI)**	**Ch (RTLib)**
Conflicts Concerning Slave DSP 3-Phase PWM Signal Generation as a Whole					
▪ If you perform space vector PWM signal generation (PWMSV) or square-wave signal generation (D2F), you cannot generate 3-phase PWM signals at the same time.					
*) Related RTI blocks and RTLib functions: ▪ DS1104SL_DSP_PWM3 ▪ See Slave DSP PWM3 Generation (DS1104 RTLib Reference 🕮)			**) Related RTI blocks and RTLib functions: PWMSV: ▪ DS1104SL_DSP_PWMSV ▪ See Slave DSP PWMSV Generation (DS1104 RTLib Reference 🕮) D2F: ▪ DS1104SL_DSP_D2F ▪ See Square Wave Signal Generation (D2F) (DS1104 RTLib Reference 🕮)		

Conflicts for Slave DSP Space Vector PWM Signal Generation (PWMSV)

The following I/O features of the DS1104 conflict with Slave DSP Space Vector PWM Signal Generation:

Slave DSP Space Vector PWM Signal Generation (PWMSV) *)		Signal	Conflicting I/O Feature **)		
Ch (RTI)	**Ch (RTLib)**			**Ch (RTI)**	**Ch (RTLib)**
Conflicts Concerning Slave DSP 3-Phase PWM Signal Generation as a Whole					
▪ If you perform 3-phase PWM signal generation (PWM3) or square-wave signal generation (D2F), you cannot generate space vector PWM signals at the same time.					
*) Related RTI blocks and RTLib functions: ▪ DS1104SL_DSP_PWMSV ▪ See Slave DSP PWMSV Generation (DS1104 RTLib Reference 🕮)			**) Related RTI blocks and RTLib functions: 3-phase PWM signal generation (PWM3): ▪ DS1104SL_DSP_PWM3 ▪ See Slave DSP PWM3 Generation (DS1104 RTLib Reference 🕮) D2F: ▪ DS1104SL_DSP_D2F		

Slave DSP Space Vector PWM Signal Generation (PWMSV) *)		Signal	Conflicting I/O Feature **)		
Ch (RTI)	**Ch (RTLib)**			**Ch (RTI)**	**Ch (RTLib)**
			▪ See Square Wave Signal Generation (D2F) (DS1104 RTLib Reference 🕮)		

Conflicts for Slave DSP Square-Wave Signal Generation (D2F)

The following I/O features of the DS1104 conflict with Slave DSP Square-Wave Signal Generation:

Slave DSP Square-Wave Signal Generation (D2F) *)		Signal	Conflicting I/O Feature **)		
Ch (RTI)	**Ch (RTLib)**			**Ch (RTI)**	**Ch (RTLib)**
Conflicts Concerning Slave DSP Square-Wave Signal Generation as a Whole					
▪ If you perform 3-phase or space vector PWM signal generation (PWM3 or PWMSV), you cannot generate square-wave signals at the same time.					
Conflicts Concerning Single Channels					
Ch 4	Ch 4	ST2PWM	▪ Slave DSP Bit I/O unit ▪ PWM	▪ Bit 4 ▪ Ch 1	▪ Group 2, bit 4 ▪ Ch 1
*) Related RTI blocks and RTLib functions: ▪ DS1104SL_DSP_D2F ▪ See Square Wave Signal Generation (D2F) (DS1104 RTLib Reference 🕮)			**) Related RTI blocks and RTLib functions: PWM3/PWMSV: ▪ DS1104SL_DSP_PWM3 DS1104SL_DSP_PWMSV ▪ See Slave DSP PWM3 Generation/Slave DSP PWMSV Generation (DS1104 RTLib Reference 🕮) Slave DSP Bit I/O Unit: ▪ DS1104SL_DSP_BIT_IN_Cx DS1104SL_DSP_BIT_OUT_Cx ▪ See Slave DSP Bit I/O Unit (DS1104 RTLib Reference 🕮) PWM: ▪ DS1104SL_DSP_PWM ▪ See Slave DSP PWM Generation (DS1104 RTLib Reference 🕮)		

Conflicts for Slave DSP PWM Signal Measurement (PWM2D)

The following I/O features of the DS1104 conflict with Slave DSP PWM Signal Measurement:

Slave DSP PWM Signal Measurement (PWM2D) *)		Signal	Conflicting I/O Feature **)		
Ch (RTI)	**Ch (RTLib)**			**Ch (RTI)**	**Ch (RTLib)**
Conflicts Concerning Slave DSP PWM Signal Measurement as a Whole					
▪ If you perform square-wave signal measurement (F2D), you cannot measure PWM signals at the same time.					
Conflicts Concerning Single Channels					
Ch 1	Ch 1	SCAP1	Slave DSP Bit I/O unit	Bit 6	Group 3, bit 4
Ch 2	Ch 2	SCAP2	Slave DSP Bit I/O unit	Bit 7	Group 3, bit 5
Ch 3	Ch 3	SCAP3	Slave DSP Bit I/O unit	Bit 8	Group 3, bit 6
Ch 4	Ch 4	SCAP4	Slave DSP Bit I/O unit	Bit 9	Group 3, bit 7
*) Related RTI blocks and RTLib functions: ▪ DS1104SL_DSP_PWM2D ▪ See Slave DSP PWM Measurement (PWM2D) (DS1104 RTLib Reference 🕮)			**) Related RTI blocks and RTLib functions: F2D: ▪ DS1104SL_DSP_F2D ▪ See Square Wave Signal Generation (D2F) (DS1104 RTLib Reference 🕮) Slave DSP Bit I/O Unit: ▪ DS1104SL_DSP_BIT_IN_Cx DS1104SL_DSP_BIT_OUT_Cx ▪ See Slave DSP Bit I/O Unit (DS1104 RTLib Reference 🕮)		

Conflicts for Slave DSP Square-Wave Signal Measurement (F2D)

The following I/O features of the DS1104 conflict with Slave DSP Square-Wave Signal Measurement:

Slave DSP Square-Wave Signal Measurement (F2D) *)		Signal	Conflicting I/O Feature **)		
Ch (RTI)	**Ch (RTLib)**			**Ch (RTI)**	**Ch (RTLib)**
Conflicts Concerning Slave DSP Square-Wave Signal Measurement as a Whole					
▪ If you perform PWM signal measurement (PWM2D), you cannot measure square-wave signals at the same time.					
Conflicts Concerning Single Channels					
Ch 1	Ch 1	SCAP1	Slave DSP Bit I/O unit	Bit 6	Group 3, bit 4
Ch 2	Ch 2	SCAP2	Slave DSP Bit I/O unit	Bit 7	Group 3, bit 5
Ch 3	Ch 3	SCAP3	Slave DSP Bit I/O unit	Bit 8	Group 3, bit 6
Ch 4	Ch 4	SCAP4	Slave DSP Bit I/O unit	Bit 9	Group 3, bit 7
*) Related RTI blocks and RTLib functions: ▪ DS1104SL_DSP_F2D ▪ See Square Wave Signal Generation (D2F) (DS1104 RTLib Reference 🕮)			**) Related RTI blocks and RTLib functions: PWM2D: ▪ DS1104SL_DSP_PWM2D ▪ See Slave DSP PWM Measurement (PWM2D) (DS1104 RTLib Reference 🕮)		

Slave DSP Square-Wave Signal Measurement (F2D) *)		Signal	Conflicting I/O Feature **)		
Ch (RTI)	Ch (RTLib)			Ch (RTI)	Ch (RTLib)
			Slave DSP Bit I/O Unit: ▪ DS1104SL_DSP_BIT_IN_Cx DS1104SL_DSP_BIT_OUT_Cx ▪ See Slave DSP Bit I/O Unit (DS1104 RTLib Reference 🕮)		

Conflicts for the Slave DSP Serial Peripheral Interface (SPI)

The following I/O features of the DS1104 conflict with the Slave DSP Serial Peripheral Interface (SPI):

Slave DSP Serial Peripheral Interface *)	Signal	Conflicting I/O Feature **)		
			Bit (RTI)	Bit (RTLib)
Conflicts Concerning the Slave DSP Serial Peripheral Interface (SPI) as a Whole				
▪ If you use the following bits of the Slave DSP Bit I/O Unit you cannot use the SPI.				
	SCLK	Slave DSP Bit I/O unit	Bit 10	Group 4, bit 0
	SSTE	Slave DSP Bit I/O unit	Bit 11	Group 4, bit 1
	SSIMO	Slave DSP Bit I/O unit	Bit 12	Group 4, bit 2
	SSOMI	Slave DSP Bit I/O unit	Bit 13	Group 4, bit 3
*) Related RTLib functions: ▪ See Slave DSP Serial Peripheral Interface (DS1104 RTLib Reference 🕮)		**) Related RTI blocks and RTLib functions: ▪ Related RTI blocks: DS1104SL_DSP_BIT_IN_Cx DS1104SL_DSP_BIT_OUT_Cx ▪ Related RTLib functions: see Slave DSP Bit I/O Unit (DS1104 RTLib Reference 🕮)		