DS2301 Direct Digital Synthesis Board

Hardware Reference Guide

Document Version 3.1

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1 Introduction

The DS2301 Direct Digital Synthesis (DDS) board is a member of the DSP-CITpro hardware family specifically designed for high speed signal generation. The DS2301 Direct Digital Synthesis board can be used for fast and complex waveform generation. Its key features are:

- Six independent direct digital synthesis channels featuring
  - TMS320C31 floating-point DSP with 33ns cycle time,
  - 16-bit low glitch DA converter with ±10V output range and 1.5µs settling time,
  - 4Kx32-bit dual-port memory for program downloading and host communication,
  - digital trigger input,
  - digital strobe output.
  - additionally two digital output signals usable alternatively to the DAC.
- All DSPs can communicate with each other via dual-port memory.
- All inputs and outputs are optoisolated.
- All DSPs can be interrupted by each other.
- All analog output signals can be summed onto each other.
- On Board 14-bit customization register.
- PHS - bus interface.
- PC host interface.

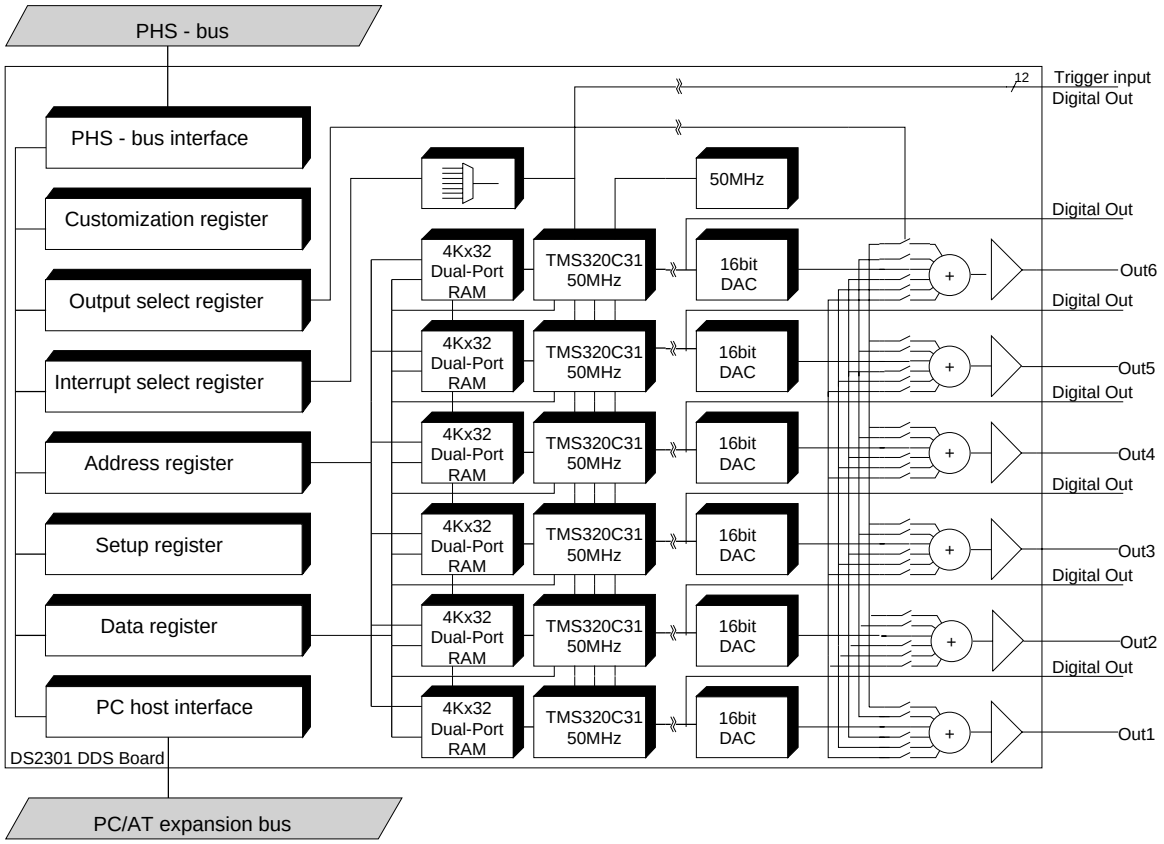


Figure 1.1. Block diagram of the DS2301.

The DS2301 consists of six independent channels each based on the Texas Instruments TMS320C31 3rd generation floating point Digital Signal Processor (DSP), which builds the main processing unit providing fast instruction cycle time for numerically intensive algorithms. Each DSP has been supplemented by a 4 KWords dual-port memory for program downloading and communication by a host, a master DSP or any of the on-board DSPs. Each DSP is connected to a fast 16-bit DAC which can be updated at a maximum rate of 890kHz.

The DS2301 can act as an intelligent output unit which generates complex waveforms in a dSPACE modular system. It can also be used as a stand-alone PC/AT expansion card with parameters coming directly from the PC/AT.

2 Host PC interface

The DS2301 interfaces to the host by a block of eight 16-bit I/O-ports. The I/O interface is used to perform board setups, program downloads, and runtime data transfers.

The DS2301 DDS board may be used in every 80286/386/486-based IBM-PC/AT or compatible personal computer providing a free 13.4" length industry standard architecture (ISA) slot with 16-bit connector (long socket on the motherboard). For proper operation of the DS2301 the following conditions must be met:

- The host computer's power supply must deliver an additional 4.0 Amp. on the + 5 Volt line.
- 16 unused consecutive 8-bit I/O-ports must be available in the 64K host I/O-space.
- The host clock frequency must not exceed 8.33 MHz during expansion bus accesses. Many faster PC/AT compatibles have a bus clock differing from the actual CPU speed.

If you are not sure that your computer meets these requirements consult your computer's technical reference manual or ask your dealer. If still in doubt contact dSPACE customer support before proceeding.

2.1 Setting up the DS2301

Before inserting the DS2301 DDS board the I/O-port base address must be set by the 8-bit switch-set (S1) located at the bottom side of the board (refer to Figure 2.1.1).

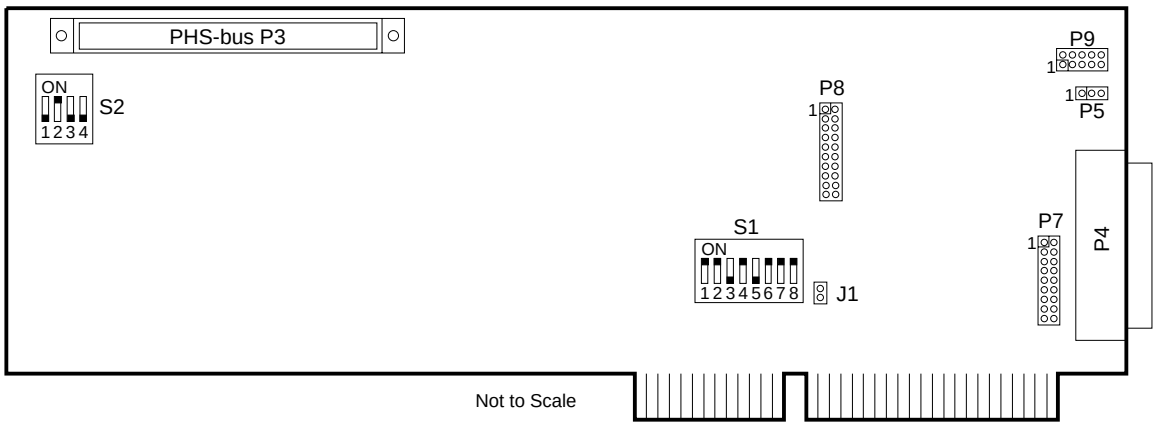


Figure 2.1.1. Location of the address switches and connectors.

Switches 1 and 2 determine address lines A15 and A14 of the I/O-port base address and switches 3 to 8 address lines A9 to A4. A switch turned ON represents a binary zero and OFF a binary one. Address lines A10 to A11 are always treated as binary zero.

Figure 2.1.2 shows which address lines are selectable (marked as 'S' followed by the respective switch number) and which are fixed (marked by their logical value). The address lines which don't care are marked as X. A3 to A0 are used to select the various registers of the DS2301. This address selection scheme has been chosen to avoid address overlap with other PC/AT expansion boards like printer cards or serial interfaces.

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4
S1	S2	X	X	0	0	S3	S4	S5	S6	S7	S8

Figure 2.1.2. I/O-base address selection.

The DS2301 uses eight 16-bit I/O-port addresses in the host's I/O-space which are selected by address bits A3 to A1. The decoding scheme of the DS2301 requires the board's I/O-port base address to be set to a value with A3 to A0 as zero. Since many peripheral boards do not use all 16 address bits for I/O decoding, care must be taken to select a proper I/O-port base address which must not overlap

with other boards residing in the host computer. The DS2301 is factory set to an I/O-port base address of 280H. The address range from 280H to 28FH is usually unused. The prototype area (address range 300H to 31FH) mirrors repeatedly in the 64K address space at an interval of 400H (i.e. 700H to 71FH, B00H to B1FH, etc.). All these address ranges can be used for the DS2301 if they are not occupied by other peripheral boards.

Note: Assigning an I/O-address already used by other devices may lead to system failure, data losses on the hard disk and even hardware damage. Refer to the IBM-PC/AT Technical Reference Manual for a description of the standard I/O-map.

Table 2.1.1 shows some usable I/O-base addresses for the DS2301 and their corresponding switch settings (check availability before use).

I/O base address	Switch setting								Predefined function in the PC/AT
	1	2	3	4	5	6	7	8	
0200H	0	0	1	0	0	0	0	0	none
0280H	0	0	1	0	1	0	0	0	(default)
0300H	0	0	1	1	0	0	0	0	prototype area
0310H	0	0	1	1	0	0	0	1	prototype area
0380H	0	0	1	1	1	0	0	0	SDLC bisync 2
8300H	1	0	1	1	0	0	0	0	prototype area (mirrored)

Note 0 = Switch is ON
1 = Switch is OFF

Table 2.1.1. I/O-port base address setup.

The DS2301 PC interface can be disabled by jumper J1. To disable the PC interface jumper J1 has to be inserted. To enable the PC interface the jumper J1 has to be removed. J1 is located on the right bottom side of the DS2301 (refer to Figure 2.1.1).

2.2 PC interface description

The I/O-interface between the host computer and the DS2301 consists of a block of eight consecutive 16-bit I/O-ports. The on-board dip-switches are used to select the base address of this block within the 64K I/O-address range of the PC/AT. Table 2.2.1 shows the relationship between I/O-operations and the associated registers. For I/O-address calculation the offsets given must be added to the board's base address as set according to Section 2.1.

Offset	Width	Name	Access	Function
00H	16	LDR	RD/WR	Lower data register. Contains the lower 16 bits of the 32-bit word during host accesses to dual-port memory.
02H	16	UDR	RD/WR	Upper data register. Contains the upper 16 bits of the 32-bit word during host accesses to dual-port memory.
04H	16	AR	RD/WR	Autoincrement address register.
06H	16	STP	RD/WR	Setup register.
08H	16	LOSR	RD/WR	Lower output summing register. Contains the lower 16 bits of the 32-bit word during host access to OSR register.
0AH	16	UOSR	RD/WR	Upper output summing register. Contains the upper 16 bits of the 32-bit word during host access to OSR register.
0CH	16	LISR	RD/WR	Lower interrupt select register. Contains the lower 16 bits of the 32-bit word during host access to ISR register.
0EH	16	UISR	RD/WR	Upper interrupt select register. Contains the upper 16 bits of the 32-bit word during host access to ISR register.

Table 2.2.1. Host I/O interface.

The DS2301's host interface maps the 32-bit registers into 16-bit registers for the PC. To access a 16-bit register a 16-bit I/O-instruction is required. Using

8-bit I/O-instructions will give erroneous results. If a high-level language is used to program the host interface registers it must be guarantied that the compiler generates the correct instructions.

All 32-bit registers of the host interface have to be accessed in a particular order. For reading or writing the dual-port memory, the output summing register and the interrupt select register a particular sequence is mandatory. Refer to Section 2.3 for further details.

Figure 2.2.1 shows the alignment of the 16-bit PC registers within the 32-bit board registers.

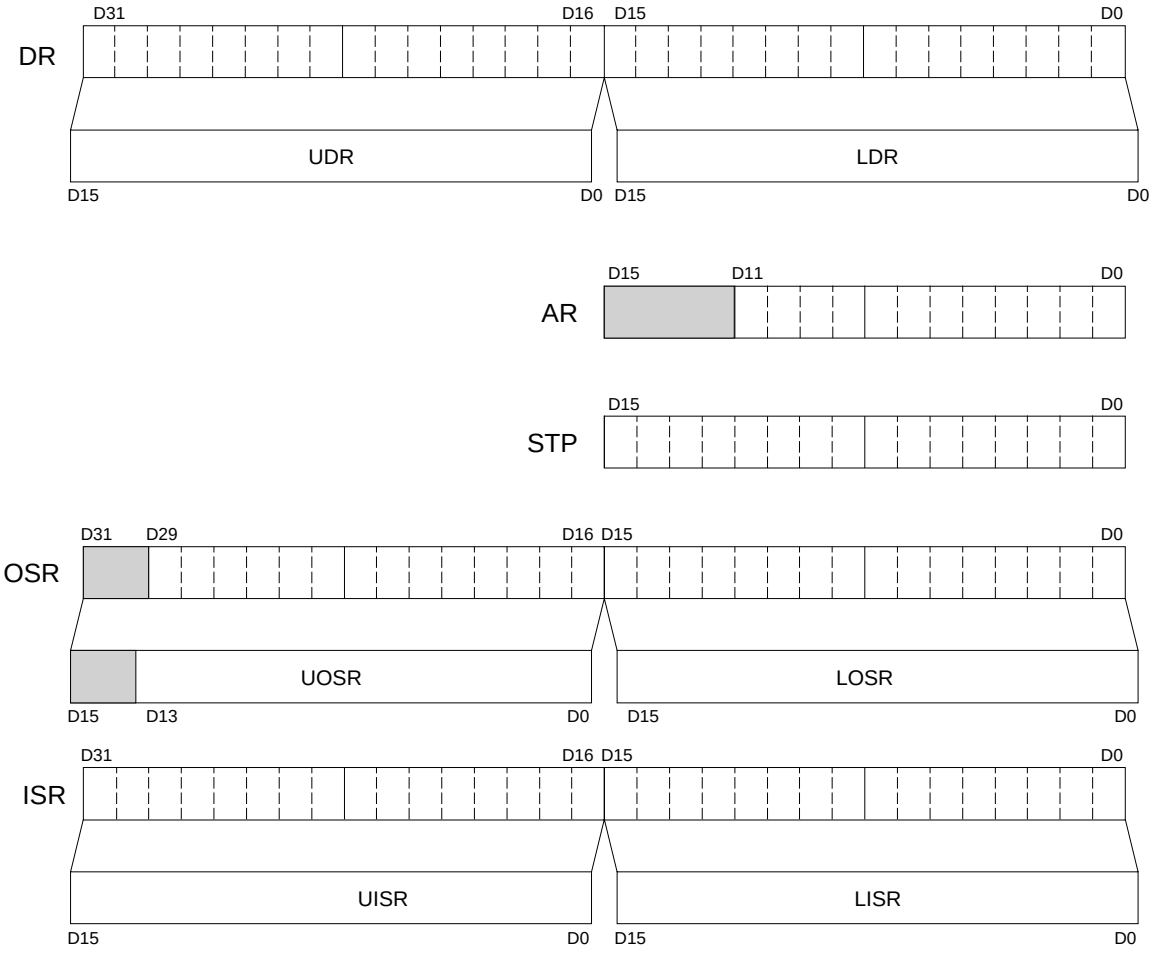


Figure 2.2.1. PC register alignment.

2.3 PC 32-bit register access

For PC access the 32-bit registers are split into two 16-bit registers (refer to Section 2.2). To transfer a 32-bit word between host computer and DS2301 two consecutive 16-bit read or write operations are required. First the lower 16 bits are accessed using the lower half register (e.g. LDR), and then the upper 16 bits by using the upper half register (e.g. UDR). The on-board bus-width converter temporarily stores the 32-bit value and performs only a single 32-bit access to the DS2301. For correct operation of the bus-width converter the lower - upper accessing sequence as described above is mandatory.

3 PHS-bus interface description

The DS2301 appears on the PHS-bus as a set of 32-bit random access registers. The base address of this register set (board address) must be manually set by the DIP-switches (S2) located on the left side of the board (refer to Figure 2.1.1). This base address is set in increments of 16 according to Table 3.1. The labels shown in the table correspond to the numbers printed on the DIP-switches on the DS2301. The default PHS-bus base address of the DS2301 is B0H.

Base addr.	S1	S2	S3	S4
00H	On	On	On	On
10H	On	On	On	Off
20H	On	On	Off	On
30H	On	On	Off	Off
40H	On	Off	On	On
50H	On	Off	On	Off
60H	On	Off	Off	On
70H	On	Off	Off	Off
80H	Off	On	On	On
90H	Off	On	On	Off
A0H	Off	On	Off	On
B0H	Off	On	Off	Off
C0H	Off	Off	On	On
D0H	Off	Off	On	Off
E0H	Off	Off	Off	On
F0H	Off	Off	Off	Off

Table 3.1. Base address setting.

Before setting the base address check that this value is not occupied by another PHS-bus peripheral board. The setup program delivered with the PHS-bus master (processor board) can be used to obtain a list of all connected peripheral boards and their corresponding base addresses.

The DS2301 contains six registers to access and control the six independent DDS channels. To access a particular register the offset given must be added to the board base address. Table 3.2 shows the address map of the DS2301.

Offset	Access	Name	Function
00H	RD/WR	DR	Data register
01H	RD/WR	AR	Address register
02H	RD/WR	STP	Setup register
03H	RD/WR	OSR	Output summing register
04H	RD/WR	ISR	Interrupt select register
05H · 0EH	RD / WR	-	Not used, reserved
0FH	RD	IDR	Identification register

Table 3.2. PHS-bus register address map.

The alignments of the registers within the 32-bit word are shown in Figure 3.1. All unused bits of a 32-bit word (in gray shaded areas) are undefined when read and should be zero when written.

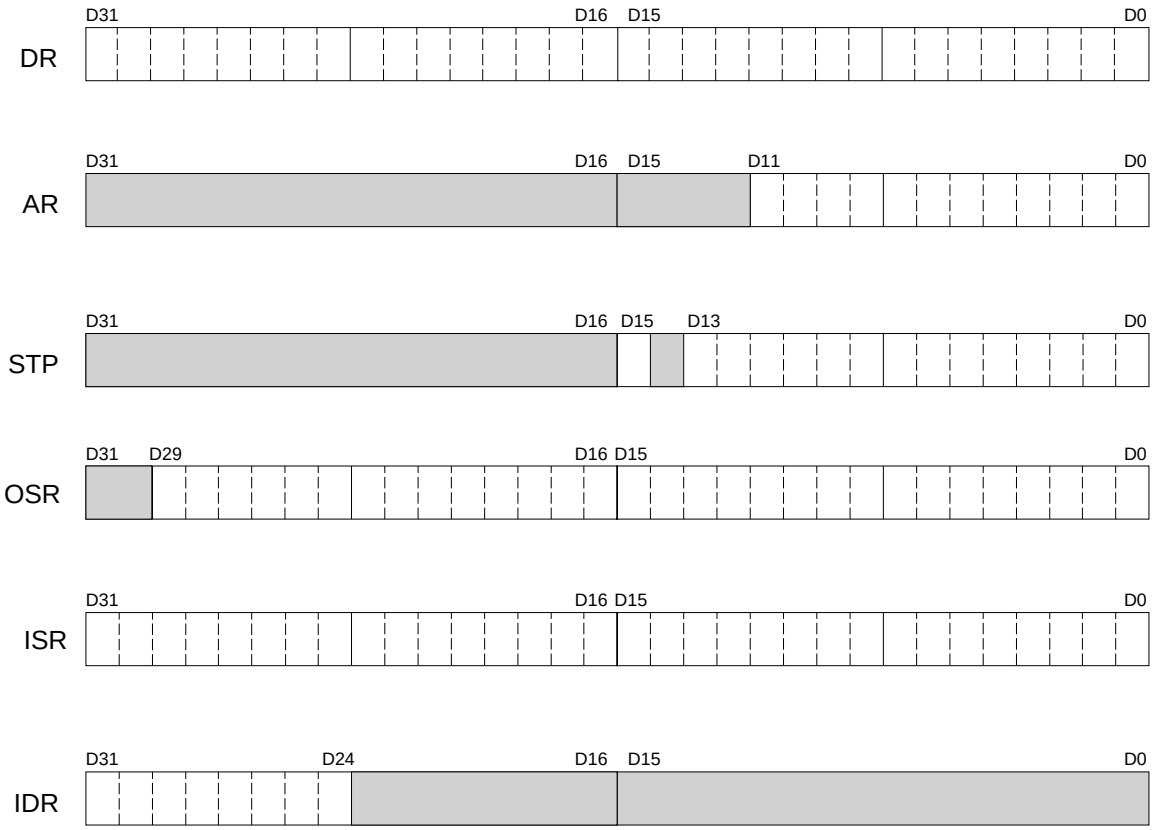


Figure 3.1. PHS-bus register alignment.

4 Register description

4.1 Data register

The data register is a 32-bit wide read/write register used to access the dual- port memory. Read and write operations on the data register are always performed on the memory location currently selected by the address register on the chosen channel.

Figure 4.1.1 shows the format of the data register (DR).

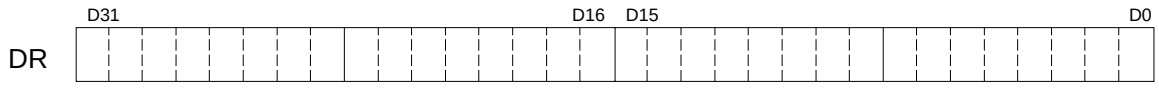


Figure 4.1.1. Data register.

Depending on the content of the INCSTAT bit in the channel select register, the content of the address register is incremented after each data register access thus supporting block transfer without the need to modify the address register for each transfer (refer to section 4.2).

The DS2301 supports simultaneous write operations to several channels by setting the corresponding channel select bits in the STP register (refer to section 4.3).

4.2 Address register

The address register is a 12 bit wide read/write register used to select a location of the dual-port memory of the current channel. The memory location the address register is pointing to can be read or written via the data register.

The address register has an autoincrement mode which can be used for block transfers between the host and the dual-port memory. To enable this mode the INCSTAT bit in the STP register must be set. (Refer to section 4.3). If autoincrement mode is enabled the contents of the address register will be incremented automatically after a 32-bit data register read or write operation has been completed, thus allowing to access consecutive blocks of DSP memory without the need to change the address register for each transfer.

For subsequent accesses to the same memory location (e.g. to poll a ready flag in the dual port memory modified by the DSP), the address register needs only to be written once. The autoincrement mode must be disabled for this type of application.

All unused bits of the AR are undefined when read and should be zero when written.

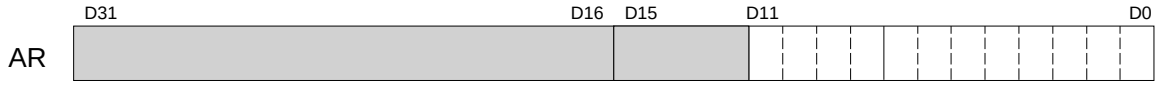


Figure 4.2.1. Address register.

4.3 Setup register

The setup register (STP) is a 15-bit read/write register used to control several modes and states of the DS2301. The STP register includes the reset bits, channel select bits, the autoincrement mode of the address register, the PC / PHS-bus access control bit and the global DSP interrupt request bit. Table 4.3.1 shows the format of the STP register.

	D15	D14	D13	D12	D11 - D6	D5 - D0
STP	ENINT3	PCPHS	GINT2	INCSTAT	CHANNEL	RESET

Bit	Name	Function
0 · 5	RESET	Reset line field. RESET = 0 resets the corresponding DSP. RESET = 1 restarts the respective DSP. The format of RESET is as follows: Bit 0 channel 1 Bit 1 channel 2 Bit 2 channel 3 Bit 3 channel 4 Bit 4 channel 5 Bit 5 channel 6 Note : After reset is released, the DSP will load an application from dual-port memory. Make sure that a valid application is loaded into dual-port memory as the DSP will start in bootloader mode (refer to Section 5.2) On power-up RESET = 0.

Table 4.3.1. Setup register.

Bit	Name	Function
6 · 11	CHANNEL	CHANNEL select bits. CHANNEL selects the channels of the DS2301 which will be accessed by the following Data register accesses. CHANNEL = 1 selects the respective channel. With CHANNEL = 0 the respective channel is not selected. The bits are described as follows. Bit 6 channel 1 Bit 7 channel 2 Bit 8 channel 3 Bit 9 channel 4 Bit 10 channel 5 Bit 11 channel 6 Note : For read operations only one channel must be selected. Otherwise erroneous results will be read. On power-up CHANNEL = 0
12	INCSTAT	Address register autoincrement or static mode. INCSTAT = 1 enables autoincrement mode. INCSTAT = 0 disables autoincrement mode. On power-up INCSTAT = 0.
13	GINT2	Global interrupt request. GINT2 = 1 activates the INT2 interrupt line on all six DSPs. This bit can be used to synchronize several DSPs. GINT2 = 0 releases the INT2 lines. On power-up GINT2 = 0.
14	PCPHS	PC or PHS-bus selection. This write-only bit selects the board access. PCPHS = 0 selects PC as host: the PHS-bus has no access to the DS2301. PCPHS = 1 selects PHS-bus as host: The PC has no access to the DS2301. On power up the PCPHS = 0. **The PCPHS bit can only be accessed by the PC.**
15	ENINT3	Global interrupt 3 enable. This bit enables or disables the interrupt 3 lines of all DSPs. ENINT3 = 0 enables the interrupt 3 lines. ENINT3 = 1 disables the interrupt 3 lines. The interrupt 3 lines must be disabled while the DSP is booting. On power-up ENINT3 = 0.

Table 4.3.1. Setup register (continued).

4.4 Output summing register

The output summing register (OSR) is a 30-bit read/write register to control the output summing amplifiers (refer to section 6.1.2).

	D31 - D30	D29 - D25	D24 - D20	D19 - D15	D14 - D10	D9 - D5	D4 - D0
OSR	unused	SEL6	SEL5	SEL4	SEL3	SEL2	SEL1

Bit	Name	Function
0 · 4	SEL1	Channel 1 select bits. If a bit is set the corresponding output is added to channel 1. If a bit is zero the corresponding output has no effect on channel 1. The bits are described as follows: Bit 0 channel 2 Bit 1 channel 3 Bit 2 channel 4 Bit 3 channel 5 Bit 4 channel 6
5 · 9	SEL2	Channel 2 select bits. If a bit is set the corresponding output is added to channel 2. If a bit is zero the corresponding output has no effect on channel 2. The bits are described as follows: Bit 5 channel 1 Bit 6 channel 3 Bit 7 channel 4 Bit 8 channel 5 Bit 9 channel 6
10 · 14	SEL3	Channel 3 select bits. If a bit is set the corresponding output is added to channel 3. If a bit is zero the corresponding output has no effect on channel 3. The bits are described as follows: Bit 10 channel 1 Bit 11 channel 2 Bit 12 channel 4 Bit 13 channel 5 Bit 14 channel 6

Table 4.4.1 Output summing register.

Bit	Name	Function
15 · 19	SEL4	Channel 4 select bits. If a bit is set the corresponding output is added to channel 4. If a bit is zero the corresponding output has no effect on channel 4. The bits are described as follows: Bit 15 channel 1 Bit 16 channel 2 Bit 17 channel 3 Bit 18 channel 5 Bit 19 channel 6
20 · 24	SEL5	Channel 5 select bits. If a bit is set the corresponding output is added to channel 5. If a bit is zero the corresponding output has no effect on channel 5. The bits are described as follows: Bit 20 channel 1 Bit 21 channel 2 Bit 22 channel 3 Bit 23 channel 4 Bit 24 channel 6
25 · 29	SEL6	Channel 6 select bits. If a bit is set the corresponding output is added to channel 6. If a bit is zero the corresponding output has no effect on channel 6. The bits are described as follows: Bit 25 channel 1 Bit 26 channel 2 Bit 27 channel 3 Bit 28 channel 4 Bit 29 channel 5

Table 4.4.1 Output summing register (continued).

Example : If output channel 4 and channel 5 should be added to channel 1 SEL1 must be set to 01100b.

All unused bits of the OSR are undefined when read and should be zero when written.

4.5 Interrupt select register

All DSPs of the DS2301 can be interrupted by each other. The interrupt select register (ISR) is used to select one of eight interrupt sources. The DSPINT1 input of the DSP is connected to the selected interrupt source.

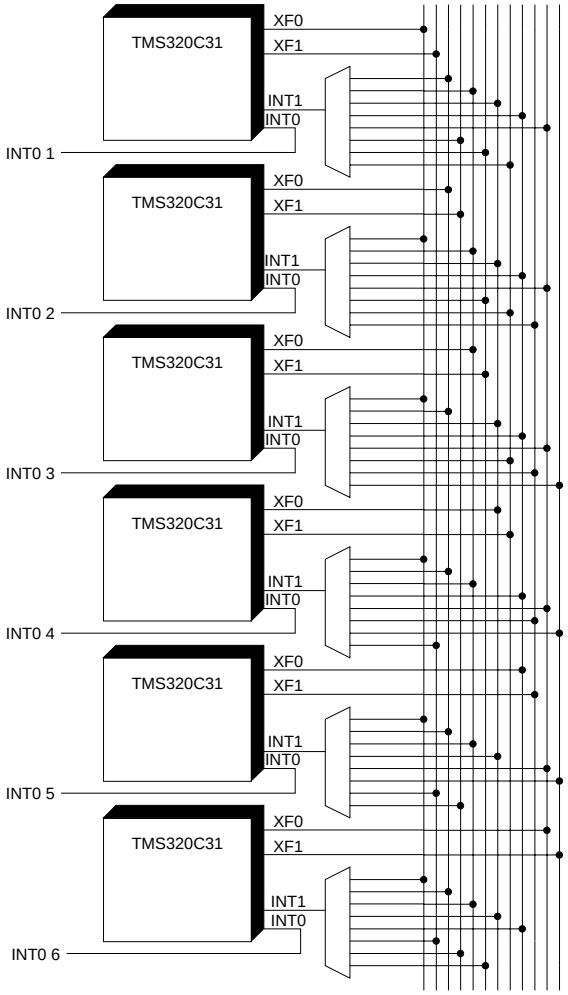


Figure 4.5.1. Interrupt select system.

The DS2301 provides an interrupt multiplexer for each channel. The TMS320C31 I/O-flags (XF0 and XF1) must be set up as outputs and are used as interrupt multiplexer inputs. The I/O flags are accessible at the I/O flag register (IOF) of the TMS320C31.

	D31 - D29	D28 - D26	D25 - D23	D22 - D20	D19 - D17	D16 - D14	D13 - D0
ISR	INT6	INT5	INT4	INT3	INT2	INT1	CUSTOM

Bit	Name	Function
0 · 13	CUSTOM	CUSTOM bit field. The CUSTOM bits are output bits which are connected to the digital customization connector.
14 · 16	INT1	Channel 1 interrupt line select field. The format of INT1 is as follows: 000 channel 2 XF0 001 channel 3 XF0 010 channel 4 XF0 011 channel 5 XF0 100 channel 6 XF0 101 channel 2 XF1 110 channel 3 XF1 111 channel 4 XF1
17 · 19	INT2	Channel 2 interrupt line select field. The format of INT2 is as follows: 000 channel 1 XF0 001 channel 3 XF0 010 channel 4 XF0 011 channel 5 XF0 100 channel 6 XF0 101 channel 3 XF1 110 channel 4 XF1 111 channel 5 XF1

Table 4.5.1. Interrupt select register.

Bit	Name	Function
20 · 22	INT3	Channel 3 interrupt line select field. The format of INT3 is as follows: 000 channel 1 XF0 001 channel 2 XF0 010 channel 4 XF0 011 channel 5 XF0 100 channel 6 XF0 101 channel 4 XF1 110 channel 5 XF1 111 channel 6 XF1
23 · 25	INT4	Channel 4 interrupt line select field. The format of INT4 is as follows: 000 channel 1 XF0 001 channel 2 XF0 010 channel 3 XF0 011 channel 5 XF0 100 channel 6 XF0 101 channel 5 XF1 110 channel 6 XF1 111 channel 1 XF1
26 · 28	INT5	Channel 5 interrupt line select field. The format of INT5 is as follows: 000 channel 1 XF0 001 channel 2 XF0 010 channel 3 XF0 011 channel 4 XF0 100 channel 6 XF0 101 channel 6 XF1 110 channel 1 XF1 111 channel 2 XF1

Table 4.5.1. Interrupt select register (continued).

Bit	Name	Function
29 · 31	INT6	Channel 6 interrupt line select field. The format of INT6 is as follows: 000 channel 1 XF0 001 channel 2 XF0 010 channel 3 XF0 011 channel 4 XF0 100 channel 5 XF0 101 channel 1 XF1 110 channel 2 XF1 111 channel 3 XF1

Table 4.5.1. Interrupt select register (continued).

Example : To interrupt channel 1 by the XF0 pin from channel 6, INT1 must be set to 100b.

4.6 ID register

Each slave-board of the dSPACE DSP-CITpro hardware family contains an identification register at address offset 0FH. This register is used by the DSP-CITpro monitor program to check hardware-software integrity. The IDR is a read-only register and contains a four-bit ID-number in data bits D28 to D31. Bit D24 to D27 are read as zero. All other bits are undefined when read. The ID-number of the DS2301 board is 10.

5 The TMS320C31 DSP

All six channels of the DS2301 contain a TMS320C31 floating-point DSP with 4 KWords external dual-port memory. For synchronized operation the DSPs are driven by the same 60 MHz clock signal. All DSPs can communicate with each other via the dual-port memories as the dual-port memories are mapped in the memory map of each DSP (refer to Section 5.1).

The TMS320C31 third generation floating-point DSP is a high-performance member of Texas Instruments' TMS320 family of VLSI digital signal processors. It performs parallel multiply and ALU operations on integers or floating-point numbers in a single cycle. The TMS320C31 supports a large address space with various addressing modes allowing the use of high-level languages for application development. Some key features of the TMS320C31 are:

- 33 ns single cycle instruction execution time
- object code compatible with the TMS320C30
- two 1K x 32-bit dual access on-chip data RAM blocks
- 64 x 32-bit instruction cache
- 32-bit instruction and data words, 24-bit addresses
- 40/32-bit floating-point / integer multiplier and ALU
- 32-bit barrel shifter
- Eight 40-bit accumulators
- Two independent address arithmetic units
- 2- and 3-operand instructions
- Serial port
- DMA controller for concurrent DMA and CPU operation
- Four external interrupts
- Two 32-bit timers

This section describes only those TMS320C31 features necessary for understanding the DS2301's architecture and operation. For further information about the TMS320C31 refer to the Third Generation TMS320C3x User's Guide available from Texas Instruments.

The TMS320C31 high-speed serial interface is connected to the 16-bit DAC. Section 6 describes the communication between DSP and DAC.

Four interrupt inputs (INT0 to INT3) are supported by the DS2301. INT0, the input with the highest priority, is available on the I/O connector. INT1 can be driven by any other DSP on the DS2301. The interrupt select register connects the INT1 interrupt input to any other DSP (refer to section 4.5). INT2 is used to generate an interrupt to all six DSPs from the host or PHS-bus master. INT3, the interrupt with the lowest priority, is activated by writing to dual-port memory address 0FFFH. INT3 can be used by all DSPs, the PC and the PHS-bus master.

The bus ready signal of the TMS320C31 (RDY) is used to adapt the TMS320C31 timing to the dual-port memory. The bus control register of the TMS320C31 is programmed for two wait states and external ready generation. The DS2301 will then provide a proper ready signal for the external memory.

5.1 DSP memory map

The TMS320C31 supports a linear address space of 16 M 32-bit words. The DS2301 contains 4 KWords of two wait state dual-port RAM located at address 01000H to 01FFFH. Additionally the six 4 KWords on-board dual-port memories are mapped from address 08000H to 0DFFFH. The I/O control register (IOCTL) is located at address 02000H and the I/O status register (IOSTS) at address 03000H. Figure 5.1.1 shows the complete TMS320C31 memory map.

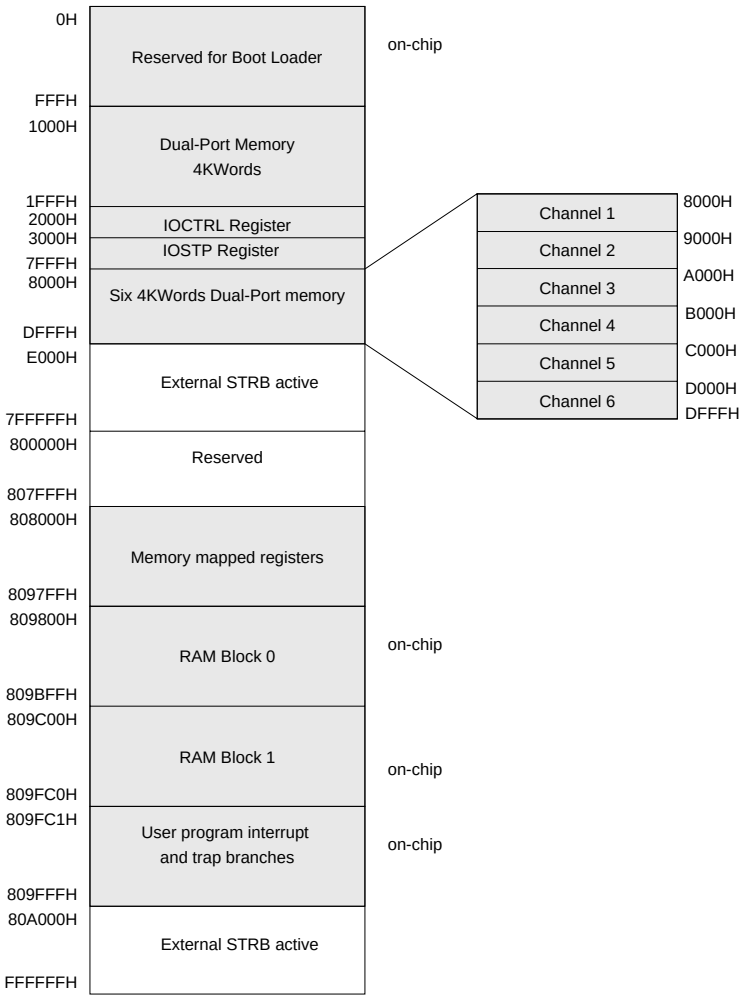


Figure 5.1.1. DS2301 memory map.

5.2 Memory

The TMS320C31 DSP provides two different modes of operation: microprocessor mode and microcomputer mode. The DS2301 uses the TMS320C31 in microcomputer mode. In this mode the on-chip bootloader is mapped into memory locations 0H through 0FFFH. The bootloader loads the application from dual-port memory into the internal memory or any other memory location. The loader software distributed with the board is configured to load the applications into on-chip memory. For further information about the bootloader refer to the Third Generation TMS320C3x User's Guide available from Texas instruments.

The base timing of the primary bus is controlled by the primary bus control register (PBCR) of the TMS320C31. The PBCR is memory mapped at address 808064H (refer to the TMS320C3x User's Guide). When the TMS320C31 is reset the slowest possible memory bus timing is selected. It must be reprogrammed by the application program to allow full speed operation of the DS2301. The various fields of the PBCR should be programmed as follows:

BNKCMP — The bank compare field allows the automatic insertion of wait states when crossing a memory bank boundary. This is necessary if memories are require several cycles to turn on. The memories installed on the DS2301 do not require the insertion of wait states so BNKCMP is programmed to all zeros (00000B).

WTCNT — The wait count field specifies the number of wait cycles to insert when software wait state generation is selected. For the DS2301 the WTCNT is set to two wait states for accessing the dual-port memory.

SWW — The SWW field determines how the memory ready signal is generated. The DS2301 contains a hardware ready generator that activates the DSP's RDY input when the dual-port memory has finished the access. The minimum access time to the dual-port memory requires two wait states. This wait signal is generated by the on-chip wait state counter (WTCNT). The external RDY input is controlled by the dual-port memory busy line. If the host

and the DSP try to access the same memory location at the same time the dual-port memory activates the busy line to signal that the access is currently not possible. The SWW field must contain 11B to select the logical AND of the RDY input and the software ready generation.

HIZ — Setting the HIZ bit forces the TMS320C31 into a hold state thus releasing the external bus. The DS2301 doesn't use the arbitration logic of the TMS320C31 so the HIZ must be programmed to zero.

NOHOLD — The NOHOLD bit controls whether the bus is released when an external hold is requested. Since the DS2301 doesn't use the arbitration logic of the TMS320C31, NOHOLD should be set to one.

After a reset is applied to the TMS320C31 the instruction fetch cache system is turned off. To enable the cache system the cache enable bit (CE) in the DSP's status register must be set and the cache freeze bit (CF) must be cleared. When the cache system is enabled the host should not modify the DSP program while the DSP is running since it is not predictable whether the TMS320C31 will fetch the modified program code from memory or the unmodified instructions already residing in its internal cache memory. The TMS320C31's cache system only applies to instruction fetches while data transfers always bypass the cache. This allows to keep the cache enabled when the host accesses DSP data at runtime. Correct programming of the cache control bits and the PBCR is mandatory to achieve the full performance of the DS2301.

In microcomputer mode, memory locations 0809FC1H to 0809FFFH are reserved for interrupt service and trap vectors and contain the branch instructions to the entry points of the respective service routines.

To load an application to the DSP the program data must be written in a special format to the dual-port memory. The on-chip bootloader needs a four-word header including information for memory configuration, program block size and destination address followed by the program code. For subsequent code blocks the bootloader needs a two-word header consisting of the block size and the destination address of the next code block. The loader is terminated by appending the value 00000000H to the last block. Table 5.2.1 shows the bootloader format for the DS2301. For further information refer to the TMS320C3X User's Guide.

Memory location	Description	Data for DS2301
0	Boot memory type (8, 16 or 32)	00000020H
1	Boot memory configuration (primary bus control register)	0000005AH
2	Program block size	BLK1
3	Destination address	00809800H
4	Program code starts here	
…	…	
BLK1+4	Program code ends here	
BLK1+5	Program block size	BLK2
BLK1+6	Destination address	
BLK1+7	Program code starts here	
…	…	
	Program code ends here	
	End of boot image	00000000H

Table 5.2.1. Bootloader program format.

Note that the GINT2 bit must be deactivated and the ENINT3 bit must disable the INT3 interrupt while the DSPs are booting.

5.3 Serial interface

The TMS320C31's serial port is connected to the on-board DAC. For the communication between the DSPs and the DACs the variable burst mode is used. The initialization of the serial port and the communication method between the DSPs and the DACs are described in section 6.

5.4 External DSP interrupts

The interrupt input with the highest priority (INT0) is available on the I/O connector P4 and can be used as external interrupt input. INT1 is connected to one of the eight on-board interrupt sources depending on the contents of the interrupt select register (refer to section 4.5). INT2 is a global interrupt which enables the host to generate an interrupt to all six DSPs simultaneously. INT3 is activated by writing to dual-port memory location 0FFFH. Table 5.4.1 shows the corresponding DSP interrupt lines.

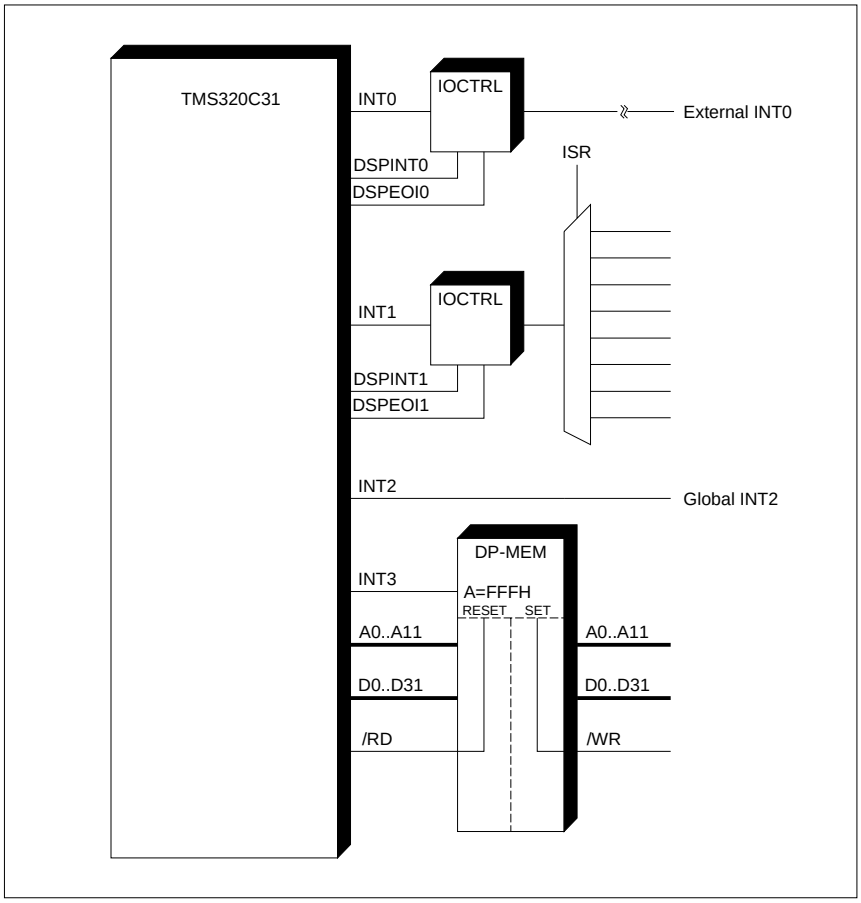


Figure 5.4.1. External DSP interrupts.

Source	Interrupt line
External interrupt input	INT0
One of eight on-board interrupt sources	INT1
Global host interrupt	INT2
Other DSPs, PC or PHS-bus master	INT3

Table 5.4.1 DSP interrupt sources.

The external interrupt lines are TTL compatible inputs with 47KΩ pull-up resistors to +5 Volt.

A low to high edge on INT0 or INT1 sets the respective DSPINT flag in the IOCTL register and activates the DSP's interrupt line. If the interrupt is enabled in the TMS320C31's interrupt enable register (IE), and the global interrupt enable bit (GIE) is set in the DSP's status register, an interrupt call is performed to the interrupt address in internal memory. This address must contain a branch instruction to the interrupt service routine. After the interrupt has been serviced the DSP must set the DSPEOIx bit in the IOCTL register to reset the DSPINTx flag and to release the corresponding interrupt line. Then the respective interrupt flag in the DSP's interrupt flag register (IF) must be cleared. Due to the interrupt system of the TMS320C31 a delay of two cycles (NOP instructions) must be inserted between the two operations. Refer to the TMS320C3x User's guide for further information about the interrupt system.

To generate a global interrupt from the host or PHS-bus master, the GINT2 bit in the STP register must be set high. This interrupt is used for simultaneous program start, or for program synchronization. After the interrupt service the corresponding interrupt flag in the DSP interrupt flag register (IF) must be cleared.

To generate an INT3 interrupt, any value must be written to dual-port memory location 0FFFH. This will activate the INT3 interrupt input line. The DSP must read the value from dual-port memory location 0FFFH to clear the interrupt

INT3. After the interrupt has been serviced the DSP must clear the respective interrupt flag in the DSP's interrupt flag register (IF). Due to the interrupt system of the TMS320C31 a delay of two cycles (NOP instructions) must be inserted between the reading of the dual-port memory and the clearing of the interrupt flag. Note that the ENINT3 bit in the STP register must be cleared to enable the INT3 lines.

5.5 I/O control register (IOCTL)

The I/O control register (IOCTL) is a 2-bit read/write register used to control and query the states of the two interrupt lines (INT0 and INT1) of each TMS320C31. The end-of-interrupt bits can be set to release the TMS320C31's interrupt input. The DSPINTx flags display the state of the interrupt lines.

Table 5.5.1.1 shows the format of the IOCTL register during read operations and table 5.5.2.1 the format during write operations.

5.5.1 Reading the IOCTL register

The I/O-control register contains two DSPINT flags. Table 5.5.1.1 shows the format of the IOCTL register when read.

	D31	D30	D29 - D0
IOCTL	DSPINT1	DSPINT0	unused

Bit	Name	Function
30	DSPINT0	TMS320C31 interrupt line 0. DSPINT0 = 1 indicates an active interrupt request. DSPINT0 = 0 indicates that the DSP has finished interrupt service. DSPINT0 is set when an interrupt is pending on the external interrupt input. DSPINT0 is cleared by setting the DSPEOI0 bit in the IOCTL register.
31	DSPINT1	TMS320C31 interrupt line 1. DSPINT1 = 1 indicates an active interrupt request. DSPINT1 = 0 indicates that the DSP has finished interrupt service. DSPINT1 is set when an interrupt was generated by one of the other DSPs. DSPINT1 is cleared by setting the DSPEOI1 bit in the IOCTL register.

Table 5.5.1.1. Reading the IOCTL register.

5.5.2 Writing the IOCTL register

The IOCTL register contains the two end-of-interrupt bits. Table 5.5.2.1 shows the format of the IOCTL register during write operations.

	D31	D30	D29 - D0
IOCTL	DSPEOI1	DSPEOI0	unused

Bit	Name	Function
30	DSPEOI0	End of interrupt line. Writing a 1 resets the DSPINT0 flag in the IOCTL register and the respective DSPINT0 line. Writing a zero has no effect. Before leaving the corresponding interrupt routine with the RETI instruction this flag must be set to clear the TMS320C31’s interrupt input.
31	DSPEOI1	End of interrupt line. Writing a 1 resets the DSPINT1 flag in the IOCTL register and the respective DSPINT1 line. Writing a zero has no effect. Before leaving the corresponding interrupt routine with the RETI instruction this flag must be set to clear the TMS320C31’s interrupt input.

Table 5.5.2.1 Writing the IOCTL register.

5.6 I/O status register (IPSTS)

The I/O status register (IOSTS) is a 2-bit read-only register used to monitor the external input INT0 and the external input INT0 from the neighbour channel. Table 5.6.1 shows the contents of the I/O status register for each channel.

	D31	D30	D29 - D0
Channel 1	INT0 2	INT0 1	unused
Channel 2	INT0 1	INT0 1	unused
Channel 3	INT0 4	INT0 3	unused
Channel 4	INT0 3	INT0 4	unused
Channel 5	INT0 6	INT0 5	unused
Channel 6	INT0 5	INT0 6	unused

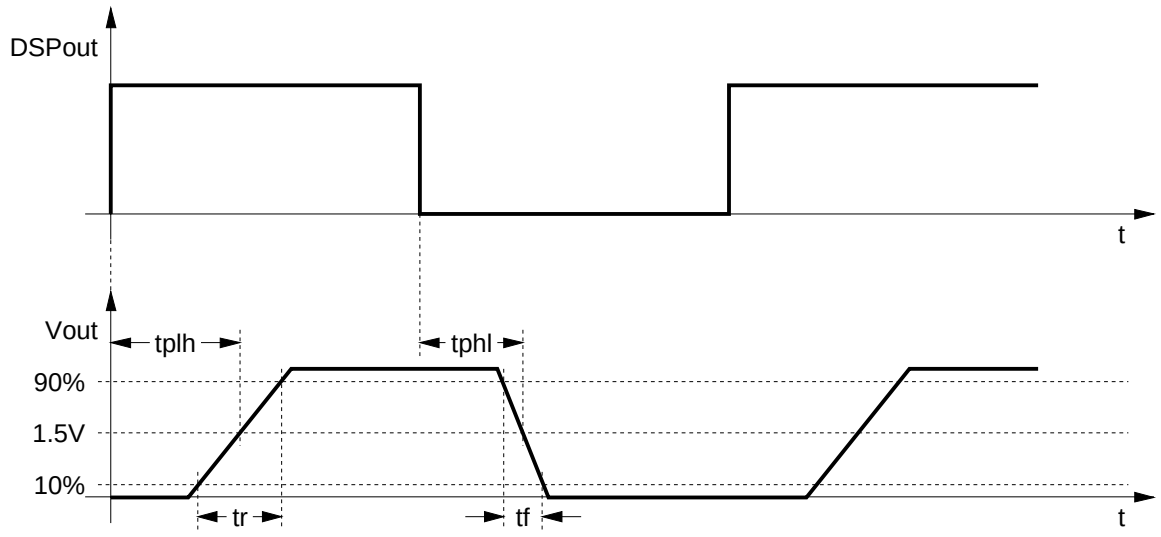
Table 5.5.1.1. I/O status register (IOSTS)

5.7 Digital output

The TCLK0 pin of the TMS320C31 is opto isolated and available on the I/O connector (P4). The outputs are TTL compatible open collector outputs with 680Ω pull-up resistors to +5V. Due to the opto-isolation the maximum output frequency is 10MHz. The TCLK0 pin can be configured as a general purpose output or as pulse generator driven by timer 0.

Several bits in the TMS320C31's Timer0 Global-Control register are used to configure the TCLK0 pin. The Timer0 Global-Control register is located at the on-chip address 0808020H. To configure the TCLK0 pin as a general purpose output, CLKSRC must be set to one and FUNC must be set to zero. The DATOUT bit drives the TCLK0 pin.

To configure the TCLK0 pin as a pulse generator driven by timer 0, CLKSRC and FUNC must be set to one. In this mode the TCLK0 pin is driven by the output of the timer 0. For further information refer to the Texas Instruments TMS320C3x User's Guide.



TCLK0	tplh=60ns, tr=50ns, tphl=80ns, tf=15ns	typ. (Cl=15pF)
DX	tplh=30ns, tr=15ns, tphl=30ns, tf=10ns	typ. (Cl=15pF)
FSX	tplh=70ns, tr=90ns, tphl=40ns, tf=10ns	typ. (Cl=15pF)

Figure 5.7.1. Digital output timing.

Two signals of each TMS320C31's serial port normally used by the DAC can also be used as digital outputs. The signals are DX0 and FSX0. If these signals are used as digital outputs the DAC must be unconnected while delivering erroneous output signals. The signals are opto-isolated and available on the I/O connector (P4). The FSX0 signal is a TTL compatible open collector output with 2.2KΩ pull-up resistor to +5 Volt. The DX0 signal is a TTL compatible totem pole output.

Several bits in the TMS320C31's FSX/DX/CLKX Port-Control register are used to configure the DX0 and FSX0 pins. The FSX/DX/CLKX Port-Control register is located at the on-chip address 0808042H. To configure the DX0 pin as a general purpose output DXFUNC must be set to zero and DXI/O must be set to one. To configure FSX0 pin as a general purpose output FSXFUNC must be set to zero and FSXIO must be set to one. The DXDATOUT and FSXDATOUT bits drives the output pins.

6 DA subsystem

The DS2301 contains six identical 16-bit low glitch DA-converters followed by a software controlled output summing amplifier. The DA-converters are connected to the serial port of their corresponding DSP. To prevent ground loops, all supply voltages and signals of the DA subsystem are isolated from the PC/AT power supply.

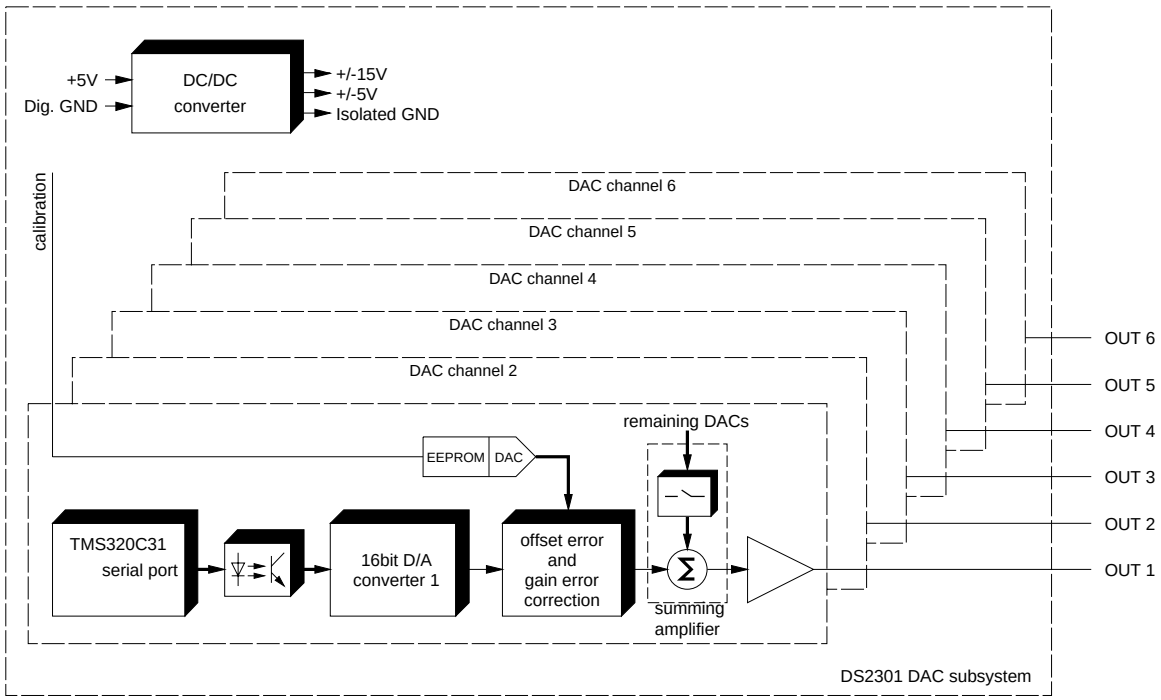


Figure 6.1. Block diagram of DAC subsystem.

The DA subsystem is controlled by several registers. The OSR, which controls the output summer, is accessible by the PC interface and the PHS-bus interface (refer to Section 2 and Section 3). Since the DACs are connected to the serial ports of the DSPs the data transfer to the DACs is controlled by the register sets of the serial ports of the DSPs (refer to Section 6.2.).

6.1 DA-channel description

Each of the six DAC channels is opto-isolated from the digital part of the DS2301. It contains a 16-bit low glitch DAC, an offset- and gain error correction circuit and an output summing amplifier connected to the output buffer. The serial data transmission to the DACs allows a maximum update rate of 890KHz. The DACs accept left aligned two's complement input code and have a single ended voltage output with a ±10V output span. The return lines of the analog outputs are connected to isolated ground.

6.1.1 DAC register

The DACs of the DS2301 are connected to the serial ports of the DSPs. For proper operation of the DACs the serial ports must be initialized before writing data to the DAC for the first time. Writing a value to the DAC is then accomplished by writing this value to the DXR register of the corresponding DSP. No further control statements are required for writing a value to the DAC, because the serial port transfers data automatically.

Register	Peripheral Address	D15..D0
Data transmit register DXR	808048H	DAC data

Table 6.1.1.1. DAC register

Output voltage range	32-bit data range		Code
	HEX	INTEGER	
10V	7FFF	32767	2's complement
.	.	.	
0V	0000	0	
.	.	.	
-10V	8000	-32768	

Note: Only the lower 16 bits (D0 to D15) of the 32-bit word are significant.

Table 6.1.1.2. DAC input format

The serial data transmission to the input register of the DAC is hardware controlled and does not affect the performance of the DSP. During data transmission the DSP continues program execution.

The DAC keeps its previous output voltage until the serial transmission is completed. The transmitted value is latched into the output register of the DAC automatically after the serial transmission is completed. This transmission requires 1.26µs at a system clock of 60MHz. After the data is latched into the output register of the DAC, The DAC begin to settle to its new output voltage. Figure 6.1.1.1. shows the DAC output timing.

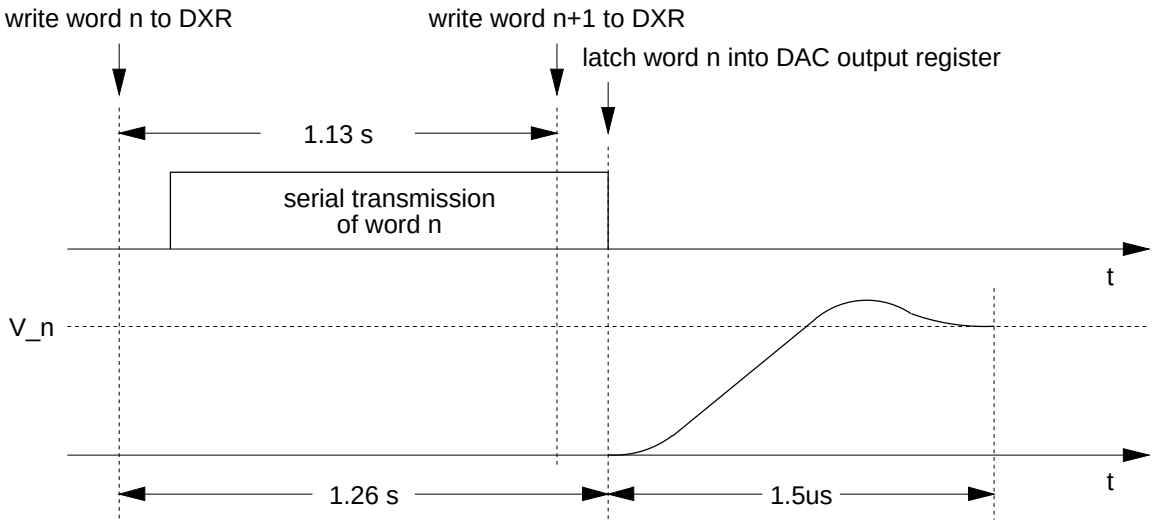


Figure 6.1.1.1. DAC output timing

After the serial transmission has been started by writing to the DXR register, further data must not be written to the DXR during the following 1.13µs. The minimum update interval of the DXR amounts to 1.13µs. However, note that the DAC needs about 1.5µs to settle to its final value.

Using an update interval of less than 1.13µs causes the FSX signal of the DSP's serial port not to occur. Values written to the DAC can not be latched into the DAC's output register. The analog output of the corresponding channel keeps

its previous output voltage until the update interval is increased to a value greater or equal to 1.13µs. Figure 6.1.1.2. shows the relationship between the signals of the serial port of the DSP and the behavior of the DAC output voltage.

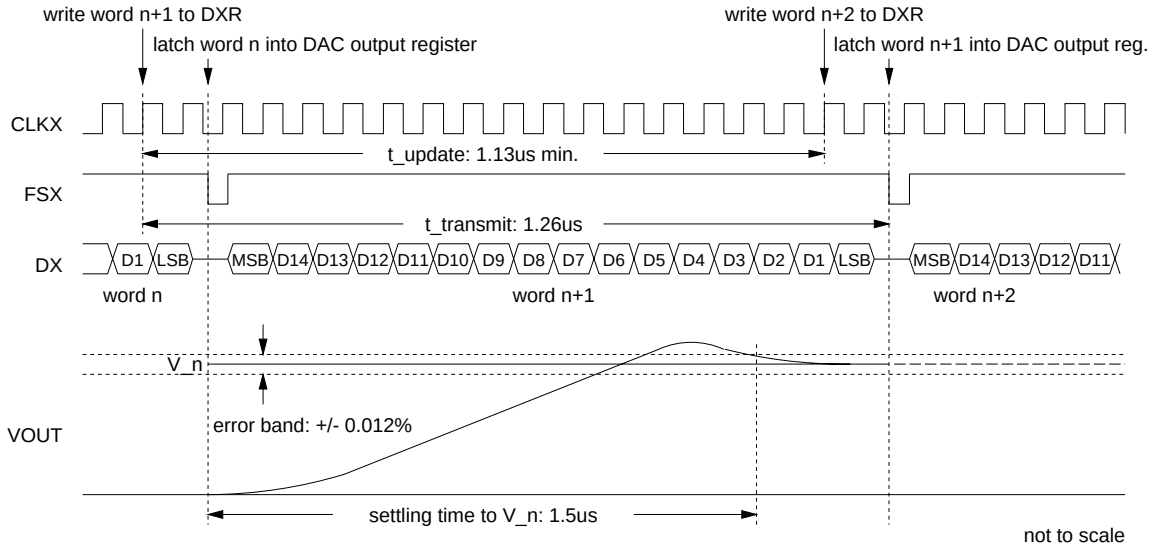


Figure 6.1.1.2. DAC output timing

6.1.2 Output summing amplifier

The output summing amplifier offers high flexibility in signal generation of complex waveforms without decreasing the performance of the DSP. Complex signals with high resolution can be created by generating partial signals separately by single channels and then adding them by the output summing amplifier.

Each output of the DS2301 can be added to each other. The OSR register is used to setup the output summing amplifier (refer to section 4.4).

6.1.3 Analog output as digital output

Since the maximum output current of the analog outputs of the DS2301 is 5mA they can be used as digital outputs with TTL drive capability. This can be useful if disturbed signals for certain test purposes have to be generated. Otherwise the digital outputs should be used instead (refer to section 5.7).

IMPORTANT

After power-up the analog outputs of the DS2301 are set to an undefined value within the full scale range of ±10V. If the analog outputs of the DS2301 are used as digital outputs the following precautions may be required in the given order before every power up to protect the externally connected devices from damage:

- Disconnect the I/O connector (P4) before power up.
- Power up the PC with the DS2301.
- Run an application which loads the DACs with a defined value or which resets the DACs.
- Finally connect the I/O connector (P4).

Note that the analog outputs of the DS2301 have a slew rate of about 15V/µs. For most digital design technologies a much higher slew rate is mandatory. To avoid undefined input levels at the digital input circuits the use of Schmitt Trigger circuits is recommended. This also solves the above overvoltage problem. For that purpose the customization module may be used (refer to section 7.3)

6.2 Initialization of DA-channel

The serial port of the TMS320C31 can operate in various modes, but on the DS2301 the variable burst mode is mandatory. This section only describes how to initialize the serial port. To understand the architecture and the operation of the serial interface refer to the TMS320C3x User's Guide available from Texas Instruments.

Table 6.2.1 shows all the registers of the serial port which must be initialized for operating in variable burst mode. All registers shown must be loaded with the given values.

Register	Peripheral Address	Data
Global control	808040H	0C041144H
Transmit port control	808042H	00000333H
S_port timer control	808044H	0000000BH
S_port timer period	808046H	00010001H

Table 6.2.1. Serial port initialization values

7 Connector pin-outs

7.1 PHS-bus connector

Pin	Signal
a1	GND
a2	D31
a3	D29
a4	D27
a5	D25
a6	D23
a7	D21
a8	D19
a9	D17
a10	D15
a11	D13
a12	D11
a13	D9
a14	D7
a15	D5
a16	D3
a17	D1
a18	A7
a19	A5
a20	A3
a21	A1
a22	
a23	
a24	
a25	
a26	
a27	
a28	/IOWAIT
a29	/IORD
a30	
a31	
a32	GND

Pin	Signal
c1	GND
c2	D30
c3	D28
c4	D26
c5	D24
c6	D22
c7	D20
c8	D18
c9	D16
c10	D14
c11	D12
c12	D10
c13	D8
c14	D6
c15	D4
c16	D2
c17	D0
c18	A6
c19	A4
c20	A2
c21	A0
c22	
c23	
c24	
c25	
c26	
c27	
c28	
c29	/IOWR
c30	
c31	
c32	GND

Table 7.1.1. PHS-bus connector pin-out

7.2 I/O connector (P4)

Pin	Signal
1	OUT 1
2	Analog GND
3	OUT 3
4	Analog GND
5	OUT 5
6	Analog GND
7	FSX 1
8	FSX 4
9	DX 1
10	DX 4
11	Digital GND
12	TCLK 1
13	TCLK 4
14	INT0 1
15	INT0 4

Pin	Signal
16	Analog GND
17	Analog GND
18	Analog GND
19	Analog GND
20	Analog GND
21	Analog GND
22	FSX 2
23	FSX 5
24	DX 2
25	DX 5
26	Digital GND
27	TCLK 2
28	TCLK 5
29	INT0 2
30	INT0 5

Pin	Signal
31	OUT 2
32	Analog GND
33	OUT 4
34	Analog GND
35	OUT 6
36	FSX 3
37	FSX 6
38	DX 3
39	DX 6
40	Digital GND
41	TCLK 3
42	TCLK 6
43	INT0 3
44	INT0 6

Table 7.2.1. I/O connector pin-out.

The I/O connector is a 44-pin high-density female SUB-D connector located on the rear bracket of the DS2301 (refer to figure 2.1.1). The connector provides various signal groups as shown in table 7.2.2. A mating 44-pin high-density male SUB-D connector is delivered with the board.

Name	Function
OUT 1 - 6	Analog outputs. Isolated from system ground.
Analog GND	Analog return lines. Isolated from system ground. Internally connected to Digital GND.
Digital GND	Digital return line. Isolated from system ground. Internally connected to Analog GND.
DX 1 - 6	TMS320C31 serial port output. Can be used alternatively to the DAC. Isolated from system ground.
FSX 1 - 6	TMS320C31 serial port output. Can be used alternatively to the DAC. Isolated from system ground.
TCLK 1 - 6	TMS320C31 timer outputs. Isolated from system ground.
INT0 1 - 6	TMS320C31 interrupt line 0 inputs. Isolated from system ground.

Table 7.2.2. I/O connector signal description.

All digital input pins have 47KΩ pull-up resistors to +5V. The TCLK output is a open collector output with 680Ω pull-up resistor to +5V. The FSX, TCLK and DX outputs are totem pole outputs.

7.3 Customization module

The customization module can be used to include filters, signal conditioners, amplifiers or Schmitt Trigger circuits (to generate TTL signals) in the output path of the DS2301. Factory installed jumpers connect the analog output signals to the 25-pin SUB-D connector. All output signals, isolated ground, system ground, and system +5V are available on the analog customization connector (P7). A 14-bit parallel output port is available at connector (P8). Table 7.3.1 shows the pin-out of the connector P7. Table 7.3.3 shows the pin-out of the parallel output port of P8. Figure 7.3.1 shows the maximum outline of the customization module with the connector locations.

Pin	Signal	Pin	Signal
1	OUT I1	2	OUT 1
3	OUT I2	4	OUT 2
5	OUT I3	6	OUT 3
7	OUT I4	8	OUT 4
9	OUT I5	10	OUT 5
11	OUT I6	12	OUT 6
13	IGND	14	IGND
15	GND	16	GND
17	GND	18	GND
19	VCC	20	VCC

Table 7.3.1. Analog customization module pin-out (P7).

The analog customization module connector is a 20-pin header supporting plug-on customization modules. The analog customization module connector is factory equipped with 10 jumpers feeding the analog I/O-signals to the 25-pin SUB-D I/O connector.

Note: The supply voltage for the components on the customization module must be generated by a DC/DC converter to maintain isolation between the output signals and system ground. The DC/DC converter must be connected to VCC and GND.

Name	Function
OUT 1 - 6	Analog outputs, connected to SUB-D connector
OUT I1 - I6	Analog signals from the output multiplexer
IGND	Isolated GND lines. DC/DC converter output return line and customization module GND.
GND	System GND line. Required for DC/DC converter input return.
VCC	System +5V line. Required for DC/DC converter input power.

Table 7.3.2. Analog customization module signal description.

Pin	Signal
1	VCC
3	GND
5	GND
7	D13
9	D11
11	D9
13	D7
15	D5
17	D3
19	D1

Pin	Signal
2	VCC
4	GND
6	GND
8	D12
10	D10
12	D8
14	D6
16	D4
18	D2
20	D0

Table 7.3.3. Digital customization module pin-out (P8).

The digital customization module connector is a 20-pin ribbon connector supporting plug-on customization modules.

Name	Function
D0 - D13	14-bit parallel port (accessible via the ISR).
GND	System GND line. Required for DC/DC converter input return.
VCC	System +5V line. Required for DC/DC converter input power.

Table 7.3.4. Digital customization module signal description.

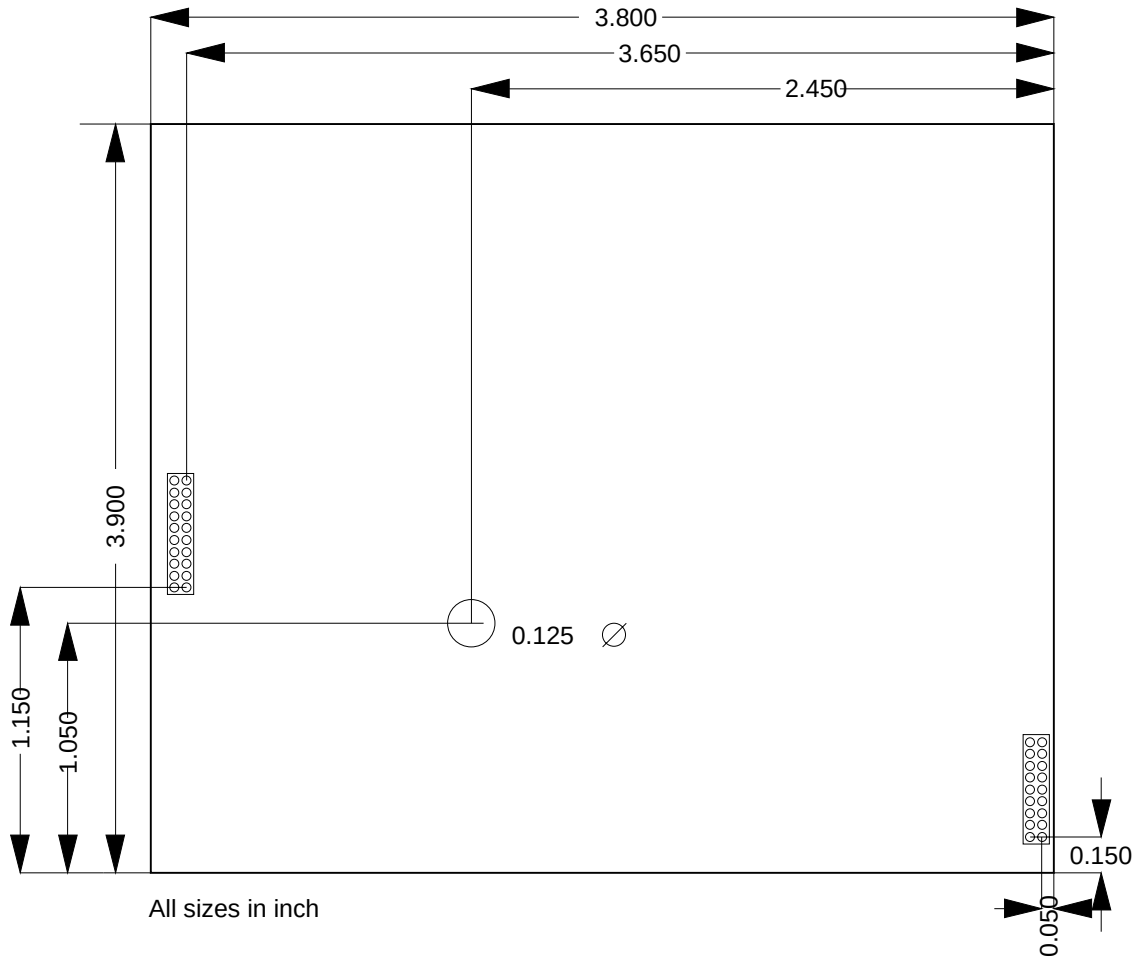


Figure 7.3.1. Customization module outline.

7.4 Calibration connector

The calibration connector (P5) is a 3-pin connector located at the right top of the DS2301 near the I/O connector (refer to figure 2.1.1.). This connector features all signals required to control the digital offset and gain adjust circuits of the DS2301. Each DAC is adjusted during manufacturing of the DS2301 and needs not to be changed under normal operating conditions. This connector is reserved.

7.5 Board programming connector

The board programming connector (P9) is for internal use only. Do not touch this connector when power is applied to the DS2301. This connector is reserved.

8 DS2301 data sheet

Digital section

Configuration	
Six Processors:	Texas Instruments TMS320C31 floating-point DSP. 60 MHz clock rate and 33 ns cycle time. Two 32-bit on-chip timers/event counters. On-chip DMA.
Memory:	4K x 32-bit dual port memory per DSP. 2K x 32-bit on-chip memory per DSP.
Interrupts:	One external interrupt source per DSP. One of eight internal interrupt sources per DSP. One global host interrupt.
Digital outputs:	One open collector output with 680Ω pull-up resistor per DSP. Two totem pole outputs per DSP. (alternatively to the DAC)
Digital input:	One digital input per DSP. TTL compatible input with 47KΩ pull-up resistor.
PHS-bus interface:	Six 32-bit registers. Dual port memory with autoincrement address register.
Host-Interface:	Eight 16-bit registers in the 64K host I/O space. Dual port memory with autoincrement address register.
Physical size:	338 mm x 114 mm x 20 mm Requires one full size length 16-bit AT-slot.
Power supply:	+ 5V ± 5%, 4.0A via PC/AT

Analog section

Configuration	
Number of channels:	Six, isolated
Resolution:	16 bit
Output voltage:	± 10V
Output summing amplifier:	Summing of any combination of the six DAC-channels, software programmable separately for each output.
Isolation voltage:	$50V_{DC}$
Digital DAC interface	
Code:	Two's complement
Data transmission to DACs:	Serial (f_{clock}=15MHz)
Data transmission time	1.26µs
Update rate:	890KHz max.
Analog output (typical values at 25 °C)	
Settling time to ±0.012% of FSR:	1.5 µs typ.
Output current:	± 5 mA max.
Initial offset error:	± 2 mV
Initial gain error:	± 0.5 %
Monotonicity:	14 bit
THD:	-90dB (10KHz)
Offset drift:	± 15ppm of FSR/K
Gain drift:	± 25ppm of FSR/K
Environment	
Board temperature range:	0 .. 70°C

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