DS641 VME Interface

Hardware Reference

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dSPACE

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Important Notice

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About This Reference

Contents

This reference gives information on the DS641 VME Interface. Beginning with the system overview, you will find detailed information on the memory map and the access speed of the IP Module.

In addition, the mounting positions of the connectors and the status LED are shown and their functions described.

Symbols

dSPACE user documentation uses the following symbols:

Symbol	Description
DANGER	Indicates a hazardous situation that, if not avoided, will result in death or serious injury.
WARNING	Indicates a hazardous situation that, if not avoided, could result in death or serious injury.
CAUTION	Indicates a hazardous situation that, if not avoided, could result in minor or moderate injury.
NOTICE	Indicates a hazard that, if not avoided, could result in property damage.
Note	Indicates important information that you should take into account to avoid malfunctions.
Tip	Indicates tips that can make your work easier.
	Indicates a link that refers to a definition in the glossary, which you can find at the end of the document unless stated otherwise.
	Precedes the document title in a link that refers to another document.

Naming conventions

dSPACE user documentation uses the following naming conventions:

%name% Names enclosed in percent signs refer to environment variables for file and path names.

< > Angle brackets contain wildcard characters or placeholders for variable file and path names, etc.

Special folders

Some software products use the following special folders:

Common Program Data folder A standard folder for application-specific configuration data that is used by all users.

```
%PROGRAMDATA%\dSPACE\<InstallationGUID>\<ProductName>
```

or

```
%PROGRAMDATA%\dSPACE\<ProductName>\<VersionNumber>
```

Documents folder A standard folder for user-specific documents.

```
%USERPROFILE%\Documents\dSPACE\<ProductName>\
<VersionNumber>
```

Local Program Data folder A standard folder for application-specific configuration data that is used by the current, non-roaming user.

```
%USERPROFILE%\AppData\Local\dSPACE\<InstallationGUID>\
<ProductName>
```

Accessing dSPACE Help and PDF Files

After you install and decrypt dSPACE software, the documentation for the installed products is available in dSPACE Help and as PDF files.

dSPACE Help (local) You can open your local installation of dSPACE Help:

- On its home page via Windows Start Menu
- On specific content using context-sensitive help via **F1**

dSPACE Help (Web) You can access the Web version of dSPACE Help at www.dspace.com/go/help.

To access the Web version, you must have a *mydSPACE* account.

PDF files You can access PDF files via the icon in dSPACE Help. The PDF opens on the first page.

System Overview

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Introduction to the DS641 VME Interface

Overview

The DS641 VME Interface provides an interface between dSPACE systems and other computer systems, especially VMEbus systems.

Every computer environment which provides an IP Module slot can use the DS641 to connect to a DS4121 ECU Interface Board and therefore to the dSPACE system.

The DS641 VME Interface consists of two modules:

- IP Module
- Transition Module

The connection between the IP Module and the Transition Module is made by a flat ribbon cable.

IP Module

The IP Module is based on the VITA 4-1995 IP Module specification and the dSPACE proprietary ECU Interface standard. This standard is used on the DS4121 ECU Interface Board.

The interface to the dSPACE system is realized by a DS4121 compatible reflective memory. This allows you to connect the DS641 to the DS4121 ECU Interface Board via the Transition Module.

Transition Module

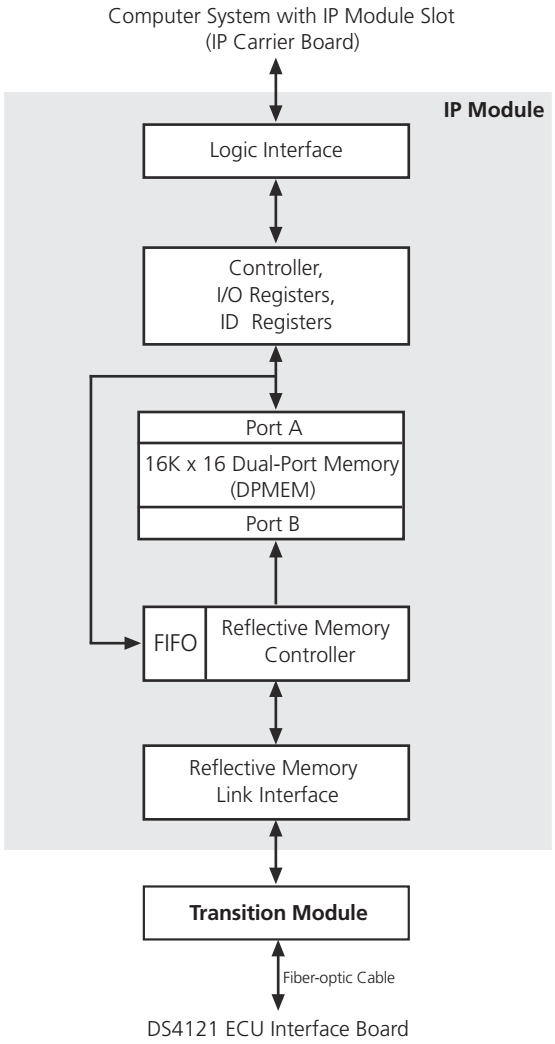
The Transition Module contains an optoelectronic transducer, which converts the electrical signals into optical signals and vice versa. You can make the connection between the Transition Module and the DS4121 with a fiber-optic cable.

The Transition Module is designed to be mounted in a VME chassis.

Block Diagram and Features

Block diagram

The following block diagram shows the functional units of the DS641 VME Interface.



Features

The DS641 VME Interface provides the following features:

- The IP Module complies with:
  - IP Modules Draft Standard VITA 4-1995
  - dSPACE proprietary ECU interface standard
  - Single-size IP Module, Type II
  - VITA 4-1995 compliant ID PROM Data Format I
- 8 MHz and 32 MHz IP clock frequency supported
- 16 K x 16 dual-port memory (DPMEM) for communication with the dSPACE system: Data can be written and read out at the same time.

- Word, low-byte and high-byte access supported
- Supported interrupts:
  - One bidirectional DPMEM interrupt line
  - FIFO memory almost full interrupt (FIFO = First In - First Out)
  - FIFO memory overflow interrupt
  - Connection lost interrupt
- Status LED: checks the optical link between the IP Module and the DS4121 and shows the status

Related Documents

Overview

There is currently no further specific documentation available on the DS641. Below is a list of documents on the *DS4121 ECU Interface Board* that you are also recommended to read when working with the DS641.

Document	Contents
DS4121 Features 🕮	Provides feature-oriented access to the information you need to implement your control models on your real-time hardware.
DS4121 RTI Reference 🕮	Provides concise information on the board's RTI library.
RTI and RTI-MP Implementation Guide 🕮	Gives detailed information and instructions on using Real-Time Interface (RTI and RTI-MP) to implement your real-time models.
RTI and RTI-MP Implementation Reference 🕮	Provides reference information on the various dialogs, files, options, etc. of Real-Time Interface (RTI and RTI-MP) for dSPACE systems. It also describes the blocks introduced by RTI-MP.
DS4121 RTLib Reference 🕮	Provides detailed descriptions of the C functions needed to program RTI-specific Simulink S-functions or implement your real-time models manually via C programs (handcoding).

Memory Map

Objective

From the programmer's perspective, the IP Module contains three sections.

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ID Section

ID Register

Register description

The ID section is used to identify the IP Module in a system. The ID information is compatible with the ID Data Format I (VITA 4-1995 IP Module specification). Format I uses an 8-bit-wide data path and 8-bit manufacturer ID field.

The ID section is read-only.

Address	Value	Name	Access
01H	49H	ASCII "I"	RD
03H	50H	ASCII "P"	RD
05H	41H	ASCII "A"	RD
07H	48H	ASCII "H"	RD
09H	01H	Manufacturer ID	RD
0BH	01H	Model number	RD
0DH	01H	Revision	RD
0FH	00H	Reserved	RD
11H	00H	Driver ID, low byte	RD
13H	00H	Driver ID, high byte	RD
15H	0CH	Byte count	RD
17H	75H	CRC	RD

I/O Section

Purpose

The I/O section describes the registers mapped to the I/O space of the IP Module. This section contains setup, status and interrupt registers.

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Registers in the I/O Section

Purpose of I/O section

The I/O section describes the registers mapped to the I/O space of the IP Module. It contains setup, status and interrupt registers.

Purpose of registers

The registers are used to control and check the correct operation of the IP Module. They are usually required during initialization or exception handling.

Mapping of registers to adresses

Address	Register Name	Access	Power-up Default
01H	Setup Register	RD/WR	00H
03H	Status Register	RD	-
05H	Interrupt Enable Register	RD/WR	00H
07H	Interrupt Control Register	RD/WR	00H
09H	Interrupt Vector Register	RD/WR	0FH

Setup Register 01H

Register description

The Setup Register is used to set different modes, for example the clock frequency. The following table gives a bit definiton of the Setup Register. The labels of the data links (connector pins) according to the IP Module specification are also listed.

Bit	Label of Data Link	Name	Function	Value	Description
0	D0	RST	FIFO mode	0	FIFO is not in reset mode. (Power-up default)
				1	FIFO is in reset mode. Must be active for at least 200 ns.
1	D1	WD	Writing data (See note below)	0	Write enabled. Data is written to the DPMEM and the FIFO. (Power-up default)
				1	Write disabled. Data is written only to the DPMEM. Writes to the FIFO are discarded.
2	D2	RD	Receiving data (See note below)	0	Receive enabled. Data received on the reflective memory link is written to the DPMEM. (Power-up default)
				1	Receive disabled. Data received on the reflective memory link is not written to the DPMEM.
3	D3	32 MHz	IP clock frequency	0	8 MHz operation (Power-up default)
				1	32 MHz operation
4 - 7	D4 - D7	Reserved	–	–	–

Note

If you disable "Wd" and "RD", there will be no data transmission! This setup option is used only for the dSPACE production test.

Related topics

References

Interrupt Control Register 07H....16
Interrupt Enable Register 05H....16
Interrupt Vector Register 09H....18
Status Register 03H....15

Status Register 03H

Register description

The Status Register is used to check the correct operation of the IP Module.

The following table gives bit definitions for the Status Register. The labels of the data links (connector pins) according to the IP Module specification are also listed.

Bit	Label of Data Link	Name	Function	Value	Description
0	D0	TX	Data transmission	0	Data transmission through the reflective memory link is possible.
				1	Data transmission is not possible. Reflective memory link is not valid.
1	D1	LK	Reflective memory link	0	Reflective memory link is valid. Reception of data is possible.
				1	Reflective memory link is not valid. Reception of data is not possible.
2	D2	AF	FIFO almost full flag	0	FIFO is not almost full.
				1	FIFO is almost full. Less than 64 entries free.
3	D3	FF	FIFO full flag	0	FIFO is not full.
				1	FIFO is full.
4	D4	RST	State of the IP reset line	0	Inactive
				1	Active
5 - 7	D5 - D7	Reserved	–	–	–

Related topics

References

Interrupt Control Register 07H....16
Interrupt Enable Register 05H....16
Interrupt Vector Register 09H....18
Setup Register 01H....14

Interrupt Enable Register 05H

Register description

The Interrupt Enable Register is used to enable or disable the interrupt sources.

The following table gives bit definitions for the Interrupt Enable Register. The labels of the data links (connector pins) according to the IP Module specification are also listed.

Bit	Label of Data Link	Name	Function	Value	Description
0	D0	DP	Dual-port memory interrupt	0	Disabled (Power-up default)
				1	Enabled
1	D1	LK	Connection lost interrupt	0	Disabled (Power-up default)
				1	Enabled
2	D2	FO	FIFO overflow interrupt	0	Disabled (Power-up default)
				1	Enabled
3	D3	AF	FIFO almost full interrupt	0	Disabled (Power-up default)
				1	Enabled
4 - 7	D4 - D7	Reserved	–	–	–

Related topics

References

Interrupt Control Register 07H 16
Interrupt Vector Register 09H 18
Setup Register 01H 14
Status Register 03H 15

Interrupt Control Register 07H

Register description

The Interrupt Control Register is used:

- to read the status of the interrupt sources
- to clear the interrupt sources

Note

Before the bit in the Interrupt Control Register is cleared, the interrupt source must be cleared.

The following table gives bit definitions for the Interrupt Control Register. The labels of the data links (connector pins) according to the IP Module specification are also listed.

Bit	Label of Data Link	Name	Value	Function	Write to clear the interrupt
0	D0	DP	1	Dual-port memory interrupt active	Clear dual-port memory interrupts by reading the respective DPMEM location (7FFCH).
1	D1	LK	1	Connection lost interrupt pending	Writing "1" to this bit clears the interrupt latch for the lock lost interrupt.
2	D2	FO	1	FIFO overflow interrupt pending	Writing "1" to this bit clears the interrupt latch for the FIFO overflow interrupt.
3	D3	AF	1	FIFO almost full interrupt pending	Writing "1" to this bit clears the interrupt latch for the FIFO almost full interrupt.
4 - 7	D4 - D7	Reserved	–	–	–

Tip

The power-up default of the Interrupt Control Register is "00H".

Related topics

References

Interrupt Enable Register 05H 16
Interrupt Vector Register 09H 18
Setup Register 01H 14
Status Register 03H 15

Interrupt Vector Register 09H

Register description

The Interrupt Vector Register supplies a user-programmable vector during interrupt acknowledge cycles.

	User-Programmable Vectors						Interrupt Source	
Vector	**V7**	**V6**	**V5**	**V4**	**V3**	**V2**	**S1**	**S0**
Bit	7	6	5	4	3	2	X	X

Tip

The power-up default of the Interrupt Vector Register is "0FH".

The register supplies the upper six bits of the interrupt vector to the CPU during interrupt acknowledge cycles. The lower two bits of the vector encode the interrupt source, so they are not under user control.

S1 ... S0	Interrupt Source
00B	Dual-port memory interrupt
01B	Connection lost interrupt
10B	FIFO overflow interrupt
11B	FIFO almost full interrupt

Related topics

References

Interrupt Control Register 07H....16
Interrupt Enable Register 05H....16
Setup Register 01H....14
Status Register 03H....15

Memory Section

Memory Register

Register description

The memory section consists of a 16 K x 16 dual-port memory (DPMEM) used for communication with the dSPACE system.

This section can be accessed as bytes or 16-bit words. The addresses displayed in the memory maps are 8-bit byte addresses.

Address	Name
0000H – 7FFAH	16382 x 16 bit DPMEM space
7FFCH	1 x 16 bit; interrupt location
7FFEH	1 x 16 bit; reserved for internal use!

Note

The address "7FFEH" of this DPMEM is reserved. It is used only for the dSPACE production test. The user is not allowed to use this address!

Tip

Writes to the address "7FFCH" generate an interrupt on the dSPACE side of the connection.

Related topics

References

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Access Speeds

Objective

In this chapter you will find information about access speeds.

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I/O Access Speed

Possible speeds

The IP Module supports 8 MHz and 32 MHz clock frequencies at I/O accesses. At both clock frequencies, the IP Module accesses the I/O section with two cycles.

The following table shows the maximum possible access speeds.

Parameter	8 MHz	32 MHz
Cycles	2	2
Time	250 ns	50 ns
Speed	4 MW/s	20 MW/s

Related topics

References

Memory Access Speed....22

Memory Access Speed

Possible speeds

The IP Module also supports 8 MHz and 32 MHz clock frequencies at memory accesses. At both clock frequencies, the IP Module automatically inserts one wait state every memory access. The following table shows the maximum possible access speeds to the memory section.

Parameter	8 MHz	32 MHz
Cycles	3	4
Time	375 ns	125 ns
Speed	2.6 MW/s	8 MW/s

Characteristics of FIFO

All data written to the memory space of the IP Module is buffered in a FIFO memory (First In - First Out) before it is transmitted through the reflective memory link. The FIFO depth is 256 words. The speed at which the reflective memory controller reads the data from the FIFO and sends it to the remote side is 5 MW/s.

Note the following characteristics:

- At 8 MHz clock frequency, the maximum access speed to the FIFO is 2.6 MW/s. The device is cleared faster than it is filled. There is no possibility to overrun the FIFO, so it is not necessary to take care of the flags "AF" and "FF" in the Status Register.
- At 32 MHz clock frequency, the maximum access speed to the FIFO is 8 MW/s. Here it is possible to fill the device faster than it is cleared, so it is possible to overrun the FIFO. To avoid such overruns, the FIFO flags in the Status Register must be checked regularly at burst writes. Additionally, the block size of a block write sequence should be limited to 600 words.

Related topics

References

I/O Access Speed 21

Connectors and Status LED

Objective

This section provides an overview of the mounting positions of connectors and the status LED and their functions

Where to go from here

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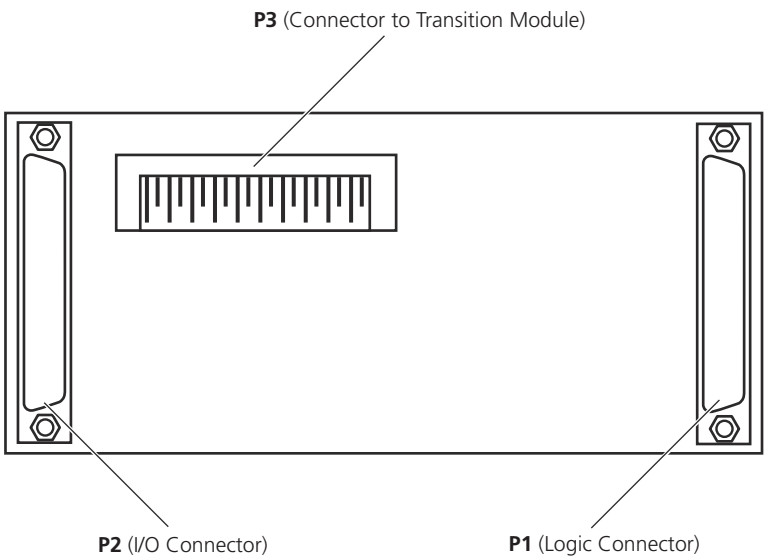
IP Module

Module illustration



Connectors

P1 Logic connector to the IP carrier board (lLogic interface)

P2 I/O connector to the IP carrier board. The I/O interface is not used on the DS641 VME Interface.

P3 Connector for the flat ribbon cable to the Transition Module (reflective memory link interface)

The logic connector (P1) and the I/O connector (P2) are 50-pin AMP plug connectors, part no. 173279-3, as described in the VITA 4-1995 IP Module specification.

Related topics

References

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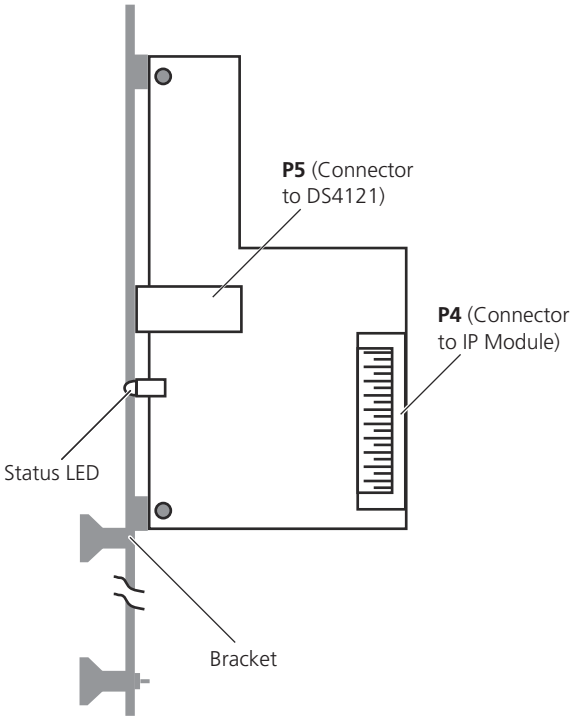
Transition Module

Module illustration

The Transition Module is designed to be mounted in a VME chassis. Therefore it is available with a 6 HE bracket.



Connectors

P4 Connector for the flat ribbon cable to the IP Module (reflective memory link interface)

P5 Connector for the fiber-optic cable to the DS4121

Status LED

The status LED checks the optical link between the IP Module and the DS4121 ECU Interface Board:

- LED is on → The link is valid and data can be transmitted or received.
- LED is off → There is no valid connection between the IP Module and the DS4121.

Related topics

References

IP Module.....23

Data Sheet

DS641 Data Sheet

Technical characteristics

The following table summarizes the technical characteristics of the DS641 VME Interface.

Parameter		Value
Data and memory	Data bus	16 bit, synchronous
	Clock frequency	8 or 32 MHz
	Max. access speed to IP Module	8 MW/s
	Max. data transfer rate to DS4121	5 MW/s
	Memory	16 K × 16 bit dual-port memory (DPMEM)
Power	Power supply	5 V; approx. 0.5 A (via IP carrier board)
	Power consumption	approx. 2.5 W
Physical Size	IP Module	45.72 mm × 99.06 mm
	Bracket of the Transition Module	6 HE (256.8 mm) 4 TE (20.32 mm)
Cable length	Flat ribbon cable from IP Module to Transition Module	0.02 m
	Fiber-optic cable to DS4121	▪ Available: 1 ... 100 m ▪ Standard: 10 m
Environment	Ambient temperature range	0 … 70 °C
	Relative humidity	not condensing

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