DS4003 Digital I/O Board

Features

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dSPACE

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Important Notice

Contents

About This Document

Contents

This document provides feature-oriented access to the information you need to implement the functions of the DS4003.

Symbols

dSPACE user documentation uses the following symbols:

Symbol	Description
DANGER	Indicates a hazardous situation that, if not avoided, will result in death or serious injury.
WARNING	Indicates a hazardous situation that, if not avoided, could result in death or serious injury.
CAUTION	Indicates a hazardous situation that, if not avoided, could result in minor or moderate injury.
NOTICE	Indicates a hazard that, if not avoided, could result in property damage.
Note	Indicates important information that you should take into account to avoid malfunctions.
Tip	Indicates tips that can make your work easier.
	Indicates a link that refers to a definition in the glossary, which you can find at the end of the document unless stated otherwise.
	Precedes the document title in a link that refers to another document.

Naming conventions

dSPACE user documentation uses the following naming conventions:

%name% Names enclosed in percent signs refer to environment variables for file and path names.

< > Angle brackets contain wildcard characters or placeholders for variable file and path names, etc.

Special folders

Some software products use the following special folders:

Common Program Data folder A standard folder for application-specific configuration data that is used by all users.

`%PROGRAMDATA%\dSPACE\<InstallationGUID>\<ProductName>`

or

`%PROGRAMDATA%\dSPACE\<ProductName>\<VersionNumber>`

Documents folder A standard folder for user-specific documents.

`%USERPROFILE%\Documents\dSPACE\<ProductName>\<VersionNumber>`

Local Program Data folder A standard folder for application-specific configuration data that is used by the current, non-roaming user.

`%USERPROFILE%\AppData\Local\dSPACE\<InstallationGUID>\<ProductName>`

Accessing dSPACE Help and PDF Files

After you install and decrypt dSPACE software, the documentation for the installed products is available in dSPACE Help and as PDF files.

dSPACE Help (local) You can open your local installation of dSPACE Help:

- On its home page via Windows Start Menu
- On specific content using context-sensitive help via **F1**

dSPACE Help (Web) You can access the Web version of dSPACE Help at www.dspace.com.

To access the Web version, you must have a *mydSPACE* account.

PDF files You can access PDF files via the icon in dSPACE Help. The PDF opens on the first page.

Introduction to the Features of the DS4003

Introduction

The DS4003 Digital I/O Board provides 96 digital I/O lines grouped into three I/O ports of 32 bits, each with handshake and strobe signals.

Note

In the documentation, the three ports are named port A, port B and port C as well as port 1, port 2 and port 3.

Where to go from here

Information in this section

Information in other sections

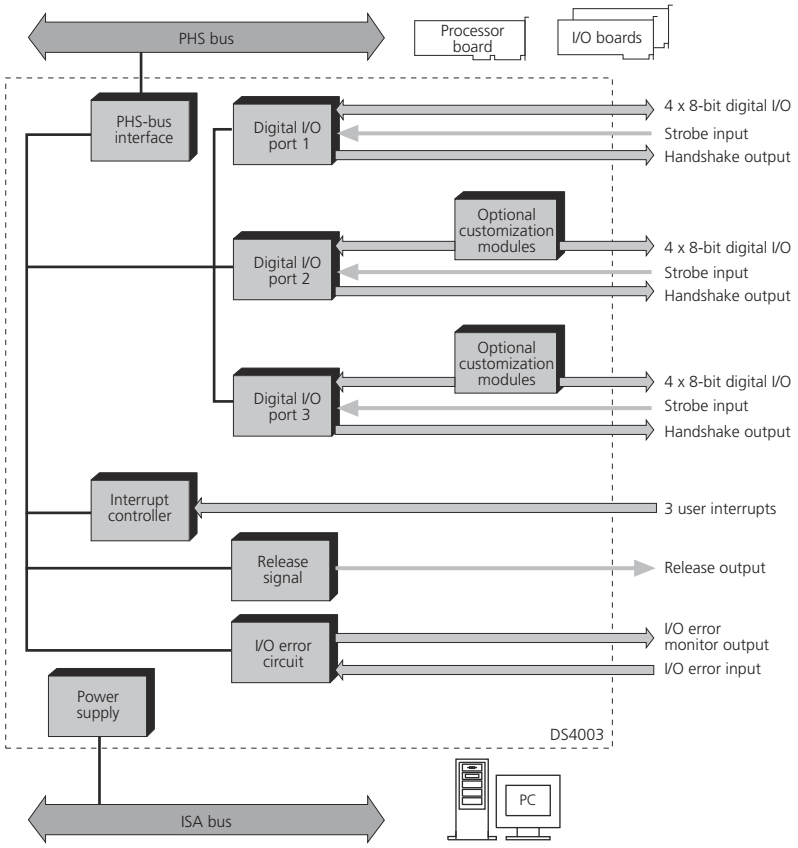
Data Sheets (PHS Bus System Hardware Reference 🕮)
Summarizes the technical specifications of the hardware components.

Signal Connection to External Devices (PHS Bus System Hardware Reference 🕮)
Shows the I/O circuits of the board and gives tips and notes on connecting devices.

DS4003 Architecture

Introduction

The following illustration gives an overview of the functional units and architecture of the DS4003:



Related topics

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Feature Overview

Introduction

The DS4003 provides a digital I/O unit and interrupts inputs.

Digital I/O unit

Provides access to 96 bidirectional TTL lines, refer to Digital I/O Unit on page 11.

Interrupt control

Provides access to 7 interrupt inputs, refer to Interrupts Provided by the DS4003 on page 19.

Related topics

Basics

DS4003 Interfaces

Introduction

The DS4003 has interfaces for connection to a PHS-bus-based system and external devices.

Integration into a PHS-bus-based system

To be used, the DS4003 must be integrated into a PHS-bus-based system. While the DS4003 performs the required I/O tasks, the processor board takes over the calculation of the real-time model. That is, applications using DS4003 I/O features are implemented on the processor board.

Communication between processor board and I/O boards is performed via the peripheral high-speed bus: That is the PHS bus for a connection to a dSPACE processor board.

Partitioning the PHS bus with the DS802 With the DS802 PHS Link Board you can spatially partition the PHS bus by arranging the I/O boards in several expansion boxes.

The DS802 can be used in combination with many types of available dSPACE I/O boards. However, some I/O boards and some functionalities of specific I/O boards are not supported.

The I/O board support depends on the dSPACE software release which you use. For a list of supported I/O boards, refer to DS802 Data Sheet (PHS Bus System Hardware Reference 🕮).

Connection to external devices

There are two different ways to connect external devices to the DS4003. To access the digital I/O unit of the DS4003, connect external devices

- to the 50-pin I/O connectors P1, P2, P3 of the DS4003
- to the optional connector panel CP4003 or the combined connector/LED panel CLP4003

Related topics

Basics

Digital I/O Unit

Introduction

The DS4003 offers a digital I/O unit to handle a great number of digital signals.

Where to go from here

Information in this section

Information in other sections

Basics on the Digital I/O Unit

Introduction

In rapid control prototyping and hardware-in-the-loop simulation, a great number of digital signals have to be handled.

The DS4003 offers a digital I/O unit with the following characteristics:

- 96 bi-directional TTL lines (three 32-bit ports)
- 3 sets of handshake signals
- Direction programmable in 8-bit groups
- TTL voltage range for digital I/O
- Customization module
- Error handling

Direct and strobed input mode

The four 8-bit groups of each of the digital I/O unit's ports can be driven in two input modes:

- In the *direct input mode*, the current status of the I/O pins is returned when the data register is read. No additional strobe signal is necessary in this mode.
- In the *strobed input mode*, new data is latched into the digital I/O unit with a strobe signal. For details, see Strobing Inputs on page 15.

  This mode is not supported by RTI.

The input mode can be selected for each group individually.

Initialization to output direction

If the digital I/O lines are initialized to output direction, the output lines can be initialized to either high or low.

Customizing signals

With the DS4003, you can customize signals. Other signal levels than TTL can be achieved by inserting a customization module that you design for your needs. Customization modules can be connected to ports B and C, not to port A.

For more information on designing your own customization module, refer to Customization Modules (PHS Bus System Hardware Reference 🕮).

Interrupt handling

The DS4003 provides 7 interrupts of different type. These include 3 strobe interrupts, 3 user interrupts and 1 I/O error interrupt. For more information, refer to Interrupts Provided by the DS4003 on page 19.

Power-up state

On power-up of the DS4003, the direction of the digital I/O lines is set to input and the *direct input mode* is selected.

On power-up, the *automatic reset mode* is disabled. By enabling or disabling the *automatic reset mode*, you can determine the board's reaction to I/O errors.

The *error mode* is enabled on power-up. The error mode enables or disables automatic generation of PHS-bus I/O errors.

RTI/RTLib support

You can access the digital I/O unit via DS4003 Blockset and RTLib. Refer to

- RTI: Digital I/O Unit (DS4003 RTI Reference 🕮)
- RTLib: Digital I/O Unit (DS4003 RTLib Reference 🕮)

Execution times

The execution times required by the RTLib functions have been measured. For details on the results and the corresponding measurement setup, refer to Function Execution Times (DS4003 RTLib Reference 🕮).

Connecting external devices

An excerpt from the circuit diagram that shows the I/O circuit and information on the electrical characteristics of the digital I/O unit are available. You can also get information on signal conditioning and the handshake lines. Refer to Signal Connection to External Devices (PHS Bus System Hardware Reference 🕮).

I/O mapping

The following table shows the mapping between the RTI blocks and the RTLib functions and the corresponding pins used by the digital I/O unit:

Related RTI Block	Bit (RTI)	Related RTLib Functions	Bit (RTLib)	Conn. Pin	Pin on CP	Signal
DS4003IN_Bx_Py_Gz; DS4003IN8_Bx_Py_Gz; DS4003OUT_Bx_Py_Gz; DS4003OUT8_Bx_Py_Gz	Port A, gr 0, bit 0 Port B, gr 0, bit 0 Port C, gr 0, bit 0	See Digital I/O Unit (DS4003 RTLib Reference 🕮)	Port A, gr 0, bit 0 Port B, gr 0, bit 0 Port C, gr 0, bit 0	P1 1 P2 1 P3 1	CP1 1 CP2 1 CP3 1	IO0
	Port A, gr 0, bit 1 Port B, gr 0, bit 1 Port C, gr 0, bit 1		Port A, gr 0, bit 1 Port B, gr 0, bit 1 Port C, gr 0, bit 1	P1 34 P2 34 P3 34	CP1 18 CP2 18 CP3 18	IO1
	Port A, gr 0, bit 2 Port B, gr 0, bit 2 Port C, gr 0, bit 2		Port A, gr 0, bit 2 Port B, gr 0, bit 2 Port C, gr 0, bit 2	P1 18 P2 18 P3 18	CP1 2 CP2 2 CP3 2	IO2
	Port A, gr 0, bit 3 Port B, gr 0, bit 3 Port C, gr 0, bit 3		Port A, gr 0, bit 3 Port B, gr 0, bit 3 Port C, gr 0, bit 3	P1 2 P2 2 P3 2	CP1 19 CP2 19 CP3 19	IO3
	Port A, gr 0, bit 4 Port B, gr 0, bit 4 Port C, gr 0, bit 4		Port A, gr 0, bit 4 Port B, gr 0, bit 4 Port C, gr 0, bit 4	P1 35 P2 35 P3 35	CP1 3 CP2 3 CP3 3	IO4
	Port A, gr 0, bit 5 Port B, gr 0, bit 5 Port C, gr 0, bit 5		Port A, gr 0, bit 5 Port B, gr 0, bit 5 Port C, gr 0, bit 5	P1 19 P2 19 P3 19	CP1 20 CP2 20 CP3 20	IO5
	Port A, gr 0, bit 6 Port B, gr 0, bit 6 Port C, gr 0, bit 6		Port A, gr 0, bit 6 Port B, gr 0, bit 6 Port C, gr 0, bit 6	P1 3 P2 3 P3 3	CP1 4 CP2 4 CP3 4	IO6
	Port A, gr 0, bit 7 Port B, gr 0, bit 7		Port A, gr 0, bit 7 Port B, gr 0, bit 7	P1 36 P2 36	CP1 21 CP2 21	IO7

Related RTI Block	Bit (RTI)	Related RTLib Functions	Bit (RTLib)	Conn. Pin	Pin on CP	Signal
	Port C, gr 0, bit 7		Port C, gr 0, bit 7	P3 36	CP3 21	
	Port A, gr 1, bit 8 Port B, gr 1, bit 8 Port C, gr 1, bit 8		Port A, gr 1, bit 8 Port B, gr 1, bit 8 Port C, gr 1, bit 8	P1 20 P2 20 P3 20	CP1 5 CP2 5 CP3 5	IO8
	Port A, gr 1, bit 9 Port B, gr 1, bit 9 Port C, gr 1, bit 9		Port A, gr 1, bit 9 Port B, gr 1, bit 9 Port C, gr 1, bit 9	P1 4 P2 4 P3 4	CP1 22 CP2 22 CP3 22	IO9
	Port A, gr 1, bit 10 Port B, gr 1, bit 10 Port C, gr 1, bit 10		Port A, gr 1, bit 10 Port B, gr 1, bit 10 Port C, gr 1, bit 10	P1 37 P2 37 P3 37	CP1 6 CP2 6 CP3 6	IO10
	Port A, gr 1, bit 11 Port B, gr 1, bit 11 Port C, gr 1, bit 11		Port A, gr 1, bit 11 Port B, gr 1, bit 11 Port C, gr 1, bit 11	P1 21 P2 21 P3 21	CP1 23 CP2 23 CP3 23	IO11
	Port A, gr 1, bit 12 Port B, gr 1, bit 12 Port C, gr 1, bit 12		Port A, gr 1, bit 12 Port B, gr 1, bit 12 Port C, gr 1, bit 12	P1 5 P2 5 P3 5	CP1 7 CP2 7 CP3 7	IO12
	Port A, gr 1, bit 13 Port B, gr 1, bit 13 Port C, gr 1, bit 13		Port A, gr 1, bit 13 Port B, gr 1, bit 13 Port C, gr 1, bit 13	P1 38 P2 38 P3 38	CP1 24 CP2 24 CP3 24	IO13
	Port A, gr 1, bit 14 Port B, gr 1, bit 14 Port C, gr 1, bit 14		Port A, gr 1, bit 14 Port B, gr 1, bit 14 Port C, gr 1, bit 14	P1 22 P2 22 P3 22	CP1 8 CP2 8 CP3 8	IO14
	Port A, gr 1, bit 15 Port B, gr 1, bit 15 Port C, gr 1, bit 15		Port A, gr 1, bit 15 Port B, gr 1, bit 15 Port C, gr 1, bit 15	P1 6 P2 6 P3 6	CP1 25 CP2 25 CP3 25	IO15
	Port A, gr 2, bit 16 Port B, gr 2, bit 16 Port C, gr 2, bit 16		Port A, gr 2, bit 16 Port B, gr 2, bit 16 Port C, gr 2, bit 16	P1 39 P2 39 P3 39	CP1 9 CP2 9 CP3 9	IO16
	Port A, gr 2, bit 17 Port B, gr 2, bit 17 Port C, gr 2, bit 17		Port A, gr 2, bit 17 Port B, gr 2, bit 17 Port C, gr 2, bit 17	P1 23 P2 23 P3 23	CP1 26 CP2 26 CP3 26	IO17
	Port A, gr 2, bit 18 Port B, gr 2, bit 18 Port C, gr 2, bit 18		Port A, gr 2, bit 18 Port B, gr 2, bit 18 Port C, gr 2, bit 18	P1 7 P2 7 P3 7	CP1 10 CP2 10 CP3 10	IO18
	Port A, gr 2, bit 19 Port B, gr 2, bit 19 Port C, gr 2, bit 19		Port A, gr 2, bit 19 Port B, gr 2, bit 19 Port C, gr 2, bit 19	P1 40 P2 40 P3 40	CP1 27 CP2 27 CP3 27	IO19
	Port A, gr 2, bit 20 Port B, gr 2, bit 20 Port C, gr 2, bit 20		Port A, gr 2, bit 20 Port B, gr 2, bit 20 Port C, gr 2, bit 20	P1 24 P2 24 P3 24	CP1 11 CP2 11 CP3 11	IO20
	Port A, gr 2, bit 21 Port B, gr 2, bit 21 Port C, gr 2, bit 21		Port A, gr 2, bit 21 Port B, gr 2, bit 21 Port C, gr 2, bit 21	P1 8 P2 8 P3 8	CP1 28 CP2 28 CP3 28	IO21
	Port A, gr 2, bit 22 Port B, gr 2, bit 22 Port C, gr 2, bit 22		Port A, gr 2, bit 22 Port B, gr 2, bit 22 Port C, gr 2, bit 22	P1 41 P2 41 P3 41	CP1 12 CP2 12 CP3 12	IO22
	Port A, gr 2, bit 23		Port A, gr 2, bit 23	P1 25	CP1 29	IO23

Related RTI Block	Bit (RTI)	Related RTLib Functions	Bit (RTLib)	Conn. Pin	Pin on CP	Signal
	Port B, gr 2, bit 23 Port C, gr 2, bit 23		Port B, gr 2, bit 23 Port C, gr 2, bit 23	P2 25 P3 25	CP2 29 CP3 29	
	Port A, gr 3, bit 24 Port B, gr 3, bit 24 Port C, gr 3, bit 24		Port A, gr 3, bit 24 Port B, gr 3, bit 24 Port C, gr 3, bit 24	P1 9 P2 9 P3 9	CP1 13 CP2 13 CP3 13	IO24
	Port A, gr 3, bit 25 Port B, gr 3, bit 25 Port C, gr 3, bit 25		Port A, gr 3, bit 25 Port B, gr 3, bit 25 Port C, gr 3, bit 25	P1 42 P2 42 P3 42	CP1 30 CP2 30 CP3 30	IO25
	Port A, gr 3, bit 26 Port B, gr 3, bit 26 Port C, gr 3, bit 26		Port A, gr 3, bit 26 Port B, gr 3, bit 26 Port C, gr 3, bit 26	P1 26 P2 26 P3 26	CP1 14 CP2 14 CP3 14	IO26
	Port A, gr 3, bit 27 Port B, gr 3, bit 27 Port C, gr 3, bit 27		Port A, gr 3, bit 27 Port B, gr 3, bit 27 Port C, gr 3, bit 27	P1 10 P2 10 P3 10	CP1 31 CP2 31 CP3 31	IO27
	Port A, gr 3, bit 28 Port B, gr 3, bit 28 Port C, gr 3, bit 28		Port A, gr 3, bit 28 Port B, gr 3, bit 28 Port C, gr 3, bit 28	P1 43 P2 43 P3 43	CP1 15 CP2 15 CP3 15	IO28
	Port A, gr 3, bit 29 Port B, gr 3, bit 29 Port C, gr 3, bit 29		Port A, gr 3, bit 29 Port B, gr 3, bit 29 Port C, gr 3, bit 29	P1 27 P2 27 P3 27	CP1 32 CP2 32 CP3 32	IO29
	Port A, gr 3, bit 30 Port B, gr 3, bit 30 Port C, gr 3, bit 30		Port A, gr 3, bit 30 Port B, gr 3, bit 30 Port C, gr 3, bit 30	P1 11 P2 11 P3 11	CP1 16 CP2 16 CP3 16	IO30
	Port A, gr 3, bit 31 Port B, gr 3, bit 31 Port C, gr 3, bit 31		Port A, gr 3, bit 31 Port B, gr 3, bit 31 Port C, gr 3, bit 31	P1 44 P2 44 P3 44	CP1 33 CP2 33 CP3 33	IO31

Related topics

References

DS4003IN_Bx_Py_Gz (DS4003 RTI Reference 🕮)
DS4003IN8_Bx_Py_Gz (DS4003 RTI Reference 🕮)
DS4003OUT_Bx_Py_Gz (DS4003 RTI Reference 🕮)
DS4003OUT8_Bx_Py_Gz (DS4003 RTI Reference 🕮)

Strobing Inputs

Introduction

The four 8-bit groups (bits 0 … 7, 8 … 15, 16 … 23, 24 … 31) of each of the three digital I/O ports can be used in the *strobed input mode*. In this case, new data is latched into the digital I/O unit using a strobe signal. To use this mode, the PSTB line must be connected.

The *strobed input mode* is not supported by RTI.

PSTB signal

The strobe signal must be connected to the PSTB line. Input data is latched with the rising edge of the strobe signal.

Before the rising edge, the strobe signal must be low for at least 100 ns. After the rising edge, the strobe signal must be high for at least 50 ns.

Tip

The PSTB input can also be used as an external interrupt source. PSTB issues an interrupt to the processor board. Refer to Strobe Interrupts on page 21.

I/O mapping

The following table shows the mapping between the RTLib functions and the corresponding pins used by the PSTB line:

Related RTLib Functions	Ch/Bit (RTLib)	Conn. Pin	Pin on CP	Signal
`ds4003_pio_init`	Port A Port B Port C	P1 28 P2 28 P3 28	CP1 35 CP2 35 CP3 35	$\overline{\text{PSTB}}$

Related topics

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References

Digital I/O Unit (DS4003 RTLib Reference 🕮)
ds4003_pio_init (DS4003 RTLib Reference 🕮)

Handshaking with External Devices

Introduction

For each of the three digital I/O ports, the DS4003 provides two output signals that acknowledge that data was written to or read from the digital I/O port successfully.

Handshaking is not supported by RTI.

PRDY handshake line

When data was written to the digital I/O unit, this is indicated by a 100 ns low pulse at the PRDY handshake line. The duration of the pulse cannot be changed.

PACK handshake line

When data was read from the digital I/O unit, this is indicated by a 100 ns low pulse at the PACK handshake line. The duration of the pulse cannot be changed.

Output pins for the handshake lines

The following table shows the pins used by the handshake lines:

Port	Conn. Pin	Pin on CP	Signal
Port A	P1 45	CP1 37	$\overline{\text{PACK}}$
Port B	P2 45	CP2 37	
Port C	P3 45	CP3 37	
Port A	P1 12	CP1 39	$\overline{\text{PRDY}}$
Port B	P2 12	CP2 39	
Port C	P3 12	CP3 39	

Related topics

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Error Handling

Introduction

The DS4003 provides an I/O error logic that has the following features:

- I/O error monitor line (OIOERR) at each port to reflect the current state of the PHS-bus error line
- I/O error input line (PIOERR) at each port to notify the DS4003 about an I/O error of devices connected to the DS4003; the PHS-bus error line is activated
- RELEASE signal to indicate the initialization status of the DS4003 and therefore signal proper initialization of the DS4003 to the external devices connected to it

Setting the input mode following I/O error

If the automatic reset mode is enabled the DS4003 sets all bit groups of all ports to non-strobed input mode after an I/O error occurred.

The automatic reset mode can be enabled or disabled via the `ds4003_set_reset_mode` function.

The automatic reset mode is not supported by RTI.

The automatic reset mode is disabled by default.

Activating the PHS-bus I/O error line

If the error mode is enabled the PHS-bus I/O error line is activated automatically on occurrence of an error notification at one of the three ports.

The error mode can be enabled or disabled via the `ds4003_set_error_mode` function.

With RTI, you cannot disable the error mode.

The error mode is enabled by default to ensure compatibility to the DS4001 board.

Interrupt on I/O error

The DS4003 provides an I/O error interrupt. The I/O error logic generates an interrupt if the input for one of the I/O error input lines (PIOERR) is set. For more information, refer to I/O Error Interrupt on page 23.

I/O mapping

The following table shows the mapping between the RTLib functions and the corresponding pins used for error handling:

Related RTLib Functions	Port	Conn. Pin	Pin on CP	Signal
`ds4003_set_error_mode` and `ds4003_set_reset_mode`.	Port A Port B Port C	P1 31 P2 31 P3 31	CP1 46 CP2 46 CP3 46	$\overline{\text{OIOERR}}$
	Port A Port B Port C	P1 29 P2 29 P3 29	CP1 41 CP2 41 CP3 41	$\overline{\text{PIOERR}}$
	Port A Port B Port C	P1 33 P2 33 P3 33	CP1 48 CP2 48 CP3 48	RELEASE

Related topics

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References

Digital I/O Unit (DS4003 RTLib Reference 🕮)
Interrupts (DS4003 RTI Reference 🕮)

Interrupts Provided by the DS4003

Introduction

The DS4003 provides access to seven hardware interrupts.

Where to go from here

Information in this section

Basics on Interrupts of the DS4003

Interrupts

The DS4003 provides access to seven hardware interrupts:

Interrupt Type	Description
PIO strobe: Port A PIO strobe: Port B PIO strobe: Port C	Strobe interrupt. The PSTB input of the respective port can be used as an additional external interrupt source.
User interrupt: Port A User interrupt: Port B User interrupt: Port C	Interrupt defined by the user. The user interrupts are triggered by an external signal and can be used freely.
I/O error	An I/O error input line (PIOERR) can generate an interrupt.

Transparent and latched interrupt mode

The DS4003 provides two interrupt modes:

- In the transparent interrupt mode the interrupt signal is directly used as the input signal of the interrupt controller.
- In the latched interrupt mode the interrupt signal is latched to ensure proper interrupt operation in case of short interrupt pulses.

To set the interrupt mode, use the `ds4003_set_int_mode` function.

The latched interrupt mode is not supported by RTI.

The transparent interrupt mode is set by default.

Interrupt processing

Via the interrupt lines of the PHS bus, interrupts from the DS4003 are sent to the interrupt controller of the connected dSPACE processor board. Using RTI, the interrupts of the DS4003 can therefore be used to implement interrupt-driven tasks. Refer to Tasks Driven by Interrupt Blocks (RTI and RTI-MP Implementation Guide 🕮).

Related topics

References

ds4003_int_pending (DS4003 RTLib Reference 🕮)
ds4003_set_int_mode (DS4003 RTLib Reference 🕮)
Interrupts (DS4003 RTI Reference 🕮)

Strobe Interrupts

Introduction

The DS4003 provides three strobe interrupts. The PSTB input of the respective port can be used as an additional external interrupt source.

Basics

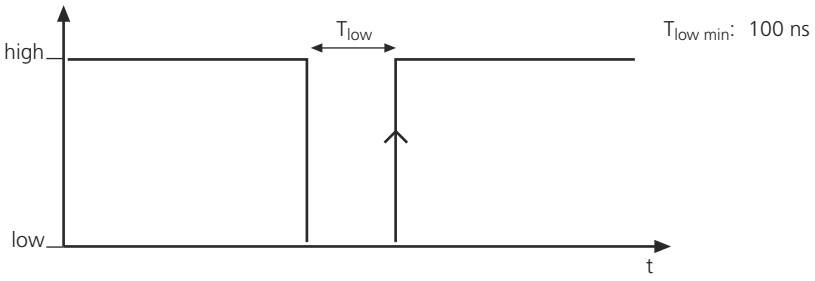
The strobe interrupts are independent of the strobed input mode or the direct input mode. For more information on the input modes, refer to Direct and strobed input mode on page 12.

Timing requirements

Strobe interrupts are triggered at the rising edge of the corresponding external signal.

The interrupt signal should be high all the time, and it should be set to low for approximately 100 ns before the interrupt, so that the interrupt is triggered by the rising edge of the signal.

The following illustration shows the timing of the interrupt:



I/O mapping

The following table shows the mapping between the RTLib functions and the corresponding pins used by the PSTB line:

Related RTI Block	Int (RTI)	Related RTLib Functions	Int (RTLib)	Conn. Pin	Pin on CP	Signal
DS4003_HWINT_Bx_Iy	Port A Port B Port C	See ds4003_pio_init (DS4003 RTLib Reference 🕮) and PHS-Bus Interrupt Handling	Port A Port B Port C	P1 28 P2 28 P3 28	CP1 35 CP2 35 CP3 35	$\overline{PSTB}$

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References

DS4003_HWINT_Bx_Iy (DS4003 RTI Reference 🕮)

User Interrupts

Introduction

The DS4003 provides three user interrupts that you can use as trigger sources in a real-time application. The user interrupt sources have to be connected externally to the DS4003.

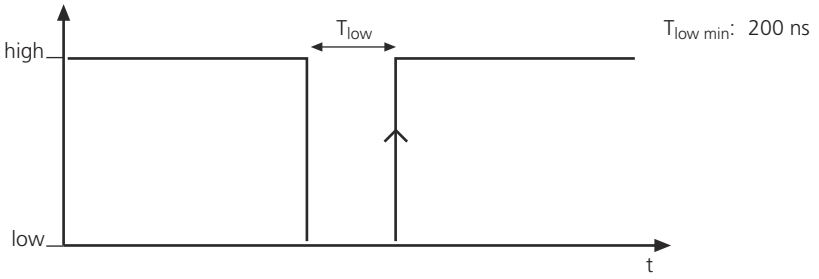
The PSTB input of the respective port can be used as an additional external interrupt source for the user interrupts, but only if the direct input mode is used.

Timing requirements

User interrupts are triggered at the rising edge of the corresponding external signal.

The interrupt signal should be high all the time, and it should be set to low for approximately 200 ns before the interrupt, so that the interrupt is triggered by the rising edge of the signal.

The following illustration shows the timing of the interrupt:



RTI/RTLib support

For information on how to access the user interrupt, refer to DS4003_HWINT_Bx_Iy (DS4003 RTI Reference 🕮).

I/O mapping

The following table shows the mapping between the RTI block and the RTLib functions and the corresponding pins used by the user interrupt:

Related RTI Block	Int (RTI)	Related RTLib Functions	Int (RTLib)	Conn. Pin	Pin on CP	Signal
DS4003_HWINT_Bx_Iy	Port A Port B Port C	See PHS-Bus Interrupt Handling (DS1006 RTLib Reference 🕮) (DS1006) orPHS-Bus Interrupt Handling (DS1007 RTLib Reference 🕮) (DS1007)	Port A Port B Port C	P1 46 P2 46 P3 46	CP1 43 CP2 43 CP3 43	USRINT

Related topics

References

DS4003_HWINT_Bx_Iy (DS4003 RTI Reference 🕮)

I/O Error Interrupt

Introduction

The DS4003 provides an I/O error input line (PIOERR) at each port to notify the DS4003 about an I/O error of devices connected to the DS4003. If such an error notification occurs an interrupt can be generated on the processor board.

An I/O error request does not only generate an interrupt on the processor board. It can also influence other dSPACE I/O boards via the I/O error line of the PHS bus, which may result in zeroed outputs of D/A conversion boards, for example.

Automatic generation of PHS-bus I/O errors is enabled or disabled via the `ds4003_set_error_mode` function.

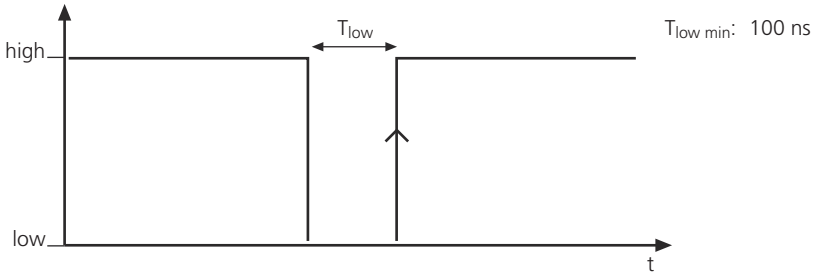
The error mode is enabled by default to ensure compatibility to the DS4001.

Timing requirements

I/O error interrupts are triggered at the rising edge of the corresponding external signal.

The interrupt signal should be high all the time, and it should be set to low for approximately 100 ns before the interrupt, so that the interrupt is triggered by the rising edge of the signal.

The following illustration shows the timing of the interrupt:



RTI/RTLib support

You can access the I/O error interrupt via DS4003 Blockset and RTLib. For details, refer to Interrupts (DS4003 RTI Reference 🕮).

I/O mapping

The following table shows the mapping between the RTLib functions and the corresponding pins used for error handling:

Related RTI Block	Int (RTI)	Related RTLib Functions	Int (RTLib)	Conn. Pin	Pin on CP	Signal
DS4003_HWINT_Bx_Iy	Port A Port B Port C	See PHS-Bus Interrupt Handling (DS1006 RTLib Reference 🕮) (DS1006) or PHS-Bus Interrupt Handling (DS1007 RTLib Reference 🕮) (DS1007)	Port A Port B Port C	P1 29 P2 29 P3 29	CP1 41 CP2 41 CP3 41	$\overline{\text{PIOERR}}$

Related topics

References

DS4003_HWINT_Bx_Iy (DS4003 RTI Reference 🕮)
ds4003_set_error_mode (DS4003 RTLib Reference 🕮)

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