DS1104 R&D Controller Board

RTI Reference

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dSPACE

How to Contact dSPACE

Mail:	dSPACE GmbH Rathenaustraße 26 33102 Paderborn Germany
Tel.:	+49 5251 1638-0
Fax:	+49 5251 16198-0
E-mail:	info@dspace.de
Web:	http://www.dspace.com

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  Tel.: +49 5251 1638-941 or e-mail: support@dspace.de

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Software Updates and Patches

dSPACE strongly recommends that you download and install the most recent patches for your current dSPACE installation. Visit http://www.dspace.com/go/patches for software updates and patches.

Important Notice

Contents

About This Reference

Content

This document provides you with detailed information about Real-Time Interface (RTI) of your DS1104 R&D Controller Board.

Symbols

dSPACE user documentation uses the following symbols:

Symbol	Description
DANGER	Indicates a hazardous situation that, if not avoided, will result in death or serious injury.
WARNING	Indicates a hazardous situation that, if not avoided, could result in death or serious injury.
CAUTION	Indicates a hazardous situation that, if not avoided, could result in minor or moderate injury.
NOTICE	Indicates a hazard that, if not avoided, could result in property damage.
Note	Indicates important information that you should take into account to avoid malfunctions.
Tip	Indicates tips that can make your work easier.
	Indicates a link that refers to a definition in the glossary, which you can find at the end of the document unless stated otherwise.
	Precedes the document title in a link that refers to another document.

Naming conventions

dSPACE user documentation uses the following naming conventions:

%name% Names enclosed in percent signs refer to environment variables for file and path names.

< > Angle brackets contain wildcard characters or placeholders for variable file and path names, etc.

Examples:

- Where you find terms such as `rti<XXXX>` replace them by the RTI platform support you are using, for example, `rti1007`.
- Where you find terms such as `<model>` or `<submodel>` in this document, replace them by the actual name of your model or submodel. For example, if the name of your Simulink model is `smd_1007_sl.slx` and you are asked to edit the `<model>_usr.c` file, you actually have to edit the `smd_1007_sl_usr.c` file.

RTI block name conventions All I/O blocks have default names based on dSPACE's board naming conventions:

- Most RTI block names start with the board name.
- A short description of functionality is added.
- Most RTI block names also have a suffix.

Suffix	Meaning
B	Board number (for PHS-bus-based systems)
M	Module number (for MicroAutoBox II)
C	Channel number
G	Group number
CON	Converter number
BL	Block number
P	Port number
I	Interrupt number

A suffix is followed by the appropriate number. For example, DS2201IN_B2_C14 represents a digital input block located on a DS2201 board. The suffix indicates board number 2 and channel number 14 of the block. For more general block naming, the numbers are replaced by variables (for example, DS2201IN_Bx_Cy).

Special folders

Some software products use the following special folders:

Common Program Data folder A standard folder for application-specific configuration data that is used by all users.

`%PROGRAMDATA%\dSPACE\<InstallationGUID>\<ProductName>`

or

`%PROGRAMDATA%\dSPACE\<ProductName>\<VersionNumber>`

Documents folder A standard folder for user-specific documents.

`%USERPROFILE%\Documents\dSPACE\<ProductName>\<VersionNumber>`

Local Program Data folder A standard folder for application-specific configuration data that is used by the current, non-roaming user.

`%USERPROFILE%\AppData\Local\dSPACE\<InstallationGUID>\<ProductName>`

Accessing dSPACE Help and PDF Files

After you install and decrypt dSPACE software, the documentation for the installed products is available in dSPACE Help and as PDF files.

dSPACE Help (local) You can open your local installation of dSPACE Help:

- On its home page via Windows Start Menu
- On specific content using context-sensitive help via **F1**

dSPACE Help (Web) You can access the Web version of dSPACE Help at www.dspace.com.

To access the Web version, you must have a *mydSPACE* account.

PDF files You can access PDF files via the icon in dSPACE Help. The PDF opens on the first page.

General Information on the RTI Blockset of the DS1104

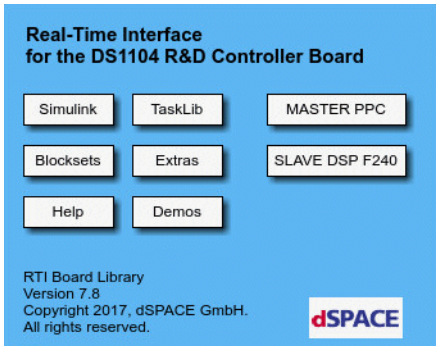
Overview of RTI1104

Introduction

The Real-Time Interface (RTI) board library for the DS1104 R&D Controller Board – the rtilib1104 – provides the RTI blocks that implement the I/O capabilities of the DS1104 in Simulink models. These RTI blocks are designed to specify the hardware setup for real-time applications. Furthermore, the rtilib1104 provides additional RTI blocks, demo models, and useful information.

RTI blockset

When entering **`rti1104`** in the MATLAB Command Window, the RTI board library for the DS1104 is displayed.



The following rtilib1104 components are available in the **Library: rtilib1104** window:

Simulink Calls the standard Simulink Block Library.

Blocksets Includes optional RTI blocks for the DS1104.

Help Displays this reference information.

TaskLib Offers RTI blocks for modeling interrupts in Simulink.

For more information, refer to TaskLib Block Reference (RTI and RTI-MP Implementation Reference 🕮).

EXTRAS Offers RTI blocks for special purposes – for example the service code for ControlDesk.

For more information, refer to Extras Block Reference (RTI and RTI-MP Implementation Reference 🕮).

DEMOS Shows example models.

Master PPC Is a sub-library comprising the RTI blocks for the I/O units served by the Power PC processor.

For more information, refer to Overview of the Master PPC Blockset on page 14.

Slave DSP F240 Is a sub-library comprising the RTI blocks for the I/O units served by the Texas Instruments TMS320F240 DSP.

For more information, refer to Overview of the Slave DSP Blockset on page 72.

Demo model

For Simulink models, that show how to use the RTI blocks, refer to the RTI demo library of the DS1104 board.

RTI Blockset for the Master PPC

Where to go from here

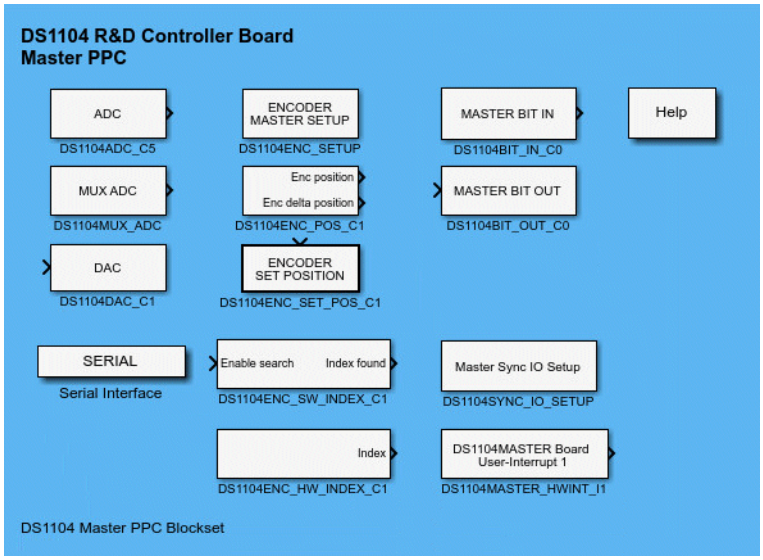
Information in this section

Overview of the Master PPC Blockset

Overview of the Master PPC Blockset

Blockset overview

After you click the Master PPC button in the Library: rtilib1104 window, the Library: rtilib1104/DS1104 MASTER PPC window is displayed. It contains the I/O blocks served by the Power PC processor.



The following I/O units can be accessed by the RTI blockset for the master PPC of the DS1104:

- ADC Unit on page 15
- DAC Unit on page 19
- Bit I/O Unit on page 23
- Incremental Encoder Interface on page 28
- Serial Interface on page 43
- Interrupts on page 63
- Synchronizing I/O Unit on page 66

ADC Unit

Introduction

The master PPC library contains several blocks for programming the A/D converters.

Demo model

For a demo model using the ADC unit, refer to the model ADC, Mux ADC and DAC units, which you can find in the processor board's demo library.

Where to go from here

Information in this section

Information in other sections

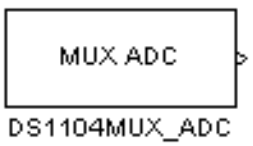
DS1104MUX_ADC

Where to go from here

Information in this section

Block Description (DS1104MUX_ADC)

Block



Purpose

To read from up to 4 channels of the A/D converter.

Description

The width of the block output vector (comprising the selected channels assigned to one converter) matches the number of the selected channels.

I/O mapping

For information on the I/O mapping, refer to ADC Unit (DS1104 Features 🕮).

I/O characteristics

Scaling between the analog input voltage and the output of the block:

Input Voltage Range	Simulink Output
–10 V ... +10 V	–1 ... +1 (double)

Dialog pages

The dialog settings can be specified on the following page:

- Unit Page (DS1104MUX_ADC) on page 16

Related RTLib functions

This RTI block is implemented using the following RTLib functions. The DS1104 RTLib Reference contains descriptions of these functions.

- ds1104_adc_start
- ds1104_adc_mux
- ds1104_adc_read_mux
- ds1104_adc_read_conv
- ds1104_adc_trigger_setup

Unit Page (DS1104MUX_ADC)

Purpose

To specify the channels to be multiplexed.

Dialog settings

Channel selection Lets you select a set of up to 4 channels.

Related topics

References

Block Description (DS1104MUX_ADC) 15
DS1104MUX_ADC 15

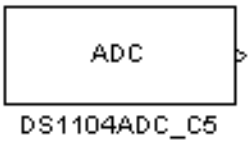
DS1104ADC_Cx

Where to go from here

Information in this section

Block Description (DS1104ADC_Cx)

Block



Purpose

To read from a single channel of one of 4 parallel A/D converter channels.

I/O mapping

For information on the I/O mapping, refer to ADC Unit (DS1104 Features 🕮).

I/O characteristics

Scaling between the analog input voltage and the output of the block:

Input Voltage Range	Simulink Output
–10 V ... +10 V	–1 ... +1 (double)

Dialog pages

The dialog settings can be specified on the following page:

- Unit Page (DS1104ADC_Cx) on page 18

Related RTLib functions

This RTI block is implemented using the following RTLib functions. The DS1104 RTLib Reference contains descriptions of these functions.

- ds1104_adc_start
- ds1104_adc_read_conv
- ds1104_adc_trigger_setup

Unit Page (DS1104ADC_Cx)

Purpose

To specify the channel to be read.

Dialog settings

Channel number Lets you select a single channel within the range 5 … 8.

Related topics

References

DAC Unit

Introduction

The master PPC library contains one block for programming the D/A converters.

Demo model

For a demo model using the DAC unit, refer to the model ADC, Mux ADC and DAC units, which you can find in the processor board's demo library.

Where to go from here

Information in this section

DS1104DAC_Cx..... 19

Information in other sections

DS1104SYNC_IO_SETUP..... 66
To setup the synchronously triggering of master PPC's analog I/O units.

DS1104DAC_Cx

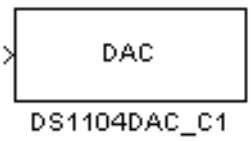
Where to go from here

Information in this section

Block Description (DS1104DAC_Cx)..... 19
Unit Page (DS1104DAC_Cx)..... 20
Initialization Page (DS1104DAC_Cx)..... 21
Termination Page (DS1104DAC_Cx)..... 21

Block Description (DS1104DAC_Cx)

Block



Purpose

To write to one of the 8 parallel D/A converter channels.

I/O mapping

For information on the I/O mapping, refer to DAC Unit (DS1104 Features 🕮).

I/O characteristics

- Scaling between the analog output voltage and the input of the block:

Simulink Input	Output Voltage Range
–1 ... +1 (double)	–10 V ... +10 V

- The block provides its outputs in:
  - Transparent mode, that is the channel is converted and output immediately.
  - Latched mode, that is the channel is converted after synchronous triggering.

Note

The mode used is relevant for all D/A converter channels.

Dialog pages

The dialog settings can be specified on the following pages:

- Unit Page (DS1104DAC_Cx) on page 20
- Initialization Page (DS1104DAC_Cx) on page 21
- Termination Page (DS1104DAC_Cx) on page 21

Related RTLib functions

This RTI block is implemented using the following RTLib functions. The DS1104 RTLib Reference contains descriptions of these functions.

- ds1104_dac_init
- ds1104_dac_trigger_setup
- ds1104_dac_write

Unit Page (DS1104DAC_Cx)

Purpose

To specify a channel for the D/A conversion.

Dialog settings

Channel number Lets you select a single channel within the range 1 … 8.

Related topics

References

Initialization Page (DS1104DAC_Cx)

Purpose

To specify the initial output voltage.

Description

- During the model initialization phase, an initial output voltage value is written to each D/A channel. This is especially useful if a channel is used within a triggered or enabled subsystem that is not executed right from the start of the simulation.
- With the initialization value, the channel has a defined output during this simulation phase.

Dialog settings

Initialization value Lets you specify the initial output voltage at the start of the simulation. The value must remain in the output voltage range ±10 V.

Related topics

References

Termination Page (DS1104DAC_Cx)

Purpose

To specify the output voltage at termination.

Description

When the simulation terminates, the channel holds the last output value by default. You can specify a user-defined output value on termination, and use these settings to drive your external hardware into a safe final condition.

The specified termination values of I/O channels are set when the simulation executes its termination function by setting the simState variable to STOP. If the

real-time process is stopped by using ControlDesk's Stop RTP command, the processor resets immediately without executing termination functions. The current values of the I/O channels are kept and the specified termination values are not set.

Dialog settings

Output on termination Lets you either keep the current output voltage when the simulation terminates, or set the output to a specified value. The value must remain in the output voltage range ±10 V.

Related topics

References

Block Description (DS1104DAC_Cx)..... 19
Initialization Page (DS1104DAC_Cx)..... 21
Unit Page (DS1104DAC_Cx)..... 20

Bit I/O Unit

Introduction

The master PPC library contains several blocks for programming the digital I/O unit.

Tip

You can also use the DSP built-in bit I/O unit. For detailed description, refer to Slave DSP Bit I/O Unit on page 73.

Demo model

For a demo model using the bit I/O unit, refer to the model Digital I/O units, which you can find in the processor board's demo library.

Where to go from here

Information in this section

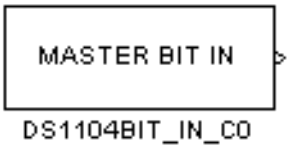
DS1104BIT_IN_Cx

Where to go from here

Information in this section

Block Description (DS1104BIT_IN_Cx)

Block



Purpose

To read a single bit of the 20-bit digital input.

I/O mapping

For information on the I/O mapping, refer to Bit I/O Unit (DS1104 Features 🕮).

Note

The I/O mapping of this block can conflict with other I/O features. For further information, refer to Conflicting I/O Features (DS1104 Features 🕮).

I/O characteristics

Relationship between the digital input and the output of the block:

Digital Input (TTL)	Simulink Output	
	Without Data Typing	With Data Typing
High	1 (double)	1 (boolean)
Low	0 (double)	0 (boolean)

Dialog pages

The dialog settings can be specified on the following page:

- Unit Page (DS1104BIT_IN_Cx) on page 24

Related RTLib functions

This RTI block is implemented using the following RTLib functions. The DS1104 RTLib Reference contains descriptions of these functions.

- ds1104_bit_io_init
- ds1104_bit_io_read

Unit Page (DS1104BIT_IN_Cx)

Purpose

To specify a channel for digital input.

Dialog settings

Channel number Lets you select a channel within the range 0 … 19 where as the channels 16 … 19 are multiplexed with 4 external interrupts.

Related topics

References

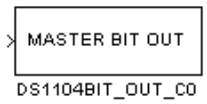
DS1104BIT_OUT_Cx

Where to go from here

Information in this section

Block Description (DS1104BIT_OUT_Cx)

Block



Purpose

To write to a single bit of the 20-bit digital output.

I/O mapping

For information on the I/O mapping, refer to Bit I/O Unit (DS1104 Features 🕮).

Note

The I/O mapping of this block can conflict with other I/O features. For further information, refer to Conflicting I/O Features (DS1104 Features 🕮).

I/O characteristics

Relation between the digital output and the input of the block:

Simulink Input		Digital Output (TTL)
Without Data Typing	**With Data Typing**	
> 0 (double)	1 (boolean)	High
≤ 0 (double)	0 (boolean)	Low

Dialog pages

The dialog settings can be specified on the following pages:

- Unit Page (DS1104BIT_OUT_Cx) on page 26
- Parameters Page (DS1104BIT_OUT_Cx) on page 26

Related RTLib functions

This RTI block is implemented using the following RTLib functions. The DS1104 RTLib Reference contains descriptions of these functions.

- ds1104_bit_io_init
- ds1104_bit_io_set
- ds1104_bit_io_clear

Unit Page (DS1104BIT_OUT_Cx)

Purpose

To specify a channel for digital output.

Dialog settings

Channel number Select a channel within the range 0 … 19 where as channels 16 … 19 are multiplexed with four external interrupts.

Related topics

References

Block Description (DS1104BIT_OUT_Cx)....25
Parameters Page (DS1104BIT_OUT_Cx)....26

Parameters Page (DS1104BIT_OUT_Cx)

Purpose

To specify the digital output at initialization and termination.

Description

- During the model initialization phase, an initial digital output value is written to each channel. This is especially useful if a channel is used within a triggered or enabled subsystem that is not executed right from the start of the simulation. With the initialization value, all channels have defined outputs during this simulation phase.
- When the simulation terminates, all channels hold their last digital output values by default. You can specify a user-defined output value on termination, and use these settings to drive your external hardware into a safe final condition.

The specified termination values of I/O channels are set when the simulation executes its termination function by setting the `simState` variable to STOP. If you stop the real-time application by using ControlDesk's **Stop RTP** command, the processor resets immediately without executing termination functions. The

current values of the I/O channels are kept and the specified termination values are not set.

Dialog settings

Initial output state The initial digital output at the start of the simulation.

Termination output state Either keep the current digital output when the simulation terminates, or set the digital output to a specified value.

Related topics

References

Block Description (DS1104BIT_OUT_Cx)..... 25
DS1104BIT_OUT_Cx..... 25
simState (RTI and RTI-MP Implementation Reference 🕮)
Stop RTP (ControlDesk Platform Management 🕮)

Incremental Encoder Interface

Introduction

The master PPC library contains several blocks for programming the incremental encoder interface.

Note

The basic settings for the encoder channels – for example the encoder signal type – can only be set via the master-setup block which is named DS1104ENC_SETUP.

For basic information, refer to Incremental Encoder Interface (DS1104 Features 🕮).

Demo model

For demo models using the incremental encoder interface, refer to the models **Encoder demo 1** and **Encoder demo 2**, which you can find in the processor board's demo library.

Where to go from here

Information in this section

Information in other sections

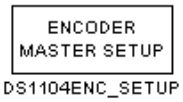
DS1104ENC_SETUP

Where to go from here

Information in this section

Block Description (DS1104ENC_SETUP)

Block



Purpose

To set the global parameters for the 2 encoder channels.

Note

This block must be placed in your model if you want to use any of the other encoder interface blocks.

I/O mapping

For information on the I/O mapping, refer to Incremental Encoder Interface (DS1104 Features 🕮).

Dialog pages

The dialog settings can be specified on the following page:

- Unit Page (DS1104ENC_SETUP) on page 30

Related RTLib functions

This RTI block is implemented using the following RTLib functions. The DS1104 RTLib Reference contains descriptions of these functions.

- ds1104_inc_init
- ds1104_inc_trigger_setup

Unit Page (DS1104ENC_SETUP)

Purpose

To set the global parameters for the encoder channels.

Dialog settings

Encoder signal type Differential (RS422) or single-ended (TTL) can be chosen for channels 1 … 2.

Related topics

Basics

Incremental Encoder Interface (DS1104 Features 🕮)

References

Block Description (DS1104ENC_SETUP)..... 29
DS1104ENC_SETUP..... 29

DS1104ENC_POS_Cx

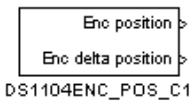
Where to go from here

Information in this section

Block Description (DS1104ENC_POS_Cx)..... 30
Unit Page (DS1104ENC_POS_Cx)..... 32
Initialization Page (DS1104ENC_POS_Cx)..... 32

Block Description (DS1104ENC_POS_Cx)

Block



Purpose

To read the position and delta position of one of the 2 encoder channels.

Description

The position is given in encoder lines plus the increment of the 4-fold line subdivision. The delta position provides the difference of the position value from the last to the current sample step, measured in encoder lines. You can use the delta position value to compute the velocity by dividing it by the sample time that the RTI block is executed with. In addition, this RTI block allows to initialize the encoder position at the start of the simulation.

For further information, refer to Encoder Signals and Line Count (DS1104 Features 🕮).

Note

- A master setup block (DS1104ENC_SETUP on page 29) must be placed in your model if you want to use DS1104ENC_POS_Cx.
- If reset-on-index is set for the specified encoder channel, you have to regard the following situation: When an index has occurred between the actual and the last evaluation of the delta position, the previously read position is set either to 0 or to the specified position value. This causes a deviation between the real and the calculated delta position.

I/O characteristics

The encoder channels 1 ... 2 use 4-fold line subdivision. This means that the position values for channels 1 ... 2 are represented in 1/4 lines. This leads to the following valid ranges for the position value:

Channel(s)	Signal Type	Position Information				Encoder Position (encoder lines + line subdivision)
		Sum	Line Count	Fine Count	Line Sub-division	
1 … 2	digital	24 bit	24 bit	–	4-fold	-2,097,152.0 … +2,097,151.75

I/O mapping

For information on the I/O mapping, refer to Incremental Encoder Interface (DS1104 Features 🕮).

Dialog pages

The dialog settings can be specified on the following pages:

- Unit Page (DS1104ENC_POS_Cx) on page 32
- Initialization Page (DS1104ENC_POS_Cx) on page 32

Related RTLib functions

This RTI block is implemented using the following RTLib functions. The DS1104 RTLib Reference contains descriptions of these functions.

- ds1104_inc_position_read
- ds1104_inc_position_read_immediately
- ds1104_inc_delta_position_read
- ds1104_inc_delta_position_read_immediately

- ds1104_inc_position_write
- ds1104_inc_trigger_setup

Related topics

Basics

Encoder Signals and Line Count (DS1104 Features 🕮)

References

DS1104ENC_SETUP.....29

Unit Page (DS1104ENC_POS_Cx)

Purpose

To specify the encoder channel.

Dialog settings

Channel number Select a single channel within the range 1 … 2.

Related topics

References

Block Description (DS1104ENC_POS_Cx).....30
Initialization Page (DS1104ENC_POS_Cx).....32

Initialization Page (DS1104ENC_POS_Cx)

Purpose

To specify the encoder position value at initialization.

Description

During the model initialization phase, the position counter of the channel is set to the position value specified in this page. This is especially useful if a channel resides in a triggered or enabled subsystem that is not executed at the start of the simulation.

Dialog settings

Position value The initial encoder position at the start of the simulation. You can specify the position value in lines only, or you may specify the line subdivision in steps of 0.25, too. For example, the position value 1000.75 corresponds to

1000 lines and 3/4 line subdivision. For information on the valid position values, refer to the table below.

Channel(s)	Signal Type	Position Information				Encoder Position (encoder lines + line subdivision)
		Sum	Line Count	Fine Count	Line Sub-division	
1 … 2	digital	24 bit	24 bit	–	4-fold	-2,097,152.0 … +2,097,151.75

Related topics

References

Block Description (DS1104ENC_POS_Cx)..... 30
Unit Page (DS1104ENC_POS_Cx)..... 32

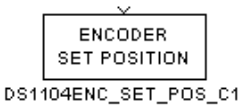
DS1104ENC_SET_POS_Cx

Where to go from here

Information in this section

Block Description (DS1104ENC_SET_POS_Cx)

Block



Purpose

To write to the position counter of one of 2 encoder channels.

Note

A master setup block (DS1104ENC_SETUP) must be placed in your model if you want to use DS1104ENC_POS_Cx.

Description

When the block is triggered during simulation by a rising edge signal, the counter of the specified channel is set to the adjusted position value, which must be given in lines.

I/O mapping

For information on the I/O mapping, refer to Incremental Encoder Interface (DS1104 Features 🕮).

I/O characteristics

The encoder channels 1 ... 2 use 4-fold line subdivision. This means that the position values for channels 1 ... 2 are represented in 1/4 lines. This leads to the following valid ranges for the position value:

Channel(s)	Signal Type	Position Information				Encoder Position (encoder lines + line subdivision)
		Sum	Line Count	Fine Count	Line Sub-division	
1 … 2	digital	24 bit	24 bit	–	4-fold	-2,097,152.0 … +2,097,151.75

Dialog pages

The dialog settings can be specified on the following page:

- Unit Page (DS1104ENC_SET_POS_Cx) on page 34

Related RTLib functions

This RTI block is implemented using the following RTLib functions. The DS1104 RTLib Reference contains descriptions of these functions.

- ds1104_inc_position_write

Unit Page (DS1104ENC_SET_POS_Cx)

Purpose

To specify a position value for the selected channel.

Dialog settings

Channel number Select a single channel within the range 1 … 2.

Position value The value the position counter is set when the block is triggered by a rising edge signal. You can specify the value in lines only, or you may specify the line subdivision in steps of 0.25, too. For example, the position value 1000.75 corresponds to 1000 lines and 3/4 line subdivision. For information on the valid position values, refer to the I/O characteristics of this block (see *I/O characteristics* in DS1104ENC_SET_POS_Cx on page 33).

Related topics

References

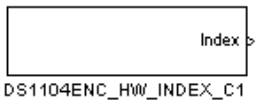
DS1104ENC_HW_INDEX_Cx

Where to go from here

Information in this section

Block Description (DS1104ENC_HW_INDEX_Cx)

Block



Purpose

To poll the encoder index and optionally to set the position counter without delay by hardware.

Note

- A master setup block (DS1104ENC_SETUP) must be placed in your model if you want to use DS1104ENC_HW_INDEX_Cx.
- You cannot use DS1104ENC_HW_INDEX_Cx and DS1104ENC_SW_INDEX_Cx for the same channel at the same time.

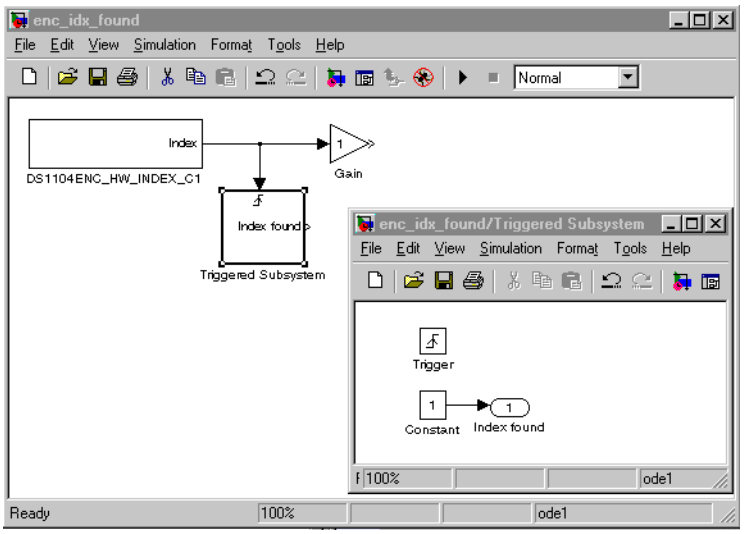
Description

When the index is detected, the corresponding position counter can be set immediately by hardware without any additional time delay. The hardware

reaction time between the detection of the index and the setting of the position counter is smaller than 1 µs.

- If you want to continually read the index - making a note of whether the index was passed for the first time - select the "current index" signal for the **Block output** in the **Parameters** page.

  Connect the DS1104ENC_HW_INDEX_Cx block output to the trigger port of a triggered subsystem. The subsystem contains a constant block, set to the value 1, which is connected to an outport that can be accessed by the root system. The rising edge of the index signal triggers the subsystem. The following picture gives an example:



- The time delay between the index detection and the (re)setting of the position counter by hardware is reduced to a minimum. The time delay does not depend on the processor utilization because the setting of the position counter and the program execution are decoupled. Furthermore, no model execution time is required for the (re)setting of the position counter.
- If the index should not be read, that is the block outport is not connected, this block can be placed in any subsystem because the (re)setting of the position counter does not depend on the program execution.

Note

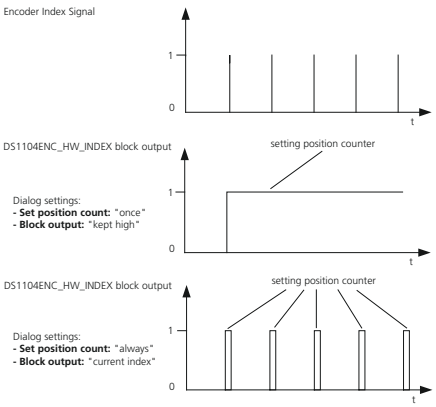
If the block is unconnected, no code for the block output is generated, that is the block is not accessible from ControlDesk. However, the index detection and setting of the position counter will be performed nevertheless.

I/O mapping

For information on the I/O mapping, refer to Incremental Encoder Interface (DS1104 Features 🕮).

I/O characteristics

- If "current index" is selected, the block outputs 1 if an index was detected since the previous sample hit. If no index was detected, the output is zero. The following figure shows the block output depending on the selected options:



Dialog pages

The dialog settings can be specified on the following pages:

- Unit Page (DS1104ENC_HW_INDEX_Cx) on page 37
- Parameters Page (DS1104ENC_HW_INDEX_Cx) on page 38

Related RTLib functions

This RTI block is implemented using the following RTLib functions. The DS1104 RTLib Reference contains descriptions of these functions.

- ds1104_inc_set_idxmode
- ds1104_inc_index_read

Unit Page (DS1104ENC_HW_INDEX_Cx)

Purpose

To specify the encoder channel.

Dialog settings

Channel number Select a single channel within the range 1 … 2.

Related topics

References

Parameters Page (DS1104ENC_HW_INDEX_Cx)

Purpose

To specify the behavior on index detection.

Dialog settings

Reset position count Select how often the position counter is reset: never/once/always. If you choose "once", the counter will only be set for the first index detection. "always" sets the position counter on every index.

Block output Select whether the output should be "kept high" after the first detection of an index or if the output should follow the "current index" signal.

Related topics

References

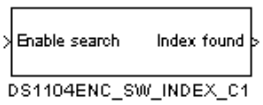
DS1104ENC_SW_INDEX_Cx

Where to go from here

Information in this section

Block Description (DS1104ENC_SW_INDEX_Cx)

Block



Purpose

To poll the encoder index of the channel selected and optionally to set the position counter by software.

Note

- A master setup block (DS1104ENC_SETUP) must be placed in your model if you want to use DS1104ENC_SW_INDEX_Cx.
- You cannot use DS1104ENC_HW_INDEX_Cx and DS1104ENC_SW_INDEX_Cx for the same channel at the same time.
- Sample times can be set using workspace variables. This does not apply for initial and termination values.

Description

The information whether an index was found is available to the model in its next execution step. Then the corresponding position counter can be set to the specified value by software (S-function).

The DS1104ENC_SW_INDEX_Cx block refers to the S-function file ds1104_enc_sw_index_s.c, which is available from the directory `<RCP_HIL_InstallationPath>\MATLAB\RTI\RTI1104\SFcn`. If a different functionality is required for your application, you should customize a copy of the source code of the S-function.

For a sequential index search of the different encoder channels the inputs of up to two DS1104ENC_SW_INDEX_Cx blocks can be cascaded. For this purpose, the output of the first block can be used as an input for the second one.

You can use the Ramp Generator for Encoder Index Search Block block to generate a reference output depending on the results of the index search (see Ramp Generator for Encoder Index Search Block (RTI and RTI-MP Implementation Reference 🕮)).

I/O mapping

For information on the I/O mapping, refer to Incremental Encoder Interface (DS1104 Features 🕮).

I/O characteristics

- An input value greater than zero, for example from a Simulink Constant input block, enables an index search for the selected interface channel.
- The block output depends on the selected search mode (**Type of index search**). By default, the index is searched once (the Search index twice for speed-up checkbox is cleared).

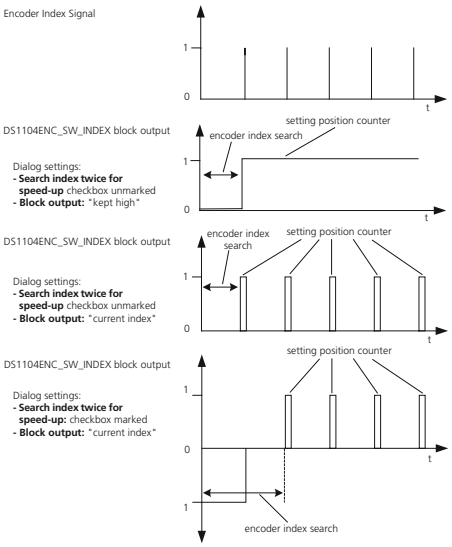
  If "Search index twice for speed-up" is cleared:

State	Simulink Output	
	Without Data Typing	With Data Typing
Index has not been found yet.	0 (double)	0 (int8)
Index has been found. Search is finished.	1 (double)	1 (int8)

If "Search index twice for speed-up" is selected:

State	Simulink Output	
	Without Data Typing	With Data Typing
Index has not been found yet.	–1 (double)	-1 (int8)
Index has been found once.	0 (double)	0 (int8)
Index has been found for the second time. Search is finished.	1 (double)	1 (int8)

The following figure shows the block output depending on the selected search options:



Dialog pages

The dialog settings can be specified on the following pages:

- Unit Page (DS1104ENC_SW_INDEX_Cx) on page 41
- Parameters Page (DS1104ENC_SW_INDEX_Cx) on page 41
- Options Page (DS1104ENC_SW_INDEX_Cx) on page 42

Related RTLib functions

This RTI block is implemented using the following RTLib functions. The DS1104 RTLib Reference contains descriptions of these functions.

- ds1104_inc_index_read
- ds1104_inc_position_write

Related topics

References

Ramp Generator for Encoder Index Search Block (RTI and RTI-MP Implementation Reference 🕮)

Unit Page (DS1104ENC_SW_INDEX_Cx)

Purpose

To specify the encoder channel.

Dialog settings

Channel number Select a single channel within the range 1 … 2.

Related topics

References

Block Description (DS1104ENC_SW_INDEX_Cx)....38
Options Page (DS1104ENC_SW_INDEX_Cx)....42
Parameters Page (DS1104ENC_SW_INDEX_Cx)....41

Parameters Page (DS1104ENC_SW_INDEX_Cx)

Purpose

To specify the behavior on index detection.

Dialog settings

Type of index search If "Search index twice for speed-up" is selected, the search is performed in two steps. Otherwise, the encoder index is searched once.

Set position count If selected, the position counter is set to the specified position value when the index search is finished.

Position value The value to which the position counter of the specified channel is set when the index search is finished. You can specify the value in lines only, or you may specify the line subdivision in steps of 0.25, too. For example, the position value 1000.75 corresponds to 1000 lines and 3/4 line subdivision.

Valid position values: The encoder channels 1 … 2 use 4-fold line subdivision. This means that the position values for channels 1 … 2 are represented in 1/4 lines. This leads to the following valid input ranges for the Position value:

Channel(s)	Signal Type	Position Information				Encoder Position (encoder lines + line subdivision)
		Sum	Line Count	Fine Count	Line Sub-division	
1 … 2	digital	24 bit	24 bit	–	4-fold	-2,097,152.0 … +2,097,151.75

Block output Select whether the output should be "kept high" after the completion of the index search or if the state of the "current index" should be available.

Related topics

References

Block Description (DS1104ENC_SW_INDEX_Cx)..... 38
Options Page (DS1104ENC_SW_INDEX_Cx)..... 42
Unit Page (DS1104ENC_SW_INDEX_Cx)..... 41

Options Page (DS1104ENC_SW_INDEX_Cx)

Purpose

To specify the sample time and the S-function for the encoder index search.

Dialog settings

Sample time The sample time of the task in which the encoder index search should be executed. Values are "-1" (inherited) or any multiple of the "Fixed step size" chosen for the model in the Solver page of the Simulation parameters dialog.

Solving S-function The underlying C-code S-function for the encoder index search.

Related topics

References

Block Description (DS1104ENC_SW_INDEX_Cx)..... 38
Parameters Page (DS1104ENC_SW_INDEX_Cx)..... 41
Unit Page (DS1104ENC_SW_INDEX_Cx)..... 41

Serial Interface

Where to go from here

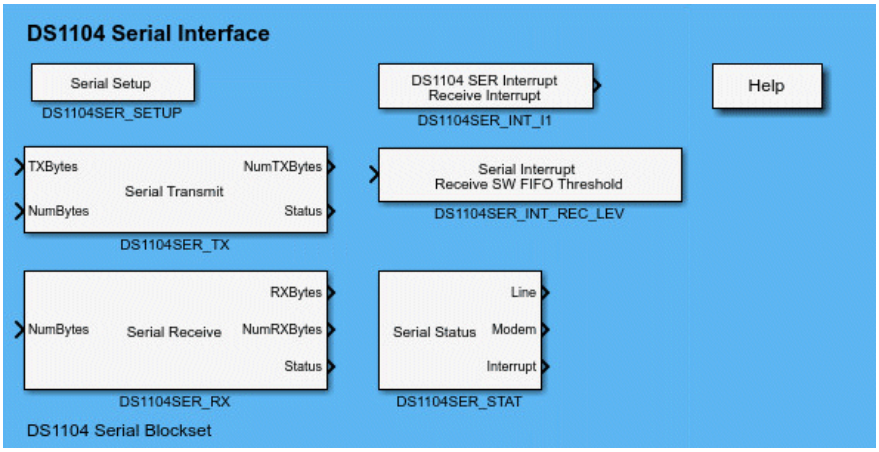
Information in this section

General Information on the Serial Interface

Overview of the Serial Interface

Introduction

After you double-click the SERIAL button in the rtilib1104/DS1104 MASTER PPC window, the Library: rti1104serlib is displayed.



The Serial Interface blocks can be used to implement serial communication.

Basic principles

Refer to Serial Interface (DS1104 Features 🕮).

Note

Although the serial blocks of different boards are almost the same, you must always use the board-specific serial blocks.

Library components

The library contains the following RTI blocks:

- DS1104SER_SETUP on page 45
- DS1104SER_STAT on page 49
- DS1104SER_TX on page 52
- DS1104SER_RX on page 56

- DS1104SER_INT_Iy on page 59
- DS1104SER_INT_REC_LEV on page 61

Related topics

Basics

Serial Interface (DS1104 Features 🕮)

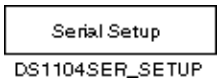
DS1104SER_SETUP

Where to go from here

Information in this section

Block Description (DS1104SER_SETUP)

Block



Purpose

To set the global parameters for the serial interface.

Note

- This block has to be placed in the model if any of the other serial blocks is used for the corresponding board.
- This block must not be used more than once per channel.

I/O mapping

For information on the I/O mapping, refer to Serial Interface (DS1104 Features 🕮).

Dialog pages

The dialog settings can be specified on the following pages:

- **UART Page** (refer to UART Page (DS1104SER_SETUP) on page 46)
- **FIFO Page** (refer to FIFO Page (DS1104SER_SETUP) on page 48)
- **Advanced Page** (refer to Advanced Page (DS1104SER_SETUP) on page 49)

Related RTLib functions

This RTI block is implemented using the following RTLib functions:

- dsser_init
- dsser_config
- dsser_set

Related topics

References

UART Page (DS1104SER_SETUP)

Purpose

To specify the UART parameters.

Dialog settings

Transceiver Lets you select the transceiver mode:

Transceiver Mode	Meaning
RS232	RS232 mode
RS422	RS422 mode
RS485	RS485 mode

Note

In RS485 mode, a transmission call waits for the transmission to be completed. This increases the turnaround time compared to the RS232 mode. As a consequence, task overruns might occur.
To reduce the risk of task overruns, you can use an external RS232/RS485 converter.

Baud rate Lets you specify the baud rate in bits per second.

Mode	Baud Rate Range
RS232	300 … 115,200 baud
RS422	300 … 1,000,000 baud
RS485	300 … 1,000,000 baud

For further information, refer to Specifying the Baud Rate of the Serial Interface (DS1104 Features 🕮).

Data bits Lets you choose the number of data bits. The valid values are: 5, 6, 7, 8.

Stop bits Lets you choose the number of stop bits. The valid values are: 1, 1.5 or 2. If you select 1.5 or 2, the number of stop bits depends on the number of specified data bits: For 5 data bits there are 1.5 stop bits; for 6, 7 and 8 data bits there are 2 stop bits.

Parity Lets you choose the parity mode:

Parity Mode	Meaning
No	No parity bits
Odd	Parity bit is set so that there is an odd number of "1" bits in the byte, including the parity bit
Even	Parity bit is set so that there is an even number of "1" bits in the byte, including the parity bit
Forced parity one	Parity bit is forced to a logical 1

Copy data to RX SW FIFO after reception of <value> byte(s) at latest Lets you choose the UART threshold at which data is copied from the UART to the receive buffer. Values are: 1, 4, 8, 14.

Note

Use the highest UART threshold possible to generate fewer interrupts, i.e., to decrease the UART's workload.

Enable RTS/CTS mode Lets you enable a hardware handshake (RTS/CTS).

Related topics

References

Advanced Page (DS1104SER_SETUP) 49
Block Description (DS1104SER_SETUP) 45
FIFO Page (DS1104SER_SETUP) 48

FIFO Page (DS1104SER_SETUP)

Purpose

To specify the software FIFO buffer.

Dialog settings

SW FIFO size Lets you specify the size of the software buffer. The size must be a power of two (2^n) and at least 64 bytes great. The maximum size depends on the available memory.

Overwrite mode Lets you choose the behavior of the receive buffer when an overrun occurs:

Overwrite Mode	Meaning
Discard new data	If the receive buffer is full, the new data is discarded.
Replace old data with FIFO method	If the receive buffer is full, the new data replaces the oldest data in the buffer. The number of bytes that are replaced is defined by Block size.

Block size Lets you specify the number of bytes that are deleted in RX SW FIFO overrun (see table above). Use this parameter to set up the appropriate data consistency for your model. Value range: 1 … (`SW FIFO size`-1)

Related topics

References

Advanced Page (DS1104SER_SETUP) 49
Block Description (DS1104SER_SETUP) 45
UART Page (DS1104SER_SETUP) 46

Advanced Page (DS1104SER_SETUP)

Purpose

To specify the behavior on model termination.

Dialog settings

Disable UART on termination Lets you choose the UART behavior on model termination. If the UART is disabled, data is neither transmitted nor received. No interrupts are generated in this case.

Related topics

References

Block Description (DS1104SER_SETUP)....45
FIFO Page (DS1104SER_SETUP)....48
UART Page (DS1104SER_SETUP)....46

DS1104SER_STAT

Where to go from here

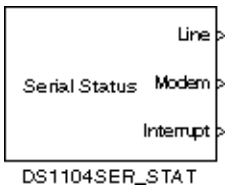
Information in this section

Block Description (DS1104SER_STAT)....49
To read the contents of the UART status register.

Status Page (DS1104SER_STAT)....52
To enable the status registers to be read.

Block Description (DS1104SER_STAT)

Block



Purpose

To read the contents of the UART status register.

Note

This block can only be used in interrupt-driven subsystems (see DS1104SER_INT_Iy on page 59).

- The Line status delivers correct results only if the block resides in a subsystem driven by the Line status interrupt.
- The Modem status delivers correct results only if the block resides in a subsystem driven by the Modem status interrupt.
- The Interrupt status is non-functional at the moment.

Description

The block reads the line, modem and interrupt statuses and writes the values to the outports. If you do not want to evaluate a status register, you can disable its outport with the block dialog.

I/O mapping

For information on the I/O mapping, refer to Serial Interface (DS1104 Features 🕮).

I/O characteristics

The outports show the values of the UART's register.

- The Line port outputs the 8 bits of the line status register. The following table shows the meanings of the individual bits:

Index	Meaning
1	Data ready (DR) indicator
2	Overrun error (OE) indicator
3	Parity error (PE) indicator
4	Framing error (FE) indicator
5	Break interrupt (BI) indicator
6	Transmitter holding register empty (THRE) indicator
7	Transmitter empty (TEMT) indicator
8	Error in receiver FIFO

- The Modem port outputs the 8 bits of the modem status register. The following table shows the meanings of the individual bits:

Index	Meaning
1	Clear-to-send (CTS) changed state
2	Data-set-ready (DSR) changed state
3	Ring-indicator (RI) changed state
4	Data-carrier-detect (DCD) changed state
5	Complement of CTS

Index	Meaning
6	Complement of DSR
7	Complement of RI
8	Complement of DCD

- The **Interrupt** port outputs the 8 bits of the interrupt status register. The following table shows the meanings of the individual bits:

Index	Meaning
1	Interrupt status: 0 if interrupt pending
2	Interrupt ID bit 1
3	Interrupt ID bit 2
4	Interrupt ID bit 3
5	Not relevant
6	Not relevant
7	FIFOs enabled (bit 0)
8	FIFOs enabled (bit 1)

- The following table shows the characteristics of the block outputs:

Port	Characteristics	Value
Line	Datatype	Boolean
	Range	0, 1
	Size	8
Modem	Datatype	Boolean
	Range	0, 1
	Size	8
Interrupt	Datatype	Boolean
	Range	0, 1
	Size	8

Dialog pages

The dialog settings can be specified on the following pages:

- **Status Page** (refer to Status Page (DS1104SER_STAT) on page 52)

Related RTLib functions

This RTI block is implemented using the following RTLib function:

- dsser_status_read

Related topics

References

dsser_status_read (DS1104 RTLib Reference 🕮)
Status Page (DS1104SER_STAT)..... 52

Status Page (DS1104SER_STAT)

Purpose

To enable the status registers to be read.

Dialog settings

Enable Line status port Lets you enable the line status output of the UART.

Enable Modem status port Lets you enable the modem status output of the UART.

Enable Interrupt status port Lets you enable the interrupt status output of the UART.

Related topics

References

Block Description (DS1104SER_STAT)..... 49

DS1104SER_TX

Where to go from here

Information in this section

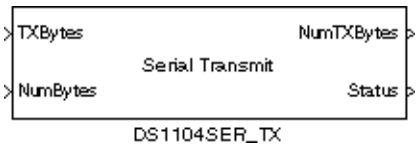
Block Description (DS1104SER_TX)..... 52
To send data via the serial interface.

TX Parameters Page (DS1104SER_TX)..... 54
To specify the transmitting parameters.

Advanced Page (DS1104SER_TX)..... 55
To specify the output.

Block Description (DS1104SER_TX)

Block



Purpose

To send data via the serial interface.

Description

The block sends the bytes of the TXBytes input via the serial interface during one sample step. The number of bytes to be sent can be either fixed or variable. If the number of bytes to be sent is fixed, you have to specify it with a block parameter. If the number of bytes to be sent is variable, you can specify it with either a block parameter or an inport. The status and the number of bytes that were sent are returned via outports.

You can disable the NumBytes input, NumTXBytes output and Status output with the block dialog.

I/O mapping

For information on the I/O mapping, refer to Serial Interface (DS1104 Features 🕮).

I/O characteristics

- The **TXBytes** input must be the stream of bytes to be written to the software buffer within one sample step.
- The **NumBytes** input must be the number of bytes to be sent within one sample step. The value must be less than or equal to the **Maximum number of bytes** block parameter. If it is less, only the specified number of bytes is sent.
- The **NumTXBytes** port outputs the number of bytes that could be written to the software buffer within the current sample step. You can use this output value and the **NumTXBytes** input to verify whether all the data could be sent.
- The **Status** port outputs the status of writing data to the software buffer within the current sample step. One of the following values is returned:

Return Value	Meaning
0	No error
202	The FIFO is filled or not all data could be copied to the FIFO

- The following table shows the characteristics of the block inputs and outputs:

Port	Characteristics	Value
TXBytes	Datatype	UInt8
	Range	0 … 255
	Size	1 … (SW FIFO size - 1)
NumBytes	Datatype	UInt32
	Range	1 … (SW FIFO size - 1)
NumTXBytes	Datatype	UInt32
	Range	1 … (SW FIFO size - 1)
Status	Datatype	Int32
	Range	int32

SW FIFO size is a block parameter. For further information, refer to DS1104SER_SETUP on page 45.

Dialog pages

The dialog settings can be specified on the following pages:

- **Tx Parameters Page** (refer to TX Parameters Page (DS1104SER_TX) on page 54)
- **Advanced Page** (refer to Advanced Page (DS1104SER_TX) on page 55)

Related RTLib functions

This RTI block is implemented using the following RTLib function:

- dsser_transmit

Related topics

References

Advanced Page (DS1104SER_TX)....55
DS1104SER_SETUP....45
dsser_transmit (DS1104 RTLib Reference 🕮)
TX Parameters Page (DS1104SER_TX)....54

TX Parameters Page (DS1104SER_TX)

Purpose

To specify the transmitting parameters.

Dialog settings

Transmission SW FIFO mode Lets you specify how to react if there is not enough free space in the transmit buffer:

Data Handling	Meaning
Discard all new data	All data in the sample step is discarded. Data consistency is ensured but you have to repeat the complete data from this sample step.
Write as much data as possible	The transmit buffer is filled until it is full. You only have to repeat bytes which did not fit into the transmit buffer.

Parameter flexibility Lets you specify whether the number of bytes to be sent is fixed (non-tunable) or variable (tunable).

Number of bytes Lets you specify the number of bytes to be sent within one sample step.

Maximum number of bytes Lets you specify the maximum number of bytes that can be sent within one sample step. The valid value range is:
1 … (SW FIFO size-1) (SW FIFO size is a block parameter, see DS1104SER_SETUP on page 45).

Specify the number of bytes Lets you specify whether to set the number of bytes to be sent within one sample step via the **NumBytes** inport or the block parameter.

Related topics

References

Advanced Page (DS1104SER_TX)

Purpose

To specify the output.

Dialog settings

Enable NumTXBytes port Lets you specify whether to output the number of bytes that could be sent or not.

Enable Status port Lets you specify whether to output the transmission status or not.

Related topics

References

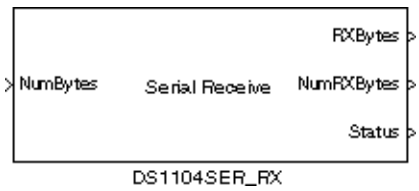
DS1104SER_RX

Where to go from here

Information in this section

Block Description (DS1104SER_RX)

Block



Purpose

To read bytes from the serial interface.

Description

The block receives bytes via a serial interface and writes them to the RXBytes output. The number of bytes to be received can be either fixed or variable. If the number of bytes to be received is fixed, you have to specify it with a block parameter. If the number of bytes to be received is variable, you can specify it with either a block parameter or an inport. The status and the number of received bytes are returned via outports.

You can disable the NumBytes input, NumRXBytes output and Status output with the block dialog.

I/O mapping

For information on the I/O mapping, refer to Serial Interface (DS1104 Features 🕮).

I/O characteristics

- The NumBytes input must be the number of bytes to be read from the software buffer within one sample step.

- The **RXBytes** port outputs the stream of data that could be read from the software buffer within one sample step. If fewer than the expected number of bytes could be received, the last bytes of the output still contain the data from the previous sample step.
- The **NumRXBytes** port outputs the number of bytes that could be read from the software buffer within one sample step.
- The **Status** port outputs the reception status. One of the following values is returned:

Return Value	Meaning
0	No error
4	The operation failed with no effect on the input or output data. No data is written to or read from the FIFO.
5	No new data is read from the FIFO.
202	The FIFO is filled or not all data could be copied to the FIFO.

- The following table shows the characteristics of the block input and outputs:

Port	Characteristics	Value
NumBytes	Datatype	UInt32
	Range	1 … (SW FIFO size - 1)
RXBytes	Datatype	UInt8
	Range	0 … 255
	Size	1 … (SW FIFO size - 1)
NumRXBytes	Datatype	UInt32
	Range	1 … (SW FIFO size - 1)
Status	Datatype	Int32
	Range	Int32

SW FIFO size is a block parameter. For further information, refer to DS1104SER_SETUP on page 45.

Dialog pages

The dialog settings can be specified on the following pages:

- **RX Parameters Page** (refer to RX Parameters Page (DS1104SER_RX) on page 58)
- **Advanced Page** (refer to Advanced Page (DS1104SER_RX) on page 59)

Related RTLib functions

This RTI block is implemented using the following RTLib functions:

- dsser_receive
- dsser_receive_term

Related topics

References

Advanced Page (DS1104SER_RX)..... 59
DS1104SER_SETUP..... 45
dsser_receive (DS1104 RTLib Reference 🕮)
dsser_receive_term (DS1104 RTLib Reference 🕮)
RX Parameters Page (DS1104SER_RX)..... 58

RX Parameters Page (DS1104SER_RX)

Purpose

To specify the receiving parameters.

Dialog settings

Reception mode Lets you specify how to react if there are fewer than the expected number of bytes in the receive buffer:

Data Handling	Meaning
Skip read operation	The new data is left in the receive buffer. The received data is collected in the receive buffer until the specified number of bytes is reached. Then it is copied to the **RXBytes** output.
Read available data anyway	All the available data is copied from the receive buffer to the **RXBytes** output.

Parameter flexibility Lets you specify whether the number of bytes to be received is fixed (non-tunable) or variable (tunable).

Number of bytes Lets you specify the number of bytes to be received within one sample step.

Maximum number of bytes Lets you specify the maximum number of bytes that can be received within one sample step. Value range: 1 … (SW FIFO size-1) (SW FIFO size is a block parameter, see DS1104SER_SETUP on page 45).

Specify the number of bytes Lets you specify whether to set the number of bytes to be received within one sample step via the **NumBytes** input or the block parameter.

Related topics

References

Advanced Page (DS1104SER_RX)..... 59
Block Description (DS1104SER_RX)..... 56

Advanced Page (DS1104SER_RX)

Purpose

To specify the output.

Dialog settings

Enable NumRXBytes port Lets you specify whether to output the number of bytes that could be received or not.

Enable Status port Lets you specify whether to output the transmission status or not.

Related topics

References

Block Description (DS1104SER_RX)..... 56
RX Parameters Page (DS1104SER_RX)..... 58

DS1104SER_INT_Iy

Where to go from here

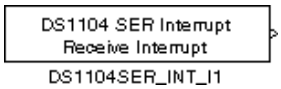
Information in this section

Block Description (DS1104SER_INT_Iy)..... 59
To make the interrupts of the serial interface available as trigger sources in the model.

Interrupt Page (DS1104SER_INT_Ix)..... 60
To specify the interrupt source.

Block Description (DS1104SER_INT_Iy)

Block



Purpose

To make the interrupts of the serial interface available as trigger sources in the model.

I/O mapping

For information on the I/O mapping, refer to Serial Interface (DS1104 Features 🕮).

I/O characteristics

The output triggers a function call to a subsystem if it is connected.

Dialog pages

The dialog settings can be specified on the following pages:

- Interrupt Page (refer to Interrupt Page (DS1104SER_INT_Ix) on page 60)

Related RTLib functions

This RTI block is implemented using the following RTLib functions:

- dsser_subint_handler_inst
- dsser_subint_enable
- dsser_subint_disable

Related topics

References

dsser_subint_disable (DS1104 RTLib Reference 🕮)
dsser_subint_enable (DS1104 RTLib Reference 🕮)
dsser_subint_handler_inst (DS1104 RTLib Reference 🕮)
Interrupt Page (DS1104SER_INT_Ix)..... 60

Interrupt Page (DS1104SER_INT_Ix)

Purpose

To specify the interrupt source.

Dialog settings

Interrupt source Lets you choose the interrupt type. The following table shows the available interrupt types:

Interrupt Type	Meaning
RX SW FIFO	Interrupt triggered when the number of bytes in the receive buffer reaches the specified threshold (see Initial RX SW FIFO threshold)
TX SW FIFO	Interrupt triggered when the transmit buffer is empty
Line status	Line status interrupt of the UART
Modem status	Modem status interrupt of the UART

Initial RX SW FIFO threshold Lets you specify the RX SW FIFO threshold for the receive interrupt in the range 1 … (SW FIFO size -1) . The value should be a multiple of the UART threshold (see **DS1104SER_SETUP** on page 45).

The RX SW FIFO threshold can be changed during run time by using the block DS1104SER_INT_REC_LEV on page 61.

Related topics

References

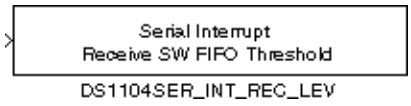
DS1104SER_INT_REC_LEV

Where to go from here

Information in this section

Block Description (DS1104SER_INT_REC_LEV)

Block



Purpose

To change the RX SW FIFO threshold during run time.

Description

The block changes the RX SW FIFO threshold that is initially specified by the DS1104SER_INT_Iy block (see DS1104SER_INT_Iy on page 59).

I/O mapping

For information on the I/O mapping, refer to Serial Interface (DS1104 Features 🕮).

I/O characteristics

- The Receive SW FIFO Threshold input sets a new RX SW FIFO threshold.
- The following table shows the characteristics of the block input:

Port	Characteristics	Value
Receive SW FIFO Threshold	Datatype	UInt32
	Range	1 … (SW FIFO size - 1)

SW FIFO size is a block parameter. For further information, refer to DS1104SER_SETUP on page 45.

Dialog pages

This block provides the Unit page (refer to Unit Page (DS1104SER_INT_REC_LEV) on page 62), but there are no settings to be specified.

Related RTLib functions

This RTI block is implemented using the following RTLib functions:

- dsser_config
- dsser_fifo_reset
- dsser_transmit_fifo_level
- dsser_receive_fifo_level

Related topics

References

DS1104SER_INT_ly....59
DS1104SER_SETUP....45
dsser_config (DS1104 RTLib Reference 🕮)
dsser_fifo_reset (DS1104 RTLib Reference 🕮)
dsser_receive_fifo_level (DS1104 RTLib Reference 🕮)
dsser_transmit_fifo_level (DS1104 RTLib Reference 🕮)
Unit Page (DS1104SER_INT_REC_LEV)....62

Unit Page (DS1104SER_INT_REC_LEV)

Dialog settings

There are no dialog settings on the Unit page to be specified.

Related topics

References

Block Description (DS1104SER_INT_REC_LEV)....61

Interrupts

Introduction

The master PPC library contains one block for programming the hardware interrupts.

Demo model

For demo models using interrupts, refer to the models **Hardware Interrupt** and **Software Interrupt**, which you can find under the topic **Task Handling** in the processor board's demo library.

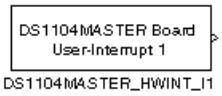
DS1104MASTER_HWINT_Ix

Where to go from here

Information in this section

Block Description (DS1104MASTER_HWINT_Ix)

Block



Purpose

To make the hardware interrupts of the DS1104 board available as trigger sources in a block diagram.

Note

For the multiplexed A/D converter (ADCH1 … 4), it is only possible to trigger the currently active channel. As the trigger signal usually occurs unsynchronized, you should use only one channel when external triggering of the multiplexed A/D converter is desired.

I/O mapping

For information on the I/O mapping, refer to Interrupts Provided by the DS1104 (DS1104 Features 🕮).

Note

The I/O mapping of this block can conflict with other I/O features. For further information, refer to Conflicting I/O Features (DS1104 Features 🕮).

Dialog pages

The dialog settings can be specified on the following page:

- Unit Page (DS1104MASTER_HWINT_Ix) on page 64

Unit Page (DS1104MASTER_HWINT_Ix)

Purpose

To specify the interrupt source.

Dialog settings

Interrupt Select the type of the interrupt source.

To feed an external interrupt signal into your system, 4 user interrupts are available. Additionally, for each of the 2 encoder position counters, an interrupt on index found is available. For the 5 ADC converter there are end-of-conversion interrupts available. You can also access the host interrupt with this block.

No	Interrupt Type	Related to
1	User interrupt 1	DS1104MASTER_HWINT_I1
2	User interrupt 2	DS1104MASTER_HWINT_I2
3	User interrupt 3	DS1104MASTER_HWINT_I3
4	User interrupt 4	DS1104MASTER_HWINT_I4
5	–	–
6	Host interrupt	Interrupt from the host PC
7	Encoder index channel 1	DS1104ENC_HW_INDEX_C1 or DS1104ENC_SW_INDEX_C1
8	Encoder index channel 2	DS1104ENC_HW_INDEX_C2 or DS1104ENC_SW_INDEX_C2
9	ADC 1 end-of-conversion	DS1104MUX_ADC
10	ADC 2 end-of-conversion	DS1104ADC_C5
11	ADC 3 end-of-conversion	DS1104ADC_C6

No	Interrupt Type	Related to
12	ADC 4 end-of-conversion	DS1104ADC_C7
13	ADC 5 end-of-conversion	DS1104ADC_C8

Related topics

References

Block Description (DS1104MASTER_HWINT_Ix)..... 63

Synchronizing I/O Unit

Introduction

The master PPC library contains one block for synchronizing the I/O units.

Demo model

For a demo model using the synchronization feature, refer to the **Slave PWM interrupt with synchronous triggering of I/O units** model, which you can find in the processor board's demo library.

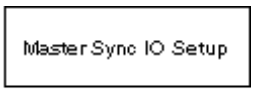
DS1104SYNC_IO_SETUP

Where to go from here

Information in this section

Block Description (DS1104SYNC_IO_SETUP)

Block



Purpose

To setup the synchronously triggering of master PPC's analog I/O units (ADC unit, DAC unit, and incremental encoder channels).

Description

By using this block in your model, triggering is enabled for the specified trigger signal. You can select the signal edge, on which the I/O shall be triggered, for the input and output components separately. The I/O units, that you want to enable for triggering can be selected individually.

Note

If you enable synchronous triggering of an ADC channel, you cannot use software triggering for the other ADC channels. You cannot mix the trigger modes.

For further information, refer to Synchronizing I/O Features of the Master PPC (DS1104 Features 🕮).

I/O mapping

For information on the I/O mapping, refer to Interrupts Provided by the DS1104 (DS1104 Features 🕮).

Note

The I/O mapping of this block can conflict with other I/O features. For further information, refer to Conflicting I/O Features (DS1104 Features 🕮).

Dialog pages

The dialog settings can be specified on the following pages:

- Trigger Source Page (DS1104SYNC_IO_SETUP) on page 67
- Input Units Page (DS1104SYNC_IO_SETUP) on page 68
- Output Units Page (DS1104SYNC_IO_SETUP) on page 69

Related RTLib functions

This RTI block is implemented using the following RTLib functions. The DS1104 RTLib Reference contains descriptions of these functions.

- ds1104_syncin_edge_setup
- ds1104_syncout_edge_setup
- ds1104_external_trigger_enable
- ds1104_adc_trigger_setup
- ds1104_dac_trigger_setup
- ds1104_inc_trigger_setup

Related topics

Basics

Synchronizing I/O Features of the Master PPC (DS1104 Features 🕮)

Trigger Source Page (DS1104SYNC_IO_SETUP)

Purpose

To specify the trigger source for all master PPC's I/O units.

Dialog settings

Trigger signal Lets you select the trigger source. If you choose "Internal source", the ST1PWM signal line is configured for providing a slave DSP PWM interrupt or a slave DSP bit I/O output as trigger signal. If you choose "External Input", the ST1PWM signal line is configured for providing an external input as synchronization signal.

Note

If you choose "External Input", it is not possible to use bits 0 … 5 of the DS1104SL_DSP_BIT_IN_Cx on page 73 respectively DS1104SL_DSP_BIT_OUT_Cx on page 76 block.

Related topics

References

Input Units Page (DS1104SYNC_IO_SETUP)

Purpose

To specify the master PPC's input units to be triggered.

Dialog settings

Trigger on … edge Lets you select the signal edge, on which the I/O shall be triggered. You can choose between "falling" and "rising" edge.

Synchronized A/D converter Lets you select the A/D converter to be synchronized.

Note

You can trigger only one channel of the multiplexed A/D converter. If you have specified more than one channel for the DS1104MUX_ADC block, triggering is disabled.

Synchronized encoder position and delta position Lets you select the encoder channels to be synchronized.

Related topics

References

Output Units Page (DS1104SYNC_IO_SETUP)

Purpose

To specify the master PPC's output units to be triggered.

Dialog settings

Trigger on ... edge Lets you select the edge at which the trigger shall be detected. You can choose between "falling" and "rising" edge.

Synchronized D/A converter Lets you select the D/A converter to be synchronized.

Related topics

References

RTI Blockset for the Slave DSP

Where to go from here

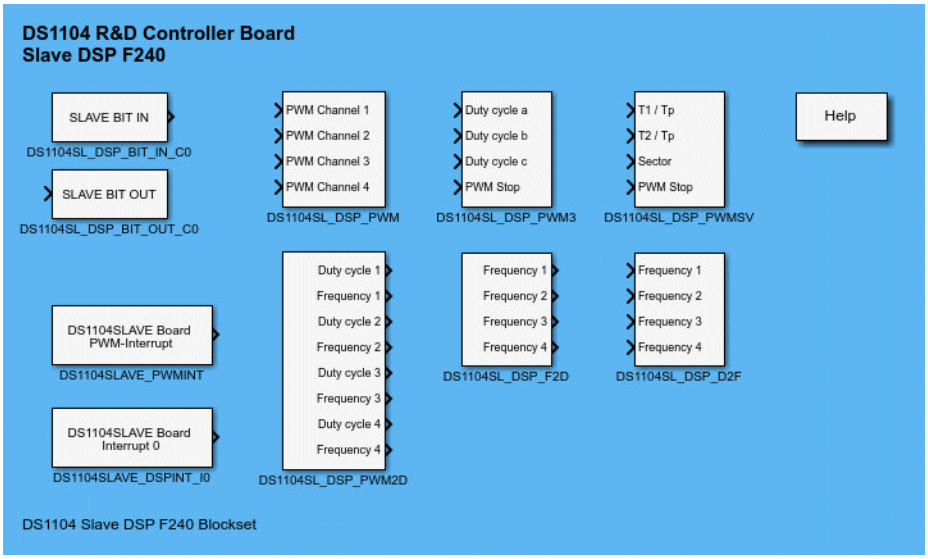
Information in this section

Overview of the Slave DSP Blockset

Overview of the Slave DSP Blockset

Blockset overview

After you click the SLAVE DSP F240 button in the Library: rtilib1104 window, the Library: rtilib1104/DS1104 SLAVE DSP window is displayed. It contains the I/O blocks served by the TI F240 slave DSP.



The following I/O units can be accessed by the RTI blockset for the slave DSP of the DS1104:

- Slave DSP Bit I/O Unit on page 73
- Slave DSP Timing I/O Unit on page 79
- Slave DSP Interrupts on page 103

Note

Due to the limited resources of the slave DSP, some units cannot be used at the same time. For further information on these specific limitations, refer to Conflicting I/O Features (DS1104 Features 🕮).

Slave DSP Bit I/O Unit

Introduction

The slave DSP library contains several blocks for programming the bit I/O unit of the slave DSP.

Tip

If you need further I/O channels, you can also use the digital I/O port directly served by the master PPC. For detailed description, refer to Bit I/O Unit on page 23.

Demo model

For a demo model using the slave DSP bit I/O unit, refer to the model **Digital I/O units**, which you can find in the demo library.

Where to go from here

Information in this section

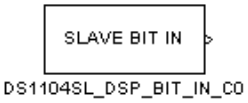
DS1104SL_DSP_BIT_IN_Cx

Where to go from here

Information in this section

Block Description (DS1104SL_DSP_BIT_IN_Cx)

Block



Purpose

To read from a single bit of the 14-bit digital input.

Description

- You can use each of the bits of the slave DSP bit I/O unit either for input or for output.
- If the slave DSP can offer the new input value in time – that is strict real-time processing – there is no difference between "Read new value" and "Read current value".

I/O mapping

For information on the I/O mapping, refer to Slave DSP Bit I/O Unit (DS1104 Features 🕮).

Note

- The I/O mapping of this block can conflict with other I/O features. For further information, refer to Conflicting I/O Features (DS1104 Features 🕮).
- If you use the DS1104SYNC_IO_SETUP block with an external input as trigger source, it is not possible to use bits 0 … 5 of this block.

I/O characteristics

Relationship between the digital input and the output of the block:

Digital Input TTL	Simulink Output	
	Without Data Typing	With Data Typing
High	1 (double)	1 (boolean)
Low	0 (double)	0 (boolean)

Dialog settings

The dialog settings can be specified on the following pages:

- Unit Page (DS1104SL_DSP_BIT_IN_Cx) on page 75
- Advanced Page (DS1104SL_DSP_BIT_IN_Cx) on page 75

Related RTLib functions

This RTI block is implemented using the following RTLib functions. The DS1104 RTLib Reference contains descriptions of these functions.

- ds1104_slave_dsp_communication_init
- ds1104_slave_dsp_bit_io_init
- ds1104_slave_dsp_bit_io_read_register
- ds1104_slave_dsp_bit_io_read_request
- ds1104_slave_dsp_bit_io_read
- ds1104_slave_dsp_bit_io_read_new

Unit Page (DS1104SL_DSP_BIT_IN_Cx)

Purpose

To specify a single bit of the digital input.

Dialog settings

Channel number Lets you select the channel to be read.

Related topics

References

Advanced Page (DS1104SL_DSP_BIT_IN_Cx)....75
Block Description (DS1104SL_DSP_BIT_IN_Cx)....74

Advanced Page (DS1104SL_DSP_BIT_IN_Cx)

Purpose

To specify the read mode of the digital input.

Dialog settings

Read mode Lets you select whether you want to read a new value - that is, the master PPC waits on the answer of the slave DSP - or whether the current value should be taken.

Related topics

References

Block Description (DS1104SL_DSP_BIT_IN_Cx)....74
Unit Page (DS1104SL_DSP_BIT_IN_Cx)....75

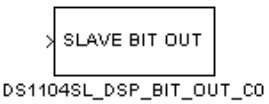
DS1104SL_DSP_BIT_OUT_Cx

Where to go from here

Information in this section

Block Description (DS1104SL_DSP_BIT_OUT_Cx)

Block



Purpose

To write to a single bit of the slave DSP bit I/O output.

Description

You can configure the channels of the slave DSP bit I/O unit for input or output. However, one digital channel can be used either for input or for output only.

I/O mapping

For information on the I/O mapping, refer to Slave DSP Bit I/O Unit (DS1104 Features 🕮).

Note

- The I/O mapping of this block can conflict with other I/O features. For further information, refer to Conflicting I/O Features (DS1104 Features 🕮).
- If you use the DS1104SYNC_IO_SETUP block with an external input as trigger source, it is not possible to use bits 0 … 5 of this block.

I/O characteristics

Relationship between the digital output and the input of the block:

Simulink Input		Digital Output (TTL)
Without Data Typing	**With Data Typing**	
> 0 (double)	1 (boolean)	High
≤ 0 (double)	0 (boolean)	Low

Dialog pages

The dialog settings can be specified on the following pages:

- Unit Page (DS1104SL_DSP_BIT_OUT_Cx) on page 77
- Parameters Page (DS1104SL_DSP_BIT_OUT_Cx) on page 77

Related RTLib functions

This RTI block is implemented using the following RTLib functions. The DS1104 RTLib Reference contains descriptions of these functions.

- ds1104_slave_dsp_communication_init
- ds1104_slave_dsp_bit_io_init
- ds1104_slave_dsp_bit_io_set_register
- ds1104_slave_dsp_bit_io_set
- ds1104_slave_dsp_bit_io_clear_register
- ds1104_slave_dsp_bit_io_clear

Unit Page (DS1104SL_DSP_BIT_OUT_Cx)

Purpose

To specify a single bit of the digital output.

Dialog settings

Channel number Lets you select the channel to be written.

Related topics

References

Block Description (DS1104SL_DSP_BIT_OUT_Cx)....76
Parameters Page (DS1104SL_DSP_BIT_OUT_Cx)....77

Parameters Page (DS1104SL_DSP_BIT_OUT_Cx)

Purpose

To specify the initialization and termination states of the specified channel.

Description

- During the model initialization phase an initial digital output value is written to each channel. This is especially useful if a channel is used within a triggered or enabled subsystem that is not executed right from the start of the simulation. With the **Initial output state** the channel has a defined output during this simulation phase.
- When the simulation terminates, all channels hold their last digital output values by default. You can specify a user-defined output value on termination, and use these settings to drive your external hardware into a safe final condition.

  The specified termination values of I/O channels are set when the simulation executes its termination function by setting the `simState` variable to STOP. If you stop the real-time application by using ControlDesk's **Stop RTP** command, the processor resets immediately without executing termination functions. The current values of the I/O channels are kept and the specified termination values are not set.

Dialog settings

Initial output state Lets you specify the initial digital output at the start of the simulation.

Termination output state Lets you either keep the current digital output when the simulation terminates, or set the digital output to a specified value.

Related topics

References

Block Description (DS1104SL_DSP_BIT_OUT_Cx)..... 76
simState (RTI and RTI-MP Implementation Reference 🕮)
Stop RTP (ControlDesk Platform Management 🕮)
Unit Page (DS1104SL_DSP_BIT_OUT_Cx)..... 77

Slave DSP Timing I/O Unit

Introduction

The slave DSP library contains several blocks for programming the timing I/O unit of the slave DSP.

Demo model

For demo models using the slave DSP timing I/O unit, refer to the models Timer I/O: PWM and PWM2D units and Timer I/O: PWM3 and PWM2D units, which you can find in the demo library.

Where to go from here

Information in this section

DS1104SL_DSP_PWM

Where to go from here

Information in this section

Block Description (DS1104SL_DSP_PWM)

Block

Purpose

To generate standard PWM signals with variable duty cycles and enable PWM stop during run time.

Tip

The dialog settings can be specified using workspace variables.

Description

For 1-phase PWM generation, a PWM stop can be specified to suspend PWM signal output during run time. The outputs of the channels are set to a defined TTL level. The dimensions of the inports are set to 2, which allows you to enter two values over the same port. This can be done via a Simulink MUX block, for example. Value 1 specifies the duty cycle and value 2 the PWM stop behavior. If you set value 2 to "0" a PWM signal is generated, "1" suspends signal generation and sets the output to the specified TTL level. If the PWM stop is disabled for a channel only the duty cycle can be input.

Although you can disable the PWM stop feature for each channel during run time, you can specify whether you want to set the PWM output to a specified TTL level or to generate a signal during the initialization phase.

I/O mapping

For information on the I/O mapping, refer to 1-Phase PWM Signal Generation (PWM) (DS1104 Features 🕮).

Note

The I/O mapping of this block can conflict with other I/O features. For further information, refer to Conflicting I/O Features (DS1104 Features 🕮).

I/O characteristics

The following table shows the available block ports related to the Simulink data types:

Simulink Inport	Input	Value	Data Type	Meaning
PWM Channel 1 … 4	Duty cycle 1 … 4	0 … 1	Double	Duty cycle of the PWM signal for channel 1 … 4.
	PWM Stop 1 … 4	0 / 1	Boolean	Enables PWM stop for channel 1 … 4: ▪ Value 1 stops PWM generation ▪ Value 0 resumes PWM generation

Note

PWM stop suspends the output of the PWM signal. Internally the signal is still generated. If you resume PWM signal generation the currently calculated value is output and not the initialization or termination value.

For the resolution for asymmetric and symmetric PWM mode, refer to 1-Phase PWM Signal Generation (PWM) (DS1104 Features 🕮).

Dialog pages

The dialog settings can be specified on the following pages:

- Unit Page (DS1104SL_DSP_PWM) on page 82
- Initialization Page (DS1104SL_DSP_PWM) on page 82
- PWM Stop and Termination Page (DS1104SL_DSP_PWM) on page 83
- Advanced Page (DS1104SL_DSP_PWM) on page 84

Related RTLib functions

This RTI block is implemented using the following RTLib functions. The DS1104 RTLib Reference contains descriptions of these functions.

- ds1104_slave_dsp_communication_init
- ds1104_slave_dsp_pwm_init
- ds1104_slave_dsp_pwm_duty_write_register
- ds1104_slave_dsp_pwm_duty_write

Unit Page (DS1104SL_DSP_PWM)

Purpose

To specify the mode and the frequency of the PWM signals.

Dialog settings

PWM mode Lets you select "asymmetric" to start the pulse at the beginning of the PWM period, or "symmetric" to generate mid-symmetric PWM waveforms.

PWM frequency Lets you select the PWM frequency. The frequency ranges correspond to the specified PWM mode:

PWM Mode	PWM Frequency
Asymmetric	2.5 Hz … 5 MHz
Symmetric	1.25 Hz … 5 MHz

Related topics

References

Initialization Page (DS1104SL_DSP_PWM)

Purpose

To set the output value of the PWM channels to TTL high/low or activate PWM generation with the initial duty cycle.

Description

If the PWM Signal option is enabled during the model initialization phase an initial duty cycle value is written to each PWM generator channel. This is especially useful if a channel is used within a triggered or enabled subsystem that is not executed right from the start of the simulation.

If you enable the PWM Stop option no signal is generated during the initialization phase and the output of each channel can be set to a defined TTL level (high or low). During the initialization phase, the inputs of the inports are not checked. See PWM Stop and Termination Page (DS1104SL_DSP_PWM) on page 83.

Dialog settings

PWM Stop (1 … 4) Lets you specify the output value, to which the channel is set without generating a PWM signal. Select the suspend to option to write the

TTL levels to the outport. Valid values are TTL High and TTL Low. By default, all **suspend to** options are selected with TTL low.

PWM Signal (1 ... 4) Lets you enter the duty cycle to be generated for each channel. Select the **output with duty cycle** option to start PWM signal generation with the defined initialization value. The default duty cycle is 0.5.

Set all to Allows you to specify the settings of all 4 channels at once. Select whether you want to use PWM stop and/or a termination value.

Related topics

References

Advanced Page (DS1104SL_DSP_PWM)....84
Block Description (DS1104SL_DSP_PWM)....80
PWM Stop and Termination Page (DS1104SL_DSP_PWM)....83
Unit Page (DS1104SL_DSP_PWM)....82

PWM Stop and Termination Page (DS1104SL_DSP_PWM)

Purpose

To specify the PWM stop and the duty cycle at termination.

Description

For each channel, PWM stop and the termination value can be specified. The PWM stop option allows you to suspend the PWM generation during run time and termination, and set the PWM channels to a defined output level. Depending on second values in the PWM channel inports, PWM signal generation is suspended or not.

If PWM signal is enabled you can specify a user-defined duty cycle value on termination and use these settings to drive your external hardware into a safe final condition.

The specified termination values of I/O channels are set when the simulation executes its termination function by setting the `simState` variable to STOP. If you stop the real-time application by using ControlDesk's **Stop RTP** command, the processor resets immediately without executing termination functions. The current values of the I/O channels are kept and the specified termination values are not set.

Dialog settings

set Ch (1 ... 4) Lets you enable the termination and the run time behavior for the PWM generation of each channel. Select the check box to enable the corresponding channel. By default, all channels are selected.

PWM Stop (1 ... 4) Lets you enable the PWM stop function for each channel and determine the output value. Select **suspend to** and select the value (TTL high or TTL low), to which the output of the channel is set when PWM

generation is suspended or the simulation is terminated. By default, all **suspend to** options are selected with TTL low.

PWM Signal (1 ... 4) Lets you enable the termination value for PWM generation. Select **output with duty cycle** and enter a termination duty cycle. Values must remain within the range 0 … 1. They can be selected for each channel. The default value is 0.5.

Set all to Allows you to specify the settings of all 4 channels at once. Select whether you want to use PWM stop and/or a termination value.

You can use the values as a template for the single channels.

Related topics

References

Advanced Page (DS1104SL_DSP_PWM)....84
Block Description (DS1104SL_DSP_PWM)....80
Initialization Page (DS1104SL_DSP_PWM)....82
simState (RTI and RTI-MP Implementation Reference 🕮)
Stop RTP (ControlDesk Platform Management 🕮)
Unit Page (DS1104SL_DSP_PWM)....82

Advanced Page (DS1104SL_DSP_PWM)

Purpose

To specify the polarity of the PWM output.

Dialog settings

Polarity Lets you select "active high" for an active high PWM output or "active low" for an active low output. They can be selected for each channel separately or for all channels at once. By default, "active high" is selected.

Related topics

References

Block Description (DS1104SL_DSP_PWM)....80
Initialization Page (DS1104SL_DSP_PWM)....82
PWM Stop and Termination Page (DS1104SL_DSP_PWM)....83
Unit Page (DS1104SL_DSP_PWM)....82

DS1104SL_DSP_PWM3

Where to go from here

Information in this section

Block Description (DS1104SL_DSP_PWM3)

Block

Purpose

To generate 3-phase PWM signals with original and inverted outputs, variable duty cycles, and a variable deadband in symmetric PWM mode.

Description

- Using the DS1104_DSP_PWM3 block, a PWM interrupt from the slave DSP to the master PPC is available. The interrupt can be triggered nearly over the whole period (interrupt alignment). The interrupt signal is provided via ST1PWM for user-specific purposes.

  To make the PWM interrupt available to your system, use the DS1104SLAVE_PWMINT block.
- Select the size of the deadband carefully to avoid effects caused by a deadband which is too big for the chosen PWM period.

Tip

The dialog settings can be specified using workspace variables.

For further information, refer to 3-Phase PWM Signal Generation (PWM3) (DS1104 Features 🕮).

I/O mapping

For information on the I/O mapping, refer to 3-Phase PWM Signal Generation (PWM3) (DS1104 Features 🕮).

Note

The I/O mapping of this block can conflict with other I/O features. For further information, refer to Conflicting I/O Features (DS1104 Features 🕮).

I/O characteristics

The following table shows the available block ports related to the Simulink data types:

Simulink Inport	Value	Data Type	Meaning
Duty cycle a, b, c	0 … 1	Double	Duty cycle of the PWM signal for channel a, b, c.
Stop PWM	0 / 1	Boolean	Enables PWM stop for channel pairs a/$\overline{a}$, b/$\overline{b}$ and c/$\overline{c}$: ▪ Value 1 stops PWM generation ▪ Value 0 resumes PWM generation

Note

- PWM stop suspends the output of the PWM signal. Internally the signal is still generated. If you resume PWM signal generation the currently calculated value is output and not the initialization or termination value.
- If you specified *Deadband* = 0 and *PWM Stop* = TTL low (termination value), and you resume the PWM signal generation, all signals are momentarily on high level. To avoid this misbehavior of the slave DSP, use always a deadband greater than 0.
- PWM stop has no influence on interrupt generation activated by the DS1104SLAVE_PWMINT block.

For the resolution, refer to 3-Phase PWM Signal Generation (PWM3) (DS1104 Features 🕮).

Dialog pages

The dialog settings can be specified on the following pages:

- Unit Page (DS1104SL_DSP_PWM3) on page 87
- Initialization Page (DS1104SL_DSP_PWM3) on page 87
- PWM Stop and Termination Page (DS1104SL_DSP_PWM3) on page 88

Related RTLib functions

This RTI block is implemented using the following RTLib functions. The DS1104 RTLib Reference contains descriptions of these functions.

- ds1104_slave_dsp_communication_init
- ds1104_slave_dsp_pwm3_init

- ds1104_slave_dsp_pwm3_duty_write_register
- ds1104_slave_dsp_pwm3_duty_write

Related topics

Basics

3-Phase PWM Signal Generation (PWM3) (DS1104 Features 🕮)

References

DS1104SLAVE_PWMINT..... 105

Unit Page (DS1104SL_DSP_PWM3)

Purpose

To specify the PWM frequency and the deadband.

Dialog settings

PWM frequency Lets you specify the PWM frequency within the range 1.25 Hz … 5 MHz.

Deadband Lets you specify the deadband between the original and the inverted output signals. The maximum value is 100 µs and nevertheless it should correspond to the PWM period, so it should not exceed 50% of the PWM period.

Related topics

References

Block Description (DS1104SL_DSP_PWM3)..... 85
Initialization Page (DS1104SL_DSP_PWM3)..... 87
PWM Stop and Termination Page (DS1104SL_DSP_PWM3)..... 88

Initialization Page (DS1104SL_DSP_PWM3)

Purpose

To specify the initial output value or the initial duty cycle.

Description

If PWM Signal is enabled during the model initialization phase an initial duty cycle value is written to each PWM generator channel. This is especially useful if a channel is used within a triggered or enabled subsystem that is not executed

right at the start of the simulation. With the initialization value all channels have defined outputs during this simulation phase.

If you enable PWM Stop no signal is generated during initialization and the output of each channel can be set to a TTL level (TTL high or TTL low). During the initialization phase, the input of the PWM Stop inport is not checked. See PWM Stop and Termination Page (DS1104SL_DSP_PWM3) on page 88.

Dialog settings

PWM Stop (a ... c) Specifies the output value, to which each channel is set when PWM generation is initialized. Select the **suspend to** option to write the TTL levels to the output channel (original signals /inverted signals). Valid values are TTL high and TTL low. By default, all suspend to options are selected. The original signal channels are set to TTL low, the inverted signal channels to TTL high.

PWM Signal (a ... c) Lets you specify the duty cycle for each channel pair. Select the **output with** option and enter the duty cycle value to start PWM signal generation with the defined initialization value. The default value is 0.5.

Related topics

References

PWM Stop and Termination Page (DS1104SL_DSP_PWM3)

Purpose

To specify the PWM stop and the duty cycle at termination.

Description

For each channel, PWM stop and the termination value can be specified. The PWM stop option allows you to suspend the PWM generation during run time and termination, and set the PWM channels to a defined output level. An additional inport is generated by any enabled PWM stop option to control the PWM generation with a constant block, for example. Depending on the inport's value, PWM generation is started or not. So, to start PWM generation, enter "0"and "1" to suspend PWM generation.

If the PWM Stop function is disabled you can specify a user-defined duty cycle value on termination, and use these settings to drive your external hardware into a safe final condition.

The specified termination values of I/O channels are set when the simulation executes its termination function by setting the `simState` variable to STOP. If you stop the real-time application by using ControlDesk's **Stop RTP** command,

the processor resets immediately without executing termination functions. The current values of the I/O channels are kept and the specified termination values are not set.

Dialog settings

Termination PWM Signal Enables setting the output modes and the termination values for each channel pair separately. Select the check box to specify the PWM stop behavior (**suspend to** settings are enabled) and the termination values.

PWM Stop (a … c) Lets you enable the PWM Stop inport and specify the output value, to which each channel is set when PWM generation is suspended. Select the **suspend to** option to write the TTL levels to the outport (original signals /inverted signals). Valid values are TTL high and TTL low. The TTL level is also used as termination value. By default, all **suspend to** options are selected. The original signal channels are set to TTL low, the inverted signal channels to TTL high.

PWM Signal (a … c) Lets you enable the termination value for PWM generation. Select **output with** and enter a termination duty cycle for the required channel pair. Values must remain within the range 0 … 1. They can be selected for each channel. The default value is 0.5.

Related topics

References

Block Description (DS1104SL_DSP_PWM3)....85
Initialization Page (DS1104SL_DSP_PWM3)....87
simState (RTI and RTI-MP Implementation Reference 🕮)
Stop RTP (ControlDesk Platform Management 🕮)
Unit Page (DS1104SL_DSP_PWM3)....87

DS1104SL_DSP_PWMSV

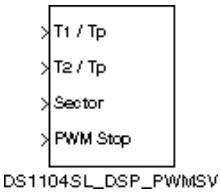
Where to go from here

Information in this section

Block Description (DS1104SL_DSP_PWMSV)....90
Unit Page (DS1104SL_DSP_PWMSV)....92
Initialization Page (DS1104SL_DSP_PWMSV)....92
PWM Stop and Termination Page (DS1104SL_DSP_PWMSV)....93

Block Description (DS1104SL_DSP_PWMSV)

Block



Purpose

To generate 3-phase Space Vector PWM with original and inverted outputs and a variable deadband.

Description

Using the DS1104SL_DSP_PWMSV block, a PWM interrupt from the slave DSP to the master PPC is available. The interrupt can be triggered nearly over the whole PWM period (interrupt alignment). The interrupt signal is provided via ST1PWM for user-specific purposes.

To make the PWM interrupt available to your system, use the DS1104SLAVE_PWMINT block.

Tip

The dialog settings can be specified using workspace variables.

For further information on PWM generation and the resolution, refer to Space Vector PWM Signal Generation (PWMSV) (DS1104 Features 🕮).

I/O mapping

For information on the I/O mapping, refer to Space Vector PWM Signal Generation (PWMSV) (DS1104 Features 🕮).

Note

The I/O mapping of this block can conflict with other I/O features. For further information, refer to Conflicting I/O Features (DS1104 Features 🕮).

I/O characteristics

The following table shows the available block ports related to the Simulink data types:

Simulink Inport	Value	Data Type	Meaning
T1/Tp	0 … 1	Double	Duration T1/Tp for PWM generation
T2/Tp	0 … 1	Double	Duration T2/Tp for PWM generation
Sectors	1 … 6	Double	Sector of the space vector

Simulink Inport	Value	Data Type	Meaning
Stop PWM	0 /1	Boolean	Enables PWM stop for the channel pairs a/$\overline{a}$, b/$\overline{b}$ and c/$\overline{c}$: ▪ Value 1 stops PWM generation ▪ Value 0 resumes PWM generation

Note

- PWM stop suspends the output of the PWM signal. Internally the signal is still generated. If you resume PWM signal generation the currently calculated value is output and not the initialization or termination value.
- PWM stop has no influence on interrupt generation activated by the DS1104SLAVE_PWMINT block.

Dialog pages

The dialog settings can be specified on the following pages:

- Unit Page (DS1104SL_DSP_PWMSV) on page 92
- Initialization Page (DS1104SL_DSP_PWMSV) on page 92
- PWM Stop and Termination Page (DS1104SL_DSP_PWMSV) on page 93

Related RTLib functions

This RTI block is implemented using the following RTLib functions. The DS1104 RTLib Reference contains descriptions of these functions.

- ds1104_slave_dsp_communication_init
- ds1104_slave_dsp_pwm3sv_init
- ds1104_slave_dsp_pwm3sv_duty_write_register
- ds1104_slave_dsp_pwm3sv_duty_write

Related topics

Basics

Space Vector PWM Signal Generation (PWMSV) (DS1104 Features 🕮)

References

DS1104SLAVE_PWMINT 105

Unit Page (DS1104SL_DSP_PWMSV)

Purpose

To specify the PWM frequency and the deadband.

Dialog settings

PWM frequency Lets you specify the PWM frequency in the range 1.25 Hz … 5 MHz.

Deadband Lets you specify the deadband between the original and the inverted output signals. The maximum value is 100 µs and nevertheless it should correspond to the PWM period, so it should not exceed 50% of the PWM period.

Related topics

References

Initialization Page (DS1104SL_DSP_PWMSV)

Purpose

To specify the initial ratios $T1/T_P$, $T2/T_P$ and the initial sector.

Description

If PWM Signal is enabled during the model initialization phase the initial duration ratios are written, that is the PWM outputs are driven into a defined state. This is especially useful if the duration ratios are used within a triggered or enabled subsystem that is not executed right from the start of the simulation. With the **Initialization value** all phases have defined outputs during this simulation phase.

If you enable PWM Stop no signal is generated during initialization and the output of each channel can be set to a TTL level (TTL high or TTL low). During the initialization phase, the input of the PWM Stop inport is not checked. See PWM Stop and Termination Page (DS1104SL_DSP_PWM3) on page 88.

Dialog settings

PWM Stop Specifies the output value, to which each channel is set when PWM generation is initialized. Select the **suspend to** option to write the TTL levels to the output channel (original signals /inverted signals). Valid values are TTL high and TTL low. By default, all suspend to options are selected. The

original signal channels are set to TTL low, the inverted signal channels to TTL high.

Duration and sectors Lets you specify the initial values for the ratios T1/TP (duration first vector/PWM period) and T2/TP (duration second vector/PWM period) and the identified sector. Values for the ratios must remain within the range 0 … 1. The sum must be less or equal to 1. The sector must be an integer value within the range 1 … 6, assuming positive sense of rotation. The default settings are for the T1/Tp value is "0.5", for the T2/Tp value "0.5" and for the sector value "1".

Note

If you select the **suspend to** option for all channels the duration and sectors are fixed and cannot be changed.

Related topics

References

Block Description (DS1104SL_DSP_PWMSV)....90
PWM Stop and Termination Page (DS1104SL_DSP_PWM3)....88
PWM Stop and Termination Page (DS1104SL_DSP_PWMSV)....93
Unit Page (DS1104SL_DSP_PWMSV)....92

PWM Stop and Termination Page (DS1104SL_DSP_PWMSV)

Purpose

To specify PWM stop and the ratios $T1/T_P$, $T2/T_P$ and the sector on termination.

Description

For each channel, PWM stop and the termination value can be specified. The PWM stop option allows you to suspend the PWM generation during run time and termination, and set the PWM channels to a defined output level. An additional inport is generated to control the PWM generation with a constant block, for example. Depending on the inport's value, PWM generation is started or not. So, to start PWM generation, enter "0"and "1" to suspend PWM generation.

If the PWM Stop function is disabled you can specify a user-defined ratio value on termination, and use these settings to drive your external hardware into a safe final condition.

The specified termination values of I/O channels are set when the simulation executes its termination function by setting the `simState` variable to STOP. If you stop the real-time application by using ControlDesk's **Stop RTP** command, the processor resets immediately without executing termination functions. The

current values of the I/O channels are kept and the specified termination values are not set.

Dialog settings

Termination PWM Signal Lets you enable the settings for the PWM stop and the termination of space vector PWM generation. If the check box is cleared no PWM stop is available during run time.

PWM Stop (channel a … c) Lets you enable the PWM Stop inport and specify the output value, to which each channel is set when PWM generation is suspended. Select the **suspend to** option to write the TTL levels to the outport (original signals /inverted signals). Valid values are TTL high and TTL low. The TTL level is also used as termination value. By default, all **suspend to** options are selected. The original signal channels are set to TTL low, the inverted signal channels to TTL high.

Duration and sectors Lets you specify the termination values for the ratios T1/TP (duration first vector/PWM period) and T2/TP (duration second vector/PWM period) and the identified sector. Values for the ratios must remain within the range 0 … 1. The sum must be less or equal to 1. The sector must be an integer value within the range 1 … 6, assuming positive sense of rotation. The default settings are for T1/Tp 0.5, for T2/Tp 0.5 and for the sector 1.

Note

If you select the **suspend to** option for all channels the duration and sectors are fixed and cannot be changed.

Related topics

References

Block Description (DS1104SL_DSP_PWMSV)..... 90
DS1104SL_DSP_PWMSV..... 89
Initialization Page (DS1104SL_DSP_PWMSV)..... 92
simState (RTI and RTI-MP Implementation Reference 🕮)
Stop RTP (ControlDesk Platform Management 🕮)
Unit Page (DS1104SL_DSP_PWMSV)..... 92

DS1104SL_DSP_D2F

Where to go from here

Information in this section

Block Description (DS1104SL_DSP_D2F)

Block

Purpose

To generate up to 4 non-negative square wave signals with variable frequencies.

I/O mapping

For information on the I/O mapping, refer to Slave DSP Square-Wave Signal Generation (D2F) (DS1104 Features 🕮).

Note

The I/O mapping of this block can conflict with other I/O features. For further information, refer to Conflicting I/O Features (DS1104 Features 🕮).

I/O characteristics

Scaling between the signal frequency and the input of the block: The frequency of the output signal specified in Hz corresponds to the input of the block.

Note

- Due to quantization effects, you will encounter considerable deviations between the input frequency and the generated frequency, especially for higher frequencies. To avoid a poor frequency resolution, you should therefore select the smallest possible frequency range.
- If D2F channel 4 is used, the frequency range 8 is not available for the D2F channels 1 … 3.
- If D2F channel 4 is used, you cannot generate standard PWM signals.
- The maximum frequencies for the D2F channels 1 … 3 are greater than 35 kHz. The precise values depend on the current channel, the frequencies generated on channels 1 … 3, and the set ranges (1 … 8).
- If in parallel interrupt-based functions – for example F2D or PWM2D – are active, the maximum frequency may decrease even more.

Dialog pages

The dialog settings can be specified on the following pages:

- Range Page (DS1104SL_DSP_D2F) on page 96
- Initialization Page (DS1104SL_DSP_D2F) on page 97
- Termination Page (DS1104SL_DSP_D2F) on page 98

Related RTLib functions

This RTI block is implemented using the following RTLib functions. The DS1104 RTLib Reference contains descriptions of these functions.

- ds1104_slave_dsp_communication_init
- ds1104_slave_dsp_d2f_init
- ds1104_slave_dsp_d2f_write_register

Range Page (DS1104SL_DSP_D2F)

Purpose

To specify the frequency range.

Dialog settings

Range selection Lets you select the range of the signal frequency. For information on the frequency ranges, refer to Slave DSP Square-Wave Signal Generation (D2F) (DS1104 Features 🕮).

Note

- Due to quantization effects, you will encounter considerable deviations between the input frequency and the generated frequency, especially for higher frequencies. To avoid a poor frequency resolution, you should therefore select the smallest possible frequency range.
- If D2F channel 4 is used, the frequency range 8 is not available for the D2F channels 1 … 3.
- If D2F channel 4 is used, you cannot generate standard PWM signals.
- The maximum frequencies for the D2F channels 1 … 3 are greater than 35 kHz. The precise values depend on the current channel, the frequencies generated on channels 1 … 3, and the set ranges (1 … 8).
- If in parallel interrupt-based functions – for example F2D or PWM2D – are active, the maximum frequency may decrease even more.

Related topics

References

Block Description (DS1104SL_DSP_D2F)....95
Initialization Page (DS1104SL_DSP_D2F)....97
Termination Page (DS1104SL_DSP_D2F)....98

Initialization Page (DS1104SL_DSP_D2F)

Purpose

To specify the initial frequency.

Description

During the model initialization phase, the output signal is either generated with an initial frequency or is set to 0. This is especially useful if a channel is used within a triggered or enabled subsystem that is not executed at the start of the simulation. With the **Initialization value**, the channel has a defined output during this simulation phase.

Dialog settings

Initialization value Lets you specify values of the initial frequency which must remain within the selected range. If a frequency below the lower limit is chosen, the signal generation starts with frequency 0. It can be selected for each channel.

Related topics

References

Block Description (DS1104SL_DSP_D2F)....95
Range Page (DS1104SL_DSP_D2F)....96
Termination Page (DS1104SL_DSP_D2F)....98

Termination Page (DS1104SL_DSP_D2F)

Purpose

To specify the frequency on termination.

Description

When the simulation terminates, the signal generation is continued with the last frequency, by default. However, to stop signal generation during this simulation phase, simply specify a frequency below the lower range limit, otherwise select one beyond the lower range limit. Use these settings to drive your external hardware into a safe final condition.

The specified termination values of I/O channels are set when the simulation executes its termination function by setting the `simState` variable to STOP. If you stop the real-time application by using ControlDesk's Stop RTP command, the processor resets immediately without executing termination functions. The current values of the I/O channels are kept and the specified termination values are not set.

Dialog settings

Output on termination Lets you set the signal frequency to a specific value, or take the last block input value when the simulation terminates. Values must remain within the selected range in general. If a frequency below the lower limit is chosen, the signal generation will stop. It can be selected for each channel.

Related topics

References

Block Description (DS1104SL_DSP_D2F)....95
Initialization Page (DS1104SL_DSP_D2F)....97
Range Page (DS1104SL_DSP_D2F)....96
simState (RTI and RTI-MP Implementation Reference 🕮)
Stop RTP (ControlDesk Platform Management 🕮)

DS1104SL_DSP_F2D

Where to go from here

Information in this section

Block Description (DS1104SL_DSP_F2D)

Block

Purpose

To measure the frequency of square wave signals on up to 4 independent channels.

Description

The measurement result is the frequency calculated by one period of the signal. The period is defined as the time between two rising edges. There is no averaging implemented.

I/O mapping

For information on the I/O mapping, refer to Slave DSP Square-Wave Signal Measurement (F2D) (DS1104 Features 🕮).

Note

The I/O mapping of this block can conflict with other I/O features. For further information, refer to Conflicting I/O Features (DS1104 Features 🕮).

I/O characteristics

Scaling between the signal frequency and the output of the block: The block outputs the signal frequency specified in Hz. For information on the ranges for frequency measurement, refer to Slave DSP Square-Wave Signal Measurement (F2D) (DS1104 Features 🕮).

Note

- The values of the maximum frequency depend on the number of used channels.
- When exceeding these ranges the measurement may be faulty.
- When using other interrupt-based functions at the same time – for example: square wave signal generation (D2F) – there may be measurement faults even in lower frequency ranges.

Dialog pages

The dialog settings can be specified on the following page:

- Range Page (DS1104SL_DSP_F2D) on page 100

Related RTLib functions

This RTI block is implemented using the following RTLib functions. The DS1104 RTLib Reference contains descriptions of these functions.

- ds1104_slave_dsp_communication_init
- ds1104_slave_dsp_f2d_init
- ds1104_slave_dsp_f2d_read_register
- ds1104_slave_dsp_f2d_read_request
- ds1104_slave_dsp_f2d_read

Range Page (DS1104SL_DSP_F2D)

Purpose

To specify the frequency limit for zero detection.

Dialog settings

Lower limit for zero detection Lets you specify the frequency limit for zero detection of the input signal. Smaller frequencies will cause a block output of zero. Value is given in Hz. It can be selected for each channel. The values must be given within the range 0.005 … 150 Hz.

Related topics

References

Block Description (DS1104SL_DSP_F2D) 99
DS1104SL_DSP_F2D 99

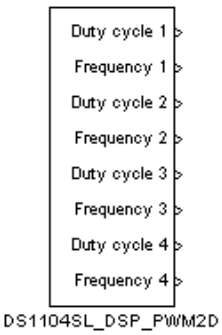
DS1104SL_DSP_PWM2D

Where to go from here

Information in this section

Block Description (DS1104SL_DSP_PWM2D)

Block



Purpose

To measure the duty cycles and the frequencies from up to 4 independent channels used for PWM-type signals.

I/O mapping

For information on the I/O mapping, refer to Slave DSP PWM Signal Measurement (PWM2D) (DS1104 Features 🕮).

Note

The I/O mapping of this block can conflict with other I/O features. For further information, refer to Conflicting I/O Features (DS1104 Features 🕮).

I/O characteristics

Scaling between the duty cycle and the input of the block: The block outputs the duty cycle (0 … 100%) within the range 0 … 1 and the PWM frequency in Hz.

Note

- The minimum period for which the duty cycle can be measured depends on the number of channels used for PWM analysis. For information on the ranges, refer to Slave DSP PWM Signal Measurement (PWM2D) (DS1104 Features 🕮).
- When these ranges are exceeded, the measurement may be faulty.
- When using other interrupt based functions at the same time – for example: square wave signal generation (D2F) – there may be measurement faults even in higher ranges.

The measurement algorithm used is accurate if the PWM period starts with the falling or rising edge of the corresponding PWM signal (asymmetric signal).

The DS1104 can also be used to measure PWM signals that are centered around the middle of the PWM period (symmetric signals). However, the measurement of the PWM frequency of symmetric PWM signals is faulty if the duty cycle of the PWM signal changes during measurement. For details, refer to Limitation for the Measurement of Symmetric PWM Signals (DS1104 Features 🕮).

Dialog pages

This block provides the Unit page, but there are no settings to be specified.

Related RTLib functions

This RTI block is implemented using the following RTLib functions. The DS1104 RTLib Reference contains descriptions of these functions.

- ds1104_slave_dsp_communication_init
- ds1104_slave_dsp_pwm2d_init
- ds1104_slave_dsp_pwm2d_read_register
- ds1104_slave_dsp_pwm2d_read_request
- ds1104_slave_dsp_pwm2d_read

Unit Page (DS1104SL_DSP_PWM2D)

Dialog settings

There are no dialog settings to be specified on the Unit page.

Related topics

References

Slave DSP Interrupts

Introduction

The slave DSP library contains several blocks for programming the hardware interrupts of the slave DSP.

Demo model

For a demo model using the slave DSP PWM interrupts, refer to the model **Slave-PWM Interrupt**, which you can find in the demo library.

Where to go from here

Information in this section

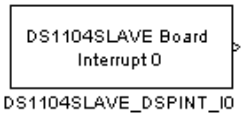
DS1104SLAVE_DSPINT_Ix

Where to go from here

Information in this section

Block Description (DS1104SLAVE_DSPINT_Ix)

Block



Purpose

To make the interrupts of the slave DSP of the DS1104 board available as trigger sources in a model.

Note

This block can only be used to access interrupts that are created by special user slave applications. To distinguish between different interrupt events, the slave application has to provide an interrupt number.

Description

The DS1104 board provides one physical line for interrupts from the slave DSP to the master. Simply specify the number of the sub-interrupt; it must correspond to the number of the interrupt that is created by the user slave application running on the slave DSP.

I/O mapping

For information on the I/O mapping, refer to Slave DSP Interrupt (DS1104 Features 🕮).

Dialog pages

The dialog settings can be specified on the following page:

- Unit Page (DS1104SLAVE_DSPINT_Ix) on page 104

Related RTLib functions

This RTI block is implemented using the following RTLib functions. The DS1104 RTLib Reference contains descriptions of these functions.

- dssint_decode

Unit Page (DS1104SLAVE_DSPINT_Ix)

Purpose

To specify the interrupt number.

Dialog settings

Interrupt number Lets you select the number of the interrupt within the range 0 … 15.

Related topics

References

Block Description (DS1104SLAVE_DSPINT_Ix)..... 103

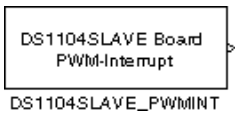
DS1104SLAVE_PWMINT

Where to go from here

Information in this section

Block Description (DS1104SLAVE_PWMINT)

Block



Purpose

To make the PWM interrupt of the slave DSP of the DS1104 board available as a trigger source in a block diagram.

Note

Depending on the PWM generation mode used, 3-phase or space vector, a DS1104SL_DSP_PWM3 or DS1104SL_DSP_PWMSV block must be part of the model. Otherwise the slave DSP PWM interrupt initialization cannot be completed and the DS1104SLAVE_PWMINT block is not ready for use.

Description

The DS1104 board provides one PWM interrupt from the slave DSP to the master. This interrupt can be generated if one of the following blocks is used:

- 3-phase PWM (see DS1104SL_DSP_PWM3 on page 85) or
- Space Vector PWM (see DS1104SL_DSP_PWMSV on page 89).

Tip

If your model contains the DS1104SYNC_IO_SETUP block, the PWM interrupt of the slave DSP can be used to synchronize the analog I/O units of the DS1104. For further information, refer to Synchronizing I/O Features of the Master PPC (DS1104 Features 🕮).

I/O mapping

For information on the I/O mapping, refer to Slave DSP PWM Interrupt (DS1104 Features 🕮).

Note

The I/O mapping of this block can conflict with other I/O features. For further information, refer to Conflicting I/O Features (DS1104 Features 🕮).

I/O characteristics

The block outputs the following signal:

I/O Pin	Signal	Range	Meaning
ST1PWM	TTL	0 … 5 V	Trigger source for external devices

Dialog pages

The dialog settings can be specified on the following page:

- Unit Page (DS1104SLAVE_PWMINT) on page 106

Related RTLib functions

This RTI block is implemented using the following RTLib functions. The DS1104 RTLib Reference contains descriptions of these functions.

- ds1104_slave_dsp_communication_init

Related topics

Basics

Synchronizing I/O Features of the Master PPC (DS1104 Features 🕮)

References

Unit Page (DS1104SLAVE_PWMINT)

Purpose

To specify the position (shift) of the PWM interrupt.

Dialog settings

Interrupt alignment Lets you specify the interrupt alignment within the range 0 … 1. Enter the interrupt position in the Position field. An alignment of 0 is not available, because 0 would disable the interrupt generation.

For more information, refer to Slave DSP PWM Interrupt (DS1104 Features 🕮).

Related topics

References

Block Description (DS1104SLAVE_PWMINT)..... 105

Numerics

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