1. Description

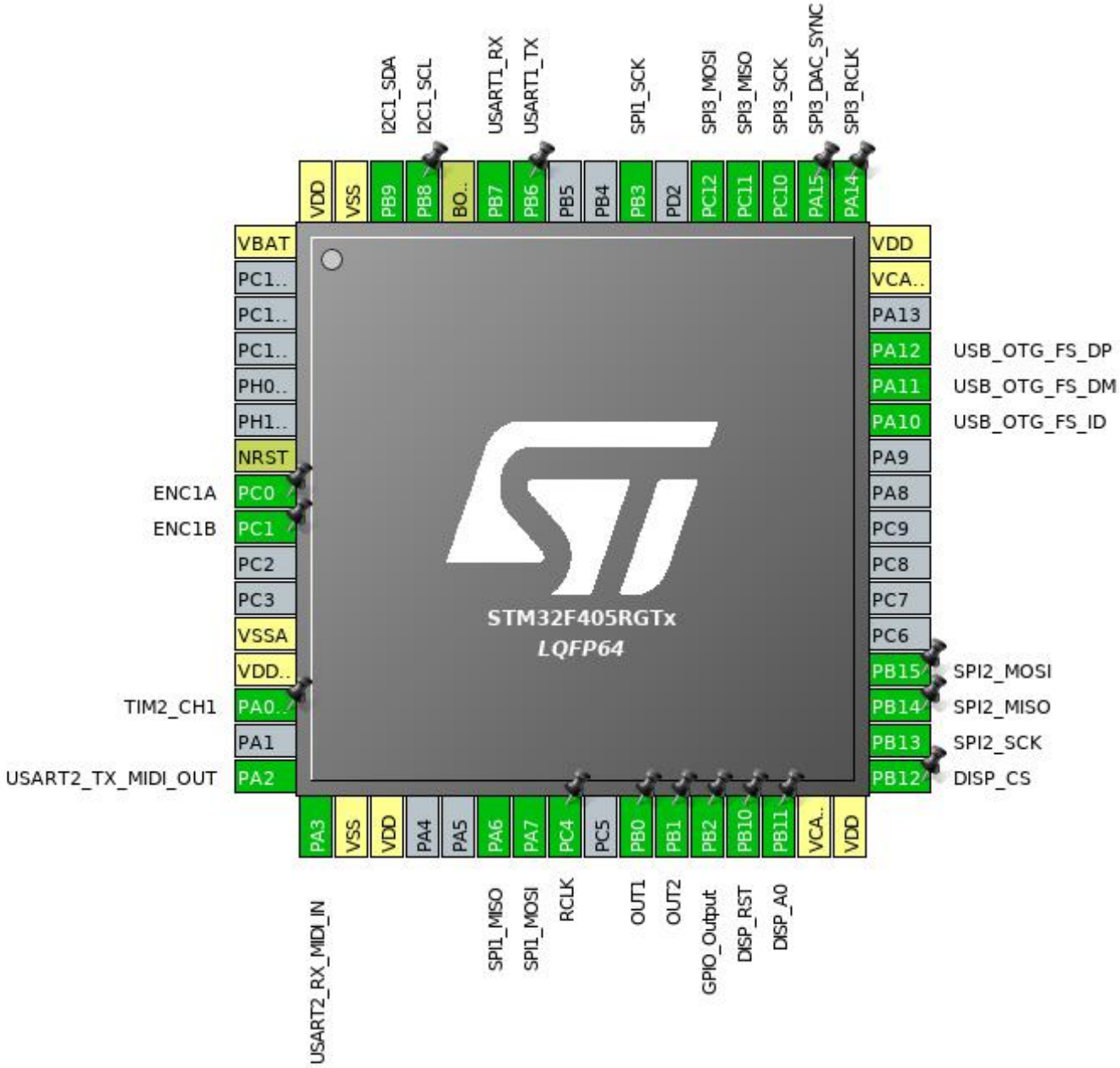
1.1. Project

Project Name	ClockModule
Board Name	custom
Generated with:	STM32CubeMX 5.0.1
Date	09/09/2019

1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F405/415
MCU name	STM32F405RGTx
MCU Package	LQFP64
MCU Pin number	64

2. Pinout Configuration



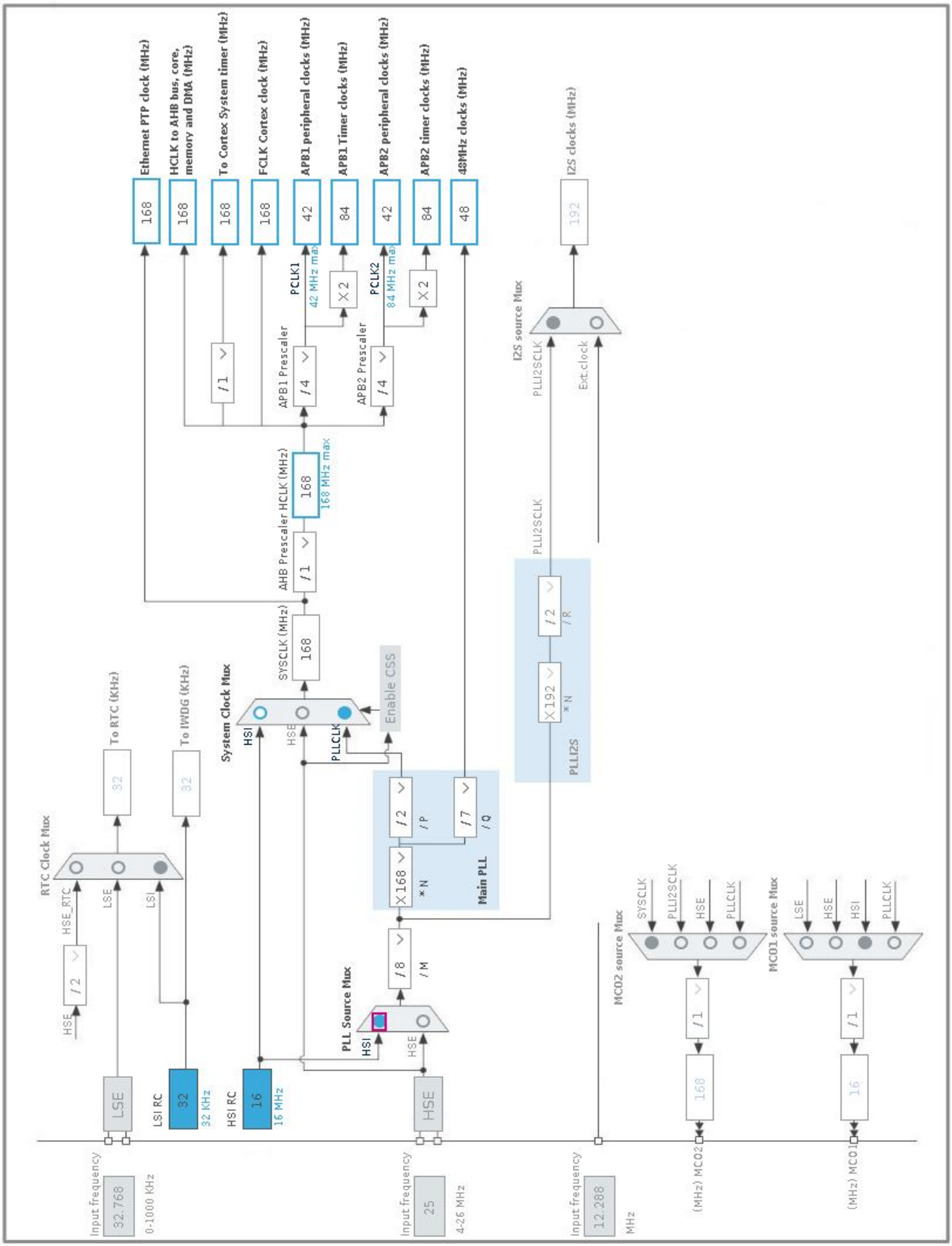
3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
7	NRST	Reset		
8	PC0 *	I/O	GPIO_Input	ENC1A
9	PC1 *	I/O	GPIO_Input	ENC1B
12	VSSA	Power		
13	VDDA	Power		
14	PA0-WKUP	I/O	TIM2_CH1	
16	PA2	I/O	USART2_TX	USART2_TX_MIDI_OUT
17	PA3	I/O	USART2_RX	USART2_RX_MIDI_IN
18	VSS	Power		
19	VDD	Power		
22	PA6	I/O	SPI1_MISO	
23	PA7	I/O	SPI1_MOSI	
24	PC4 *	I/O	GPIO_Output	RCLK
26	PB0 *	I/O	GPIO_Output	OUT1
27	PB1 *	I/O	GPIO_Output	OUT2
28	PB2 *	I/O	GPIO_Output	
29	PB10 *	I/O	GPIO_Output	DISP_RST
30	PB11 *	I/O	GPIO_Output	DISP_A0
31	VCAP_1	Power		
32	VDD	Power		
33	PB12 *	I/O	GPIO_Output	DISP_CS
34	PB13	I/O	SPI2_SCK	
35	PB14	I/O	SPI2_MISO	
36	PB15	I/O	SPI2_MOSI	
43	PA10	I/O	USB_OTG_FS_ID	
44	PA11	I/O	USB_OTG_FS_DM	
45	PA12	I/O	USB_OTG_FS_DP	
47	VCAP_2	Power		
48	VDD	Power		
49	PA14 *	I/O	GPIO_Output	SPI3_RCLK
50	PA15 *	I/O	GPIO_Output	SPI3_DAC_SYNC
51	PC10	I/O	SPI3_SCK	
52	PC11	I/O	SPI3_MISO	
53	PC12	I/O	SPI3_MOSI	
55	PB3	I/O	SPI1_SCK	

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
58	PB6	I/O	USART1_TX	
59	PB7	I/O	USART1_RX	
60	BOOT0	Boot		
61	PB8	I/O	I2C1_SCL	
62	PB9	I/O	I2C1_SDA	
63	VSS	Power		
64	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	ClockModule
Project Folder	/SYNC/FIRMWARE/GIT/ClockModule
Toolchain / IDE	TrueSTUDIO
Firmware Package Name and Version	STM32Cube FW_F4 V1.23.0

5.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F4
Line	STM32F405/415
MCU	STM32F405RGTx
Datasheet	022152_Rev8

6.2. Parameter Selection

Temperature	25
Vdd	3.3

7. IPs and Middleware Configuration

7.1. I2C1

I2C: I2C

7.1.1. Parameter Settings:

Master Features:

I2C Speed Mode	Standard Mode
I2C Clock Speed (Hz)	100000

Slave Features:

Clock No Stretch Mode	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0
General Call address detection	Disabled

7.2. SPI1

Mode: Full-Duplex Master

7.2.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**4 ***
Baud Rate	**10.5 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

7.3. SPI2

Mode: Full-Duplex Master

7.3.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**4 ***
Baud Rate	**10.5 MBits/s ***
Clock Polarity (CPOL)	**High ***
Clock Phase (CPHA)	**2 Edge ***

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

7.4. SPI3

Mode: Full-Duplex Master

7.4.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**21.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

7.5. SYS

Timebase Source: SysTick

7.6. TIM2

Clock Source : Internal Clock

Channel1: Input Capture direct mode

Channel2: Output Compare No Output

7.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**41 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**4000000000 ***
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	**Enable (Trigger delayed for master/slaves simultaneous start) ***
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Input Capture Channel 1:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

Output Compare No Output Channel 2:

Mode	Frozen (used for Timing base)
Pulse (32 bits value)	**10000 ***
CH Polarity	High

7.7. TIM5

Slave Mode: Reset Mode

Trigger Source: ITR0

mode: Clock Source

Channel2: Output Compare No Output

7.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**41 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**4000000000 ***

Internal Clock Division (CKD)	No Division
Slave Mode Controller	Reset Mode

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Output Compare No Output Channel 2:

Mode	Frozen (used for Timing base)
Pulse (32 bits value)	**10000 ***
CH Polarity	High

7.8. TIM10

mode: Activated

7.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**41 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**800 ***
Internal Clock Division (CKD)	No Division

7.9. USART1

Mode: Asynchronous

7.9.1. Parameter Settings:

Basic Parameters:

Baud Rate	**32250 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

7.10. USART2

Mode: Asynchronous

7.10.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

7.11. USB_OTG_FS

Mode: OTG/Dual_Role_Device

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
I2C1	PB8	I2C1_SCL	Alternate Function Open Drain	Pull-up	**Very High** *	
	PB9	I2C1_SDA	Alternate Function Open Drain	Pull-up	**Very High** *	
SPI1	PA6	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PA7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PB3	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
SPI2	PB13	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PB14	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PB15	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
SPI3	PC10	SPI3_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PC11	SPI3_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PC12	SPI3_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
TIM2	PA0-WKUP	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART1	PB6	USART1_TX	Alternate Function Push Pull	Pull-up	**Very High** *	
	PB7	USART1_RX	Alternate Function Push Pull	Pull-up	**Very High** *	
USART2	PA2	USART2_TX	Alternate Function Push Pull	Pull-up	**Very High** *	USART2_TX_MIDI_OUT
	PA3	USART2_RX	Alternate Function Push Pull	Pull-up	**Very High** *	USART2_RX_MIDI_IN
USB_OTG_FS	PA10	USB_OTG_FS_ID	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
GPIO	PC0	GPIO_Input	Input mode	**Pull-up ***	n/a	ENC1A
	PC1	GPIO_Input	Input mode	**Pull-up ***	n/a	ENC1B
	PC4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	RCLK
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OUT1
	PB1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OUT2
	PB2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DISP_RST
	PB11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DISP_A0
	PB12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DISP_CS
	PA14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI3_RCLK
	PA15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI3_DAC_SYNC

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
TIM1 update interrupt and TIM10 global interrupt	true	0	1
TIM2 global interrupt	true	0	0
TIM5 global interrupt	true	1	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
SPI1 global interrupt	unused		
SPI2 global interrupt	unused		
USART1 global interrupt	unused		
USART2 global interrupt	unused		
SPI3 global interrupt	unused		
FPU global interrupt	unused		

*** User modified value**

9. Software Pack Report