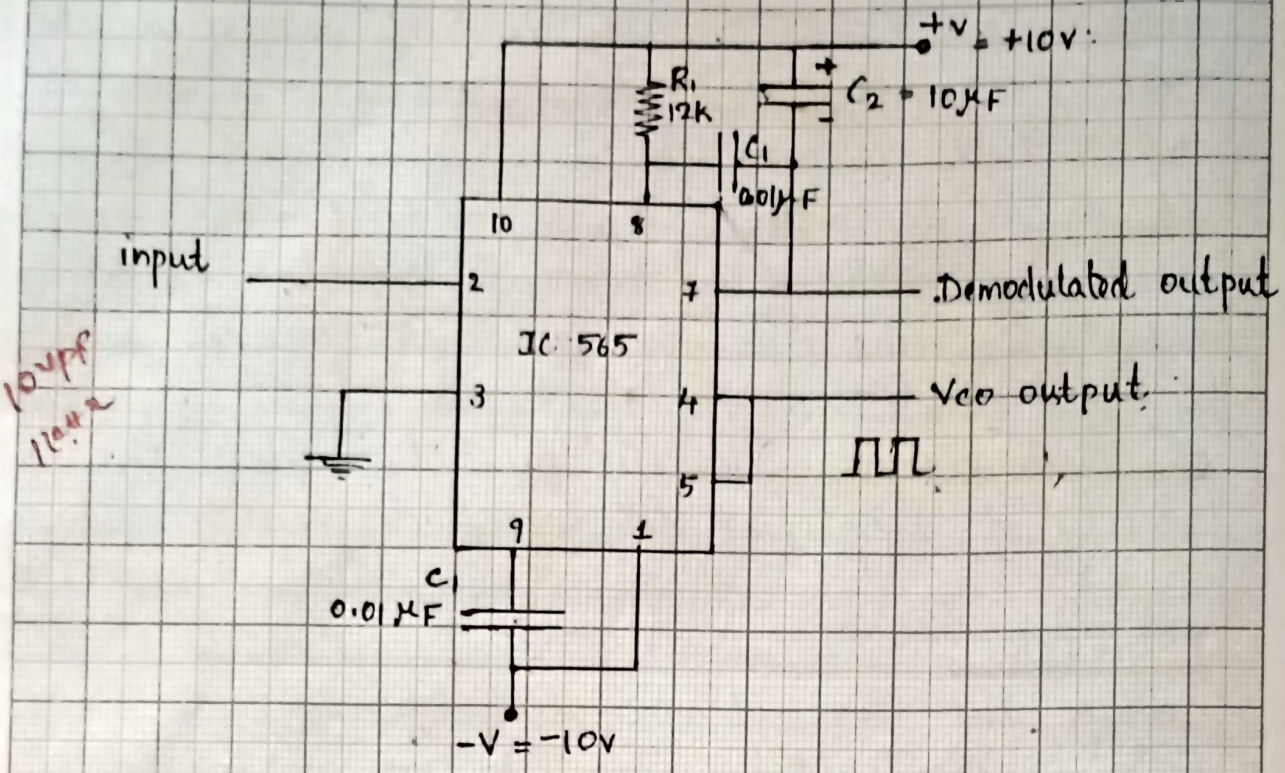
CIRCUIT DIAGRAM



DESIGN

Take $+V = +10v$ and $-V = -10V$.

Let the free running frequency f_0 be 2.5 KHz. (2.5 KHz VCO.)

$f_0 = \frac{1.2}{4 R_1 C_1} = 2.5 KHz$. Take $C_1 = 0.01 \mu F$.

Then $R_1 = 12k$.

The value of R_1 satisfieds the required condition

$2K < R_2 < 20k$.

Take $C_3 = 0.01 \mu F$ and $C_2 = 10 \mu F$. since.

$$f_L = \pm \frac{8 \times 2.5 \times 10^3}{10 - (-10)} = \pm 1 KHz.$$

$$f_C = \frac{\sqrt{10^3}}{\sqrt{2\pi \times 3.6 \times 10^3 \times 10 \times 10^6}} = 66.5 Hz$$

PLL CHARACTERISTICS

AIM:

To familiarize phase locked loop IC565 and study its functional characteristics.

COMPONENTS REQUIRED:

565 PLL, resistors, capacitors, dc power supply, signal generator, breadboard and CRO.

THEORY:

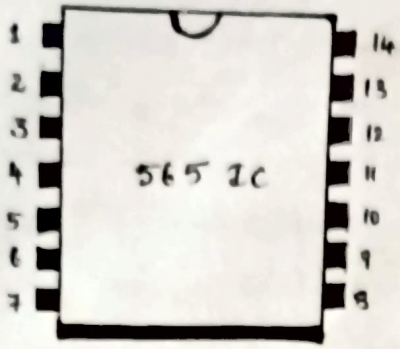
Monolithic PLL is a highly versatile device used for FM demodulation, frequency synthesizer, motor speed control, FSK demodulation etc...

PLL mainly consists of phase detector, an LPF and a VCO. Phase detector provides a dc voltage proportional to the phase difference between input frequencies. Low pass filter removes high frequency noise. The dc voltage controls VCO frequency. VCO frequency is fed back and compared with input frequency and automatically gets itself equal to the input frequency.

Functional block diagram of 565 PLL is shown in figure. The centre frequency is of the PLL is the free running frequency of VCO given by the equation.

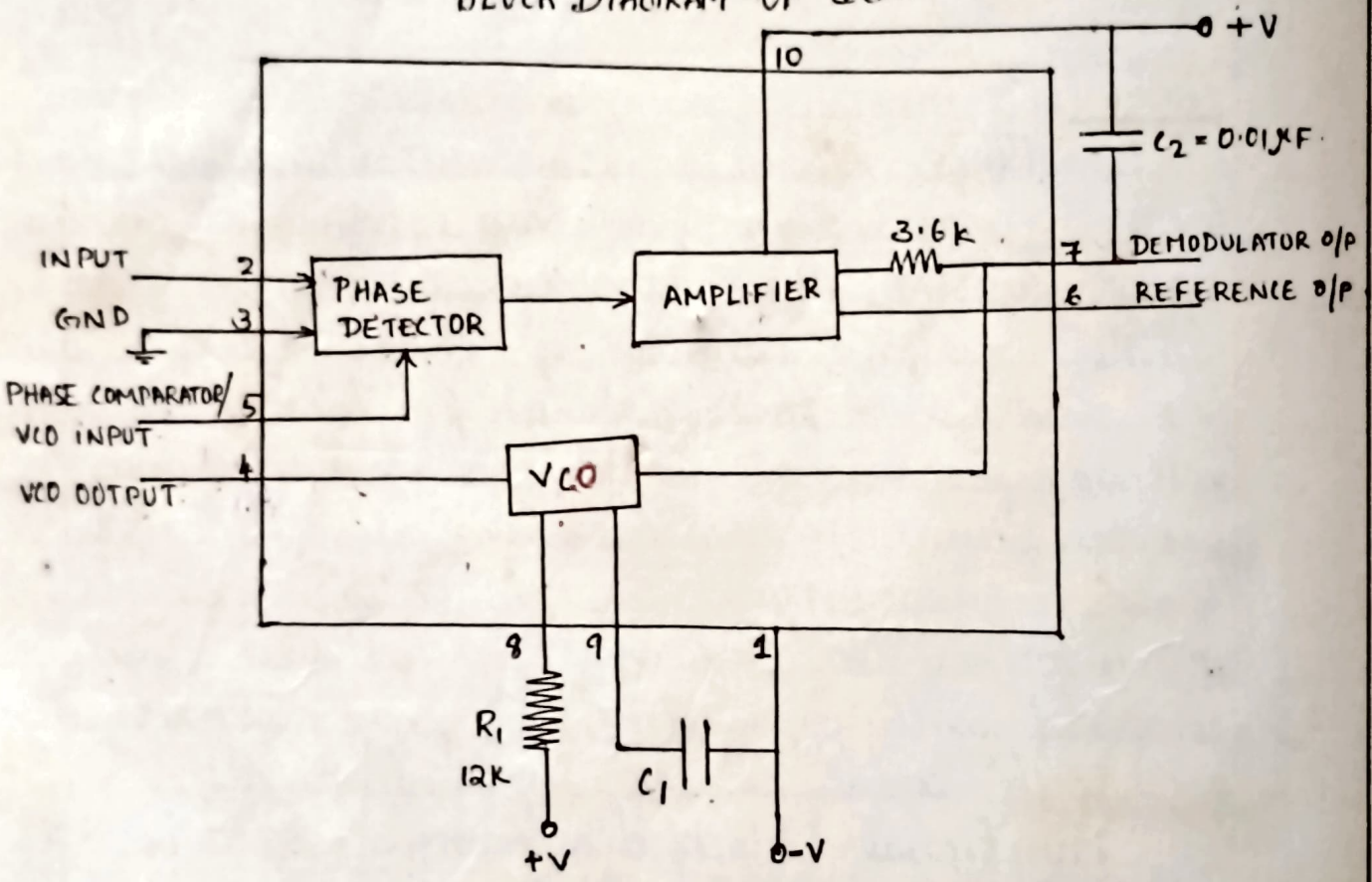
$$f_0 = \frac{1.2}{4R_1C_1} \text{ Hz}.$$

PINOUT OF IC565



1. V^-
2. INPUT
3. GND
4. VCO OUTPUT
5. PHASE COMPARATOR/ VCO INPUT
6. REFERENCE OUTPUT
7. DEMODULATED OUTPUT
8. EXTERNAL R FOR VCO
9. EXTERNAL C FOR VCO
10. V^+
11. NC
12. NC
13. NC
14. NC

BLOCK DIAGRAM OF IC565



where R_1 and C_1 are external resistor and capacitor connected to pins 8 and 1 respectively. R_1 must have value between 2k and 20k. A capacitor C_2 connected between pin 7 and the positive supply forms an LPF with an internal resistor R_2 (3.6k). C_2 is selected such that it should be large enough to eliminate variations in the demodulated output voltage inorder to stabilize vco frequency. lock range f_L of 565 PLL is given by the expression

$$f_L = \pm \frac{8 f_0}{V} \text{ Hz}$$

where f_0 - free running frequency of vco and

$$V = V_+ - V_-$$

$$\text{Capture range, } f_c = \pm \frac{\sqrt{f_L}}{\sqrt{2\pi 3.6 \times 10^3 C_2}}$$

C_2 is in farads. A small capacitor 100pF is connected between pin nos 7 and 8 to eliminate possible oscillation.

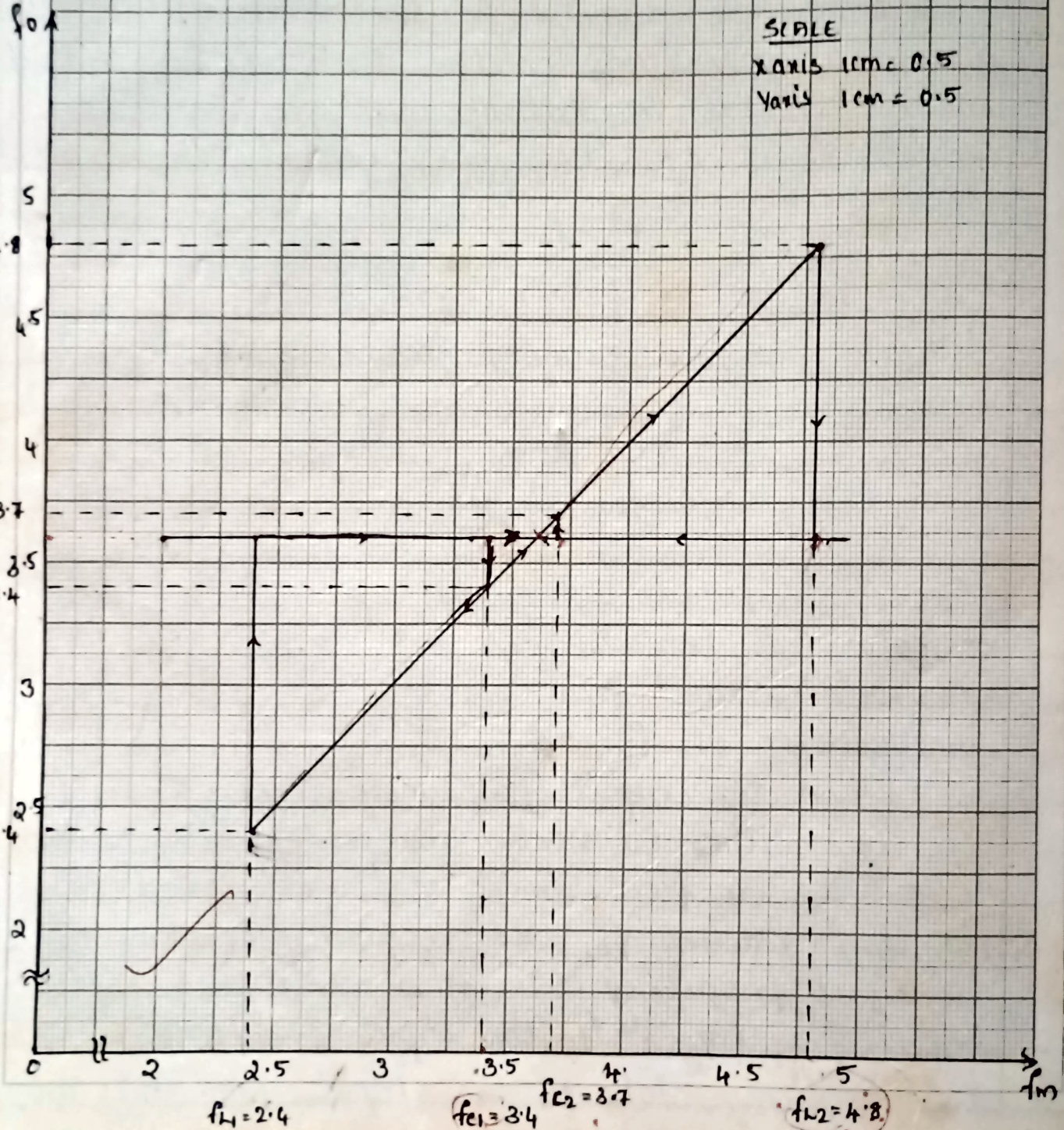
MEASUREMENT OF f_L and f_c:

When the input frequency is less than f_L, PLL is neither in lock nor in capture range. It will be in free running state. When input frequency reaches f_{c1}, vco frequency becomes equal to input frequency. In other words, vco captures input frequency. If the input frequency increases vco frequency follows the input frequency only

Lock Range, $f_L = f_{L2} - f_{L1} = 2.4\,KHz$

Capture Range, $f_c = f_{c2} - f_{c1} = 0.3\,KHz$

PLL CHARACTERISTICS



upto a limit of f_{L1}. If input frequency is again reduced, vco goes back to free running state.

Lock range $f_{L2} - f_{L1}$ can be defined as the range of frequency in which PLL keeps Lock with input frequency. Capture range $f_{c2} - f_{c1}$ is defined as range of frequencies in which PLL is able to attain lock with input frequency. Lock range is greater than capture range.

PROCEDURE:

1. Set up the circuit after verifying the condition of components.
2. Observe the waveform at pin no: 4 and note down the vco frequency. It is the free running frequency f_0 without any input signal.
3. Feed an input signal either sinewave or square wave to any one of the input term and vary its frequency from 100 Hz to 11 kHz. And note down f_{c1} and f_{L2}. Decrease the frequency from 11 kHz to 100 Hz and note down f_{c2} and f_{L1}. Calculate capture range and lock range.

RESULT:

Familiarized the phase locked loop IC 565 and studied its functional characteristics

Capture Range = 2.2 kHz

Lock Range = 2.4 kHz.

Centre frequency = 3.57 kHz.

02/02/08