To: Prof. Todd Kaiser
From: Sam Harkness
Regarding: EELE407 Final Report
Date: 8 Dec 2013

Abstract

This lab report details the theory and process behind fabricating CMOS logic on a silicon wafer.

1 Background

1.1 Fabrication Theory

1.1.1 Diffusion

Diffusion is a method by which doped regions of silicon are created. A region is infused with dopants using heat and a source of dopant atoms. In the case of wanting to create a P type silicon, our process uses Boron. In the case of N type silicon, Phosphorous is used. There are many options for dopants, but Boron and Phosphorous are some of the easier and cheaper to obtain.

The rate of diffusion of a dopant depends exponentially on temperature and follow an Arrhenius behavior, as shown in Equation 1. D_o and the activation energy E_A are constants of the dopant material. k is Boltzmann's constant.

$$D = D_o e^{-\frac{E_A}{kT}} \tag{1}$$

Diffusion also depends on whether the source of dopants is constant or limited. As time progresses in a constant source diffusion, the concentration of dopants on the wafer remains **constant**, while the concentration inside the silicon follows a complementary error function (erfc). The impurity concentration N in a constant source diffusion is determined by Equation 2, based on time t and depth x. N_o is the surface concentration determined by the temperature of the diffusion. Figure 1 can be used to determine N_o.

$$N(x,t) = N_o \; erfc\left(\frac{x}{2\sqrt{D_1 t_1}}\right) \tag{2}$$

A constant source diffusion is used to place a sufficient amount of dopant atoms on the surface of a wafer. The dopant source is then removed to prevent waste of dopant atoms, while a limited-source diffusion is used to *drive-in* the **limited** dopant. The dopant remaining on the surface of the wafer before a drive-in step is calculated as the dose Q, as shown in Equation 3. The impurity concentration N in a limited source diffusion is determined by Equation 4, based on time t and depth x.

$$Q = 2N_{o1}\sqrt{\frac{D_1 t_1}{\pi}} \tag{3}$$

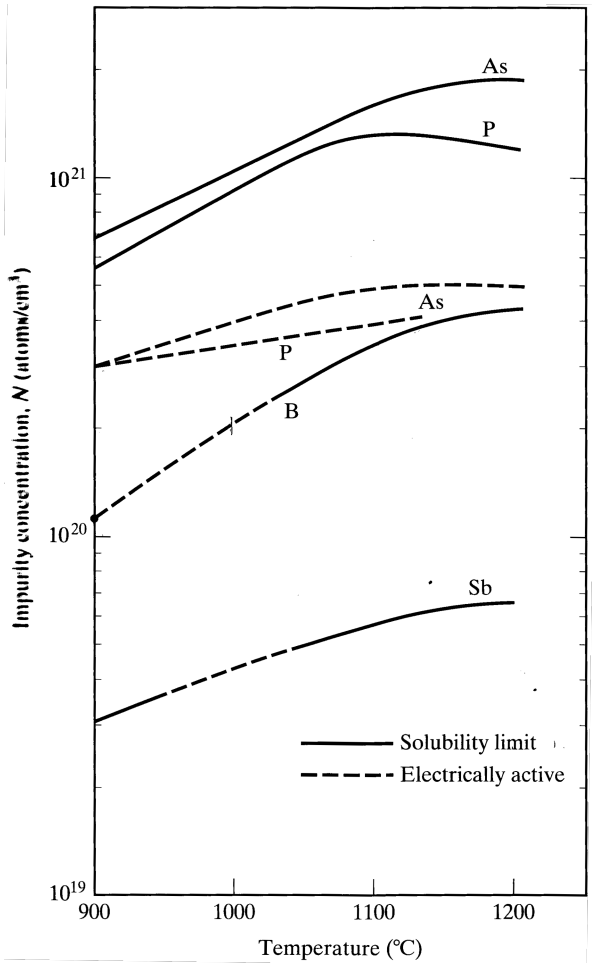


Figure 1: Impurity-Concentration Limits in Si for various dopants [1]

$$N(x,t) = \frac{Q}{\sqrt{\pi \sum\limits_{n} D_n t_n}} \; exp\left[- \left(\frac{x}{2\sqrt{\sum\limits_{n} D_n t_n}} \right)^2 \right] \tag{4}$$

The final depth of a diffusion, the *metallurgical junction depth* x_j, is useful for calculating the value of diffused resistors. x_j is calculated by setting the impurity concentration N equal to the background concentration N_B and solving for x, as shown in Equation 5.

$$x_j = 2\sqrt{\sum_{n} D_n t_n \cdot ln\frac{N_o}{N_B}} \tag{5}$$

Without physically damaging the wafer, it is difficult to measure the junction depth. However, the junction depth is directly proportional to the sheet resistance R_s of the diffused region, so it can be used as a measure of accuracy of the diffusion calculations. The resistivity ρ is a known constant of the substrate material.

$$R_s = \frac{\rho}{x_j} \tag{6}$$

The sheet resistance-junction depth product $R_s \cdot x_j$ can be calculated using Irvin curves. [1] The sheet resistance can be measured using a four-point probe, as depicted in Figure 2.

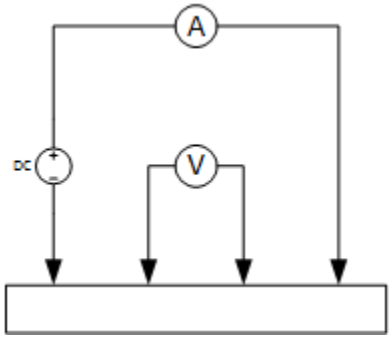


Figure 2: Schematic of a Four-Point Probe

1.1.2 Oxidation

Oxidation is the process by which an insulator is grown on a substrate; in our case Silicon Dioxide SiO_2 on Silicon Si. Oxidation can be performed using either a *wet* or *dry* process, utilizing Oxygen O_2 or Water H_2O respectively. Wet oxidation produces a worse insulator, but grows much faster. Dry oxidation produces a better insulator, but grows much slower. Regardless of process, oxidation is modeled the same way, as shown in Equation 7. The linear coefficient $\frac{B}{A}$ (Equation 8) and the parabolic coefficient B (Equation 9) are both determined by an Arrhenius relationship, very similar to the diffusion coefficient as discussed in Section 1.1.1. D_o and the activation energy E_A are constant for the oxidation process and the type of silicon.

$$X_o = \frac{A}{2}\left[-1 + \sqrt{1 + \frac{4B}{A^2}(t+\tau)}\right] \tag{7}$$

$$\frac{B}{A} = D_o e^{-\frac{E_A}{kT}} \tag{8}$$

$$B = D_o e^{-\frac{E_A}{kT}} \tag{9}$$

The only difference in dry vs. wet oxidation is the time offset τ. A dry oxidation behaves as if an initial oxide thickness X_i of 25 nm already exists on the wafer, while a dry oxide behaves as expected with no initial oxide on the wafer. τ can be calculated using Equation 10.

$$\tau = \frac{X_i^2}{B} + \frac{X_i}{B/A} \tag{10}$$

Oxide thickness can be measured using a nanospec, which utilized the reflection and refraction properties of light.

1.1.3 Photolithography

Photolithography is the process by which a mask is transmitted onto the surface of a wafer. Photolithography is used in every step of wafer fabrication, such as oxidation, diffusion, and metal deposition. A rough estimate of the minimum feature size F that can be transferred to the wafer surface is given by Equation 11, based upon the wavelength λ of light and the numerical aperture NA of the lens. The numerical aperture of a lens is simply the sine of the convergence angle θ.

$$F = 0.5\frac{\lambda}{NA} \tag{11}$$

Also important to the photolithography process is the depth of field over which focus is maintained, given by Equation 12.

$$DF = 0.6\frac{\lambda}{(NA)^2} \tag{12}$$

The photoresist used in our photolithography process is Shipley 1813, a positive resist. A positive resist is washed away in developer when exposed, whereas a negative resist is washed away in developer when not exposed. A mask is designed to be used with a certain type of resist. For this process, we use 1 μm of Shipley 1813, requiring an exposure time of 4.5 sec. To distribute an even coating of 1 μm resist, the wafer is spun at 5250 RMP for 30 sec. [4]

1.1.4 Etching and Cleaning

Our process uses wet etching remove unwanted material, such as oxide or aluminum. SiO_2 is etched with Buffered Oxide Etch (BOE), a combination of hydrofluoric acid (HF) and buffering chemicals to stabilize the reaction. BOE is highly selective to silicon dioxide so the photoresist is not etched. The only other material that needs to be etched in our process is Aluminum (Al), which is etched by Phosphoric Acid Etch (PAE) at approximately 350 Å/min. [3]

After etching SiO_2 or Al, the remaining photoresist is removed using a 3 solvent clean: Acetone, Isopropyl Alcohol, and Methanol. The acetone removes the photoresist, while isopropyl and methanol remove acetone residue. Finally, the wafers are rinsed with deionized water and dried with nitrogen. This removes errant dust particles from the surface of the wafer. [3]

Before a deposition is perfomed, an RCA clean is performed. The RCA clean consists of 3 chemical solutions. The first is a mixture of sulfuric acid and hydrogen peroxide, known as a Pirahna etch, that removes organic materials. The second is a weak BOE to strip native oxide. The final mixture, ionic clean, removes heavy metal ions with hydrochloric acid, water, and hydrogen peroxide. [3]

1.1.5 Metal Evaporation

The method of depositing a conductor for this process is Physical Vapor Deposition (PVD). In our case, Aluminum (Al) is the conductor of choice for both vias and surface level connections. In PVD, the conductive material is evaporated using heat and condenses on the surface of the wafer. Using simple geometry, the thickness of the Al can be determined for any point on the wafer. In our case, a sheet of aluminum foil is evaporated, so we use Equation 13 to find the volume of the rectangular prism. When the Al is evaporated, the cloud of gas expands in a sphere as if it were a balloon. The sphere of expanding gas does not contact the wafer at the same radius constant across the wafer, as seen in Figure 3.

$$V = L \cdot W \cdot H \tag{13}$$

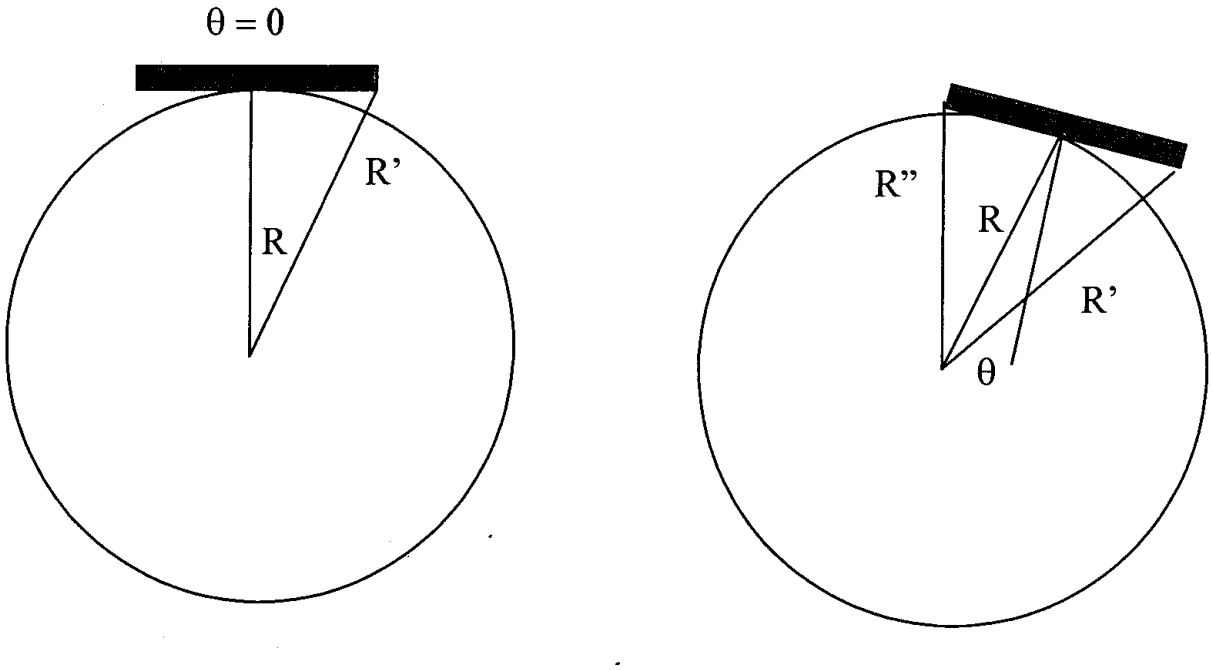


Figure 3: Geometry for a PVD Step

To determine the radius of the sphere, the law of cosines (Equation 14) is used. After finding the various radii for the sphere, the thickness of the deposited aluminum is the volume of the evaporated material divided by the surface area of the sphere (Equation 15).

$$r^2 = b^2 + c^2 - 2bc\sin(\theta) \tag{14}$$

$$A = 4\pi r^2 \tag{15}$$

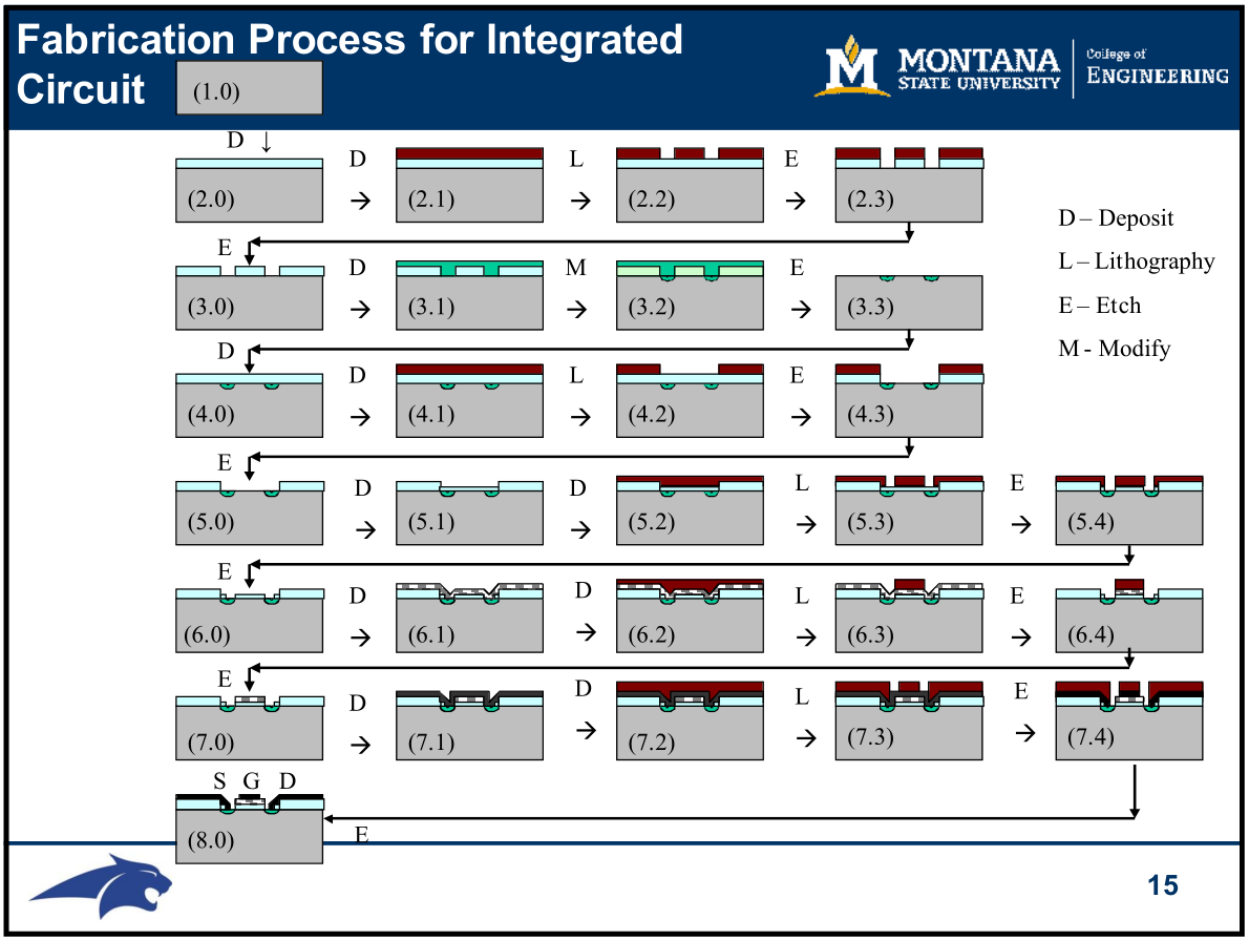


Figure 4: Fabrication Sequence for EELE407 Process [2]

1.2 Fabrication Sequence

The general sequence in CMOS fabrication is Oxidation, Photolithography, Deposition, Repeat. In this case, deposition refers to depositing any kind of material on the surface of the wafer, such as a dopant or conductor. Figure 4 shows the entire sequence for our process.

2 Analysis

2.1 Oxide Calculations

Table 1 shows our calculated values for the oxide over multiple areas of the wafer, after multiple oxidations. These values were calculated using the equations described in Section 1.1.2.

	t (Min)	T (°C)	Type (Wet/Dry)	Linear Coef. (B/A) (μm/hr)	Parabolic Coef. (B) (μm^2/hr)	(A) (μm)
1st Oxidation	240	1000	Wet	0.74226	0.31511	0.42453
	240	1000	Wet	0.74226	0.31511	0.42453
	240	1000	Wet	0.74226	0.31511	0.42453
	240	1000	Wet	0.74226	0.31511	0.42453
	240	1000	Wet	0.74226	0.31511	0.42453
2nd Oxidation	90	1000	Wet	0.74226	0.31511	0.42453
	90	1000	Wet	0.74226	0.31511	0.42453
	90	1000	Wet	0.74226	0.31511	0.42453
	90	1000	Wet	0.74226	0.31511	0.42453
	90	1000	Wet	0.74226	0.31511	0.42453
N-Well	90	1000	Wet	0.74226	0.31511	0.42453
3rd Oxidation	90	1050	Wet	1.50414	0.41226	0.27408
	90	1050	Wet	1.50414	0.41226	0.27408
	90	1050	Wet	1.50414	0.41226	0.27408
N-Well	90	1050	Wet	1.50414	0.41226	0.27408
N+	90	1050	Wet	1.50414	0.41226	0.27408
4th Oxidation	80	1050	Wet	1.50414	0.41226	0.27408
	80	1050	Wet	1.50414	0.41226	0.27408
	80	1050	Wet	1.50414	0.41226	0.27408
N-Well	80	1050	Wet	1.50414	0.41226	0.27408
N+	80	1050	Wet	1.50414	0.41226	0.27408
5th Oxidation	120	1000	Dry	0.04478	0.01042	0.23269
	120	1000	Dry	0.04478	0.01042	0.23269
	120	1000	Dry	0.04478	0.01042	0.23269
N-Well	120	1000	Dry	0.04478	0.01042	0.23269
N+	120	1000	Dry	0.04478	0.01042	0.23269
Gate Oxide	120	1000	Dry	0.04478	0.01042	0.23269

Table 1: Oxide Calculations

2.2 Diffusion Calculations

Tables 2, 3, and 4 show the calculated and measured values for the N^-, N^+, and P^+ diffusions after each step of our process. These values were calculated using the equations described in Section 1.1.1.

Constants	Value	Units
D_o	10.5	cm^2/s
E_A	3.69	eV
ρ	10	$\Omega \cdot cm$
k	8.62E-05	eV/°K
N_B (fig 4.8)	1.00E+15	cm^{-3}
N_{01} (fig 4.6) (Phosphorous)	3.00E+20	cm^{-3}
N_B/N_{01}	3.33E-06	
$erfc^{-1}(N_B/N_{01})$	3.29	

									Ervin Curve (fig 4.16a,b) Calculated	
	Step	Temp [°C]	Time [min]	D [cm^2/s]	Σ(Dt) [cm^2]	N_o [cm^{-3}]	x_j [cm]	Q [cm^{-2}]	$R_s \cdot x_j$ [Ω·μm]	R_s [Ω/□]
N^- Well	N- dep	800	20	4.89E-17	5.86E-14	3.00E+20	1.59E-06	8.20E+13		0.00
	drive in	1000	240	2.58E-14	3.72E-10	2.40E+18	1.08E-04		3.00E+02	278.82
	Oxidation	1000	90	2.58E-14	5.11E-10	2.05E+18	1.25E-04			0.00
	N+ Dep	900	60	1.47E-15	5.17E-10	2.03E+18	1.25E-04			0.00
	Oxidation	1050	90	9.21E-14	1.01E-09	1.45E+18	1.72E-04		4.00E+02	232.79
	P+ Dep	1000	120	2.58E-14	1.20E-09	1.34E+18	1.86E-04			0.00
	Drive in	1000	120	2.58E-14	1.39E-09	1.24E+18	1.99E-04		6.00E+02	301.93
	Wet	1050	80	9.21E-14	1.83E-09	1.08E+18	2.26E-04			0.00
	Dry	1000	120	2.58E-14	2.01E-09	1.03E+18	2.36E-04			0.00

Table 2: N^- Well Calculations

Constants	Value	Units
D_o	10.5	cm^2/s
E_A	3.69	eV
ρ	10	$\Omega \cdot cm$
k	8.62E-05	eV/°K
N_B (fig 4.8)	1.00E+15	cm^{-3}
N_{01} (fig 4.6) (Phosphorous)	3.00E+20	cm^{-3}
N_B/N_{01}	3.33E-06	
$erfc^{-1}(N_B/N_{01})$	3.29	

									Ervin Curve (fig 4.16a,b) Calculated	
	Step	Temp [°C]	Time [min]	D [cm^2/s]	Σ(Dt) [cm^2]	N_o [cm^{-3}]	x_j [cm]	Q [cm^{-2}]	$R_s \cdot x_j$ [Ω·μm]	R_s [Ω/□]
N^+ Source/Drain	N+ Dep	900	60	1.47E-15	5.28E-12	3.00E+20	1.51E-05	7.78E+14		0.00
	Oxidation	1050	90	9.21E-14	5.02E-10	1.96E+19	1.41E-04		1.25E+02	88.69
	P+ Dep	1000	120	2.58E-14	6.88E-10	1.67E+19	1.64E-04			0.00
	Drive in	1000	120	2.58E-14	8.74E-10	1.48E+19	1.83E-04		1.50E+02	81.84
	Wet	1050	80	9.21E-14	1.32E-09	1.21E+19	2.22E-04			0.00
	Dry	1000	120	2.58E-14	1.50E-09	1.13E+19	2.37E-04			0.00

Table 3: N^+ Source & Drain Calculations

Constants	Value	Units
D_o	10.5	cm^2/s
E_A	3.69	eV
ρ		Ω·cm
k	8.62E-05	eV/°K
N_B (fig 4.8)	1.34E+18	cm^{-3}
N_{01} (fig 4.6) (Boron)	2.00E+20	cm^{-3}
N_B/N_{01}	6.68E-03	
$erfc^{-1}(N_B/N_{01})$	1.92	

									Ervin Curve (fig 4.16c,d) Calculated	
	Step	Temp [°C]	Time [min]	D [cm^2/s]	Σ(Dt) [cm^2]	N_o [cm^{-3}]	x_j [cm]	Q [cm^{-2}]	$R_s \cdot x_j$ [Ω·μm]	R_s [Ω/□]
P^+ Source/Drain	P+ Dep	1000	120	2.58E-14	1.86E-10	2.00E+20	5.24E-05	3.08E+15		0.00
	Drive in	1000	120	2.58E-14	3.72E-10	9.00E+19	7.91E-05		2.00E+01	25.27
	Wet	1050	80	9.21E-14	8.14E-10	6.09E+19	1.12E-04			0.00
	Dry	1000	120	2.58E-14	1.00E-09	5.49E+19	1.22E-04			0.00

Table 4: P^+ Source & Drain Calculations

2.3 Resistor Calculations

The resistivity of a material or diffusion region can be determined from its geometry and resistance. In the case of a straight line, the number of squares in the resistor is as simple as dividing the length by the width. When 90° corners are added to the current path, however, an additional .56 square is added per corner. For the values in Table 5, a corresponding graph in Figure 5 is plotted, of the form in Equation 16. The slope of the line is the resistivity of the material, while the y-axis intercept is the contact resistance.

$$R = N_{sq} \cdot \rho + R_c \tag{16}$$

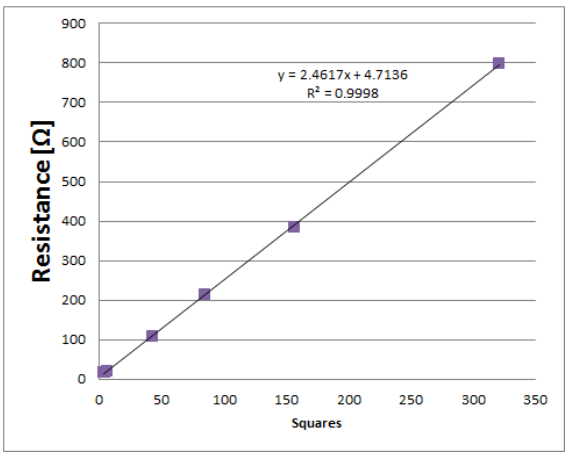
Length	Width	R	□
120	30	15.8	4.00
150	30	18.5	5.00
180	30	21.4	6.00
1300	30	109	43.33
2340	30	215	84.72
4700	30	383	156.67
8820	30	798	320.88

(a) Diffusion Resistors

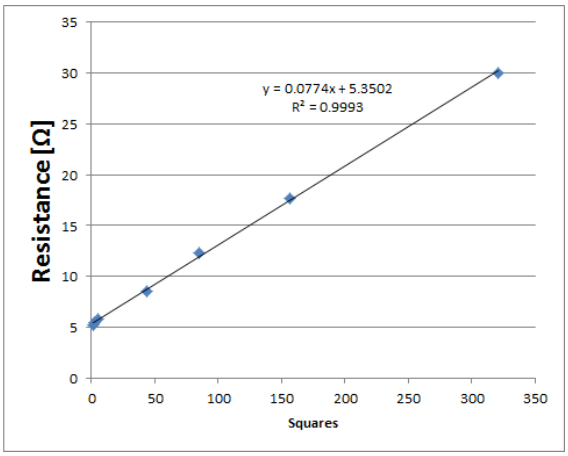
Length	Width	R	□
100	80	5.2	1.25
100	40	5.5	2.50
100	20	5.8	5.00
1300	30	8.5	43.33
2340	30	12.3	84.72
4700	30	17.7	156.67
8820	30	30	320.88

(b) Metal Resistors

Table 5: Squares Calculations given L, W, and R



(a) Diffusion Resistors



(b) Metal Resistors

Figure 5: Resistivity Calculations

2.4 PVD Calculation

Our source for the PVD step was a rolled up sheet of Al foil, measuring 40 cm^2 by 40 μm thick, for a total volume of .16 cm^3. The distance from the center of the PVD chamber to the center of a mounted wafer is 13 cm. Using geometric properties and Equation 14, we can find the distance from the center of the PVD chamber to the edges of the wafer, shown in Figure 3. Our calculations find r" to be 13.1 cm and r' to be 14.7 cm. Dividing the volume of our source by the surface area of our expanding sphere of gas, Equation 15, we calculate the thickness of the Al to be 753 nm at the center of the wafer, 589 nm at r', and 742 nm at r".

3 Measurements

3.1 Oxide Measurements

Table 6 shows the difference between the calculated and measured values of the oxide thickness, as well as the error between the calculation and measured values. Errors in the calculations can be explained by:

- Deviations from listed values (i.e. less or more time in the oxidation furnace, higher or lower temperature)
- Unaccounted for oxidation while the furnace is heating or cooling
- Natural oxide growth at room temperature
- Contamination of the wafer surface, inhibiting or accelerating oxidation

	Calculated Thickness (X_o) (µm)	Measured Thickness (X_o) (µm)	Error (%)
1st Oxidation	0.93032	0.68573	36%
	0.93032	0.72024	29%
	0.93032	0.71284	31%
	0.93032	0.67621	38%
	0.93032	0.72562	28%
2nd Oxidation	0.50727	0.41582	22%
	0.50727	0.41923	21%
	0.50727	0.41353	23%
	0.50727	0.42369	20%
	0.50727	0.43200	17%
N-Well	0.50727	0.48308	5%
3rd Oxidation	0.66119	0.48820	35%
	0.66119	0.48870	35%
	0.66119	0.48480	36%
N-Well	0.66119	0.50830	30%
N+	0.66119	0.56480	17%
4th Oxidation	0.61692	0.52310	18%
	0.61692	0.55910	10%
	0.61692	0.53510	15%
N-Well	0.61692	0.70690	-13%
N+	0.61692	0.59040	4%
5th Oxidation	0.70262	0.56620	24%
	0.70262	0.58310	20%
	0.70262	0.54020	30%
N-Well	0.70262	0.72360	-3%
N+	0.70262	0.61370	14%
Gate Oxide	0.08569	0.09580	-11%

Table 6: Oxide Thickness Measurements

3.2 Sheet Resistivity

Tables 7, 8, and 9 show the difference between our calculated and measured values of the sheet resistivity in the diffusion regions. Differences in measured and calculated values can be explained as:

- Deviations from listed values (i.e. less or more time in the diffusion furnace, higher or lower temperature)
- Unaccounted for diffusion while the furnace is heating or cooling
- Contamination of the wafer surface inhibiting diffusion

	Calculated			Measured	
Step	x_j [cm]	$R_s \cdot x_j[\Omega \cdot \mu m]$	R_s [$\Omega/\square$]	R_s [$\Omega/\square$]	x_j [cm]
N^- Deposition	1.08E-04	3.00E+02	278.82	29.765	1.01E-03
N^+ Deposition	1.72E-04	4.00E+02	232.79	34.75	1.15E-03
P^+ Deposition	1.99E-04	6.00E+02	301.93	56.55	1.06E-03

Table 7: N^- Well Measurements

	Calculated			Measured	
Step	x_j [cm]	$R_s \cdot x_j[\Omega \cdot \mu m]$	R_s [$\Omega/\square$]	R_s [$\Omega/\square$]	x_j [cm]
N^+ Deposition	1.41E-04	1.25E+02	88.69	28.1	4.45E-04
P^+ Deposition	1.83E-04	1.50E+02	81.84	2.675	5.61E-03

Table 8: N^+ Source & Drain Measurements

	Calculated			Measured	
Step	x_j [cm]	$R_s \cdot x_j[\Omega \cdot \mu m]$	R_s [$\Omega/\square$]	R_s [$\Omega/\square$]	x_j [cm]
P^+ Deposition	7.91E-05	2.00E+01	25.27	34.65	5.77E-05

Table 9: P^+ Source & Drain Measurements

3.3 Aluminum Thickness

Figure 6 shows the thickness of the aluminum on the surface of the wafer after etching. The thickness of the patterned aluminum is measured using a profilometer. The height of the aluminum and silicon are both averaged to removed local maximums and minimums, leading to a measured thickness of 417 nm of aluminum. This deviates from our worst case calculated value of 589 nm possibly because of:

- Loss of Al on the surface of the heating element
- Less Al was evaporated than in the calculation

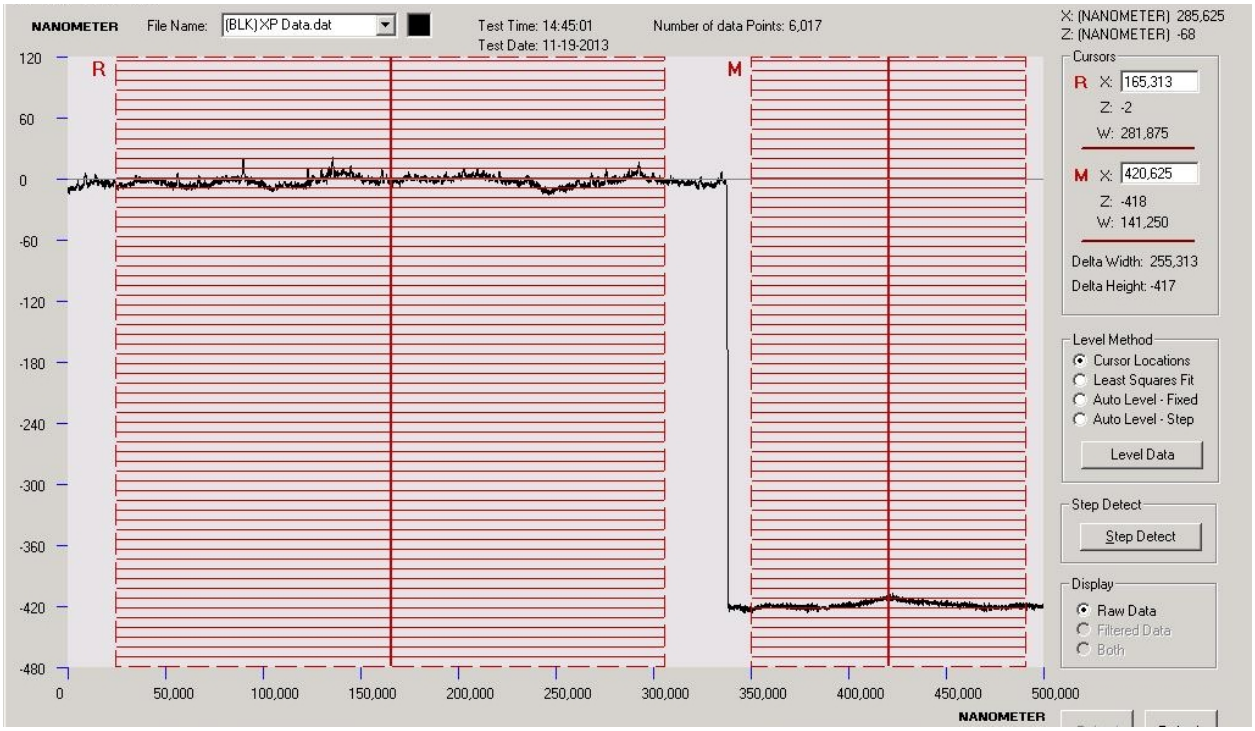
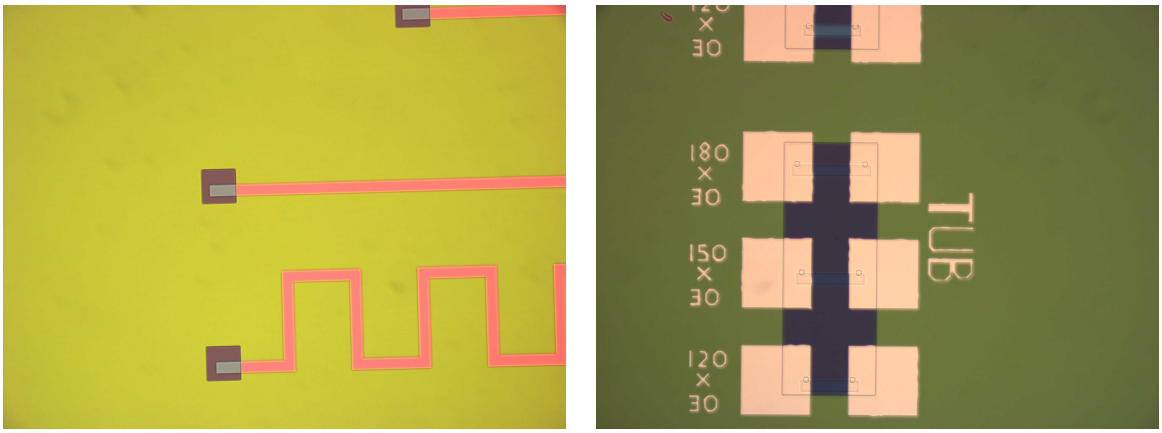


Figure 6: Aluminum Thickness

4 Device Testing

4.1 Resistors

Figure 7 shows resistors on the surface of our wafer before and after the Al Deposition step. Figures 8, 9, 10, and 11 show plots of $R(V)$ and $I(V)$. $R(V)$ could also be derived as the slope of $I(V)$.

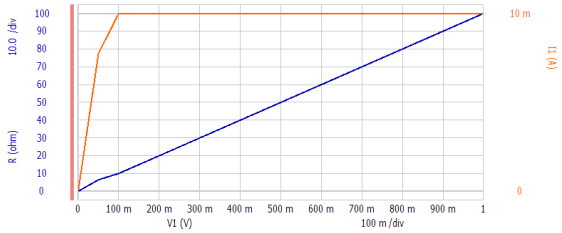


(a) Diffusion Resistors before Al Deposition (b) Diffusion Resistors after Al Deposition

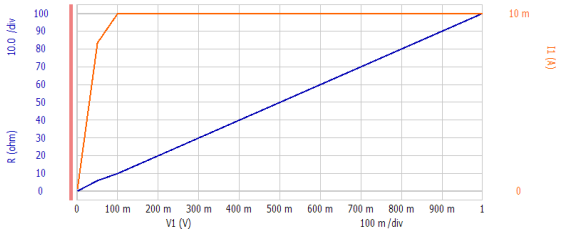
Figure 7: Captured Images of Resistors

4.1.1 Metal

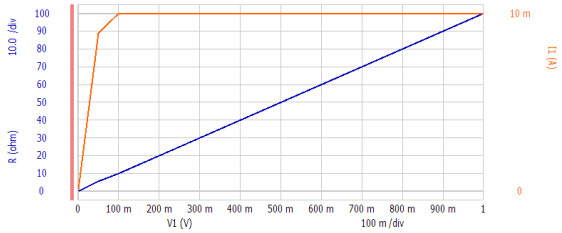
Of special note are the metal resistors. Due to the low impedance of the aluminum traces, the tester very quickly reaches its current limiting parameter of 100 mA. The resistance value displayed after this point is reached is not accurate. Instead, the true value of the resistor is the value when the slope of $R(V)$ is 0.



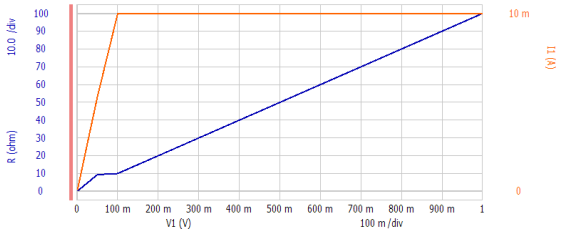
(a) 2.5 Ω Metal 100x20



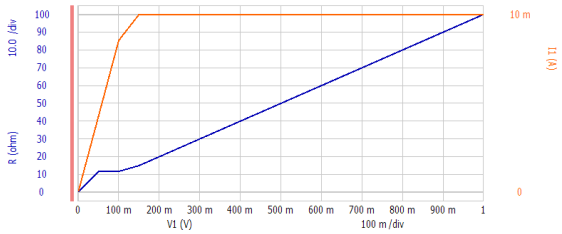
(b) 3.33 Ω Metal 100x40



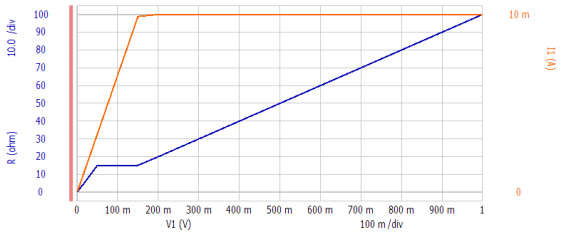
(c) 5 Ω Metal 100x80



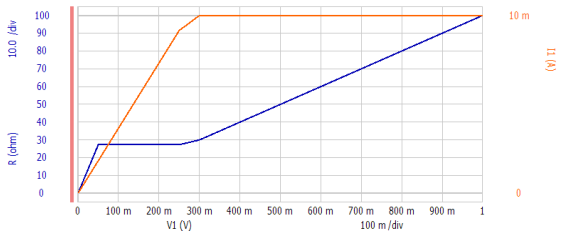
(d) 10 Ω Metal 1300x30



(e) 12.5 Ω Metal 2340x30



(f) 15 Ω Metal 4700x30

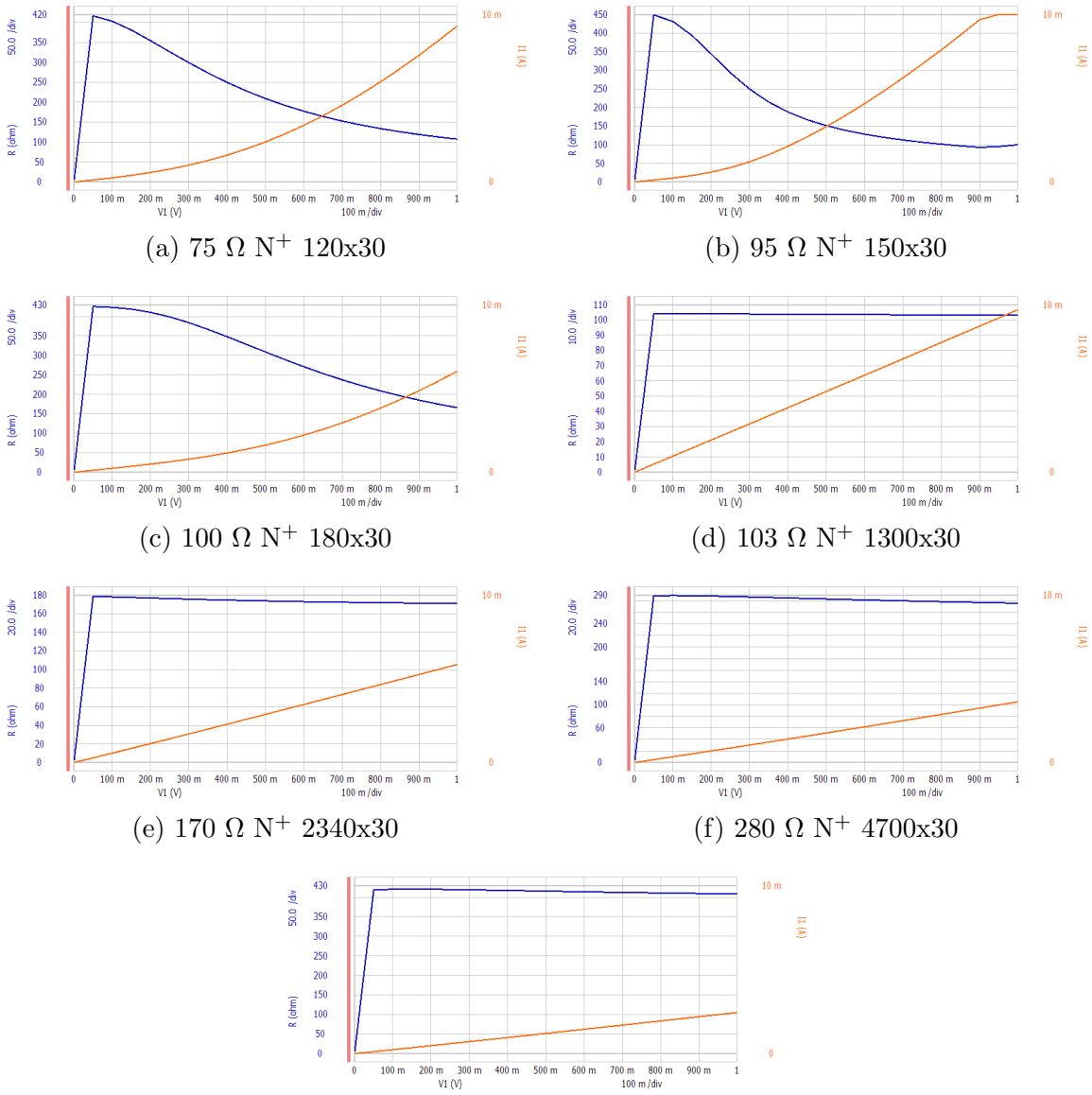


(g) 27.5 Ω Metal 8820x30

Figure 8: Metal Resistor Measurements

4.1.2 N^+

The resistance of the resistors in Figure 9 must be estimated in some cases, because the resistances never reach a steady state. In this case, it is easiest to estimate the slope of the current plot.



(a) 75 Ω N^+ 120x30

(b) 95 Ω N^+ 150x30

(c) 100 Ω N^+ 180x30

(d) 103 Ω N^+ 1300x30

(e) 170 Ω N^+ 2340x30

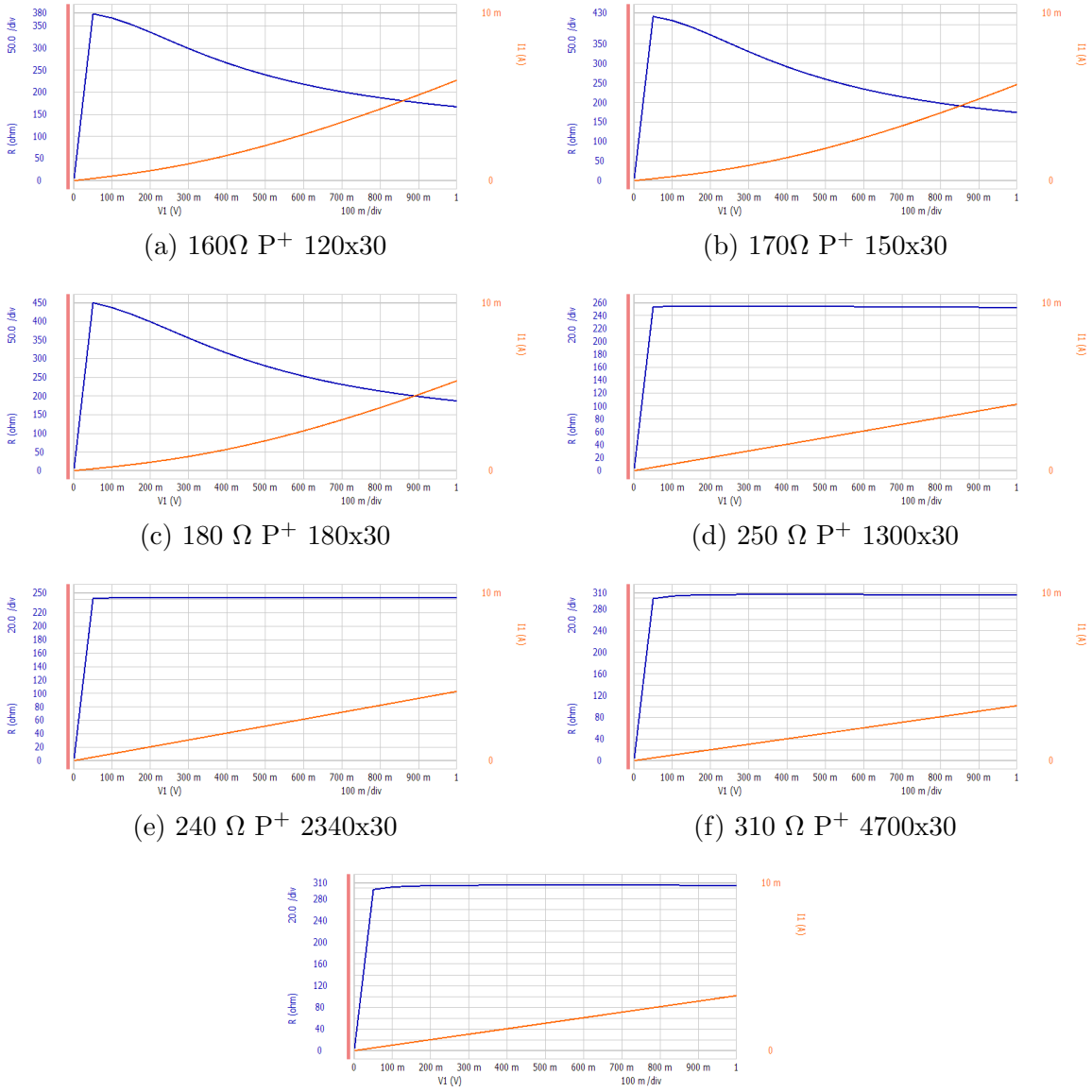
(f) 280 Ω N^+ 4700x30

(g) 410 Ω N^+ 8820x30

Figure 9: N^+ Resistor Measurements

4.1.3 P^+

The 2340x30 resistor in Figure 10 should have greater resistance than the 1300x30 resistor because of its increased length. The same holds true for the 8820x30 resistor compared to the 4700x30 resistor. These discrepancies may be the result of contamination on the wafer, or an increased contact resistance between the resistors.



(a) 160Ω P^+ 120x30

(b) 170Ω P^+ 150x30

(c) 180 Ω P^+ 180x30

(d) 250 Ω P^+ 1300x30

(e) 240 Ω P^+ 2340x30

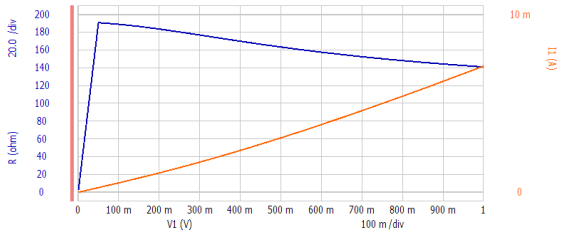
(f) 310 Ω P^+ 4700x30

(g) 310 Ω P^+ 8820x30

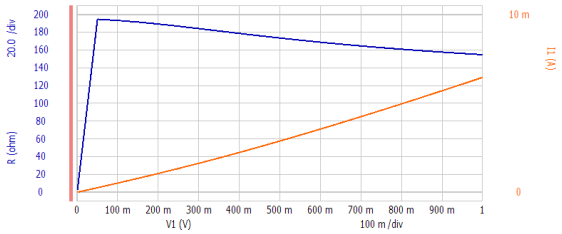
Figure 10: P^+ Resistor Measurements

4.1.4 N^- Well (Tub)

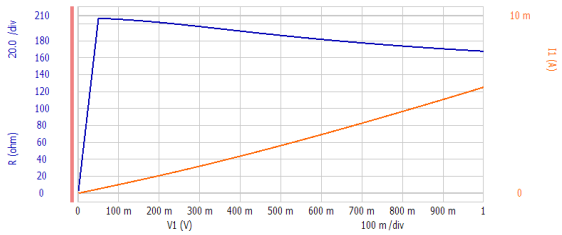
The N^- Well resistors have some of the same discrepancies as the P^+ resistors, likely for the same reasons, such as wafer contamination or contact resistance.



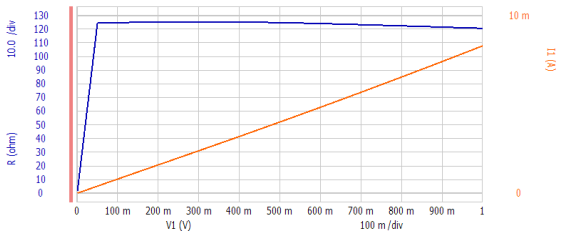
(a) 140 Ω N^- 120x30



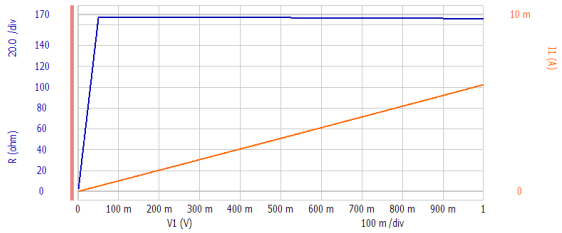
(b) 155 Ω N^- 150x30



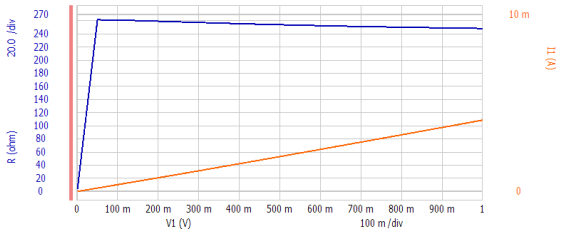
(c) 165 Ω N^- 180x30



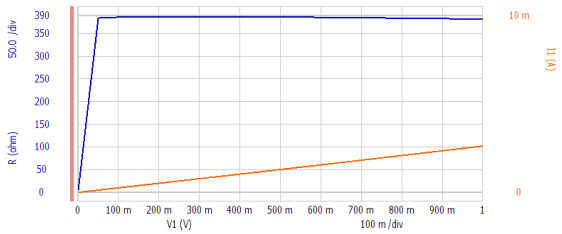
(d) 120 Ω N^- 1300x30



(e) 165 Ω N^- 2340x30



(f) 250 Ω N^- 4700x30



(g) 385 Ω N^- 8820x30

Figure 11: N^- Resistor Measurements

4.2 Diodes

Figure 12 shows some of the diodes created in our process. Figures 13 and 14 show plots for both the 1 diffusion and 2 diffusion diodes.

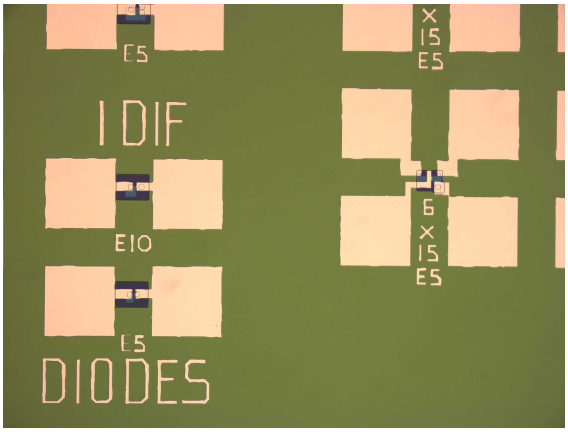
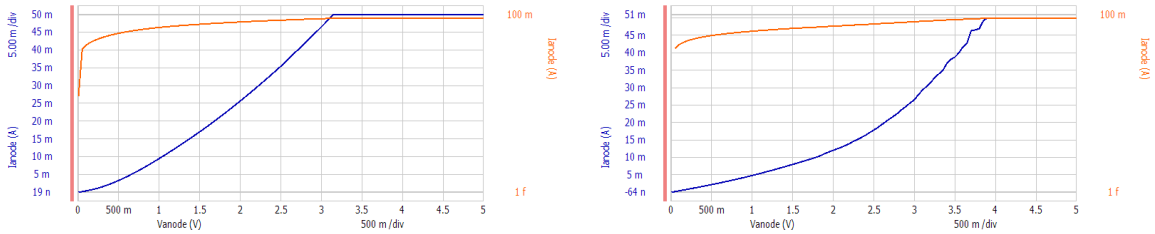


Figure 12: Captured Image of Diodes

4.2.1 1 Diffusion

The 1 diffusion diodes in both the N^- and P^+ regions are very similar. The P^+ diode is the closer of the two to an ideal diode, as it has the steeper growth, but the N^- diode still closely matches what we expect of a diode.



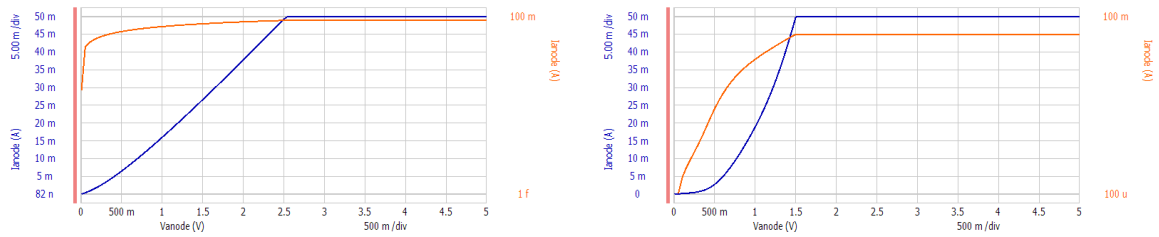
(a) N^- 1 Diffusion Diode

(b) P^+ 1 Diffusion Diode

Figure 13: 1 Diffusion Diodes

4.2.2 2 Diffusion

For the 2 diffusion diodes, the N^- diode closely resembles the 1 diffusion diode. The P^+ diode however has a much steeper curve and a much earlier threshold voltage, closely matching what we expect of a real diode. This steeper curve is due to a comparatively lower resistance in the diode structure.

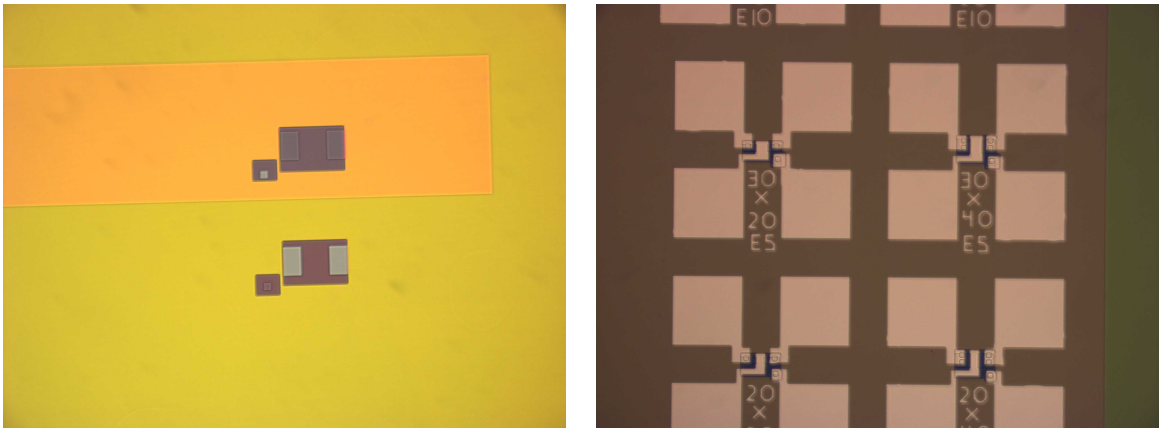


(a) N^- 2 Diffusion Diode (b) P^+ 2 Diffusion Diode

Figure 14: 2 Diffusion Diodes

4.3 Transistors

Figure 15 shows our transistors before and after the Al deposition step.



(a) Transistors before Al Deposition (b) Transistors after Al Deposition

Figure 15: Capture Images of Transistors

4.3.1 NMOS

Unfortunately, I was unable to find any working NMOS transistors on the entire wafer. The transistor operates the same regardless of the gate bias voltage. As can be seen in Figure 16, the transistor response most closely resembles a diode with an extremely high threshold voltage, at which point the current quickly reaches the tester's current limit. As we can clearly see the presence of Al over the gate region of the transistor, the gate oxide must be much thicker than expected.

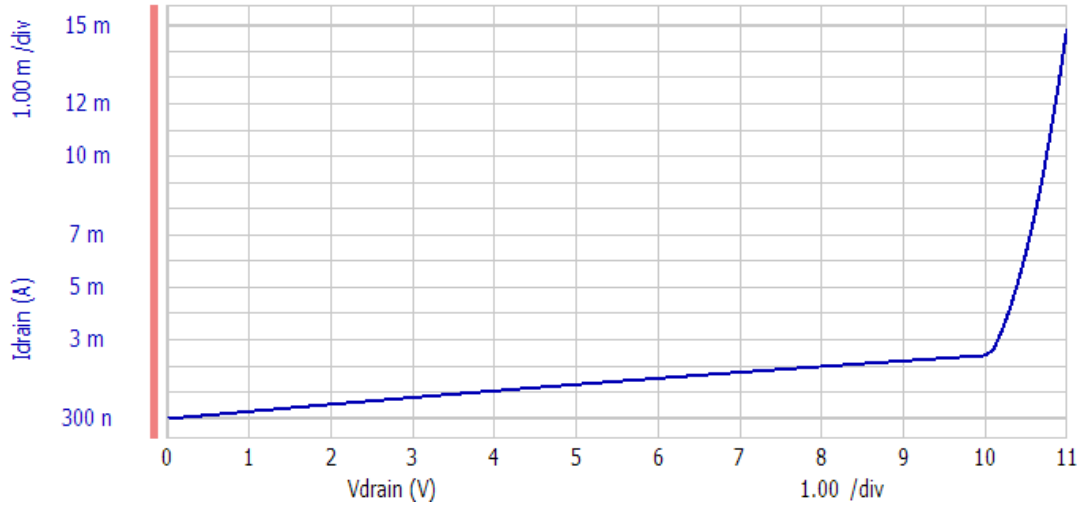


Figure 16: A NMOS transistor 190x160

4.3.2 PMOS

Similar to the NMOS transistors, I was unable to find any working PMOS transistors, and the gate bias voltage has no effect on their operation. As can be seen in Figure 17, the transistor response most closely resembles a resistor of approximately 62.5 Ω. The resistor behavior could be explained by extreme lateral diffusion, connecting the source and drain diffusions together. This would also theoretically negate the any gate bias, though it is like that the gate oxide is the same thickness as on the NMOS transistors.

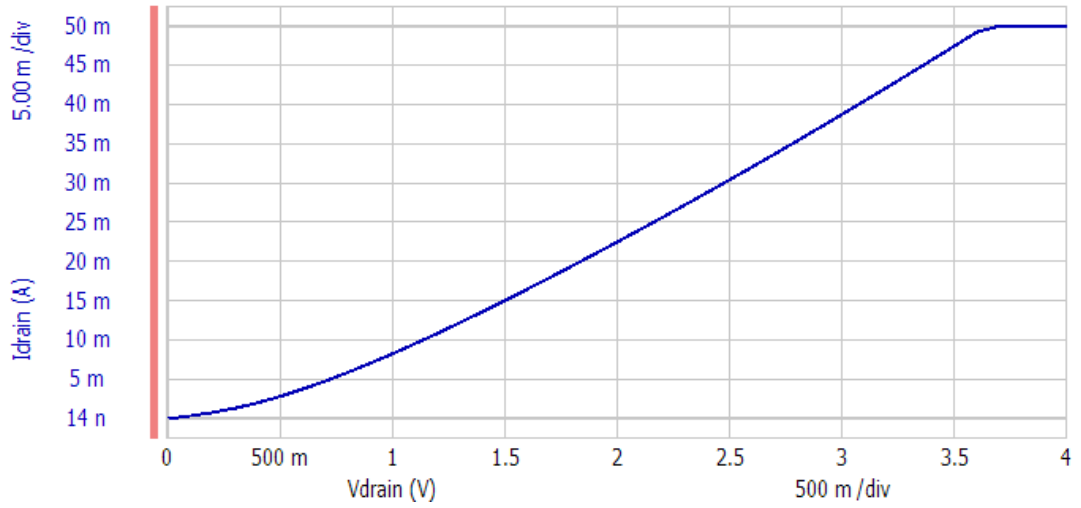


Figure 17: A PMOS transistor 190x160

5 Results

As previously stated in Section 4.3, there were no working transistors on the wafer. This is likely due to a thicker than expected gate oxide. Whether the oxide is too thick because we did not manage to strip away the field oxide before growing the gate oxide or the gate oxidation was insufficient is unknown. The PMOS transistors also behaved as resistors, suggesting that the P^+ Source and Drain were connected. This effect may be due to excess lateral diffusion of the P^+ dopant.

5.1 Recommendations

The PMOS errors could have been due to the 'experiment' of this year's class. Our lab section used 10 min of Nitrogen followed by 10 min of Oxygen during the deposition of the N^- well. Traditionally, the PMOS transistors have been difficult to make work, so further experimentation is the recommended course of action.

Personally, I wasn't sure what I was looking for whenever we looked at the wafer until the aluminum was deposited. Similar to how the entire process (N^- well, N^+ Source & Drain, P^+ Source & Drain, Gate, Contacts) is often repeated in class, it might be helpful to throw up a picture of the wafer/die before lab sections so students might understand what they are looking at under a microscope.

References

[1] Richard C. Jaeger. *Introduction to microelectronic Fabrication*. Ed. by Gerold W. Neudeck and Robert F. Pierret. 2nd ed. Vol. V. Prentice Hall, 2002.

[2] Dr. Todd J. Kaiser. *EELE407 Introduction to Microfabrication Lecture 12: Fabrication Sequence*. Montana State University.

[3] Matthew Leone and Todd Kaiser. *CMOS Lab Manual*. 3rd ed. Montana State University. Aug. 2012.

[4] *Microposit S1800 Series Photo Resists*. Shipley.