```
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| Tool Version     : Vivado v.2024.2 (win64) Build 5239630 Fri Nov 08 22:35:27 MST 2024
| Date             : Fri Mar 21 00:56:26 2025
| Host             : LAPTOP-Q3O6V45S running 64-bit major release  (build 9200)
| Command          : report_power -file microprocessor1_power_routed.rpt -pb microprocessor1_power_summary_routed.pb -rpx microprocessor1_power_routed.rpx
| Design           : microprocessor1
| Device           : xc7a200tfbg676-2
| Design State     : routed
| Grade            : commercial
| Process          : typical
| Characterization : Production
------------------------------------------------------------------------------------
```

Power Report

Table of Contents

1. Summary

Total On-Chip Power (W)	54.626 (Junction temp exceeded!)
Design Power Budget (W)	Unspecified*
Power Budget Margin (W)	NA
Dynamic (W)	52.951
Device Static (W)	1.674
Effective TJA (C/W)	1.9
Max Ambient (C)	0.0
Junction Temperature (C)	125.0
Confidence Level	Low

Setting File	---
Simulation Activity File	---
Design Nets Matched	NA

* Specify Design Power Budget using, set_operating_conditions -design_power_budget <value in Watts>

1.1 On-Chip Components

On-Chip	Power (W)	Used	Available	Utilization (%)
Slice Logic	2.397	1224	---	---
LUT as Logic	1.833	516	133800	0.39
Register	0.212	446	267600	0.17
CARRY4	0.209	51	33450	0.15
LUT as Distributed RAM	0.137	44	46200	0.10
BUFG	0.006	1	32	3.13
Others	0.000	2	---	---
Signals	5.794	1040	---	---
I/O	44.761	164	400	41.00
Static Power	1.674			
Total	54.626			

1.2 Power Supply Summary

Source	Voltage (V)	Total (A)	Dynamic (A)	Static (A)	Powerup (A)	Budget (A)	Margin (A)
Vccint	1.000	9.661	8.451	1.210	NA	Unspecified	NA
Vccaux	1.800	3.849	3.643	0.206	NA	Unspecified	NA
Vcco33	3.300	0.000	0.000	0.000	NA	Unspecified	NA
Vcco25	2.500	0.000	0.000	0.000	NA	Unspecified	NA
Vcco18	1.800	21.085	21.080	0.005	NA		

Unspecified	NA
Vcco15	1.500	0.000	0.000	0.000	NA	Unspecified	NA
Vcco135	1.350	0.000	0.000	0.000	NA	Unspecified	NA
Vcco12	1.200	0.000	0.000	0.000	NA	Unspecified	NA
Vccaux_io	1.800	0.000	0.000	0.000	NA	Unspecified	NA
Vccbram	1.000	0.048	0.000	0.048	NA	Unspecified	NA
MGTAVcc	1.000	0.000	0.000	0.000	NA	Unspecified	NA
MGTAVtt	1.200	0.000	0.000	0.000	NA	Unspecified	NA
Vccadc	1.800	0.020	0.000	0.020	NA	Unspecified	NA

1.3 Confidence Level

User Input Data	Confidence	Details	Action
Design implementation state	High	Design is routed	
Clock nodes activity	Low	User specified less than 75% of clocks	Provide missing clock activity with a constraint file, simulation results or by editing the "By Clock Domain" view
I/O nodes activity	Low	More than 75% of inputs are missing user specification	Provide missing input activity with simulation results or by editing the "By Resource Type -> I/Os" view
Internal nodes activity	Medium	User specified less than 25% of internal nodes	Provide missing internal nodes activity with simulation results or by editing the "By Resource Type" views
Device models	High	Device models are Production	

Overall confidence level	Low	

2. Settings

2.1 Environment

Ambient Temp (C)	25.0
ThetaJA (C/W)	1.9
Airflow (LFM)	250
Heat Sink	medium (Medium Profile)
ThetaSA (C/W)	3.4
Board Selection	medium (10"x10")
# of Board Layers	12to15 (12 to 15 Layers)
Board Temperature (C)	25.0

2.2 Clock Constraints

Clock	Domain	Constraint (ns)

3. Detailed Reports

3.1 By Hierarchy

Name	Power (W)
microprocessor1	52.951
regfile_reg_r1_0_31_0_5	0.015
regfile_reg_r1_0_31_12_17	0.019
regfile_reg_r1_0_31_18_23	0.019
regfile_reg_r1_0_31_24_29	0.019
regfile_reg_r1_0_31_30_31	0.005
regfile_reg_r1_0_31_30_31__0	0.005
regfile_reg_r1_0_31_6_11	0.018
regfile_reg_r2_0_31_0_5	0.017
regfile_reg_r2_0_31_12_17	0.018
regfile_reg_r2_0_31_18_23	0.024
regfile_reg_r2_0_31_24_29	0.023
regfile_reg_r2_0_31_30_31	0.005
regfile_reg_r2_0_31_30_31__0	0.004
regfile_reg_r2_0_31_6_11	0.020