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| Tool Version : Vivado v.2024.2 (win64) Build 5239630 Fri Nov 08 22:35:27 MST 2024
| Date         : Fri Mar 21 00:48:25 2025
| Host         : LAPTOP-Q3O6V45S running 64-bit major release  (build 9200)
| Command      : report_utilization -file microprocessor1_utilization_synth.rpt -pb
microprocessor1_utilization_synth.pb
| Design       : microprocessor1
| Device       : xc7a200tfbg676-2
| Speed File   : -2
| Design State : Synthesized
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Utilization Design Information

Table of Contents

1. Slice Logic

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs*	574	0	0	134600	0.43
LUT as Logic	526	0	0	134600	0.39
LUT as Memory	48	0	0	46200	0.10
LUT as Distributed RAM	48	0			
LUT as Shift Register	0	0			
Slice Registers	413	0	0	269200	0.15
Register as Flip Flop	413	0	0	269200	0.15
Register as Latch	0	0	0	269200	0.00
F7 Muxes	0	0	0	67300	0.00

| F8 Muxes | 0 | 0 | 0 | 33650 | 0.00 |
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* Warning! The Final LUT count, after physical optimizations and full implementation, is typically lower. Run opt_design after synthesis, if not already completed, for a more realistic count.
Warning! LUT value is adjusted to account for LUT combining.
Warning! For any ECO changes, please run place_design if there are unplaced instances

1.1 Summary of Registers by Type

Total	Clock Enable	Synchronous	Asynchronous
0	_	-	-
0	_	-	Set
0	_	-	Reset
0	_	Set	-
0	_	Reset	-
0	Yes	-	-
0	Yes	-	Set
413	Yes	-	Reset
0	Yes	Set	-
0	Yes	Reset	-

2. Memory

Site Type	Used	Fixed	Prohibited	Available	Util%
Block RAM Tile	0	0	0	365	0.00
RAMB36/FIFO*	0	0	0	365	0.00
RAMB18	0	0	0	730	0.00

* Note: Each Block RAM Tile only has one FIFO logic available and therefore can accommodate only one FIFO36E1 or one FIFO18E1. However, if a FIFO18E1 occupies a Block RAM Tile, that tile can still accommodate a RAMB18E1

3. DSP

Site Type	Used	Fixed	Prohibited	Available	Util%
DSPs	0	0	0	740	0.00

4. IO and GT Specific

Site Type	Used	Fixed	Prohibited	Available	Util%
Bonded IOB	164	0	0	400	41.00
Bonded IPADs	0	0	0	26	0.00
Bonded OPADs	0	0	0	16	0.00
PHY_CONTROL	0	0	0	10	0.00
PHASER_REF	0	0	0	10	0.00
OUT_FIFO	0	0	0	40	0.00
IN_FIFO	0	0	0	40	0.00
IDELAYCTRL	0	0	0	10	0.00
IBUFDS	0	0	0	384	0.00
GTPE2_CHANNEL	0	0	0	8	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	0	40	0.00
PHASER_IN/PHASER_IN_PHY	0	0	0	40	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	0	500	0.00
IBUFDS_GTE2	0	0	0	4	0.00
ILOGIC	0	0	0	400	0.00
OLOGIC	0	0	0	400	0.00

5. Clocking

Site Type	Used	Fixed	Prohibited	Available	Util%
BUFGCTRL	1	0	0	32	3.13
BUFIO	0	0	0	40	0.00
MMCME2_ADV	0	0	0	10	0.00
PLLE2_ADV	0	0	0	10	0.00
BUFMRCE	0	0	0	20	0.00
BUFHCE	0	0	0	120	0.00
BUFR	0	0	0	40	0.00

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6. Specific Feature

Site Type	Used	Fixed	Prohibited	Available	Util%
BSCANE2	0	0	0	4	0.00
CAPTUREE2	0	0	0	1	0.00
DNA_PORT	0	0	0	1	0.00
EFUSE_USR	0	0	0	1	0.00
FRAME_ECCE2	0	0	0	1	0.00
ICAPE2	0	0	0	2	0.00
PCIE_2_1	0	0	0	1	0.00
STARTUPE2	0	0	0	1	0.00
XADC	0	0	0	1	0.00

7. Primitives

Ref Name	Used	Functional Category
FDCE	413	Flop & Latch
LUT2	294	LUT
LUT6	128	LUT
LUT5	124	LUT
OBUF	98	IO
RAMD32	68	Distributed Memory
IBUF	66	IO
CARRY4	51	CarryLogic
LUT3	47	LUT
LUT4	41	LUT
RAMS32	20	Distributed Memory
LUT1	2	LUT
BUFG	1	Clock

8. Black Boxes

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| Ref Name | Used |
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9. Instantiated Netlists

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| Ref Name | Used |
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