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| Tool Version : Vivado v.2024.2 (win64) Build 5239630 Fri Nov 08 22:35:27 MST 2024
| Date         : Fri Mar 21 00:56:25 2025
| Host         : LAPTOP-Q3O6V45S running 64-bit major release  (build 9200)
| Command      : report_timing_summary -max_paths 10 -report_unconstrained -file
microprocessor1_timing_summary_routed.rpt -pb
microprocessor1_timing_summary_routed.pb -rpx
microprocessor1_timing_summary_routed.rpx -warn_on_violation
| Design       : microprocessor1
| Device       : 7a200t-fbg676
| Speed File   : -2  PRODUCTION 1.23 2018-06-13
| Design State : Routed
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Timing Summary Report

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| Timer Settings
| --------------
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  Enable Multi Corner Analysis               :  Yes
  Enable Pessimism Removal                   :  Yes
  Pessimism Removal Resolution               :  Nearest Common Node
  Enable Input Delay Default Clock           :  No
  Enable Preset / Clear Arcs                 :  No
  Disable Flight Delays                      :  No
  Ignore I/O Paths                           :  No
  Timing Early Launch at Borrowing Latches   :  No
  Borrow Time for Max Delay Exceptions       :  Yes
  Merge Timing Exceptions                    :  Yes
  Inter-SLR Compensation                     :  Conservative

  Corner  Analyze    Analyze
  Name    Max Paths  Min Paths
  ------  ---------  ---------
  Slow    Yes        Yes
  Fast    Yes        Yes
```

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| Report Methodology
| ------------------
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Rule       Severity          Description                  Violations
---------  ----------------  ---------------------------  ----------
TIMING-17  Critical Warning  Non-clocked sequential cell  534

Note: This report is based on the most recent report_methodology run and may not be
up-to-date. Run report_methodology on the current design for the latest report.



check_timing report

Table of Contents
-----------------
1. checking no_clock (534)
2. checking constant_clock (0)
3. checking pulse_width_clock (0)
4. checking unconstrained_internal_endpoints (1488)
5. checking no_input_delay (65)
6. checking no_output_delay (98)
7. checking multiple_clock (0)
8. checking generated_clocks (0)
9. checking loops (0)
10. checking partial_input_delay (0)
11. checking partial_output_delay (0)
12. checking latch_loops (0)

1. checking no_clock (534)
--------------------------
 There are 534 register/latch pins with no clock driven by root clock pin: clk
(HIGH)


2. checking constant_clock (0)
------------------------------
 There are 0 register/latch pins with constant_clock.
```

3. checking pulse_width_clock (0)

 There are 0 register/latch pins which need pulse_width check

4. checking unconstrained_internal_endpoints (1488)

 There are 1488 pins that are not constrained for maximum delay. (HIGH)

 There are 0 pins that are not constrained for maximum delay due to constant clock.

5. checking no_input_delay (65)

 There are 65 input ports with no input delay specified. (HIGH)

 There are 0 input ports with no input delay but user has a false path constraint.

6. checking no_output_delay (98)

 There are 98 ports with no output delay specified. (HIGH)

 There are 0 ports with no output delay but user has a false path constraint

 There are 0 ports with no output delay but with a timing clock defined on it or propagating through it

7. checking multiple_clock (0)

 There are 0 register/latch pins with multiple clocks.

8. checking generated_clocks (0)

 There are 0 generated clocks that are not connected to a clock source.

9. checking loops (0)

 There are 0 combinational loops in the design.

10. checking partial_input_delay (0)

There are 0 input ports with partial input delay specified.

11. checking partial_output_delay (0)

There are 0 ports with partial output delay specified.

12. checking latch_loops (0)

There are 0 combinational latch loops in the design through latch input

---
| Design Timing Summary
| ---

WNS(ns)	TNS(ns)	TNS Failing Endpoints	TNS Total Endpoints	WHS(ns)	THS(ns)	THS Failing Endpoints	THS Total Endpoints	WPWS(ns)	TPWS(ns)	TPWS Failing Endpoints	TPWS Total Endpoints
inf	0.000	0	1586	inf	0.000	0	1586	NA	NA	NA	NA

There are no user specified timing constraints.

| Clock Summary
| ---

| Intra Clock Table

| ----------------

Clock WNS(ns) TNS(ns) TNS Failing Endpoints TNS Total Endpoints
WHS(ns) THS(ns) THS Failing Endpoints THS Total Endpoints WPWS(ns)
TPWS(ns) TPWS Failing Endpoints TPWS Total Endpoints
----- ------- ------- ---------- ----------
------- ------- ---------- ---------- --------
-------- ---------- ----------

| Inter Clock Table
| ----------------

From Clock To Clock WNS(ns) TNS(ns) TNS Failing Endpoints TNS
Total Endpoints WHS(ns) THS(ns) THS Failing Endpoints THS Total
Endpoints
---------- -------- ------- ------- ----------
---------- ------- ------- ----------

| Other Path Groups Table
| ----------------------

Path Group From Clock To Clock WNS(ns) TNS(ns) TNS Failing
Endpoints TNS Total Endpoints WHS(ns) THS(ns) THS Failing Endpoints THS
Total Endpoints
---------- ---------- -------- ------- -------
---------- ---------- ------- -------
---------- ----------

| User Ignored Path Table
| ----------------------

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------------------------------------------------------------------------------
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Path Group    From Clock    To Clock
----------    ----------    --------



------------------------------------------------------------------------------
------------
| Unconstrained Path Table
| ------------------------
------------------------------------------------------------------------------
------------

Path Group    From Clock    To Clock
----------    ----------    --------
(none)



------------------------------------------------------------------------------
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| Timing Details
| --------------
------------------------------------------------------------------------------
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------------------------------------------------------------------------------
--
Path Group:  (none)
From Clock:
  To Clock:

Max Delay          1586 Endpoints
Min Delay          1586 Endpoints
------------------------------------------------------------------------------
--



Max Delay Paths
------------------------------------------------------------------------------
--
Slack:                    inf
  Source:                 ex_mem_jump_reg/C
                            (rising edge-triggered cell FDCE)
  Destination:            mem_re
```

```
                          (output port)
  Path Group:             (none)
  Path Type:              Max at Slow Process Corner
  Data Path Delay:        12.625ns  (logic 2.983ns (23.632%)  route 9.641ns
(76.368%))
  Logic Levels:           4  (FDCE=1 LUT3=2 OBUF=1)

    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  -------------------------------------------------------------------
------------------
    SLICE_X4Y122         FDCE                         0.000     0.000 r
ex_mem_jump_reg/C
    SLICE_X4Y122         FDCE (Prop_fdce_C_Q)         0.379     0.379 f
ex_mem_jump_reg/Q
                         net (fo=2, routed)           0.897     1.276    ex_mem_jump
    SLICE_X5Y118         LUT3 (Prop_lut3_I2_O)        0.105     1.381 f
mem_re_OBUF_inst_i_2/O
                         net (fo=120, routed)         2.066     3.447    pc1
    SLICE_X12Y131        LUT3 (Prop_lut3_I2_O)        0.105     3.552 r
mem_re_OBUF_inst_i_1/O
                         net (fo=1, routed)           6.678    10.230    mem_re_OBUF
    K2                   OBUF (Prop_obuf_I_O)         2.394    12.625 r
mem_re_OBUF_inst/O
                         net (fo=0)                   0.000    12.625    mem_re
    K2                                                              r  mem_re
(OUT)
  -------------------------------------------------------------------
------------------

Slack:                   inf
  Source:                rst
                          (input port)
  Destination:           id_ex_regWrite_reg/CLR
  Path Group:            (none)
  Path Type:             Max at Slow Process Corner
  Data Path Delay:       10.333ns  (logic 0.866ns (8.384%)  route 9.466ns
(91.616%))
  Logic Levels:          1  (IBUF=1)

    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  -------------------------------------------------------------------
------------------
    N8                                                0.000     0.000 f  rst (IN)
                         net (fo=0)                   0.000     0.000    rst
```

```
    N8                  IBUF (Prop_ibuf_I_O)         0.866     0.866 f
rst_IBUF_inst/O
                        net (fo=446, routed)         9.466    10.333    rst_IBUF
    SLICE_X4Y120        FDCE                                           f
id_ex_regWrite_reg/CLR
  -------------------------------------------------------------------
------------------

Slack:                    inf
  Source:                 rst
                            (input port)
  Destination:            id_ex_rs2_data_reg[0]/CLR
  Path Group:             (none)
  Path Type:              Max at Slow Process Corner
  Data Path Delay:        10.305ns  (logic 0.866ns (8.407%)  route 9.439ns
(91.593%))
  Logic Levels:           1  (IBUF=1)

    Location              Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  -------------------------------------------------------------------
------------------
    N8                                                0.000     0.000 f  rst (IN)
                        net (fo=0)                    0.000     0.000    rst
    N8                  IBUF (Prop_ibuf_I_O)         0.866     0.866 f
rst_IBUF_inst/O
                        net (fo=446, routed)         9.439    10.305    rst_IBUF
    SLICE_X3Y120        FDCE                                           f
id_ex_rs2_data_reg[0]/CLR
  -------------------------------------------------------------------
------------------

Slack:                    inf
  Source:                 rst
                            (input port)
  Destination:            if_id_instr_reg[10]/CLR
  Path Group:             (none)
  Path Type:              Max at Slow Process Corner
  Data Path Delay:        10.305ns  (logic 0.866ns (8.407%)  route 9.439ns
(91.593%))
  Logic Levels:           1  (IBUF=1)

    Location              Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  -------------------------------------------------------------------
------------------
```

```
    N8                                                0.000     0.000 f  rst (IN)
                         net (fo=0)                   0.000     0.000    rst
    N8                   IBUF (Prop_ibuf_I_O)         0.866     0.866 f
rst_IBUF_inst/O
                         net (fo=446, routed)         9.439    10.305    rst_IBUF
    SLICE_X3Y120         FDCE                                           f
if_id_instr_reg[10]/CLR
  ------------------------------------------------------------------
------------------

Slack:                    inf
  Source:                 rst
                            (input port)
  Destination:            if_id_instr_reg[11]/CLR
  Path Group:             (none)
  Path Type:              Max at Slow Process Corner
  Data Path Delay:        10.305ns  (logic 0.866ns (8.407%)  route 9.439ns
(91.593%))
  Logic Levels:           1  (IBUF=1)

    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  ------------------------------------------------------------------
------------------
    N8                                                0.000     0.000 f  rst (IN)
                         net (fo=0)                   0.000     0.000    rst
    N8                   IBUF (Prop_ibuf_I_O)         0.866     0.866 f
rst_IBUF_inst/O
                         net (fo=446, routed)         9.439    10.305    rst_IBUF
    SLICE_X3Y120         FDCE                                           f
if_id_instr_reg[11]/CLR
  ------------------------------------------------------------------
------------------

Slack:                    inf
  Source:                 rst
                            (input port)
  Destination:            if_id_instr_reg[12]/CLR
  Path Group:             (none)
  Path Type:              Max at Slow Process Corner
  Data Path Delay:        10.305ns  (logic 0.866ns (8.407%)  route 9.439ns
(91.593%))
  Logic Levels:           1  (IBUF=1)

    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
```

```
  ----------------------------------------------------------------
------------------
    N8                                                0.000     0.000 f  rst (IN)
                      net (fo=0)                      0.000     0.000    rst
    N8                IBUF (Prop_ibuf_I_O)            0.866     0.866 f
rst_IBUF_inst/O
                      net (fo=446, routed)            9.439    10.305    rst_IBUF
    SLICE_X3Y120      FDCE                                             f
if_id_instr_reg[12]/CLR
  ----------------------------------------------------------------
------------------

Slack:                  inf
  Source:               rst
                          (input port)
  Destination:          ex_mem_branch_target_reg[0]/CLR
  Path Group:           (none)
  Path Type:            Max at Slow Process Corner
  Data Path Delay:      10.248ns  (logic 0.866ns (8.453%)  route 9.382ns
(91.547%))
  Logic Levels:         1  (IBUF=1)

    Location            Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  ----------------------------------------------------------------
------------------
    N8                                                0.000     0.000 f  rst (IN)
                      net (fo=0)                      0.000     0.000    rst
    N8                IBUF (Prop_ibuf_I_O)            0.866     0.866 f
rst_IBUF_inst/O
                      net (fo=446, routed)            9.382    10.248    rst_IBUF
    SLICE_X10Y123     FDCE                                             f
ex_mem_branch_target_reg[0]/CLR
  ----------------------------------------------------------------
------------------

Slack:                  inf
  Source:               rst
                          (input port)
  Destination:          ex_mem_branch_target_reg[1]/CLR
  Path Group:           (none)
  Path Type:            Max at Slow Process Corner
  Data Path Delay:      10.248ns  (logic 0.866ns (8.453%)  route 9.382ns
(91.547%))
  Logic Levels:         1  (IBUF=1)
```

```
    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  -------------------------------------------------------------------
-------------------
    N8                                                0.000     0.000 f  rst (IN)
                         net (fo=0)                   0.000     0.000    rst
    N8                   IBUF (Prop_ibuf_I_O)         0.866     0.866 f
rst_IBUF_inst/O
                         net (fo=446, routed)         9.382    10.248    rst_IBUF
    SLICE_X10Y123        FDCE                                           f
ex_mem_branch_target_reg[1]/CLR
  -------------------------------------------------------------------
-------------------

Slack:                    inf
  Source:                 rst
                            (input port)
  Destination:            ex_mem_branch_target_reg[2]/CLR
  Path Group:             (none)
  Path Type:              Max at Slow Process Corner
  Data Path Delay:        10.248ns  (logic 0.866ns (8.453%)  route 9.382ns
(91.547%))
  Logic Levels:           1  (IBUF=1)

    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  -------------------------------------------------------------------
-------------------
    N8                                                0.000     0.000 f  rst (IN)
                         net (fo=0)                   0.000     0.000    rst
    N8                   IBUF (Prop_ibuf_I_O)         0.866     0.866 f
rst_IBUF_inst/O
                         net (fo=446, routed)         9.382    10.248    rst_IBUF
    SLICE_X10Y123        FDCE                                           f
ex_mem_branch_target_reg[2]/CLR
  -------------------------------------------------------------------
-------------------

Slack:                    inf
  Source:                 rst
                            (input port)
  Destination:            ex_mem_branch_target_reg[3]/CLR
  Path Group:             (none)
  Path Type:              Max at Slow Process Corner
  Data Path Delay:        10.248ns  (logic 0.866ns (8.453%)  route 9.382ns
(91.547%))
```

```
  Logic Levels:           1  (IBUF=1)

    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  -------------------------------------------------------------------
-------------------
    N8                                                0.000     0.000 f  rst (IN)
                         net (fo=0)                   0.000     0.000    rst
    N8                   IBUF (Prop_ibuf_I_O)         0.866     0.866 f
rst_IBUF_inst/O
                         net (fo=446, routed)         9.382    10.248    rst_IBUF
    SLICE_X10Y123        FDCE                                           f
ex_mem_branch_target_reg[3]/CLR
  -------------------------------------------------------------------
-------------------




Min Delay Paths
--------------------------------------------------------------------------------
--
Slack:                   inf
  Source:                id_ex_jalr_reg/C
                           (rising edge-triggered cell FDCE)
  Destination:           ex_mem_jalr_reg/D
  Path Group:            (none)
  Path Type:             Min at Fast Process Corner
  Data Path Delay:       0.208ns  (logic 0.141ns (67.807%)  route 0.067ns
(32.193%))
  Logic Levels:          1  (FDCE=1)

    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  -------------------------------------------------------------------
-------------------
    SLICE_X5Y118         FDCE                         0.000     0.000 r
id_ex_jalr_reg/C
    SLICE_X5Y118         FDCE (Prop_fdce_C_Q)         0.141     0.141 r
id_ex_jalr_reg/Q
                         net (fo=64, routed)          0.067     0.208
id_ex_jalr_reg_n_0
    SLICE_X5Y118         FDCE                                       r
ex_mem_jalr_reg/D
  -------------------------------------------------------------------
```

```
------------------

Slack:                    inf
  Source:                 ex_mem_ALUOut_reg[6]/C
                            (rising edge-triggered cell FDCE)
  Destination:            mem_wb_ALUOut_reg[6]/D
  Path Group:             (none)
  Path Type:              Min at Fast Process Corner
  Data Path Delay:        0.240ns  (logic 0.141ns (58.643%)  route 0.099ns
(41.357%))
  Logic Levels:           1  (FDCE=1)

    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  -------------------------------------------------------------------
------------------
    SLICE_X5Y128         FDCE                         0.000     0.000 r
ex_mem_ALUOut_reg[6]/C
    SLICE_X5Y128         FDCE (Prop_fdce_C_Q)         0.141     0.141 r
ex_mem_ALUOut_reg[6]/Q
                         net (fo=2, routed)           0.099     0.240
data_addr_OBUF[6]
    SLICE_X7Y128         FDCE                                       r
mem_wb_ALUOut_reg[6]/D
  -------------------------------------------------------------------
------------------

Slack:                    inf
  Source:                 ex_mem_ALUOut_reg[25]/C
                            (rising edge-triggered cell FDCE)
  Destination:            mem_wb_ALUOut_reg[25]/D
  Path Group:             (none)
  Path Type:              Min at Fast Process Corner
  Data Path Delay:        0.249ns  (logic 0.141ns (56.528%)  route 0.108ns
(43.472%))
  Logic Levels:           1  (FDCE=1)

    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  -------------------------------------------------------------------
------------------
    SLICE_X3Y135         FDCE                         0.000     0.000 r
ex_mem_ALUOut_reg[25]/C
    SLICE_X3Y135         FDCE (Prop_fdce_C_Q)         0.141     0.141 r
ex_mem_ALUOut_reg[25]/Q
                         net (fo=2, routed)           0.108     0.249
```

```
data_addr_OBUF[25]
    SLICE_X2Y135         FDCE                                          r
mem_wb_ALUOut_reg[25]/D
  -------------------------------------------------------------------
-------------------

Slack:                    inf
  Source:                 id_ex_rd_reg[4]/C
                            (rising edge-triggered cell FDCE)
  Destination:            ex_mem_rd_reg[4]/D
  Path Group:             (none)
  Path Type:              Min at Fast Process Corner
  Data Path Delay:        0.258ns  (logic 0.128ns (49.644%)  route 0.130ns
(50.356%))
  Logic Levels:           1  (FDCE=1)

    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  -------------------------------------------------------------------
-------------------
    SLICE_X4Y121         FDCE                         0.000     0.000 r
id_ex_rd_reg[4]/C
    SLICE_X4Y121         FDCE (Prop_fdce_C_Q)         0.128     0.128 r
id_ex_rd_reg[4]/Q
                         net (fo=2, routed)           0.130     0.258    id_ex_rd[4]
    SLICE_X2Y122         FDCE                                          r
ex_mem_rd_reg[4]/D
  -------------------------------------------------------------------
-------------------

Slack:                    inf
  Source:                 ex_mem_ALUOut_reg[21]/C
                            (rising edge-triggered cell FDCE)
  Destination:            mem_wb_ALUOut_reg[21]/D
  Path Group:             (none)
  Path Type:              Min at Fast Process Corner
  Data Path Delay:        0.260ns  (logic 0.141ns (54.255%)  route 0.119ns
(45.745%))
  Logic Levels:           1  (FDCE=1)

    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  -------------------------------------------------------------------
-------------------
    SLICE_X5Y132         FDCE                         0.000     0.000 r
ex_mem_ALUOut_reg[21]/C
```

```
    SLICE_X5Y132         FDCE (Prop_fdce_C_Q)         0.141     0.141 r
ex_mem_ALUOut_reg[21]/Q
                         net (fo=2, routed)           0.119     0.260
data_addr_OBUF[21]
    SLICE_X5Y132         FDCE                                       r
mem_wb_ALUOut_reg[21]/D
  -------------------------------------------------------------------
------------------

Slack:                    inf
  Source:                 ex_mem_ALUOut_reg[30]/C
                            (rising edge-triggered cell FDCE)
  Destination:            mem_wb_ALUOut_reg[30]/D
  Path Group:             (none)
  Path Type:              Min at Fast Process Corner
  Data Path Delay:        0.260ns  (logic 0.141ns (54.255%)  route 0.119ns
(45.745%))
  Logic Levels:           1  (FDCE=1)

    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  -------------------------------------------------------------------
------------------
    SLICE_X3Y136         FDCE                         0.000     0.000 r
ex_mem_ALUOut_reg[30]/C
    SLICE_X3Y136         FDCE (Prop_fdce_C_Q)         0.141     0.141 r
ex_mem_ALUOut_reg[30]/Q
                         net (fo=2, routed)           0.119     0.260
data_addr_OBUF[30]
    SLICE_X3Y136         FDCE                                       r
mem_wb_ALUOut_reg[30]/D
  -------------------------------------------------------------------
------------------

Slack:                    inf
  Source:                 ex_mem_ALUOut_reg[15]/C
                            (rising edge-triggered cell FDCE)
  Destination:            mem_wb_ALUOut_reg[15]/D
  Path Group:             (none)
  Path Type:              Min at Fast Process Corner
  Data Path Delay:        0.261ns  (logic 0.141ns (54.005%)  route 0.120ns
(45.995%))
  Logic Levels:           1  (FDCE=1)

    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
```

```
  ---------------------------------------------------------------------
-------------------
    SLICE_X4Y129         FDCE                           0.000     0.000 r
ex_mem_ALUOut_reg[15]/C
    SLICE_X4Y129         FDCE (Prop_fdce_C_Q)           0.141     0.141 r
ex_mem_ALUOut_reg[15]/Q
                         net (fo=2, routed)             0.120     0.261
data_addr_OBUF[15]
    SLICE_X4Y130         FDCE                                       r
mem_wb_ALUOut_reg[15]/D
  ---------------------------------------------------------------------
-------------------

Slack:                    inf
  Source:                 ex_mem_ALUOut_reg[16]/C
                            (rising edge-triggered cell FDCE)
  Destination:            mem_wb_ALUOut_reg[16]/D
  Path Group:             (none)
  Path Type:              Min at Fast Process Corner
  Data Path Delay:        0.262ns  (logic 0.141ns (53.783%)  route 0.121ns
(46.217%))
  Logic Levels:           1  (FDCE=1)

    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  ---------------------------------------------------------------------
-------------------
    SLICE_X4Y129         FDCE                           0.000     0.000 r
ex_mem_ALUOut_reg[16]/C
    SLICE_X4Y129         FDCE (Prop_fdce_C_Q)           0.141     0.141 r
ex_mem_ALUOut_reg[16]/Q
                         net (fo=2, routed)             0.121     0.262
data_addr_OBUF[16]
    SLICE_X4Y130         FDCE                                       r
mem_wb_ALUOut_reg[16]/D
  ---------------------------------------------------------------------
-------------------

Slack:                    inf
  Source:                 ex_mem_ALUOut_reg[23]/C
                            (rising edge-triggered cell FDCE)
  Destination:            mem_wb_ALUOut_reg[23]/D
  Path Group:             (none)
  Path Type:              Min at Fast Process Corner
  Data Path Delay:        0.263ns  (logic 0.141ns (53.546%)  route 0.122ns
(46.454%))
```

```
  Logic Levels:           1  (FDCE=1)

    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  -------------------------------------------------------------------
-------------------
    SLICE_X4Y134         FDCE                         0.000     0.000 r
ex_mem_ALUOut_reg[23]/C
    SLICE_X4Y134         FDCE (Prop_fdce_C_Q)         0.141     0.141 r
ex_mem_ALUOut_reg[23]/Q
                         net (fo=2, routed)           0.122     0.263
data_addr_OBUF[23]
    SLICE_X4Y134         FDCE                                       r
mem_wb_ALUOut_reg[23]/D
  -------------------------------------------------------------------
-------------------

Slack:                   inf
  Source:                id_ex_regWrite_reg/C
                           (rising edge-triggered cell FDCE)
  Destination:           ex_mem_regWrite_reg/D
  Path Group:            (none)
  Path Type:             Min at Fast Process Corner
  Data Path Delay:       0.266ns  (logic 0.141ns (52.916%)  route 0.125ns
(47.084%))
  Logic Levels:          1  (FDCE=1)

    Location             Delay type                Incr(ns)  Path(ns)    Netlist
Resource(s)
  -------------------------------------------------------------------
-------------------
    SLICE_X4Y120         FDCE                         0.000     0.000 r
id_ex_regWrite_reg/C
    SLICE_X4Y120         FDCE (Prop_fdce_C_Q)         0.141     0.141 r
id_ex_regWrite_reg/Q
                         net (fo=2, routed)           0.125     0.266
id_ex_regWrite_reg_n_0
    SLICE_X5Y121         FDCE                                       r
ex_mem_regWrite_reg/D
  -------------------------------------------------------------------
-------------------
```