ASSIGNMENT SET – II

Assignment Set II is only for those who have completed the evaluation of Assignment Set I successfully.

A universal gate is a gate which can implement any Boolean function without need to use any other gate type. The NAND and NOR gates are universal gates. In practice, this is advantageous since NAND and NOR gates are economical and easier to fabricate and are the basic gates used in all integrated circuits (IC) digital logic families.

The objective in Assignment- II is to build all the chips presented below. The only building blocks that you can use are primitive **NAND gates** and the composite gates that you have build on top of them in ASSIGNMENT-I.

The only tool that you need for this project is the ModelSim - Intel FPGA Starter Edition. All the chips should be implemented in the HDL language using Verilog code.

As the assignment progress, students has to call / use the basic logical functions that is already implemented by him / her for building other logical functions.

The list of questions are shown below. There are 8 different logical functions. Students are expected to use only **Gate-Level Modeling** (**Structural Modeling**) for the implementation of following circuits in the given order.

1. Half Adder
2. Full Adder
3. 4-bit Incrementer
4. 4-bit Adder
5. 16-bit Adder
6. 16-bit Incrementer
7. 16-bit Negator (Hint: input: x output:!x)
8. Arithmetic-Logic Unit with following functions on two 16-bit inputs (x,y):
    a. x+y
    b. x-y
    c. y–x
    d. 0
    e. 1
    f. -1
    g. x
    h. y
    i. –x
    j. –y
    k. !x
    l. !y
    m. x+1
    n. y+1
    o. x-1
    p. y-1
    q. x&y
    r. x|y