A 100 MegaFlop Double Precision IEEE Multiplier Block For Advanced Bipolar VLSI

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Abstract

Described is a megacell used in designing an ultra-high performance double precision IEEE-754 floating point multiplier, capable of better than 100 Megaflops throughput. Details of its use, construction, and performance are shown.

Concept

Future generations of mini-supercomputers and super-workstations will require very high speed floating point arithmetic hardware. The speed of the multiply operation on double precision operands is a major hurdle in increasing system performance. To help solve this problem we at National have designed a standard cell family of components in ASPECT I [1], for integrating floating point systems, the premiere component being the 'MPY54APM' multiplier megacell.

The MPY54APM was designed to minimize the delay in the critical operation of floating point mantissa multiplication. To this end it performs 54 bit multiplication on 2 two's complement numbers with a throughput delay of less than 9 nanoseconds per product.

The typical application is a three stage pipelined architecture as shown in figure 1. Two of these megacells are cascaded to form two of the pipeline stages each with a 9 ns delay. The last stage is constructed of standard cells to perform final carry-lookahead addition, normalization, rounding, and exception limiting.

The adjunct operations on the exponent fields for floating point multiplication occur concurrently with the mantissa operations. As the size and nature of these operations are neither time nor space critical (except after rounding) the hardware for their implementation would also use standard cells [2].

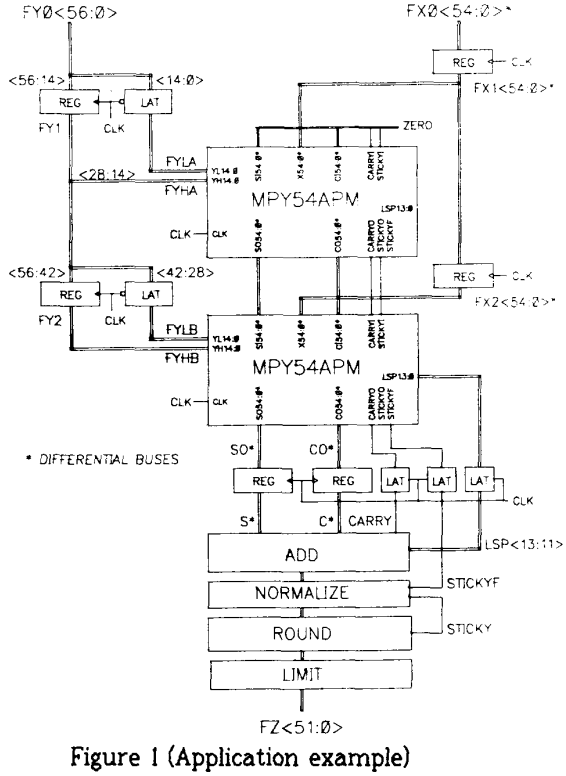

Figure 1 (Application example)

Construction

A major factor in the circuit design of the multipier was to reduce wiring delays, to make use of the inherently fast gate speeds that ASPECT I provides. ASPECT I also allows the easy integration of VLSI densities (>20 K gates) without exceeding current package heat dissipation capabilities.

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A number of decisions were made for optimal performance: (1) to use differential signals throughout (reduces swing -> faster circuits), (2) to use a dense matrix of carry-save adders to minimize wiring, (3) use a radix 4 modified Booth algorithm, (4) implement a incomplete matrix by utilizing feedback of the partial products in two internal cycles.

Figure 2 shows a block diagram for the megacell. The system clock 'CLK' usually runs at > 100 MHz and is doubled internally so that two internal cycles occur per system clock cycle. Seven rows of modified Booth carry-save adders form 14 bits of product per internal clock cycle.

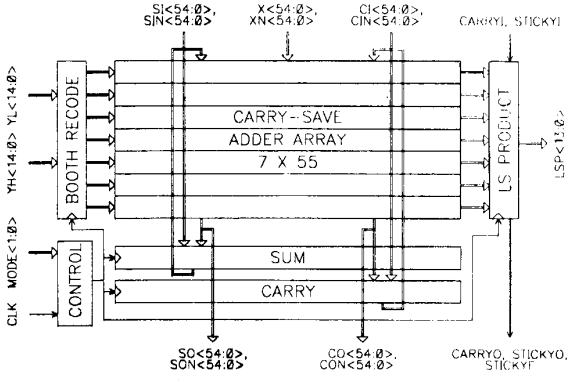

Figure 2 (Megacell block diagram)

The 'SUM' and 'CARRY' registers load the partial product value from the previous pipestage and the intermediate value during the second internal cycle of operation.

The megacell also generates the correct 'STICKY' bit and carry-in signals for final addition and rounding.

The dataflow is as follows: The Y operand is selected and decoded during the first phase of the internal clock; these signals are used to recode multiples of X (0,±1,±2) during the second phase of the internal clock; seven rows of carry-save adders then add the multiples of X with the partial product generated from the row above (after an apropriate shift); The last partial product is registered and fed back to the top of the array for processing on the next internal cycle.

The key element to the performance of the multiplier is the Booth-adder cell which is arrayed into the 7 x 55 cell matrix. Figure 3 shows the equivalent logic and figure 4 is the circuit diagram for this cell.

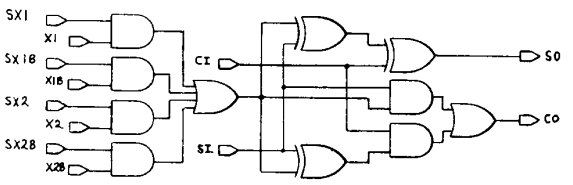

Figure 3 (Booth-adder logic)

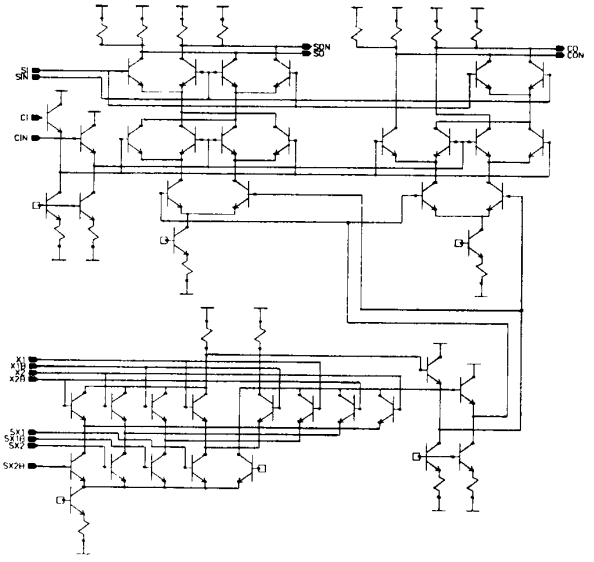

Figure 4 (Booth-adder circuit)

The cell is composed of two sections, the first is a 4 to 1 mux which selects the multiples of X into the second section which is a carry-save adder. The multiplex section has 4 select lines which are directly driven from the recoder and has a default value of 0 when all select lines are off.

As indicated in figure 4, this cell utilizes differential signals everywhere except at the selects. Doing so provided the lowest possible ripple delay within the cell matrix.

Performance

Table 1 gives the characterization data for this Booth-adder cell, over temperature and process variation, and loaded by the actual circuit it drives.

Table 1 Booth-adder cell characteristics

Area (mil^2)		36.46		
Gate Equivalence		14		
Temp	27°C		125°C	
	typ	min	typ	max
Power (mW)	6.66	5.92	7.65	9.50
Delay (ps)				
SI,SIN -> CO,CON	213	216	238	262
SI,SIN -> SO,SON	195	183	221	261
CI,CIN -> CO,CON	302	296	344	406
CI,CIN -> SO,SON	333	324	380	435
SX_i -> CO,CON	803	738	897	1073
SX_i -> SO,SON	829	763	925	1095
X_i -> CO,CON	745	697	830	993
X_i -> SO,SON	722	722	860	998

The critical path thru the multiplier is the Y selection and decode, 1st row X recode selection, 6 rows of ripple carry-save add, and setup at the carry-sum registers. This path has a delay at worst case process corners and 125°C of **4108** ps. By controlling clock skew to less than 300 ps, an overall **worst case** performance of <4.5 ns per 14 bit multiply cycle was achieved. By maintaining a clock edge spacing of 4.5 ns a full **116** Megaflops throughput rate for double precision multiplication results.

Though it was not designed specifically for single precision operation, a throughput of <5 ns per single precision multiplication is also possible (a **>200** MHz rate). Only one clock edge per pipestage is required to complete the partial product formation.

Verification

To prove the correctness of the megacell, logic, physical, and electrical simulations were performed. A logic model for a complete double precision floating point multiply chip was constructed which used 2 megacells and other standard cells from the library. This model was simulated with detailed timing information against both randomly generated patterns and a set of standard vectors (IEEE 754 test suite [4]). Compliance verifies the correct functionality of the megacell.

Physical correctness was verified via Layout Versus Schematic (LVS ECAD) and DRC and parameter extraction.

Device level circuit schematic were also compared to logic models for all cells using in-house developed software to verify that the circuit, layout, and logic representations are 100% equivalent.

The biasing network and cell design methodology was identical to that used in previous products (F100810 [3]) and verifies electrical correctness of the design.

Bibliography:

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[3] S.Menon, S. Tibbitts, W. Keshlear et al
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[4] "A Compact Test Suite for P754 Arithmetic"
Developed by ZILOG Inc, and disseminated by the floating point working group for IEEE 754-10 committee.