Implementation of MESI

Cache Coherence Protocol

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Abstract

Recent trends in processor technology use multiple cores on a single chip with dedicated instruction and data caches for each core. When programs running on different cores try to access shared memory locations, corresponding caches of the cores will be populated with redundant data from same location and coherency among the caches becomes a challenge.

Various protocols have been proposed to solve the coherency problem among the caches, MESI being the most widely used snooping based protocol.

Aim of the work is to implement Coherent Data Caches for a Quad-Core environment using MESI Bus Snooping Coherence Protocol and verify the implementation using Constrained Random Test-Bench.

Introduction

Implementation of

MESI – Line State Change

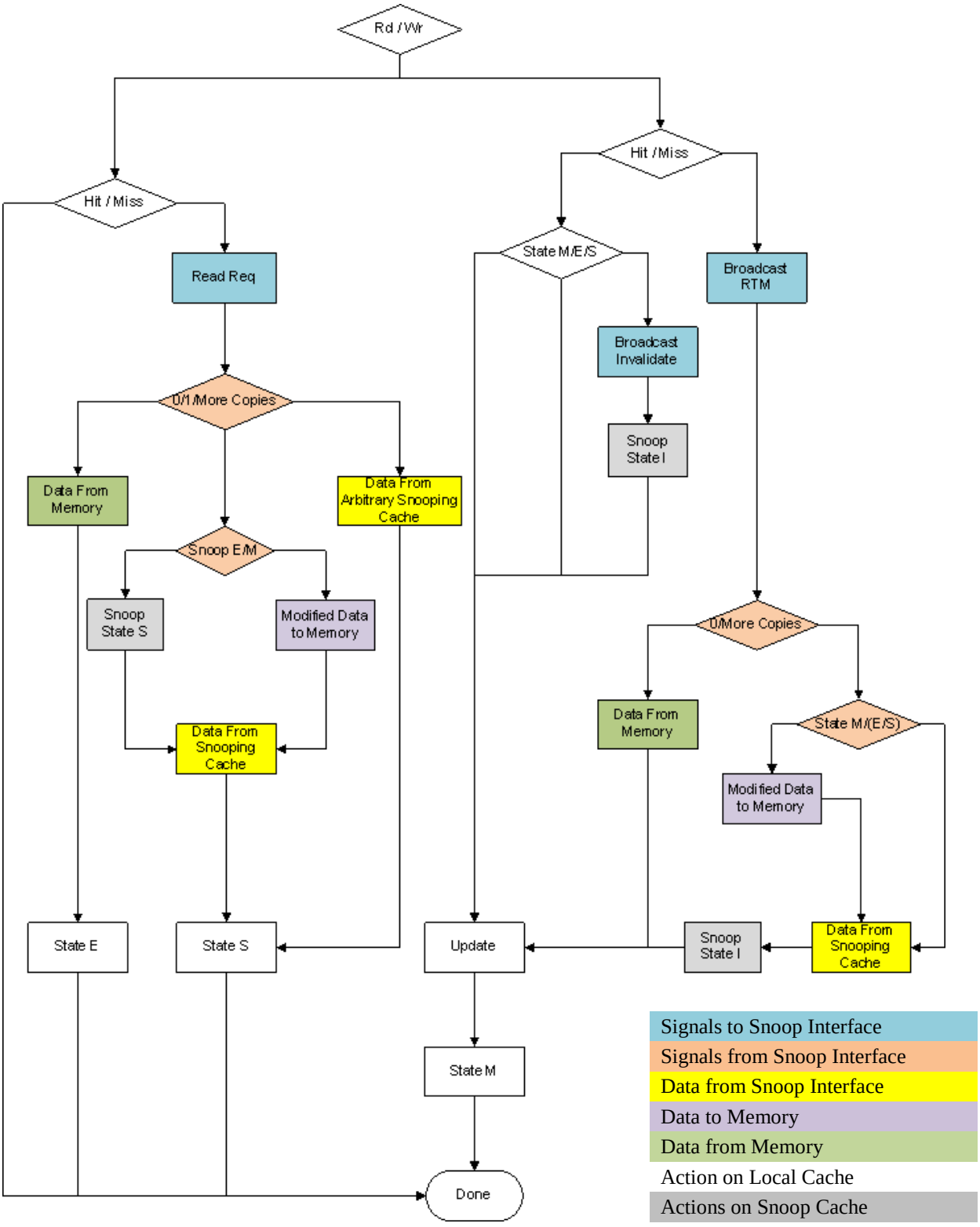

Figure 1MESI Line State Change

Implementation

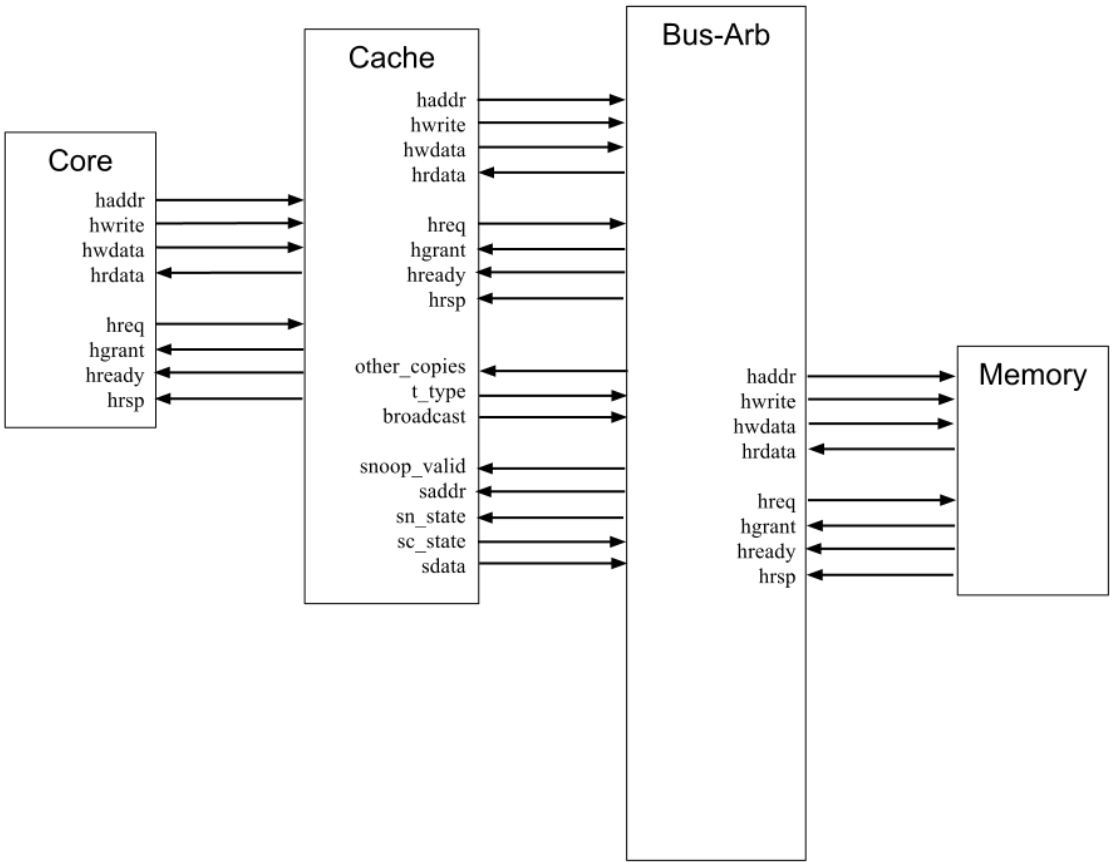

Figure 2 Block Diagram of Implementation

Code

References

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3. **Interaction of Finite State Machines and Concurrency Models.** Bilung Lee and Edward A. Lee, University of California at Berkeley, Proceeding of Thirty Second Annual Asilomar Conference on Signals, Systems, and Computers, Pacific Grove, California, November 1998.