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| Implementation of MESI |
| Cache Coherence Protocol |
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| Towards the partial fulfillment of Masters Degree in VLSI & CE at IIITH |

# Abstract

Recent trends in processor technology use multiple cores on a single chip with dedicated instruction and data caches for each core. When programs running on different cores try to access shared memory locations, corresponding caches of the cores will be populated with redundant data from same location and coherency among the caches becomes a challenge.

Various protocols have been proposed to solve the coherency problem among the caches, MESI being the most widely used snooping based protocol.

Aim of the work is to implement Coherent Data Caches for a Quad-Core environment using MESI Bus Snooping Coherence Protocol and verify the implementation using Constrained Random Test-Bench.

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# Introduction

Implementation of

# MESI – Line State Change

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| Signals to Snoop Interface |
| Signals from Snoop Interface |
| Data from Snoop Interface |
| Data to Memory |
| Data from Memory |
| Action on Local Cache |
| Actions on Snoop Cache |

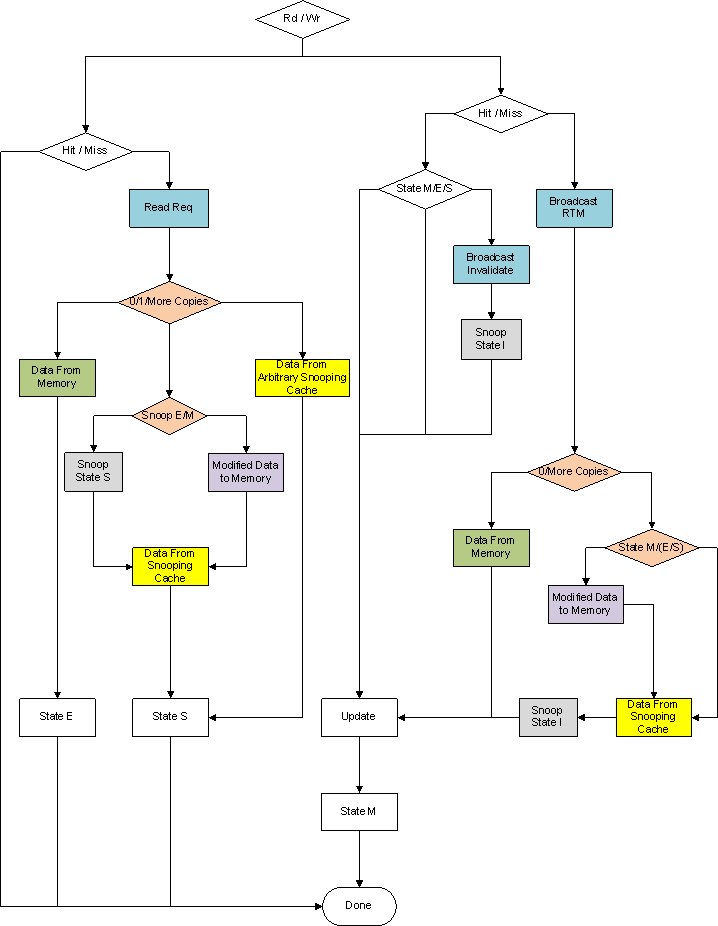


Figure MESI Line State Change

# Block_Diagram.pngImplementation

Figure Block Diagram of Implementation

# Code

# References

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