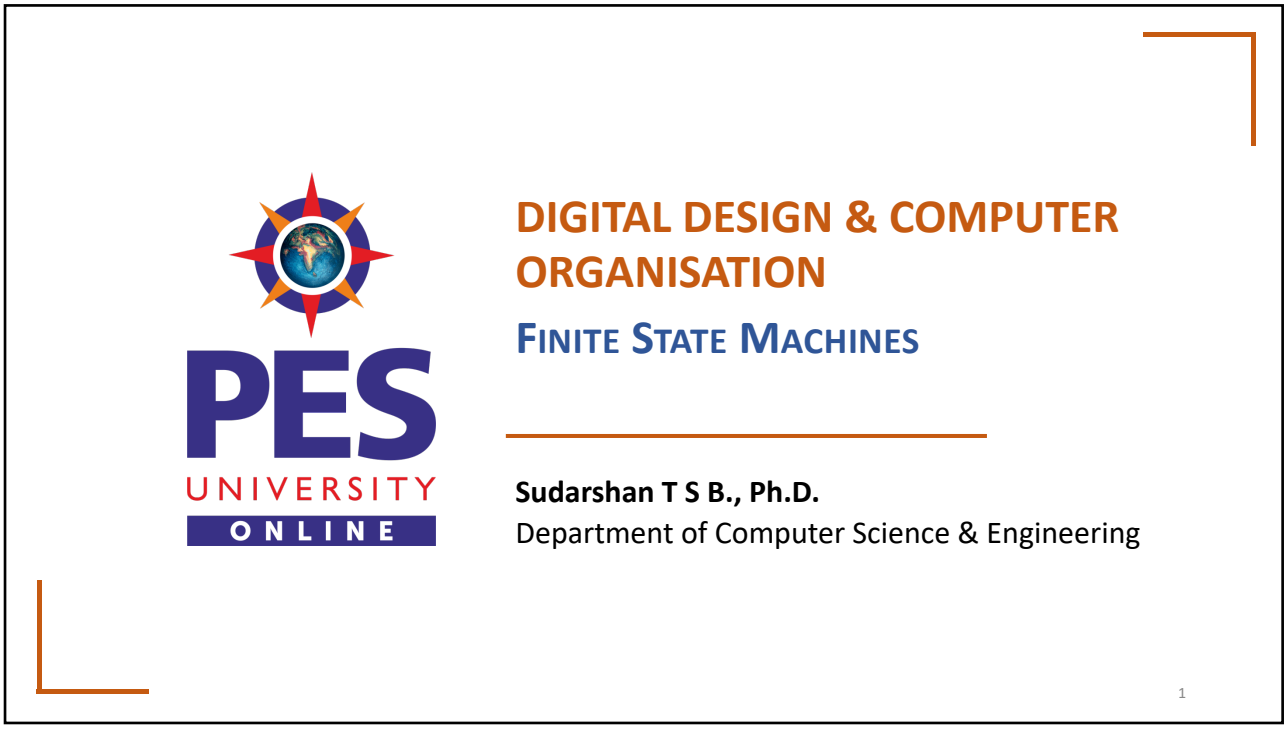
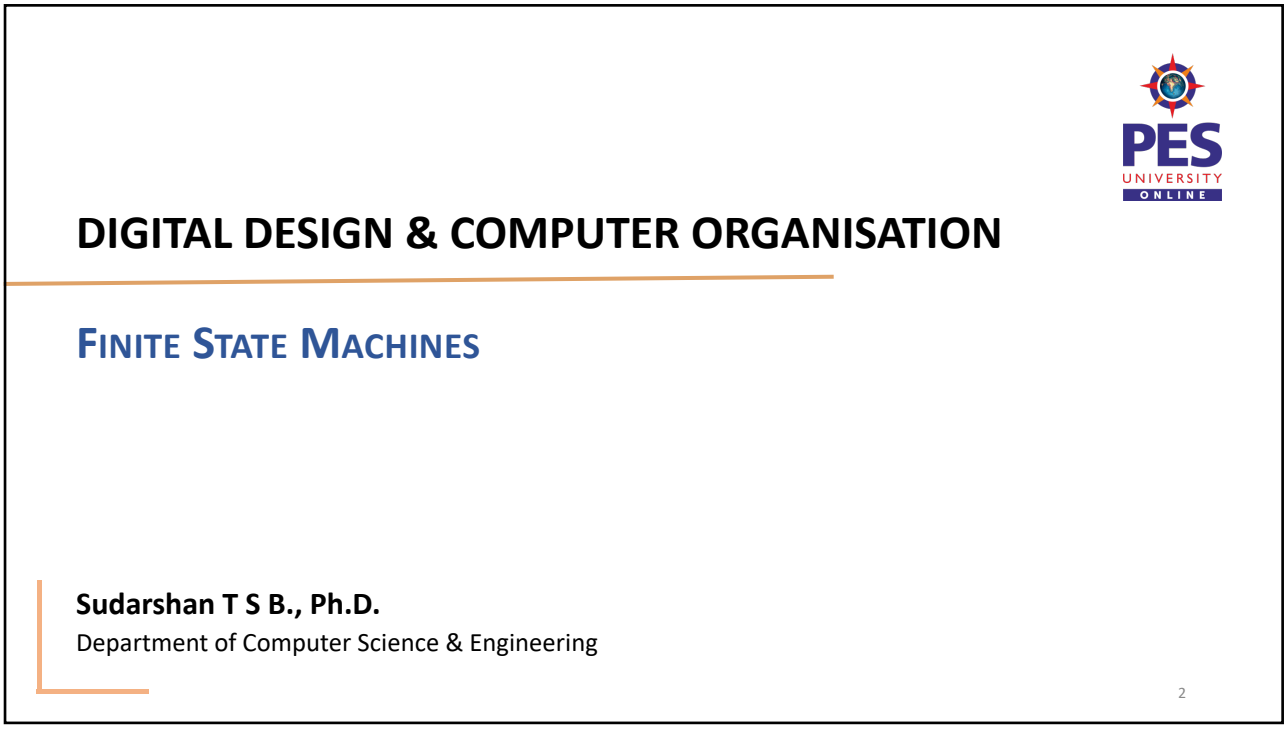

DIGITAL DESIGN & COMPUTER ORGANISATION
FINITE STATE MACHINES
Sudarshan T S B., Ph.D.
Department of Computer Science & Engineering
1

1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2

2

FINITE STATE MACHINES
Course Outline

- Digital Design
  - Combinational logic design
  - Sequential logic design
    - ★ **Finite State Machines**
- Computer Organization
  - Architecture (microprocessor instruction set)
  - Microarchitecure (microprocessor operation)

Concepts covered

- Finite State Machines
  - Mealy and Moore Machines

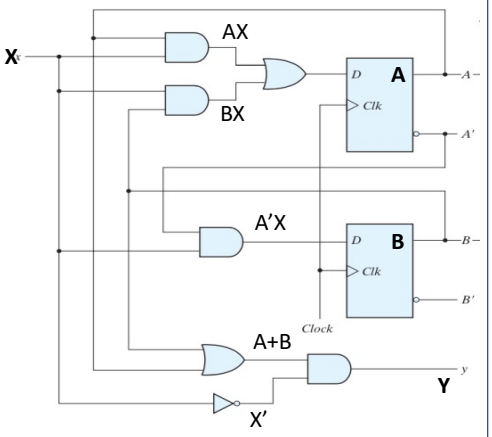
3

FINITE STATE MACHINES
Example-2

- Express State Equation
- Construct a State Table
- Construct a State Diagram

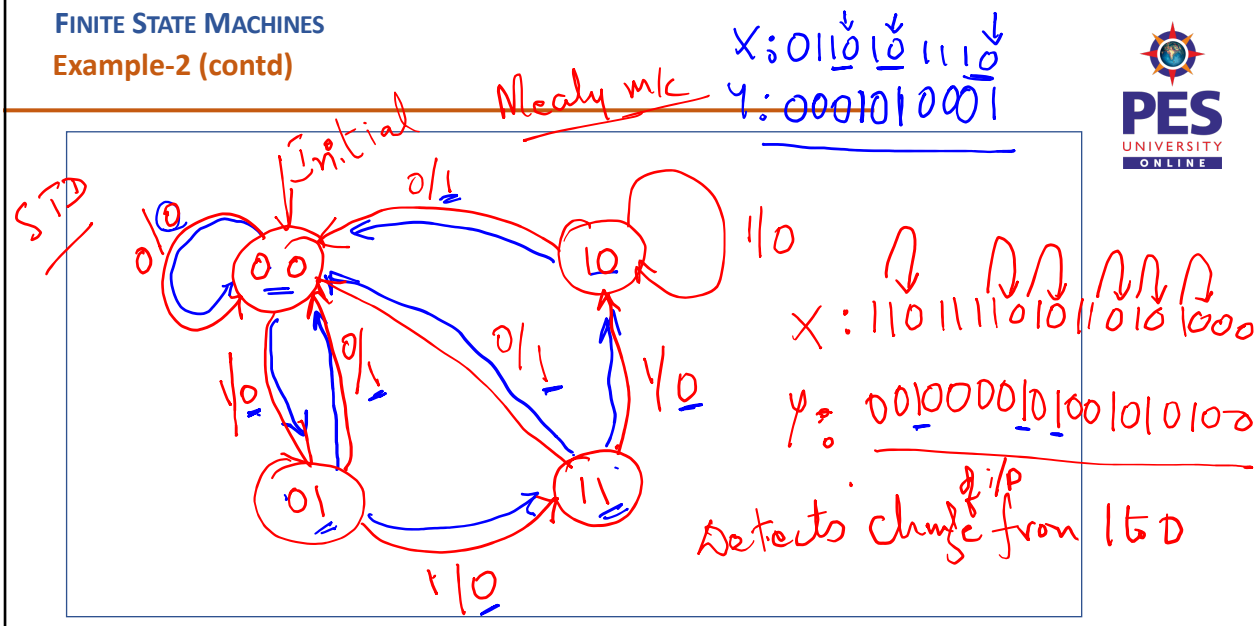
State Equation:

A(t+1) = AX + BX
B(t+1) = A'X
Y = X' (A + B)



4

FINITE STATE MACHINES
Example-2 (contd)



5

FINITE STATE MACHINES
Example-3

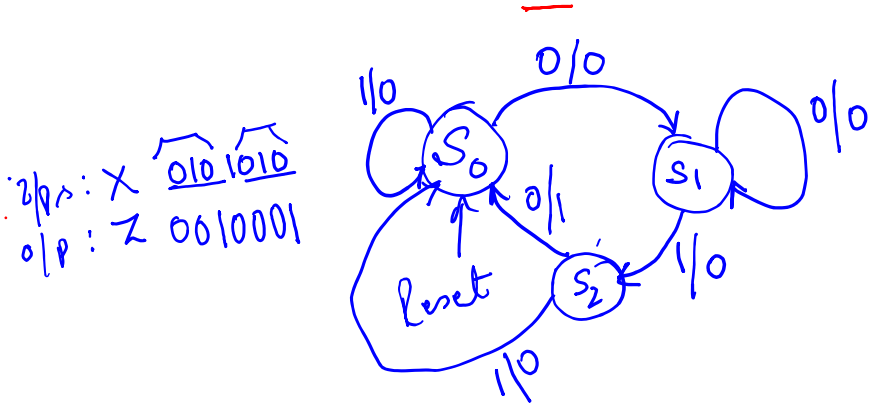
- Design a circuit using State Transition Diagram that has a serial input X and an output Z.
- Z should be 1 coinciding with the last bit of the pattern **010** or else Z is 0.
- Construct a Mealy machine and Moore machine for both **non-overlapping pattern** detection and **overlapping pattern** detection

6

FINITE STATE MACHINES
Example-3 (contd)

0111 0110 01010

Mealy Non-Overlapping:



i/p : X 010 1010
o/p : Z 0010001

7

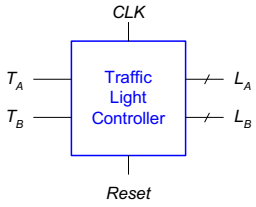
FINITE STATE MACHINES
Example-3 (contd)

Moore Overlapping:

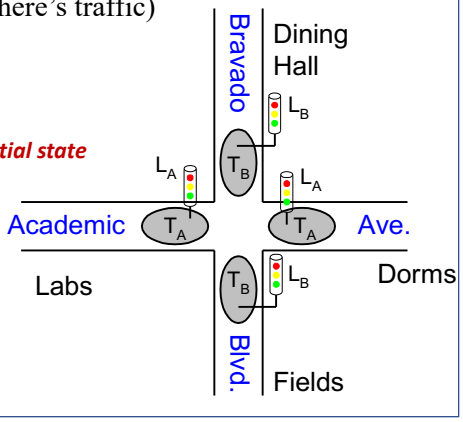
8

FINITE STATE MACHINES
Example- 4

- Traffic light controller
  - Traffic sensors: T_A, T_B (TRUE when there's traffic)
  - Lights: L_A, L_B



CLK with 5-sec period
Reset to control the initial state

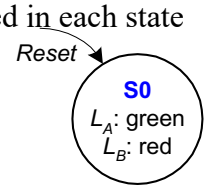


- Inputs: *CLK*, *Reset*, T_A, T_B
- Outputs: L_A, L_B

FINITE STATE MACHINES
Example-4 (contd)

FSM Diagram:

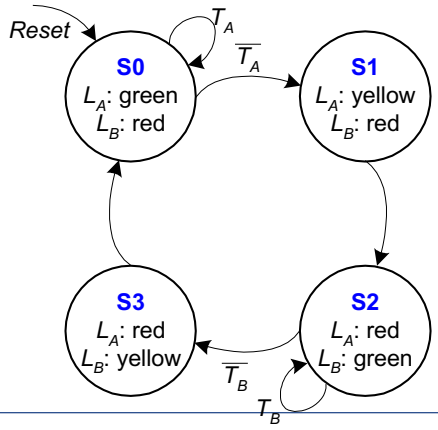
- **Moore FSM:** outputs labeled in each state



FINITE STATE MACHINES
Example-4 (contd)

FSM Diagram:

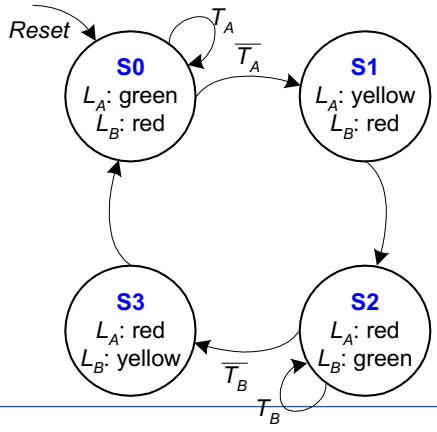
- **Moore FSM**



FINITE STATE MACHINES
Example-4 (contd)

- Obtain State Table, State Equation and design a circuit

Current State S	Inputs T_A	Inputs T_B	Next State S'
S0	0	X	S1
S0	1	X	S0
S1	X	X	S2
S2	X	0	S3
S2	X	1	S2
S3	X	X	S0



FINITE STATE MACHINES
Example-4 (contd)

- State Assignment, State Table

Current State		Inputs		Next State	
S_1	S_0	T_A	T_B	S'_1	S'_0
0	0	0	X	0	1
0	0	1	X	0	0
0	1	X	X	1	0
1	0	X	0	1	1
1	0	X	1	1	0
1	1	X	X	0	0

State	Encoding
S0	00
S1	01
S2	10
S3	11

$$S'_1 = S_1 \oplus S_0$$
$$S'_0 = S_1 S_0 T_A + S_1 S_0 T_B$$

FINITE STATE MACHINES
Example-4 (contd)

- **Output Table**

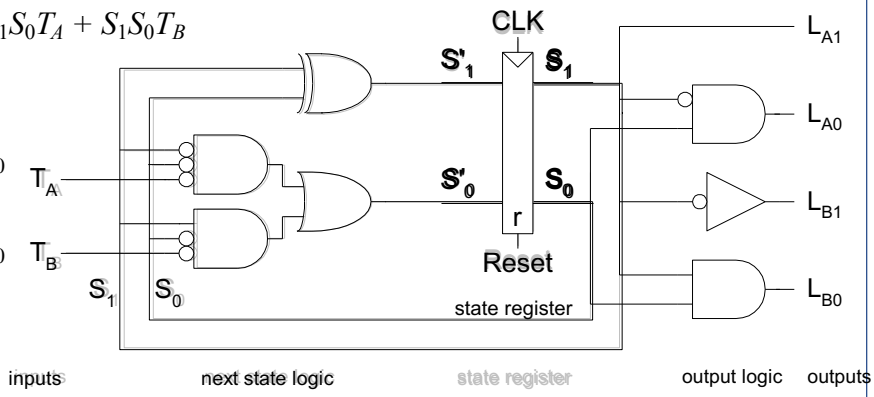
Current State		Outputs			
S_1	S_0	L_{A1}	L_{A0}	L_{B1}	L_{B0}
0	0	0	0	1	0
0	1	0	1	1	0
1	0	1	0	0	0
1	1	1	0	0	1

Output	Encoding
green	00
yellow	01
red	10

$$L_{A1} = S_1$$
$$L_{A0} = S_1 S_0$$
$$L_{B1} = S_1$$
$$L_{B0} = S_1 S_0$$

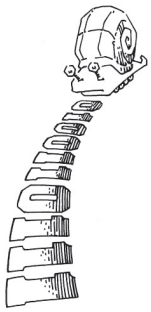
FINITE STATE MACHINES
Example-4 (contd)

$$S'_1 = S_1 \oplus S_0$$
$$S'_0 = S_1 S_0 T_A + S_1 S_0 T_B$$
$$L_{A1} = S_1$$
$$L_{A0} = S_1 S_0$$
$$L_{B1} = S_1$$
$$L_{B0} = S_1 S_0$$



FINITE STATE MACHINES
Example-5

- Alyssa P. Hacker has a snail that crawls down a paper tape with 1's and 0's on it. The snail smiles whenever the last two digits it has crawled over are 01. Design Moore and Mealy FSMs of the snail's brain.

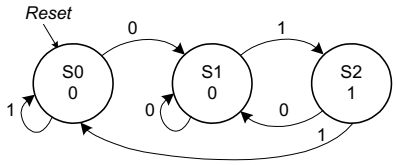


FINITE STATE MACHINES
Example-5 (contd)

- **Moore FSM:**

State	Encoding
S0	00
S1	01
S2	10

Moore FSM



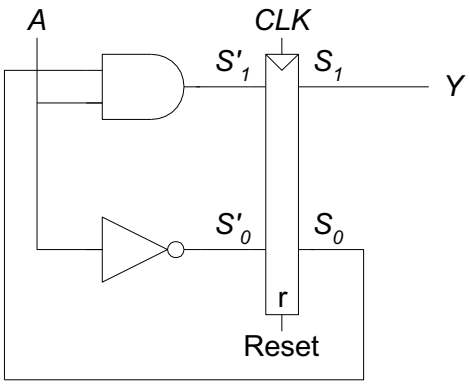
Current State S_1	Current State S_0	Inputs A	Next State S'_1	Next State S'_0
0	0	0	0	1
0	0	1	0	0
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0

$$S_1' = S_0 A$$
$$S_0' = A'$$

FINITE STATE MACHINES
Example-5 (contd)

Current State S_1	Current State S_0	Output Y
0	0	0
0	1	0
1	0	1

$$Y = S_1$$



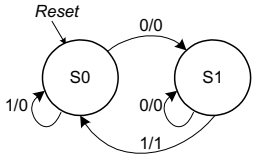
FINITE STATE MACHINES
Example-5 (contd)

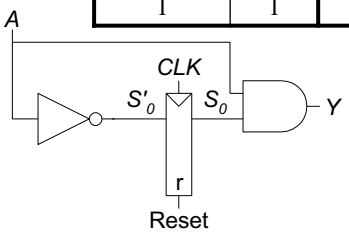
- **Mealy FSM**

State	Encoding
S0	00
S1	01

Current State	Input	Next State	Output
S_0	A	S'_0	Y
0	0	1	0
0	1	0	0
1	0	1	0
1	1	0	1

Mealy FSM

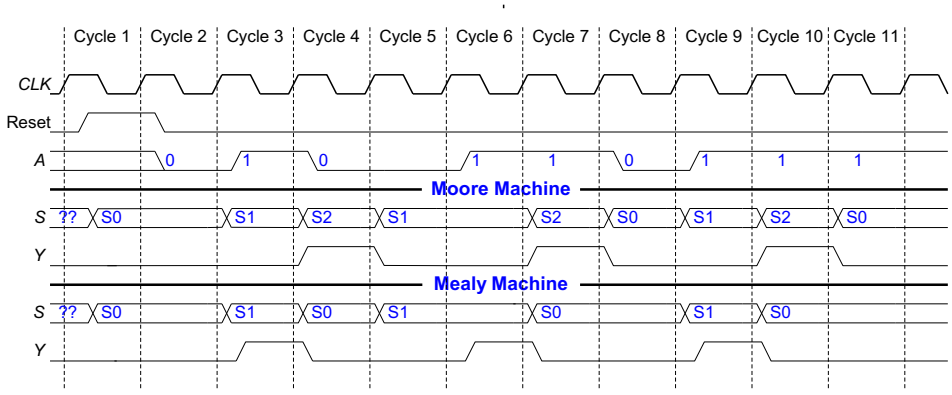




19

FINITE STATE MACHINES
Example-4 (contd)

- **Moore & Mealy Timing Diagram:**



20

THANK YOU

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21

21