Constructing an XOR Gate using Skywater 130nm CMOS Technology

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***Abstract* - This paper discusses the design and implementation of a general-purpose 2-input XOR gate using Skywater 130nm CMOS technology. The XOR gate operates at a supply voltage of 5V for a high logic level (logic 1) and approximately 0V for a low logic level (logic 0). XOR gates play a crucial role in digital systems, particularly in arithmetic and data processing applications where conditional logic operations are required**

I. INTRODUCTION

The XOR (exclusive OR) gate is a core component in digital circuit design, widely used in applications such as error detection and arithmetic functions in adders and parity checkers. It is widely used in Digital communication for differential encoding. In this paper we will see the logic equation, implementation considerations, and implementation of an XOR gate.

II. DESIGN PRINCIPLE

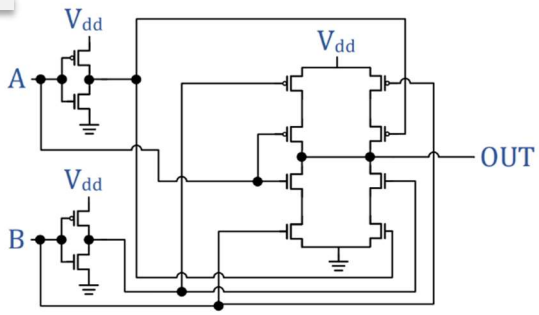
The output of a 2-input XOR gate is obtained by the Boolean function, $Y = A \oplus B. = A'B + AB'$
It's truth table,

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

CMOS XOR implementation uses complementary PMOS and NMOS transistors arranged such that they achieve the XOR function by turning on or off according to input states. Therefore, we will essentially be constructing a XNOR gate then invert the output to get XOR output.

∴ Pull Down Network = AB + A'B'
∴ Pull Up Network = A'B + AB'

III. IMPLEMENTATION



The pull-up network is implemented using 4 PMOS transistors. While the pull-down network is implemented using 4 NMOS transistors. Additionally, 2 extra sets of NMOS and PMOS are used to construct two inverters, to supply A' & B'. The Pull up network consists of 2 parallel branches of PMOS with each branch being the series of two PMOS. Similarly, the pull-down network consists of 2 parallel branches of NMOS with each branch being the series of two NMOS.

IV. ISSUES & IMPROVEMENTS

The Additional requirement of two inverters eats up precious space, and adds a significant propagation delay. It also increases the power consumption of the circuit. Work can be done to mitigate these problems.

V. CONCLUSION

The Construction & characteristics of XOR gate following Euler's path was studied. The significance of the Euler's path on delay and area optimization was noted.

VI. REFERENCES

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