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Assignment 2.

Title : CRC (Cyclic Redundancy check)

Problem statement : Write a program for error detection and correction for 7/8 bits ASCII codes using CRC. Demonstrate the packets captured using Wireshark Packet Analyzer Tool for peer to peer mode.

Software and Hardware requirements : C++ compiler, Wireshark Packet Analyzer Tool, i5 processor

Theory :

In digital systems, the analog signals will change into digital sequence (in form of bits). This sequence of bits is called as "Data Stream". The change in position of single bit also leads to catastrophic (major) error in data output

- Error :

i.) The data can be corrupted during transmission (from source to reciever).

ii.) It may be affected by external noise or some other physical imperfections.

iii.) In this case, the input data is not same as received output data. This mismatched data is called "Error".

* Types of Error

1] Single Bit Errors :

i) The change in one bit, in whole data sequence, is called single bit Error.

ii) Occurence of single bit error is very rare in serial communication system.

iii) This type of error occurs only in parallel communication system, as data is transferred bit wise in single line.

2.] Multiple bit Data Errors:

i) If there is change in two or more bits of data sequence of transmitter to reciever, it is called "Multiple Bit Errors"

ii) This type of error occurs in both serial type and parallel type data communication networks.

3.] Burst Errors:

i) The change of set of bits in data sequence is called Burst Errors

ii) The burst error is calculated in form first bit change to last bit change.

* Error detecting codes:

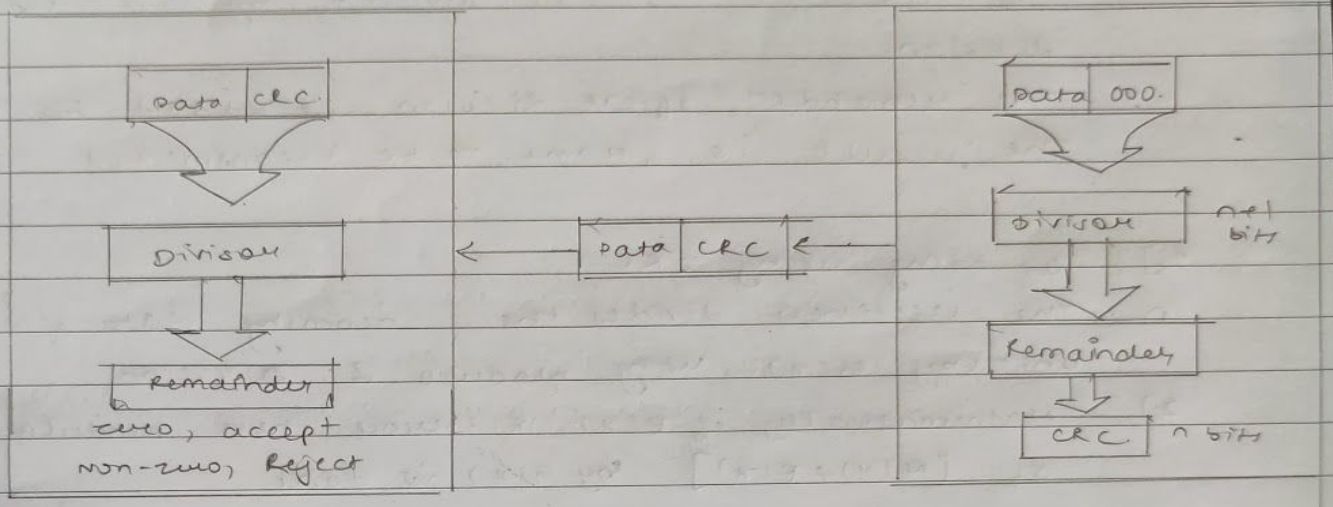
i) In digital communication system errors are transferred from one communication system to another, along with the data

ii) If these errors are not detected & corrected, data will be lost

iii) For effective communication, data should be transferred with high accuracy.

* Error detecting codes.

1) Parity checking
2) cyclic Redundancy check (CRC)
3) Longitudnal Redundancy check (LRC)
4) Check Sum



CRC (cyclic redundancy check)

* Cyclic Redundancy check (CRC)

i.) A cyclic code is a linear (n, k) block code with the property that every cyclic shift of a code word results in another code word.

ii.) Here, k indicates the length of the message at transmitter (the number of information bits).

iii.) n is the total length of the message after adding check bits (actual data + check bits).

iv.) They are easily impleemented using shift registers with feedback connection.

* Algorithm:

A.] For encoding using CRC.

1.) The communicating parties agree upon size of message, M(x) and generator polynomial G(x)

2.) If r is order of G(x), r bits are appended to lower order of M(x). This makes block size bits

the value of which is $x^n M(x)$.

3.) The block $x^n M(x)$ is divided by $G(x)$ using Modulo(2) division.

4.) The remainder after division is added to $x^n M(x)$. The result is frame to be transmitted, $T(x)$.

Decoding using CRC

1) The receiver divides the incoming data frame $T(x)$ unit by $G(x)$ using modulo 2 division.

2) Mathematically, if $E(x)$ is error, then modulo 2 division of $[M(x)+E(x)]$ by $G(x)$ is done

3) If there is no remainder, data frame is accepted.

4) A remainder indicates an error, and data frame is rejected

* Testing.

Sender side	Reciever side	Accept / Reject
1) Data : 101010 CRC : 00 Divisor : 100 Transmitted : 101010100	Recieved : 101010100 Remainder : 00	Accept
2) Data : 10011 Divisor : 1101 CRC : 011 Transmitted : 1001101 1	Recieved : 1001101 1 Remainder : 001	Reject

Conclusion:

Error detection & correction using CRC was studied & implemented successfully