Project Report

Study and Implementation of SRAM on Cadence

Project by:

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- # Introduction:

1. About SRAM:

SRAM stands for "Static Random-Access Memory." It is a type of semiconductor memory that is used in electronic devices for storing data. SRAM is "static" in that it doesn't need to be refreshed as frequently. This makes SRAM faster and more power-efficient compared to DRAM.
One key characteristic of SRAM is its structure. It's built using flip-flop circuits, which consist of multiple transistors arranged in a way that they can store a single bit of data. Each flip-flop can hold its state (0 or 1) without needing to be refreshed constantly. However, due to its more complex structure, SRAM tends to occupy more space on a chip and is more expensive to manufacture compared to DRAM.

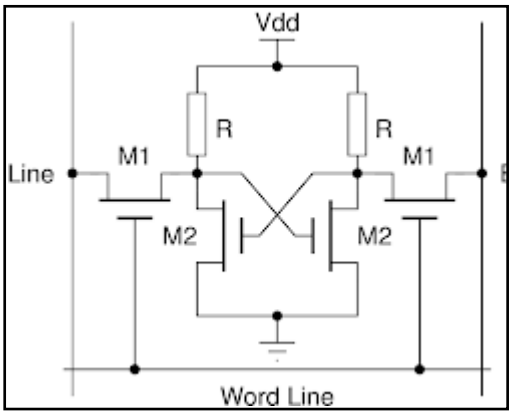
SRAM is used in a variety of applications, including:

a. **Cache memory**: Cache memory is a small, fast memory that is used to store frequently accessed data. SRAM is often used for cache memory because it is the fastest type of RAM.
b. **Registers**: Registers are small memory units that are used to store data temporarily. SRAM is often used for registers because it is fast and non-volatile.
c. **Processors**: The CPU in a computer is made up of many registers and cache memory. SRAM is often used for thes2e components because it is fast and reliable.
d. **Networking equipment**: SRAM is used in networking equipment, such as routers and switches. This is because it is fast and reliable, and it can handle the high data throughput of these devices.

Overall, SRAM is a type of fast, volatile memory that is widely used in electronics for temporary data storage due to its speed and efficiency

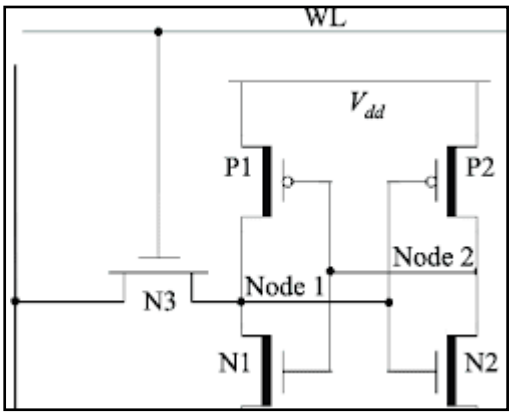
2. Different SRAM cell designs:

a. 4T (Four-Transistor) SRAM Cell:



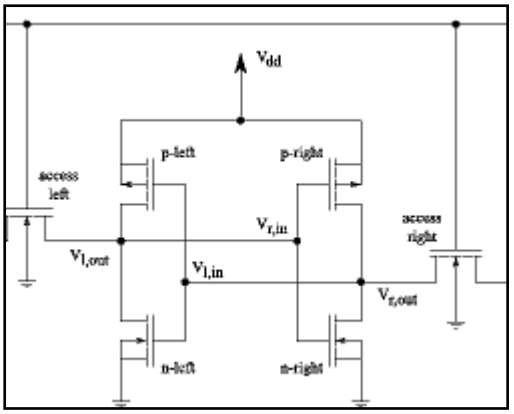
- **Structure:** It consists of four transistors: two NMOS transistors and two PMOS transistors. The NMOS transistors are used to store the data, and the PMOS transistors are used to control the access to the data
- **Significance:** It is a basic SRAM cell design with a relatively small area. However, it's more vulnerable to noise and stability issues due to the absence of a feedback loop.

b. 5T (Five-Transistor) SRAM Cell:



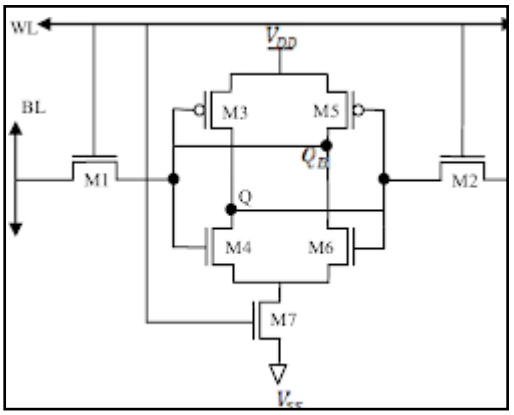
- **Structure:** This cell includes an additional read/write access transistor compared to the 4T cell.
- **Significance:** The extra access transistor isolates the storage nodes from the bitlines during read and write operations, reducing the susceptibility to disturb and improving stability. It offers better noise immunity and reduced leakage, but it's slightly larger than the 4T cell.

c. 6T (Six-Transistor) SRAM Cell:



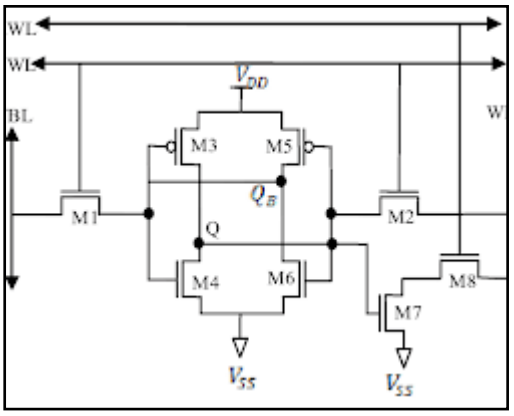
- **Structure:** This is the most common SRAM cell design, comprising six transistors arranged in a cross-coupled inverter with access transistors.
- **Significance:** The 6T cell offers good noise margins, stability, and robustness. It provides better read and write capabilities compared to 4T and 5T cells, and it's widely used in various applications, including CPU caches.

d. 7T (Seven-Transistor) SRAM Cell:



- **Structure:** This cell extends the 6T cell with an additional access transistor.
- **Significance:** The added access transistor provides an extra level of isolation, reducing leakage and improving stability further. However, the 7T cell is larger and consumes more area and power compared to the 6T cell, making it less area-efficient.

e. 8T (Eight-Transistor) SRAM Cell:



- **Structure:** This cell adds more transistors for enhanced stability and performance.
- **Significance:** The 8T cell separates the storage nodes from the bit lines using access transistors, effectively reducing read disturb issues. It offers high noise immunity and robustness, but it comes at the cost of increased area and power consumption, making it suitable for specific high-performance applications.

Table of comparison:

SRAM cell design	Speed	Power consumption	Area
4T	Fastest	Highest	Smallest
5T	Slower	Lower	Slightly larger
6T	Good compromise	Good compromise	Good compromise
7T	Slower	Lower	Larger
8T	Slowest	Lowest	Largest

3. Why 6t SRAM is standard:

The 6T (Six-Transistor) SRAM cell has become the standard design for many reasons, primarily due to its balanced trade-offs between various factors that are crucial in integrated circuit design. Some key reasons why the 6T SRAM cell is widely adopted as the standard:

1) **Read and Write Performance:** The 6T SRAM cell offers relatively fast read and write operations. It can be read and written to without destructive read operations, meaning that reading the data does not cause it to be lost or altered. This is important for efficient memory access in many applications.
2) **Stability and Noise Immunity:** The 6T SRAM cell provides good noise margins and stability. The cross-coupled inverter configuration helps maintain the stored data reliably, reducing the likelihood of data corruption due to noise or disturbances.
3) **Area Efficiency:** While the 6T cell is larger than some other designs, it strikes a balance between area efficiency and performance. It is smaller than more complex cell designs like 7T or 8T cells, making it more suitable for applications where area constraints are important.
4) **Manufacturability:** The 6T SRAM cell is relatively easier to manufacture compared to more complex designs. It requires fewer transistors and simpler interconnections, which can lead to higher yield during chip fabrication.
5) **Compatibility:** The 6T SRAM cell has been established as a de facto standard in the semiconductor industry. This means that design tools, processes, and libraries are well-developed and optimized for this cell design. This compatibility simplifies the integration of SRAM cells into larger systems.
6) **Power Efficiency:** While not as power-efficient as some newer low-power designs, the 6T SRAM cell still provides a reasonable balance between performance and power consumption. This is essential for applications that require a combination of speed and energy efficiency.
7) **Trade-offs:** The 6T cell's design strikes a balance between different trade-offs such as read and write performance, stability, leakage power, and manufacturing complexity. It's a versatile design that works well in a wide range of applications.

4. DRAM:

DRAM stands for Dynamic Random Access Memory. It is a type of random-access memory (RAM) that stores each bit of data in a memory cell, usually consisting of a tiny capacitor and a transistor, both typically based on metal–oxide–semiconductor (MOS) technology. The capacitor stores the charge that represents the data bit, and the transistor acts as a switch that controls whether the data bit can be read or written. DRAM is a volatile memory, meaning that it loses its data when power is removed. DRAM is the most common type of RAM used in computers. It is used for the main memory, which stores the data and instructions that the CPU is currently using. DRAM is also used for the cache memory, which is a small, fast memory that stores frequently accessed data. DRAM is constantly refreshed, which means that the charge in the capacitors is periodically restored to prevent data loss. This is done by a process called row refreshing. Row refreshing is performed by the DRAM controller, which is a small chip on the motherboard.

The key characteristics of DRAM include:

a. **Dynamic Nature:** The storage cells in DRAM are capacitors that store electrical charge to represent binary data (0s and 1s). Over time, the charge leaks away due to the inherent properties of capacitors. As a result, the data in a DRAM cell needs to be refreshed periodically, typically every few milliseconds, to prevent data loss.
b. **Higher Density:** DRAM cells are simpler in structure compared to SRAM cells, allowing for higher memory density. This means that more memory can be stored in a given area, making DRAM well-suited for applications that require large memory capacities.
c. **Slower Access Speed:** Compared to SRAM, DRAM has slower access times due to the need for periodic refreshing and the more complex circuitry required for read and write operations.
d. **Lower Power Consumption:** In terms of power efficiency, DRAM generally consumes less power per bit compared to SRAM. This makes it more suitable for applications where memory capacity is more important than extremely fast access times.
e. **Main Memory Usage:** DRAM is commonly used as the main system memory (RAM) in computers and other devices. It provides the working memory space that the CPU and other components use to store and retrieve data during active tasks.
f. **Hierarchical Memory Architecture:** In most computer systems, DRAM is used in a hierarchy of memory levels, where the closest and fastest levels are the CPU registers and caches (SRAM), followed by DRAM for main memory, and then possibly slower storage devices like hard drives or solid-state drives (SSDs).
g. **Cost-Effective:** DRAM is more cost-effective than SRAM when it comes to providing large amounts of memory. Its higher density and lower cost per bit make it suitable for applications where vast memory capacities are required.

Due to its higher density and cost advantages, DRAM is the primary memory type used for main system memory in computers, servers, and many consumer electronics. However, its dynamic nature and need for constant refreshing mean that it is not as fast as SRAM and is not suitable for certain applications where very low latency and high-speed access are critical.

5. Difference between SRAM and DRAM:

1) **Data Storage and Retention:**
   a) SRAM: SRAM uses flip-flop circuits to store data as long as power is supplied. It does not require constant refreshing and is inherently more stable in retaining data.
   b) DRAM: DRAM stores data as electrical charge in capacitors. This charge leaks over time, necessitating constant refreshing to maintain data integrity.
2) **Access Speed:**
   a) SRAM: SRAM provides faster access times compared to DRAM due to its simpler structure and the absence of refresh cycles.
   b) DRAM: DRAM has slower access times due to the need for refreshing and the more complex read and write circuitry.
3) **Stability and Data Integrity:**
   a) SRAM: SRAM is more stable since data is held using flip-flops. It's less susceptible to external disturbances and does not suffer from the refresh-related issues seen in DRAM.
   b) DRAM: DRAM is more sensitive to noise and disturbances. Refreshing introduces the possibility of data corruption if not managed properly.

4) **Power Consumption:**
   a) SRAM: SRAM consumes more power per bit compared to DRAM. Its stable design requires continuous power to maintain data integrity.
   b) DRAM: DRAM is more power-efficient per bit because it doesn't need constant power to retain data. However, the constant refreshing consumes some power.
5) **Density and Cost:**
   a) SRAM: SRAM cells are larger and more complex, resulting in lower memory density and higher cost per bit. It's used for small, high-speed memory like CPU caches.
   b) DRAM: DRAM cells are smaller and simpler, allowing for higher memory density and lower cost per bit. It's used for larger, main system memory.
6) **Applications:**
   a) SRAM: SRAM is used in applications where speed and low latency are crucial, such as CPU caches and high-performance embedded systems.
   b) DRAM: DRAM is used for main system memory in computers, servers, consumer electronics, and any application requiring large memory capacities.
7) **Refreshing:**
   a) SRAM: SRAM cells do not require refreshing since they are inherently stable.
   b) DRAM: DRAM cells require constant refreshing to prevent data loss, adding complexity and overhead to memory management.

In summary, SRAM offers faster access times, greater stability, and less power efficiency compared to DRAM. However, DRAM provides higher memory density, cost-effectiveness, and is better suited for applications requiring large memory capacities. The choice between SRAM and DRAM depends on the specific requirements of the application and the trade-offs between speed, power consumption, cost, and memory capacity.

Table of comparison:

Feature	SRAM	DRAM
Data storage	Latching circuitry	Capacitors
Refreshing	No	Yes
Speed	Faster	Slower
Power consumption	Higher	Lower
Reliability	More reliable	Less reliable
Cost	More expensive	Less expensive
Density	Lower density	Higher density

- **Literature Survey**

Sr No	Title	Authors	Methodology
1.	A Comparative Study of 6T and 8T SRAM Cell With Improved Read and Write Margins in 130 nm CMOS Technology	RAM MURTI RAWAT, VINOD KUMAR	Swing Restoration for Dual Node Voltage.
2.	Design and analysis of CMOS based 6T SRAM cell at different technology nodes	Meenakshi Devi, Charu Madhu , Nidhi Garg	Predictive technology model (PTM) file
3	Performance Analysis of 6T and 9T SRAM	Ezeogu Chinonso Apollos	Designing 9T SRAM the extra three transistors added to the 6T topology will improve the read, hold and write SNM
4.	Read stability and Write ability analysis of different SRAM cell structures	Ajay Gadhe, Ujwal Shirode	To characterize the DC noise margin of 6T, 8T and 9T SRAM
5.	Static noise margin of 6T and 8T SRAM Cell in 28-nm CMOS	Riya Pateliya	Cells are operated at two different voltages 1.05V and 0.5V.At lower voltage, noise margin should be as high as possible
6.	Static Noise Margin Analysis during Read Operation of 7T SRAM Cells in 45nm Technology for Increase Cell Stability	Shelendra Singh Tomar , Madhav Singh , Shyam Akashe	The techniques studied are based on transistor width, and word- and bit-line voltage modulations
7.	Performance and Analysis ofResilient 6T SRAM cell For Low Leakage and high speed CMOS	Nishtha Deora , Pankaj Shrivastava	By sizing of transistors in 6T SRAM cell an optimized 6T Cache memory cell is attained & evaluated & set up for additional capability than conventional 6T SRAM Cell.

- **Standard 6t SRAM Schematic Explanation**

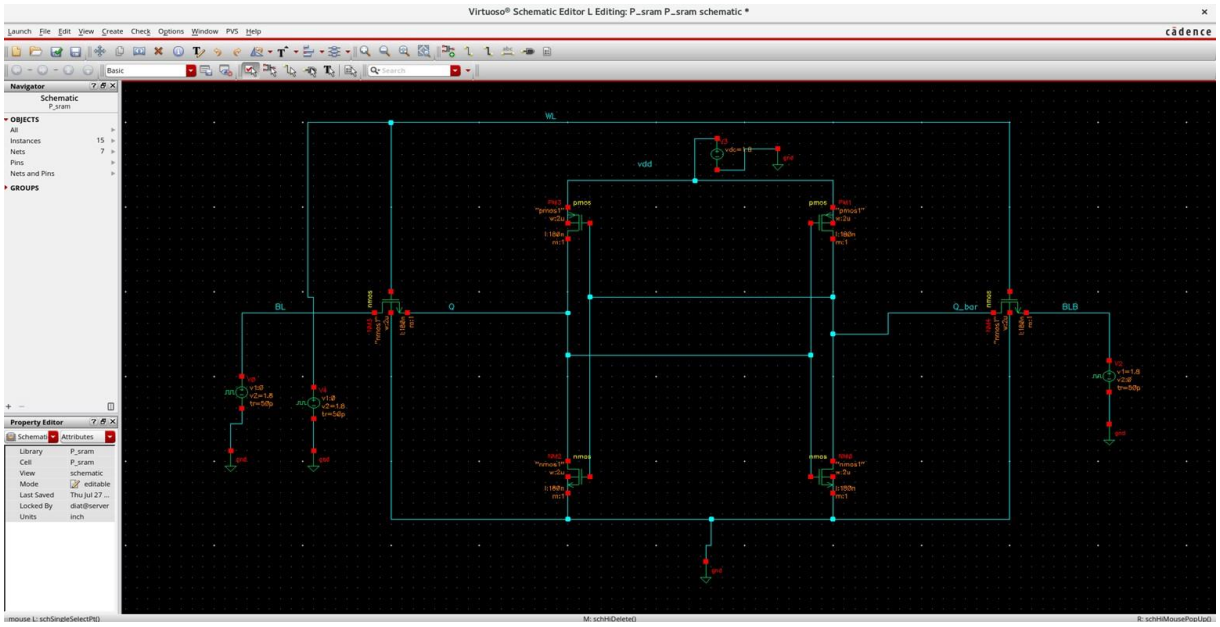


fig: 6T SRAM design using gpdk 180 foundry

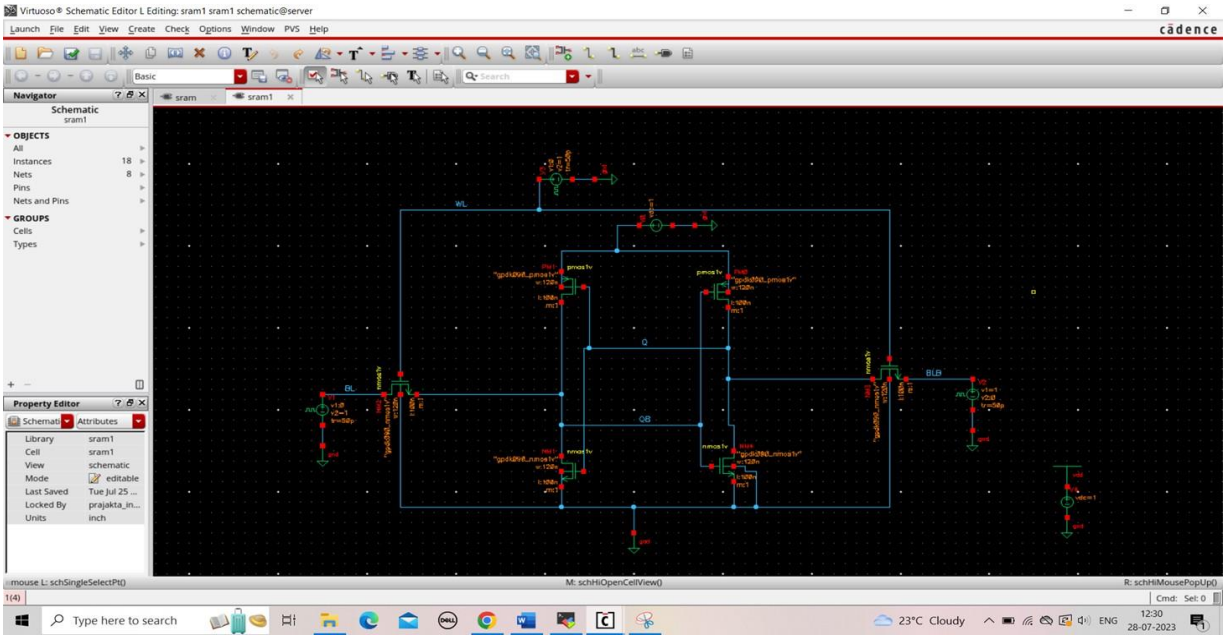


fig: 6T SRAM design using gpdk 90 foundry

According to Moore's law, the number of transistors will continue to double every 1.5 years. That means the same silicon area would accommodate more and more transistors. To achieve this, transistor size is gradually getting reduced. This we say, transistor size is shifting from one technology node to a smaller technology node by scaling process. The numbers 180 nm, 90 nm etc. represent the minimum channel length that can be used in fabrication. The numbers represent the minimum feature size of the transistor (PMOS or NMOS). The minimum feature size means that during the fabrication process of a transistor, how closely can the transistors be placed on a chip to be used for various purposes. The smaller this size is, the larger number of transistors can be fabricated on the chip. For example, suppose separate chips are to be designed using 180 nm and 90 nm transistors. Now, the number of 90 nm transistors that can be placed on a particular area of the chip would be more (nearly twice) than the number of 180 nm ones that can be placed on the same silicon area.

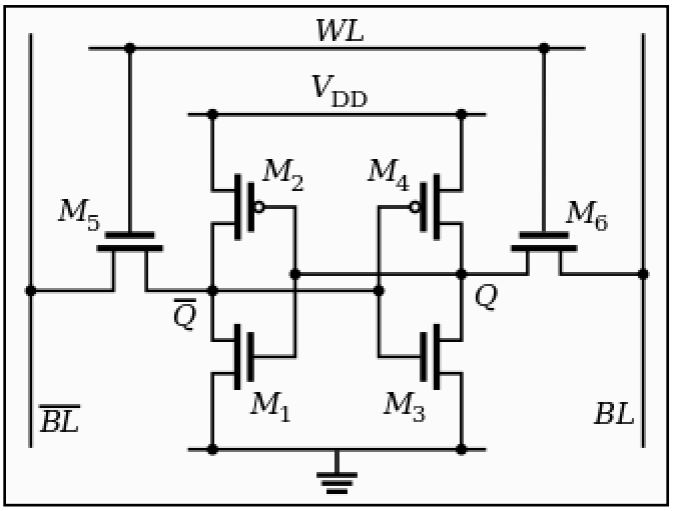


fig: typical 6T sram

A typical SRAM cell is made up of six MOSFETs, and is often called a 6T SRAM cell. Each bit in the cell is stored on four transistors (M1, M2, M3, M4) that form two cross-coupled inverters. This storage cell has two stable states which are used to denote 0 and 1. Two additional *access* transistors serve to control the access to a storage cell during read and write operations.

Access to the cell is enabled by the word line (WL in figure) which controls the two *access* transistors M_5 and M_6 which, in turn, control whether the cell should be connected to the bit lines: BL and BL. They are used to transfer data for both read and write operations. Although it is not strictly necessary to have two bit lines, both the signal and its inverse are typically provided in order to improve noise margins.

SRAM Terminologies:

Bit line (BL): A bit line is a signal line that carries the data from a row of SRAM cells.
Bit line bar (BLB): A bit line bar is a signal line that is the complement of the bit line.
Q: The data stored in a SRAM cell.
Qbar: The complement of the data stored in a SRAM cell.
Word line (WL): A signal line that is used to select a row of SRAM cells.

The bit line and bit line bar are used to read or write data from a row of SRAM cells. When the word line is activated, the transistors in the selected row are turned on, and the data on the bit line and bit line bar is transferred to the sense amplifier.

The sense amplifier amplifies the small voltage signal from the cell so that it can be read or written.

The q and qbar represent the data stored in a SRAM cell. q is the data stored in the cell, and qbar is the complement of the data stored in the cell.

The word line is used to select a row of SRAM cells. When the word line is activated, the transistors in the selected row are turned on, and the data on the bit line and bit line bar is transferred to the sense amplifier.

The significance of these terms is that they are used to describe the operation of SRAM cells. By understanding these terms, you can better understand how SRAM works.

- **Working:**

1. Read Operations:

- The read operation of SRAM is initiated by setting the word line to high. This turns on the access transistors of the SRAM cell, allowing the data in the cell to be accessed. The bit lines and bit line bar are then precharged to a high voltage. This means that the bit lines and bit line bar are initially high, regardless of the data stored in the SRAM cell.
- The read operation is completed by setting the word line back to low. This turns off the access transistors of the SRAM cell, preventing the data in the cell from being accessed. The data on the bit lines and bit line bar can then be read by the CPU.
- The conditions for the read operation are as follows:

  Word line: The word line must be high.
  Bit line: The bit line and bit line bar must be precharged to a high voltage.
  Q: The data in the SRAM cell must be stable.

2. Write Operation:

- The write operation of SRAM is initiated by setting the word line to high. This turns on the access transistors of the SRAM cell, allowing the data in the cell to be accessed. The bit lines and bit line bar are then precharged to a high voltage. This means that the bit lines and bit line bar are initially high, regardless of the data stored in the SRAM cell.
- The data to be written to the SRAM cell is then applied to the bit lines and bit line bar. If the data to be written is a logic 1, the bit line is driven high, and the bit line bar is driven low. If the data to be written is a logic 0, the bit line is driven low, and the bit line bar is driven high.
- The conditions for the write operation are as follows:

  Word line: The word line must be high.
  Bit line: The bit line and bit line bar must be driven to the desired value.
  Q: The data in the SRAM cell must be stable.

3. Hold Operation:

- The hold operation of SRAM is initiated by setting the word line to low. This turns off the access transistors of the SRAM cell, preventing the data in the cell from being accessed. The bit lines and bit line bar are then set to a high-impedance state. This means that the bit lines and bit line bar are not connected to anything, and the data in the SRAM cell is isolated from the rest of the system.
- The hold operation can be terminated by setting the word line to high again. This turns on the access transistors of the SRAM cell, allowing the data in the cell to be accessed again.
- The conditions for the hold operation are as follows:

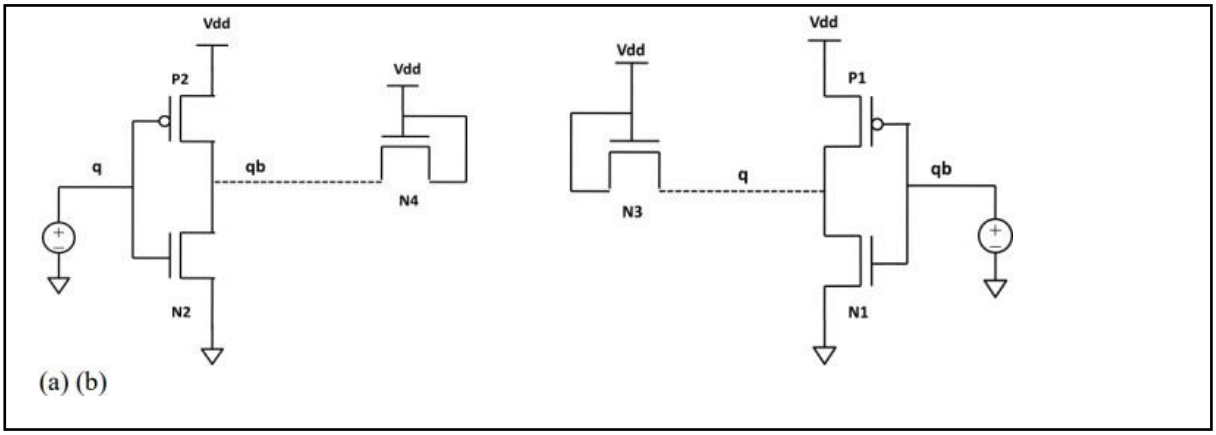
  Word line: The word line must be low.
  Bit line: The bit line and bit line bar must be in a high-impedance state.
  Q: The data in the SRAM cell must be stable.

- **Results**:

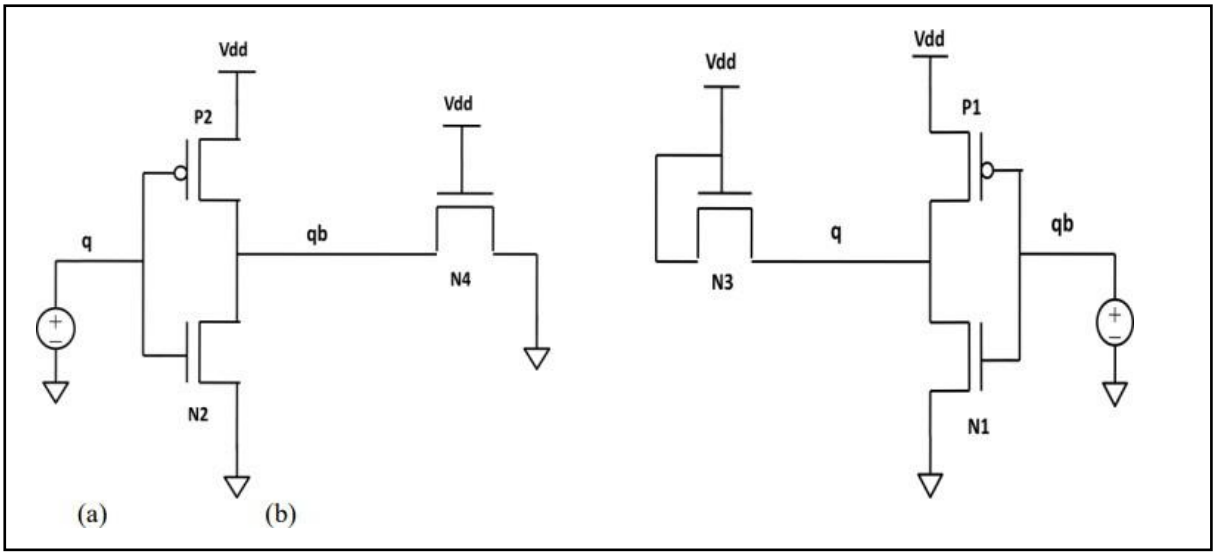
Stability Analysis:

Static Noise Margin helps to determine the stability of the SRAM.The least noise voltage needed to change the cell state is SNM.One of the methods of calculating the Static Noise Margin (SNM) is by plotting the butterfly curve.Butterfly curve is plotted by drawing and mirroring the inverter characteristics and then finding the maximum possible square between them. The length of the side of the square gives SNM. Greater the SNM better is stability

Static Noise Margin in Hold Mode. Inabsence of word line voltage, the ability of SRAM to retain the stored data is defined as hold stability. The Schematics shown in Figure 2 are used for measuring SNM by using butterfly curve measurement method in hold mode.The dashed line in Figure denotes that there is no connection between the circuits



Static Noise Margin in Write Mode. The minimum voltage required to feed new value into the SRAM cell is known as write margin. Write stability is the ability of the SRAM to allow the changes in the stored value. Figure shows the schematic for the calculation of SNM using the butterfly curve method in the write mode of SRAM.



SNM is shown in figures for various technologies

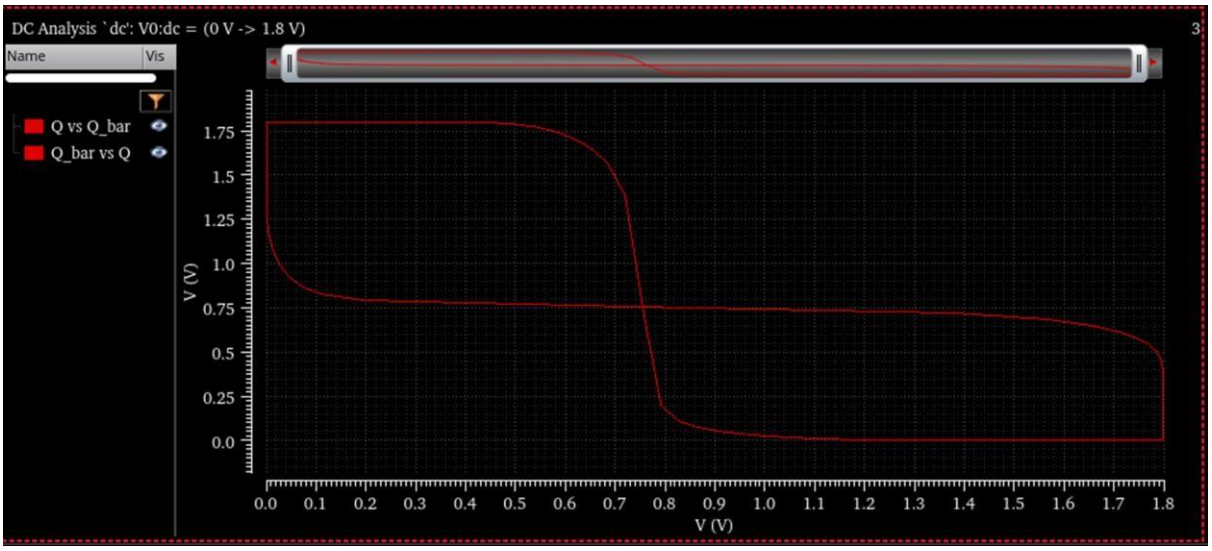


fig: Butterfly curve for 6T SRAM using gpdk180

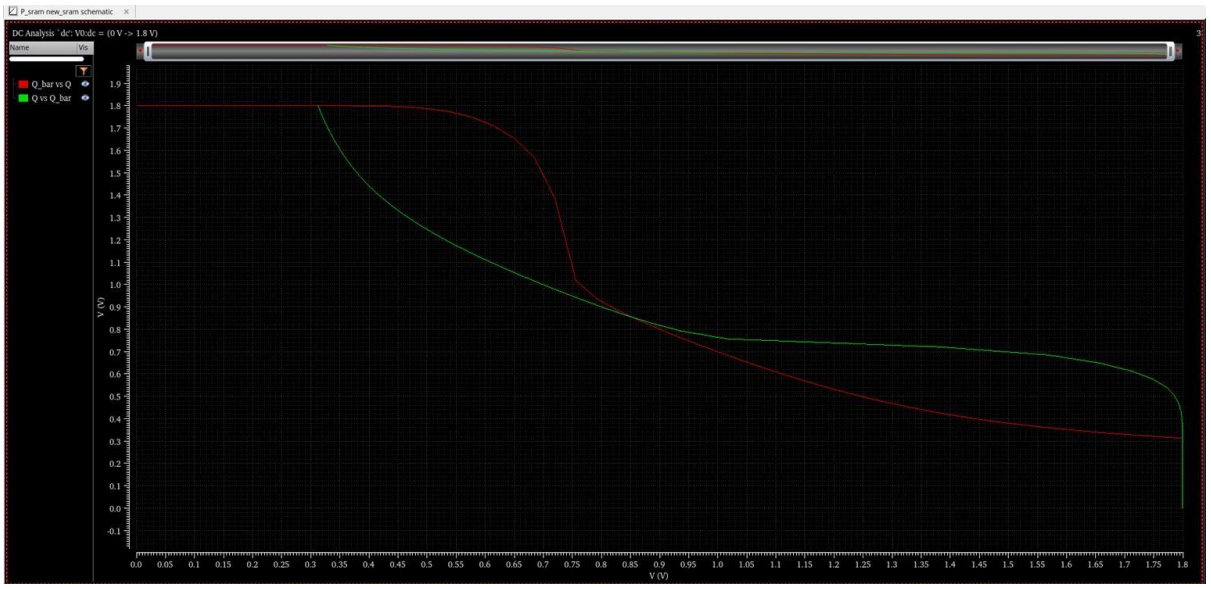


fig: Butterfly curve for 6T SRAM using gpdk90

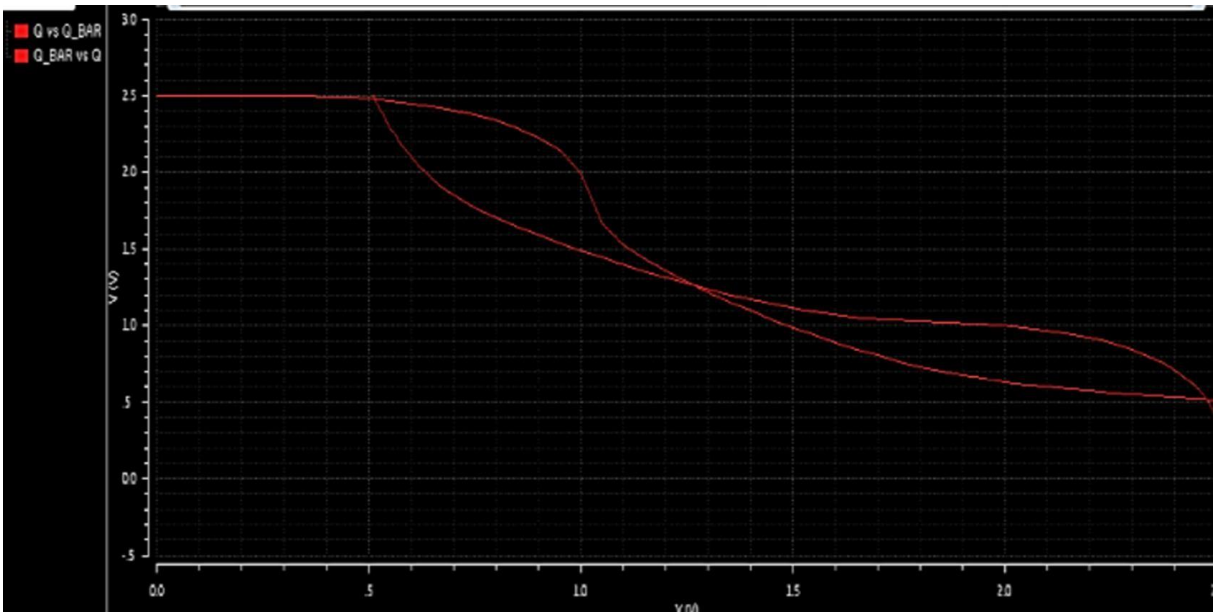


fig: Butterfly curve for 6T SRAM using gpdk90 2V

Table of comparison of SNM in various technologies:

Technology	SNM for write mode	SNM for read mode
Mos 180nm	0.30V	0.34V
Mos 90nm	0.08V	0.18V
Mos 90nm 2V	0.05V	0.15V

- # Conclusion

6T SRAM cell has been designed in this work for 180nm and 90nm technologies. Cadence Virtuoso tool has been used for design and simulation. Static Noise Margin has been estimated for SRAM using nmos1V and nmos2V cells in both 180nm and 90nm technologies. As predicted, SNM gets worse with shrinking technologies; also, it has been observed that CMOS 1v has better SNM as compared to CMOS 2v transistors.