Assignment 9

5.2 Caches are important to providing a high-performance memory hierarchy to processors. Below is a list of 32-bit memory address references, given as a word addresses.

3, 180, 43, 2, 191, 88, 190, 14, 181, 44, 44, 186, 253

5.2.1 For each of these references, identify the binary address, the tag, and the index given a direct-mapped cache with 16one word blocks. Also list if each references is a hit or a miss assuming the cache ~~is~~ is initially empty.

Each block is given to be 1 word size. So there is only 1 word in the block. This shows that there is no need to have an offset bit which is seen as 2^0

Number of offsets bits = 0

Cache = 16

index using 4 bits $2^4 = 16$

Rest of bits = 32 − 4 − 0 = 28 bits

Given the binary address, tag bits are then obtained as shown

The hit/miss depends on comparing tag of the row.

Decimal Address	Binary Address	Tag (shift >> 4)	Index	Hit or Miss
3	0000 0011	0000	0011	Miss
180	1011 0100	1011	0100	Miss
43	0010 1011	0010	1011	Miss
2	0000 0010	0000	0010	Miss
191	1011 1111	1011	1111	Miss
88	0101 1000	0101	1000	Miss
190	1011 1110	1011	1110	Miss
14	0000 1110	0000	1110	Miss
181	1011 0101	1011	0101	Miss
44	0010 1100	0010	1100	Miss
186	1011 1010	1011	1010	Miss
253	1111 1101	1111	1101	Miss

The memory reference 3 is first & then fraction of memory reference is not found. So a miss.

The fractions of remaining memory are not utilized in any upper levels of memory

5.22.

~~Size of~~

For each of these references identify binary address, the tag & the index given a direct-mapped cache with two word blocks & a total of 8 blocks
Also list if each reference is hit or a miss., assuming cache is empty.

Size of tag = 32 - (n+m+2)

N = number of index bits N=3

m = word bits within block m = 1

= 32 - (3 + 1 + 2)

= 26

The cache has 16 blocks.

index values using 3 bit = 2^3 = 8

∴ The last 3 bits after performing the shift are considered as index bits.

(Shift right by 1 bit) modulo (No. of blocks)

Decimal Address	Binary address	Tag	Index	Hit/ miss
3	0000 0011	0000	001	Miss
180	1011 0100	1011	010	Miss
43	0010 1011	0010	101	Miss
2	0000 0010	0000	001	Hit
191	1011 1111	1011	111	Miss
88	0101 1000	0101	100	Miss
190	1011 1110	1011	111	Hit
14	0000 1110	0000	111	Miss
181	1011 0101	1011	010	Hit
44	0010 1100	0011	110	Miss
186	1011 1010	1011	101	Miss
253	1111 1101	1111	110	Miss