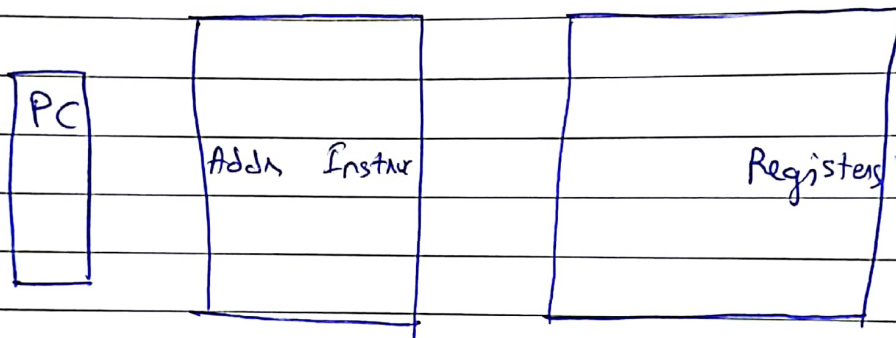


Assignment 5

4.1.1 What are the values of control signals generated by the control in Figure 4.2 for the above instruction.

Instruction = AND R_d, R_s, R_t

Fig 4.2 from text book



Solution :

AND is ALU operation so:
 BSrc will look to register
 OpSel will tell ALU to AND
 MemW is false, memory is not touched.
 RegW is true is true, register R_d is written.
 WBSrc is will set to use output from ALU
 as data RegDst is R_d

PCSrc is $PC + 4$ since no jumps occur.

opcode	ExtSel	BSrc	OpSel	MemW	RegW	WBSrc	RegDst	PCSrc
ALU	*	Reg	Func	no	yes	ALU R_d	R_d	$PC + 4$

4.1.2 Which resources (blocks) perform a useful function for this instruction.

Solution:

Ans) PC, instructionⁿ mem, ALU, registers
We are not using memory or jumping

4.1.3 Which resources (blocks) produce outputs, but their outputs are not used for this instruction which resources produce no outputs for this instruction?

Ans) From my observation

- 1) Branch Add
- 2) Data memory

produce outputs but are redundant.

4.3.1 Consider the addition of a multiplier to ALU. This addition will add 300ps to the latency of the ALU and will add a cost of 600 to the ALU. The result will be 5% fewer instructions executed since we will no longer need to emulate the MUL instruction.

4.3.1 What is the clock cycle time with & without this improvement?

	I _{mem}	Add	Mux	ALU	Regs	D _{mem}	Cost
Latency	400	100	30	120	200	350	100
Cost	1000	30	10	100	200	2000	500

$$\text{clock cycle time} = \frac{1}{\text{clock cycle rate}}$$

~~Ex~~ clock cycle time = 1330ps (without)

clock cycle time = 1330 + 300 = 1630ps (with)

Explanation: Critical path for Iw instruction

$$\begin{aligned}
 & \text{I}_{\text{mem}} \rightarrow \text{Regs} \rightarrow \text{Mux} \rightarrow \text{ALU} \rightarrow \text{D}_{\text{mem}} \rightarrow \text{Mux} \rightarrow \text{Regs} \\
 & = 400 + 200 + 30 + 120 + 350 + 30 + 200 \\
 & = \underline{1330}
 \end{aligned}$$

4.3.2] What is the speed up achieved by adding this improvement?

Solution.

$$\text{speed} = \frac{\text{cpu time old}}{\text{cpu time new}} = \frac{1 \times 1330}{0.95 \times 1630}$$

$$= \cancel{1.3} 0.85889$$

← This means that the new speed is slower than the original speed.

4.3.3] Compare cost/performance ratio with & without this improvement.

Original cost

Σ	Imem	Reg File	control	ALU, Dmem,	2 Adder,	3 mux
	1000	200	500	100 2000	2x30	3x10

$$\Sigma = \underline{3890} \quad \dots \text{Original Cost}$$

New cost

$$3890 + 600 = 4490$$

$$\text{Relative cost} = \frac{4490}{3890} = 1.15$$

$$\text{Cost/perf} = \frac{1.15}{0.85} = 1.3390$$

so this suggests that we are paying more for poor performance.