4.4.4> Which kinds of instructions require this resource?

Answer: In my opinion for Shift-left-2 we can use all the PC relative instructions except jumps that are not PC relative.

4.4.5>For which kinds of instructions (if any) is this resource on the critical path?

Answer:

* For Shift-left-2 there are no instructions because I-Mem is slower and all the instructions need to read the instruction
* We saw in previous part that this is not on the critical path of conditional branches, and it is only needed for PC-relative branches.
* MIPS does not have actual unconditional branches (bne zero,zero,Label plays that role so there is no need for unconditional branch opcodes)
* So for MIPS the answer to this question is actually “None”.

4.4.6>Assuming that we only support beq and add instructions, discuss how changes in the given latency of this resource affect the cycle time of the processor. Assume that the latencies of other resources do not change.

Answer: We know that of the two instructions (BNE and ADD), BNE has a longer critical path which results it determines the clock cycle time.

Now every path for ADD is shorter than or equal to the corresponding path for BNE, so changes in unit latency will not affect this. As a result, we focus on how the unit’s latency affects the critical path of BNE.

This unit is not on the critical path, so the only way for this unit to become critical is to increase its latency until the path for address computation through sign extend, shift left, and branch add becomes longer than the path for PCSrc through registers, Mux, and ALU.

The latency of Regs, Mux, and ALU is 200 ps and the latency of Sign-extend, Shift-left-2, and Add is 95 ps, so the latency of Shift-left-2 must be increased by 105 ps or more for it to affect clock cycle time.