1. Which of the following is not one of the typical instruction types?

A: Memory Load and Store
B: Data processing
C: Set / Get Serial Baud
D: Control Flow

○A ○B ○C ○D Clear Answer Mark For Review

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2. Which of the following is not one of the addressing modes found in processors?

A: Immediate
B: Indirect
C: Register
D: Control

○A ○B ○C ◉D Clear Answer Mark For Review

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3. What is false about a stack?

A: It is used for storing return address when a function is called
B: It is used for storing return address when interrupted
C: It is used for storing interrupt vector address
D: It is used for storing registers that are going to be possibly manipulated in ISR

○A ○B ○C ○D Clear Answer Mark For Review

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4. Find the odd instruction in the following set:

A: JNZ
B: JZ
C: CALL
D: PUSH

○A ○B ○C ○D Clear Answer Mark For Review

5. Find the odd flag in the following:

A: Zero
B: Carry
C: Half Carry
D: Dirty Bit

A B C D Clear Answer Mark For Review

6. Which of the following instruction will copy decimal 10 to accumulator?

A: MVI A, #0AH
B: MVI A, #10H
C: MVI #10H, A
D: MOV A, #10H

A B C D Clear Answer Mark For Review

7. Serial interface in 8051 has following serial communication mode

A: one full duplex synchronous and three half duplex asynchronous
B: three full duplex asynchronous and one half duplex synchronous
C: four asynchronous UART modes
D: four synchronous serial

A B C D Clear Answer Mark For Review

8. An interrupt driven IO is used

A: to handle synchronous input-outputs
B: as interrupt service routine executes fast
C: because the events are asynchronous and during the interval for wait for data the processor can perform other tasks
D: because the events are synchronous and processor can simultaneously perform other tasks

9. Dhrystone is a

A: benchmarking program, which measures the performance of a processor for processing integers and strings (characters)
B: unit of performance with 1 MIPS = 1957 Dhrystone/s
C: benchmarking program, which measures a C program performance for processing integers
D: program for strings processing in DSPs

○ A ○ B ○ C ○ D Clear Answer Mark For Review

10. A processor having Harvard architecture in main memory has
(i) distinct address spaces for accessing the program memory and data memory,
(ii) distinct control signals for accessing the program memory and data memory,
(iii) distinct processor instructions for accessing the program memory and data memory,
(iv) distinct data paths for the bytes for data and for the program,
(v) helps easier handling of streams of data that are required to be accessed in cases of single instruction multiple data type instructions and DSP instructions.

A: all correct
B: i, iii, iv and v
C: i, ii, iv
D: i, iii and iv

○ A ○ B ○ C ○ D Clear Answer Mark For Review

11. Consider the following program segment for a hypothetical CPU having three user registers R1, R2 and R3.

Instruction	Operation	Instruction Size(in words)
MOV R1, 5000;	R1 <= Memory[5000]	2
MOV R2, (R1);	R2 <= Memory[(R1)]	1
ADD R2, R3;	R2 <= R2 + R3	1
MOV 6000, R2;	Memory [6000] <= R2	2
HALT	Machine halts	1

Let the clock cycles required for various operations be as follows: Register to/ from memory transfer: 3 clock cycles ADD with both operands in register: 1 clock cycle Instruction fetch and decode: 2 clock cycles per word The total number of clock cycles required to execute the program is

A: 24
B: 29
C: 20
D: 23

A B C D Clear Answer Mark For Review

12. What are the states of the Auxiliary Carry (AC) and Carry Flag (CY) after executing the following 8085 program?

```
MVI A, FFH
MVI B, 01H
MOV H, A
ADD B
```

A: AC = 0 and CY = 0
B: AC = 0 and CY = 1
C: AC = 1 and CY = 0
D: AC = 1 and CY = 1

A B C D Clear Answer Mark For Review

13. What are the states of the Sign Carry (S) and Parity Flag (P) after executing the following 8085 program?

```
MVI A, 00H

MVI B, 01H

SUB B
```

A: S = 0 and P = 0
B: S = 0 and P = 1
C: S = 1 and P = 0
D: S = 1 and P = 1

A B C D Clear Answer Mark For Review

14. Which one of the following is not a vectored interrupt?

A: TRAP
B: INTR
C: RST 7.5
D: RST 3

A B C D Clear Answer Mark For Review

15. In 8085 microprocessor, the RST6 instruction transfer programme execution to following location

A: 0030H
B: 0024H
C: 0048H
D: 0060H

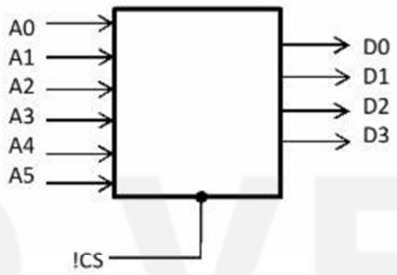
A B C D Clear Answer Mark For Review

16. Groups of flipflops, used to store information are called

A: Registers
B: Resistors-Capacitor Memory
C: Charged Capacitor Memory
D: Logic Families

◉A ○B ○C ○D Clear Answer Mark For Review

17. The following figure best describes which kind of memory



A: 64 x 16 RAM, Active High Chip Select
B: 64 x 4 RAM, Active Low Chip Select
C: 64 x 16 ROM, Active High Chip Select
D: 64 x 4 ROM, Active Low Chip Select

○A ○B ○C ○D Clear Answer Mark For Review

18. A 6 bit DAC has a current output. For a digital input of 110010, the output current of 15mA is produced. What is the Output Current when the digital input is 111001

A: 20mA
B: 17.1mA
C: 188.1mA
D: 13.3mA

○A ○B ○C ○D Clear Answer Mark For Review

19. A motor has an rpm range of 0 – 1000 rpm. In using a 9 bit DAC what will be the maximum error in resolution, when an output voltage of 737 rpm is to be generated

A: 1.957 rpm
B: 0.789 rpm
C: 1.953 rpm
D: 1.168 rpm

○A ○B ○C ○D Clear Answer Mark For Review

20. The error in an ADC is often termed as

A: ADC Error
B: Bit Error Rate
C: Quantization Error
D: Feedback Error

○A ○B ○C ○D Clear Answer Mark For Review

21. What is the binary equivalent of the octal number (7263)?

A: 111010110011
B: 011100100110
C: 011110010111
D: 111000101111

◉A ○B ○C ○D Clear Answer Mark For Review

22. What is the decimal sum of the two binary numbers (1100011000) and (0011100111)?

A: 1024
B: 1023
C: 1012
D: 1234

○A ◉B ○C ○D Clear Answer Mark For Review

23. The two's complement of a number is (10101100). What is the decimal number?

A: 0x84
B: 0x24
C: 0x54
D: 0xAC

◉A ○B ○C ○D Clear Answer Mark For Review

24. The number of bits required to represent the decimal number 12547 using Binary Coded Decimal numbers is?

A: 14
B: 10
C: 16
D: 20

◉A ○B ○C ○D Clear Answer Mark For Review

25. Which of the following is the fastest logic family?

A: CMOS
B: TTL
C: ECL
D: DTL

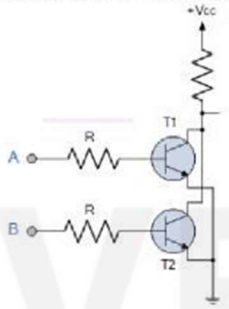
◉A ○B ○C ○D Clear Answer Mark For Review

26. What is the voltage range of TTL family for detecting an input high signal?

A: 3 – 15 V
B: 2 – 18V
C: -0 to -15 V
D: 2 – 5 V

A B C D Clear Answer Mark For Review

27. The following figure is a representation of which logic gate?



A: 2 input AND Gate
B: 2 input OR Gate
C: 2 input NAND Gate
D: 2 input NOR Gate

A B C D Clear Answer Mark For Review

28. Which of the following is an error correcting code?

A: Even/Odd Parity Code
B: Checksum
C: CRC Code
D: Hamming Code

A B C D Clear Answer Mark For Review

29. The consensus algorithm of combinational logic for X, Y and Z variables, defined as X.Y + X'.Z + Y.Z is equivalent to

A: Y.Z
B: X.Y
C: X.Y+X'.Z
D: X

A B C D Clear Answer Mark For Review

30. Simplify the Boolean expression A'C(A'BD)' + A'BC'D' + AB'C

A: B'C+A'D'(B+C)
B: A'D'(C+B) + BC'
C: ABC'
D: 1

○A ○B ○C ○D Clear Answer Mark For Review

31. The product of maxterms for the function F(A, B, C, D) = D(A'+B) +B'D is

A: Σ(0, 2, 4, 5, 6, 8, 12, 14)
B: Σ(1,3, 5, 7, 9, 11, 13, 15)
C: Π(1,3, 5, 9, 9, 11, 13, 15)
D: Π(0, 2, 4, 6, 8, 10, 12, 14)

○A ○B ○C ○D Clear Answer Mark For Review

32. If the output of a circuit depends entirely on the inputs at that time, it is called a

A: Sequential Logic Circuit
B: Asynchronous Circuit
C: Synchronous Circuit
D: Combinational Logic Circuit

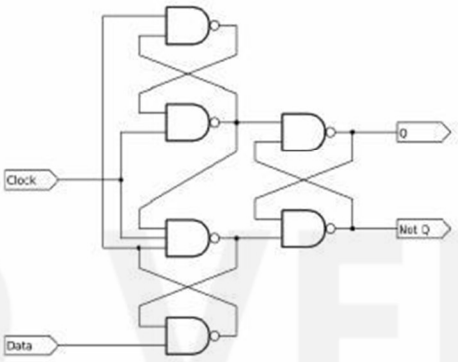
○A ○B ○C ○D Clear Answer Mark For Review

33. Which of the following is a digital circuit that maintains a binary state indefinitely as long as power is supplied to the circuit or the input forces a change of state?

A: NAND Gate
B: Flip-Flop
C: Clock
D: AND Gate

○A ○B ○C ○D Clear Answer Mark For Review

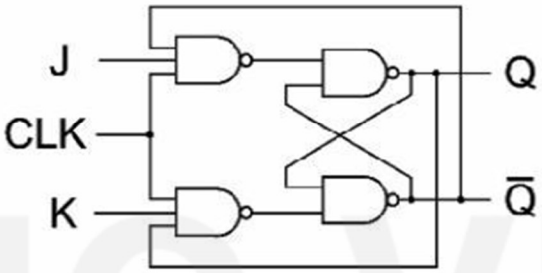
34. The following figure represents which kind of flip flop?



A: T Flip-flop
B: D Flip-flop
C: Positive Edge Triggered D Flip-flop
D: Negative Edge Triggered D Flip-flop

A B C D Clear Answer Mark For Review

35. For the flip-flop shown in the figure below, what is the output state Q(t+1) for the input sequences shown in the truth table?



Q	J	K	Q(t+1)
0	0	0	
0	0	1	
0	1	0	
1	1	1	

A: 0, 1, 0, 0
B: 0, 1, 1, 1
C: 0, 0, 1, 1
D: 1, 1, 0, 0

A B C D Clear Answer Mark For Review

36. Floating point representation is used to store

A: Boolean values
B: Whole numbers
C: Real integers
D: Integers

○A ○B ○C ○D Clear Answer Mark For Review

37. The circuit used to store one bit of data is known as

A: Register
B: Encoder
C: Decoder
D: Flip Flop

○A ○B ○C ◉D Clear Answer Mark For Review

38. WAIT instructions are used for:

A: For synchronization of slow speed peripherals with high speed CPU
B: For counting the clock ticks
C: For addressing peripherals from the CPU
D: None of the above

○A ○B ○C ○D Clear Answer Mark For Review

39. Which one is correct about serial versus parallel bus?

A: Parallel bus would be faster than serial bus
B: Serial bus can be clocked considerably faster than parallel bus, as there is no issue of clock skew between different lines of the bus
C: Serial bus would be slower than parallel bus
D: None of the above

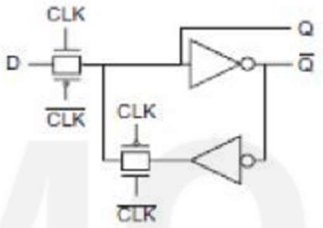
○A ○B ○C ○D Clear Answer Mark For Review

40. Evict buffer is used in:

A: Write-through accesses
B: Write-back accesses
C: Both A and B
D: None of the above

○ A ○ B ○ C ○ D Clear Answer Mark For Review

41. What does below circuit represent?



A: D Flip flop
B: Positive level sensitive D-latch
C: Negative level sensitive D-latch
D: None of the above

○ A ○ B ○ C ○ D Clear Answer Mark For Review

42. In which addressing mode the operand is given explicitly in the instruction

A: Absolute
B: Immediate
C: Indirect.
D: Direct

○ A ◉ B ○ C ○ D Clear Answer Mark For Review

43. The code used to boot up a computer is stored in

A: RAM
B: Cache
C: ROM
D: CPU registers

○ A ○ B ○ C ○ D Clear Answer Mark For Review

44. DMA (Direct Memory Access) controller has following

A: Only master interface
B: Only slave interface
C: Master and slave interface both
D: None of the above

A B C D Clear Answer Mark For Review

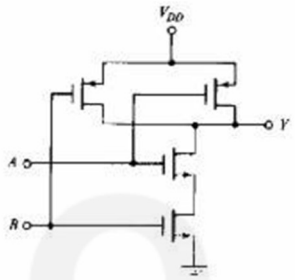
45. Which one of following type of memory can be considered as hard-disk for Smart-Phone:

A: eMMC
B: Micro SD-Card
C: DDR
D: Both A and B

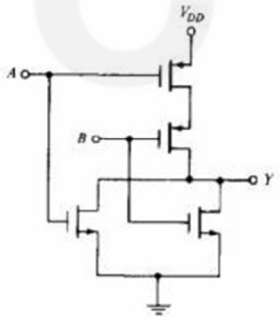
A B C D Clear Answer Mark For Review

46. Which one represents CMOS NAND gate?

A:



B:



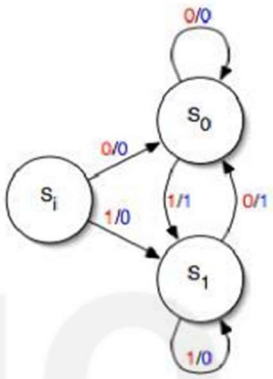
C: Both A and B
D: None of the above

47. Convert octal number (630.4) into decimal:

A: 407.5
B: 408.5
C: 408.4
D: 407.4

A B C D Clear Answer Mark For Review

48. What does below diagram represent?



A: State Diagram
B: Mealy Machine
C: Moore Machine
D: None of the above

A B C D Clear Answer Mark For Review

49. Which of the below option is correct?

A: RISC architecture is LOAD-STORE architecture.
B: RISC architecture is more compiler intensive while CISC architecture is compiler friendly.
C: RISC processors have reduced number of instruction classes while CISC architecture have huge number of instruction classes.
D: All of the above.

○ A ○ B ○ C ○ D Clear Answer Mark For Review

50. There is a 32-bit addressed CPU sub-system with 4-KB, 4-way associative L1 cache; and 4-word cache line size. How many cache line entries would be present in each way?

A: 32-cache lines
B: 1024-cache lines
C: 64-cache lines
D: 256-cache lines

○ A ○ B ○ C ○ D Clear Answer Mark For Review