Tejashree Ingale

System Validation Engineer | DDR5 | CXL | Python Automation | SoC Debug
Bangalore, India
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TECHNICAL SKILLS

Languages: Python, C, DSA, Shell scripting, HTML.
Tools: Phoenix, NGA, Git, JIRA, HSD-ES, Bifrost.
Validation Expertise: Post-silicon validation, Memory subsystem (DDR5, HBM, CXL), BIOS tuning, Debug and performance analysis, Workload automation.
DevOps / Cloud: Docker, Jenkins.
Operating Systems: Linux, Windows.

EXPERIENCE

Intel India Technology Pvt. Ltd., System Validation Engineer *Jan 2021 – Oct 2023*
Bangalore, India

- **Led validation planning** with architects and BIOS teams for **Intel Xeon platforms**, improving requirement alignment and reducing redesign iterations by **20%**.
- Expanded **memory subsystem coverage (DDR5, HBM, CXL)**, enabling **30%** more feature interaction issues to be found **pre-silicon** and reducing customer-facing escapes.
- Designed **Python-based automation** for stress, load, and regression workloads, reducing manual test execution by **40%** and accelerating feature enablement.
- Developed **performance monitoring** and **behavioral checks**, enabling early detection of bottlenecks and improving **post-silicon debug efficiency**.
- Automated **DIMM configuration validation** using **Excel–Python tooling**, cutting setup time by **50%** and eliminating recurring population errors.
- Automated **HPCG benchmarking** via **Intel oneAPI** with **80% memory utilization**, improving performance insight accuracy in **high-load conditions**.
- Executed validation across **memory configurations** up to 512GB, ensuring stable feature enablement and reducing late-stage **system performance issues**.
- Improved **failure triage** and cross-team resolution turnaround by **25%** through structured issue reporting workflows using **HSD** and **JIRA**.
- Delivered **detailed validation summaries** and **debug insights** that improved issue closure efficiency and supported **faster platform readiness** decisions.

ACADEMIC PROJECTS

Pipelined RISC Processor Architecture | *Verilog, RTL Simulation* *Jan 2020 – May 2020*

- Implemented and validated a **Verilog-based**, **5-stage pipelined RISC processor** (MIPS-style ISA) with **custom opcodes** and **RTL simulation**.
- Designed a **high-speed ALU** and evaluated **adder architectures** (Ripple, CLA, Bypass, Carry-Save) to improve **arithmetic performance**.
- Integrated **hazard mitigation** (**forwarding**, **stalling**, **pipeline flush**) and **branch control** to ensure correct **multi-instruction execution**.

EDUCATION

Birla Institute of Technology and Science *Aug 2019 – May 2021, Pilani, Rajasthan*
M.S. in Communication Engineering GPA: 8.01 / 10.

A.C. Patil College of Engineering *Aug 2013 – May 2017, Mumbai, India*
B.E. in Electronics & Telecommunication GPA: 7.75 / 10.