Semiconductor Back-End Process, Episode 2: The Roles, Process, and Evolution of Semiconductor Packaging

May 18, 2023

When sending fragile items in the mail, it is vital to use appropriate packaging to ensure the package arrives at its destination in one piece. Styrofoam, bubble wrap, and a solid box are all required to protect a package's contents. Likewise, packaging is a critical stage of the semiconductor manufacturing process that protects the chip from mechanical and chemical damage. However, the role of semiconductor packaging is not limited to protection.

In this second article of our back-end process series, we will explain the different levels, diverse roles, and evolution of packaging technology.

The Four Levels of the Semiconductor Packaging Process

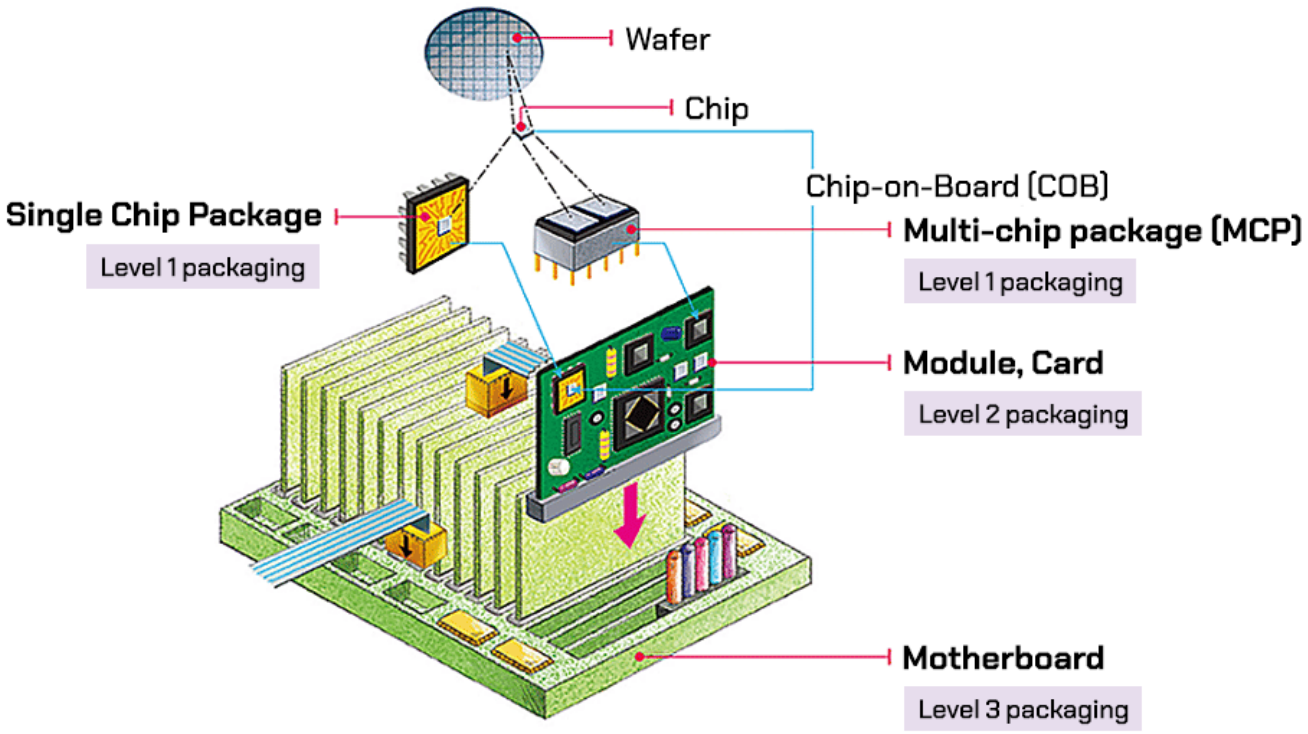
Electronic packaging technology is related to the hardware structure of devices. These hardware structures consist of active elements[1] such as semiconductors and passive

process starting from level 0 packaging which consists of detaching chips through wafer sawing. This is followed by level 1 packaging which is essentially chip-level packaging. Next, level 2 packaging mounts the chip on a module or a card before level 3 packaging equips a card that is mounted with the chip and the module to a system board. In a broad sense, this entire process is commonly referred to as “packaging” or “assembly.” In the semiconductor industry, however, semiconductor packaging generally only refers to the process of wafer sawing and chip-level packaging.

[1] ***Active element**: A device that performs a function due to the circuit implementation, just like a semiconductor memory or a logic semiconductor.*

[2] ***Passive element**: A device that does not have an active function such as amplification or conversion of electrical energy.*

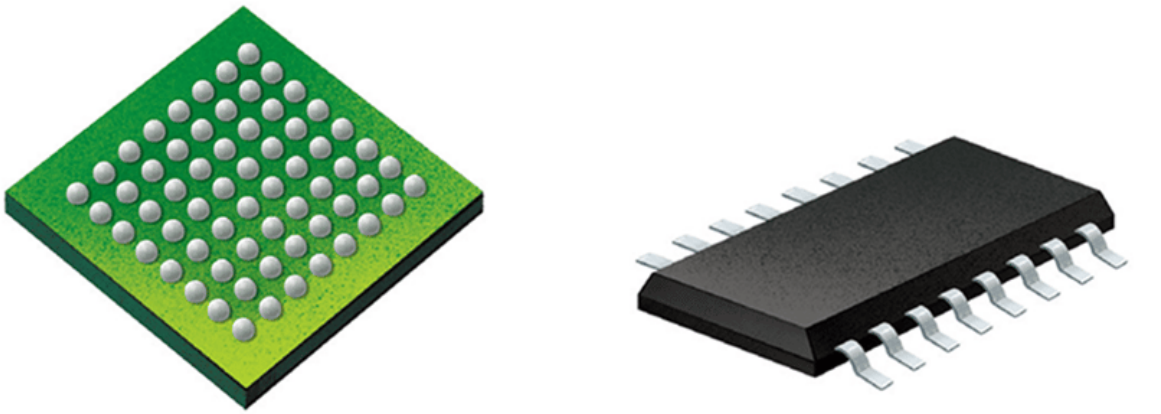
[3] ***Capacitor**: An element that stores electrons and, consequently, provides electrical capacity.*



The package generally takes the form of either the fine-pitch ball grid array (FBGA) or the thin small outline package (TSOP) as shown in Figure 2. While solder[4] balls on a FBGA and lead[5] on a TSOP act as pins, these packages allow the chip to be electrically and mechanically connected with external components.

[4] ***Solder**: A metal that is capable of both electrical and mechanical bonding as it can melt at low temperature.*

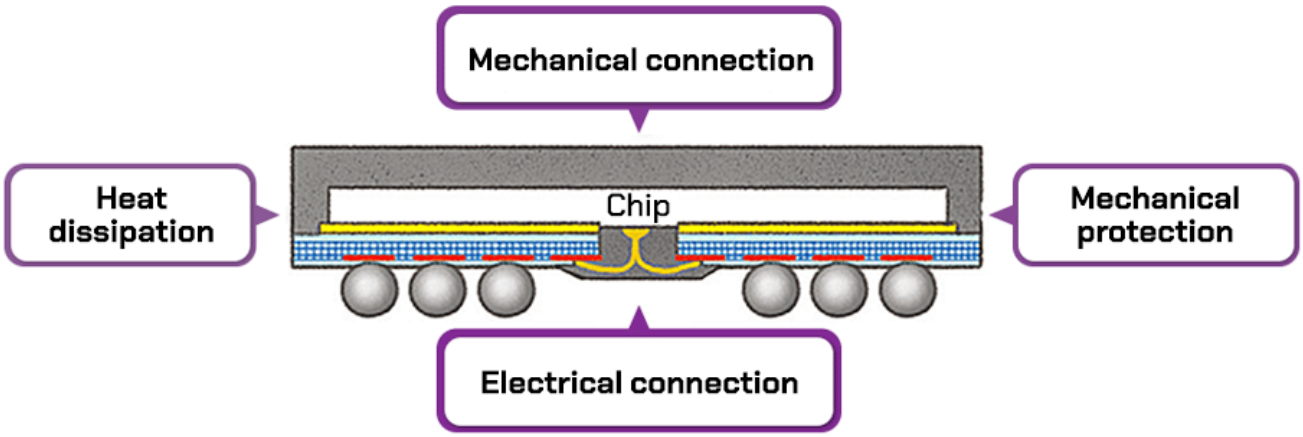
[5] ***Lead**: A wire that emerges from the terminals of an electronic circuit or component to allow connections to a circuit board.*



▲Figure 2. Examples of semiconductor packages (Source: Hanol Publishing)

The Roles of Semiconductor Packaging

and devices from external mechanical and chemical damage by sealing them in [illegible] package materials such as epoxy mold compound (EMC). Although semiconductor chips are made from hundreds of wafer processes to perform various functions, their base material is silicon. Silicon by itself can break as easily as a piece of glass, and the same applies for structures formed after the numerous wafer processes that are also vulnerable to mechanical and chemical damage. Thus, packaging materials prove to be essential in protecting the chips.



▲Figure 3. Roles of semiconductor packaging (Source: Hanol Publishing)

Additionally, the semiconductor package is responsible for electrically and mechanically connecting the chip to the system. The package electrically connects the chip to the system to provide power to the chip while also creating a pathway for the input and output of signals. As for the role of mechanical connection, the chip needs to be well connected to the system to ensure they remain physically attached while in use.

current is flowing. This inevitably creates resistance and then generates hea

Figure 3 shows, semiconductor packages completely surround chips. If the semiconductor package cannot efficiently dissipate heat, the chip may overheat and cause the internal transistors to heat up too much to operate. Thus, it is essential for the semiconductor package to dissipate heat effectively. As semiconductor products become faster and possess more functions, the cooling function of the package has become increasingly important.

Development Trends in Semiconductor Packaging

Figure 4 outlines the six development trends in semiconductor packaging technology over the years. When considering these trends, we can see how packaging has evolved to fulfill its roles.

First off, materials with good thermal conductivity[6] and package structures that can effectively dissipate heat have been developed as heat dissipation has become an important factor in the packaging process.

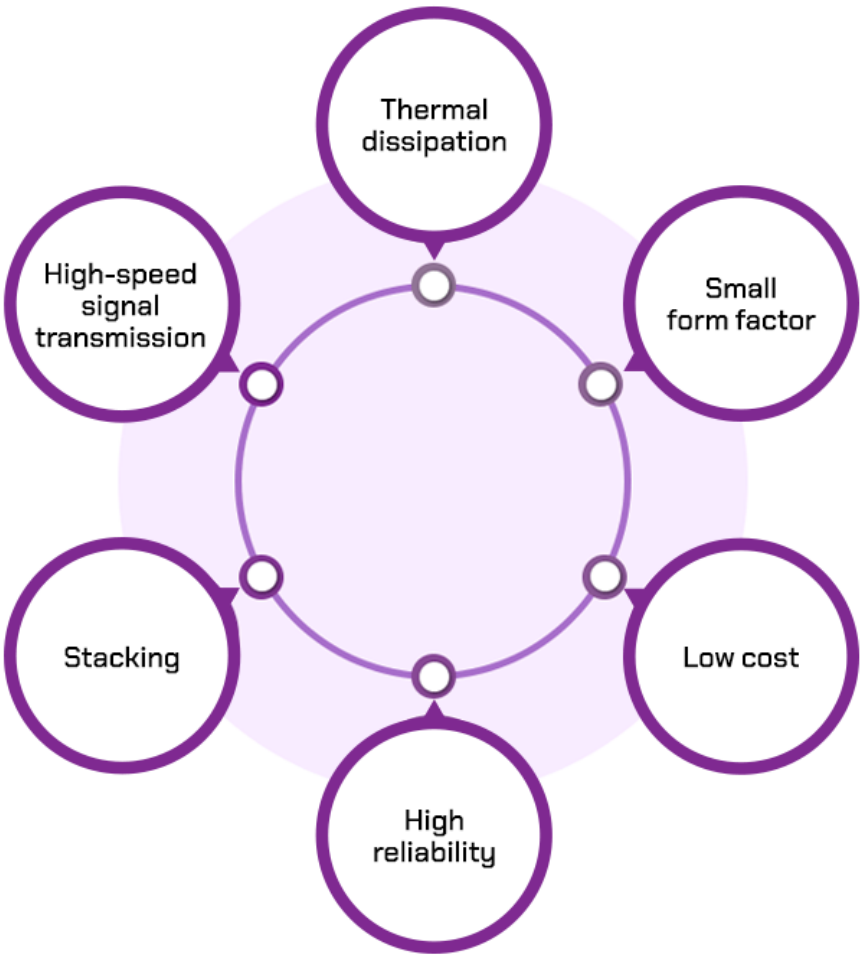
[6] ***Thermal conductivity****: A measure of the transfer of heat from a high temperature area to a bordering lower temperature area without involving the movement of matter.*

The packaging technology which can support high-speed electrical signal transmission is also an important trend, as the packaging can limit the speed of the semiconductor product. For example, if a semiconductor chip or device that can reach a speed of 20 gigabits per second (Gbps) is connected with a semiconductor package that can only support 2 Gbps, the system will perceive the semiconductor to have a speed of 2 Gbps. Regardless of how fast the chip is, the speed of the semiconductor product is greatly affected by the package as the electrical pathway heading to the system is created in the package. This emphasizes how increases in chip speeds need to be

chip[7] packaging and through-silicon via (TSV)[8] have been developed to support high-speed electrical signal transmission.

[7] ***Flip chip***: *An interconnection technology which connects chips and substrates electrically with bumps on the substrate flipped over.*

[8] ***Through-silicon via (TSV)***: *A type of vertical interconnect access (via) that completely passes through a silicon die or wafer to enable the stacking of silicon dice.*



▲Figure 4. Development trends in semiconductor packaging technology (Source: Hanol Publishing)

only one chip was packaged in the past, there are now technologies that pack multiple chips into one package such as multi-chip package (MCP) and system-in-package (SiP)[9].

[9] ***System-in-package (SiP)****: A type of packaging that combines multiple devices into a single package to implement a system.*

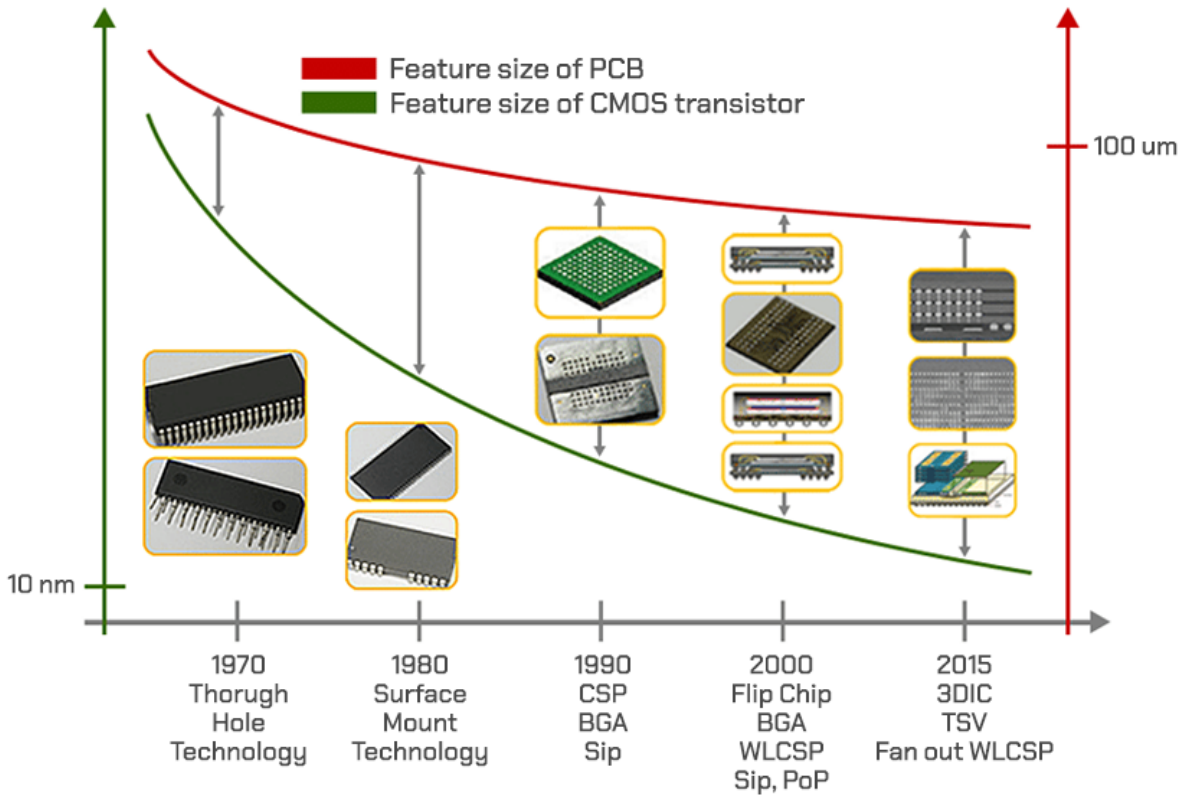
Miniaturization, the process of reducing the size of semiconductor devices, is a trend which has also been applied to packaging technology. As semiconductor products are being implemented in mobile and even wearable products, miniaturization is becoming an important requirement for customers. To meet this demand, many technologies have been developed to reduce packaging size.

Moreover, semiconductor products are increasingly being used in a diverse range of environments. In addition to everyday environments such as the gym, office, or home, they are used in tropical rainforests, polar regions, deep oceans, and even space. As the basic role of the package is to protect the semiconductor chip and device, it is necessary to develop highly reliable packaging technology to enable these semiconductor products to operate normally in these extreme environments.

Lastly, as the semiconductor package is the final product, it is important to develop packaging technologies that have low manufacturing costs and can fulfill desired functions.

Alongside the trends mentioned above that focused on advancing specific roles of packaging technology, another driving force behind the evolution of packaging is the development of the semiconductor industry as a whole. In Figure 5, the red line in the graph represents the change since the 1970s in the feature size of a PCB[10] mounted during the assembly process, and the green line shows the changes in the feature size

components soldered on its surface. These boards are found in most electronic devices.



▲Figure 5. Changes over the years in the feature size of wafers and PCBs (Source: Hanol Publishing)

In the 1970s, the difference of the feature size in PCBs and wafers was relatively small. However, wafers today are being mass-produced and CMOS transistors are being developed to have feature sizes smaller than 10 nanometers (nm), while PCBs still have features sizes in the 100 micrometer (um) range. This gap has widened significantly over the decades.

As the boards are fabricated in the form of panels and there are other factors such as

photolithography which has widened the gap in sizes with PCBs. The problem semiconductor package must compensate for this difference between a PCB and a wafer, as it is tasked with individualizing the chips cut from the wafer and mounting them on the PCB. This difference in the feature size was not significant in the past, so it was possible to use through-hole technology—where the semiconductor package's lead is inserted in the socket of the PCB—such as dual in-line package (DIP)[11] or zig-zag in-line package (ZIP)[12]. However, as the gap grew wider, it became necessary to use technology that attached leads to the surface of the board such as TSOP, which is a type of surface-mount technology (SMT)[13]. Subsequently, packaging technologies such as ball grid array (BGA), flip chip, fan out wafer level chip scale package (WLCSP)[14], and through silicon via (TSV) were developed sequentially to compensate for the widening gap between the wafer and board's sizes.

[11] ***Dual in-line package (DIP)****: A package where electrical connection pins are arranged in two parallel rows.*

[12] ***Zig-zag in-line package (ZIP)****: A package where the pins are arranged in zig-zag form, a replacement for the dual in-line package to increase mounting density.*

[13] ***Surface Mount Technology (SMT)****: A package mounting method that fixes a chip to the system board surface via soldering.*

[14] ***Wafer level chip scale package (WLCSP)****: A variant of flip chip technology which packages integrated circuits at the wafer level. Fan out WLCSP features connections for the package which spread out ("fan out") beyond the chip's surface.*

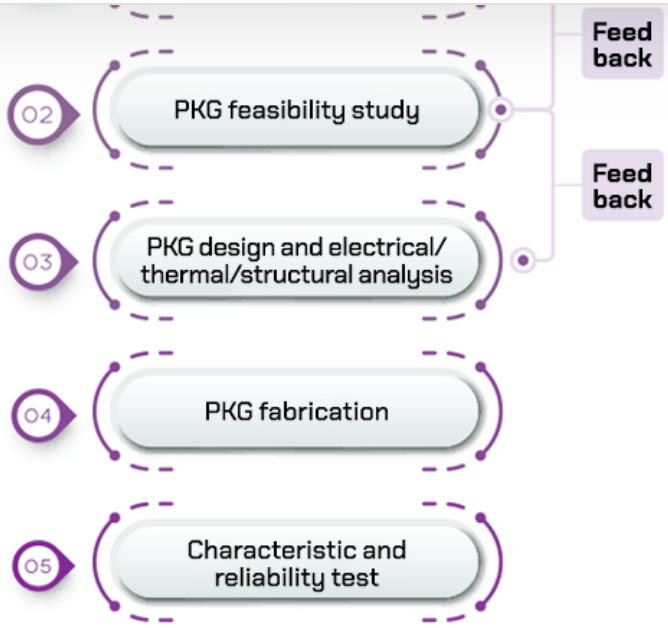
Ensuring Effectiveness of Semiconductor Packaging Through Testing

There are two methods to develop a semiconductor package and ensure it works effectively. The first involves using existing packaging technology to create a package suitable for a newly developed semiconductor chip and evaluating the package. The

In general, it is not common to develop a new chip and apply a new packaging technology at the same time as it is difficult to identify the cause of any problems after the packaging is completed if both the chip and the packaging are untested. Therefore, new packaging technologies are tested with existing mass-produced chips that are known to have few defects in order to verify the packaging technology alone. Once a packaging technology is verified, it can then be applied to the development of new chips and, furthermore, lead to the production of semiconductor products.

Figure 6 shows the packaging development process for a new chip. Normally, the design of the chip and the package is developed together when fabricating a semiconductor product so that their characteristics can be optimized holistically. For this reason, the packaging department looks at whether the chip is packageable before it is designed. During this feasibility study, the package's design is roughly tested so the electrical, thermal, and structural evaluations can be analyzed to ensure that there would be no problems in the actual mass-production stage. In this context, semiconductor packaging design refers to the wiring design of the substrate or leadframe, which is the medium for the chip to be mounted on the board.

The package department provides feedback to the chip designers on the packages' feasibility based on the results of the package's temporary design and analysis. The chip design is only completed when the package feasibility study is finished. This process is followed by wafer fabrication. While the wafers are being fabricated, the package department designs the substrate or leadframe required for package production and proceeds with its production through a company that carries out the back-end process. At the same time, tools for the package process are prepared in advance, and package production begins immediately when the wafers are delivered to the package department after the wafer test.



▲Figure 6. The development process for semiconductor packaging (Source: Hanol Publishing)

Semiconductor products must be manufactured in packages so that their physical characteristics can be measured and verified. Meanwhile, the design and the processes can be checked with evaluation methods such as a reliability test. If the characteristics and reliability are not satisfied, the cause is investigated and the process is repeated again from the stage where the cause can be resolved. Ultimately, development is only completed after the desired characteristics and reliability standards can be met.

Looking Beyond the Roles of Semiconductor Packaging

As we looked into packaging technology's role of protecting and connecting various components of a semiconductor, it will also be vital to know which materials and methods are used in this process. The next episode will touch on the differences

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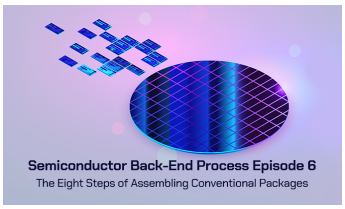

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