Semiconductor Back-End Process Episode 1: Understanding Semiconductor Testing

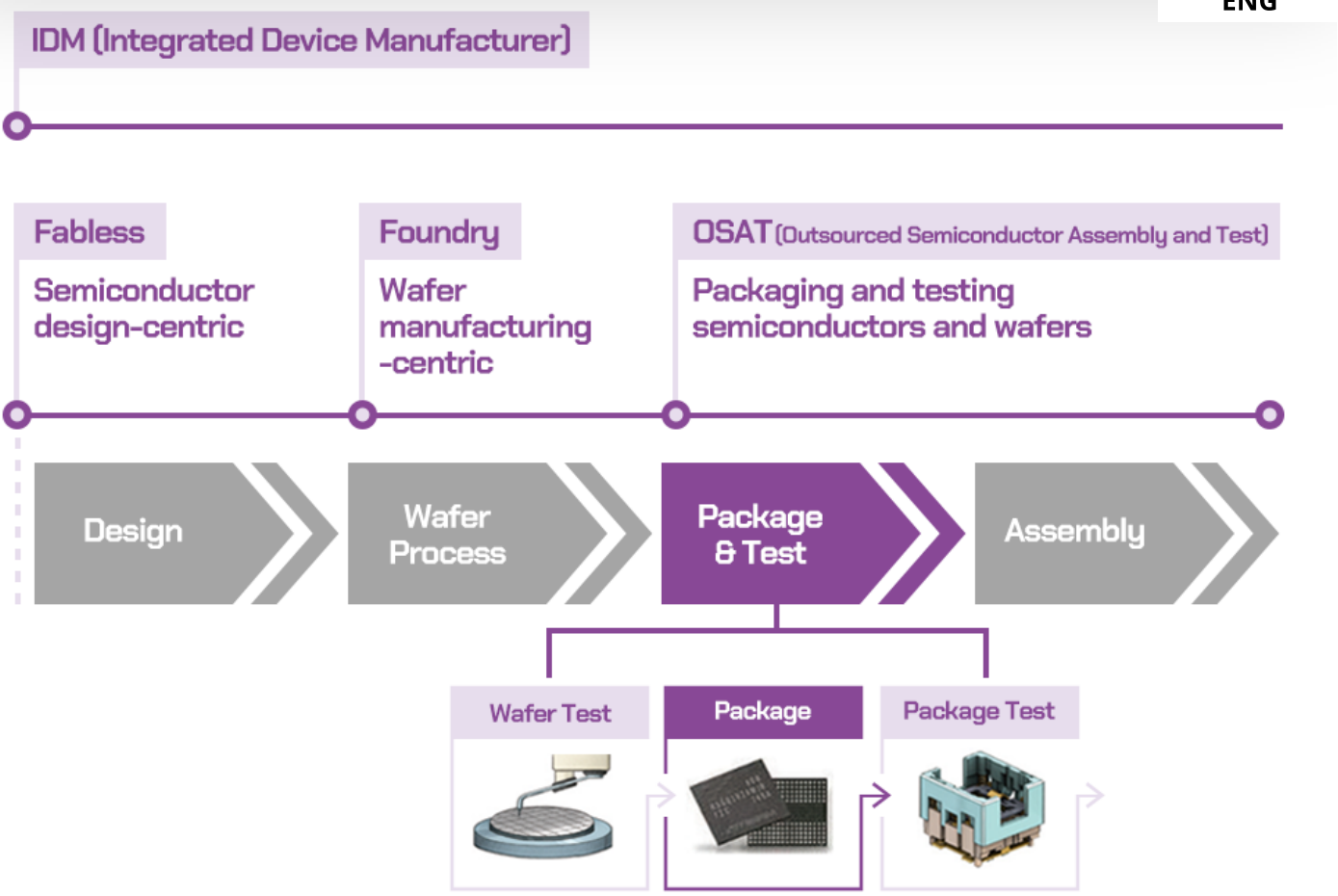
April 6, 2023

The process of making semiconductors is split into two main stages: the front-end process of manufacturing wafers and engraving circuits, and the back-end process of packaging the chips. As the miniaturization of semiconductors has now nearly reached its limit, the importance of the back-end process has been growing.

This episode will explain the various packaging and testing practices that are required in the later stages of semiconductor manufacturing to ensure the accuracy and quality of the products.

The Back-end Process of Semiconductors

The simple order of the manufacturing process consists of the wafer process, the packaging process, and testing. The front-end process refers to the manufacturing of wafers, while the back-end process consists of packaging and testing. Even the wafer manufacturing process is split into a front-end and back-end process. The front-end



▲ Figure 1. The relationship between the semiconductor manufacturing process and the semiconductor industry (Source: Hanol Publishing)

Figure 1 is a flow chart that shows the relationship between the semiconductor manufacturing process and the semiconductor industry. Companies like Qualcomm and Apple that only design semiconductors are called “fabless.” Products designed by fabless companies are made into wafers, and the facilities that produce these wafers are called “foundries.” Global companies with these facilities include Taiwan’s TSMC and UMC. Then, there are companies that test and package products that were designed by fabless vendors and, later, made into wafers at foundries. These are

Device Manufacturer), and SK hynix is one of the leading IDMs in the world.

As shown in Figure 1, the first phase of the packaging and testing process is wafer testing. Afterwards, packages are made in the packaging process and followed by the package test stage.

One of the main reasons for semiconductor testing is to prevent the shipment of defective products. Therefore, it's necessary to have an exhaustive inspection process that includes various types of testing to secure the quality and reliability of the products. But these extensive processes increase testing time, equipment, required manpower, and manufacturing costs.

Testing Temperature, Speed, and Movement

Test by Temperature	Test by Speed	Test by Operation
Hot Test	Core Test	DC Test
Cold Test	Speed Test	AC Test
Room Test		Function Test

▲ Table 1. Test classification (Source: Hanol Publishing)

and operation—as shown in Table 1.

The temperature applied to the test subject is the standard for temperature tests. Hot tests apply a temperature of 10% or more above the maximum temperature stated in the products' spec[1], while cold tests apply a temperature 10% or less than the minimum temperature. Room tests usually apply a temperature of 25°C (77°F). Since semiconductor products are used in different settings with various temperatures, these tests exist to verify the product's ability to operate under various temperatures and to know their temperature margins.

[1]***Spec**: As the abbreviation for "specifications," the term refers to the blueprint that outlines what's required during the manufacturing of products such as design regulations, manufacturing methods, or regulations of desired properties in products.*

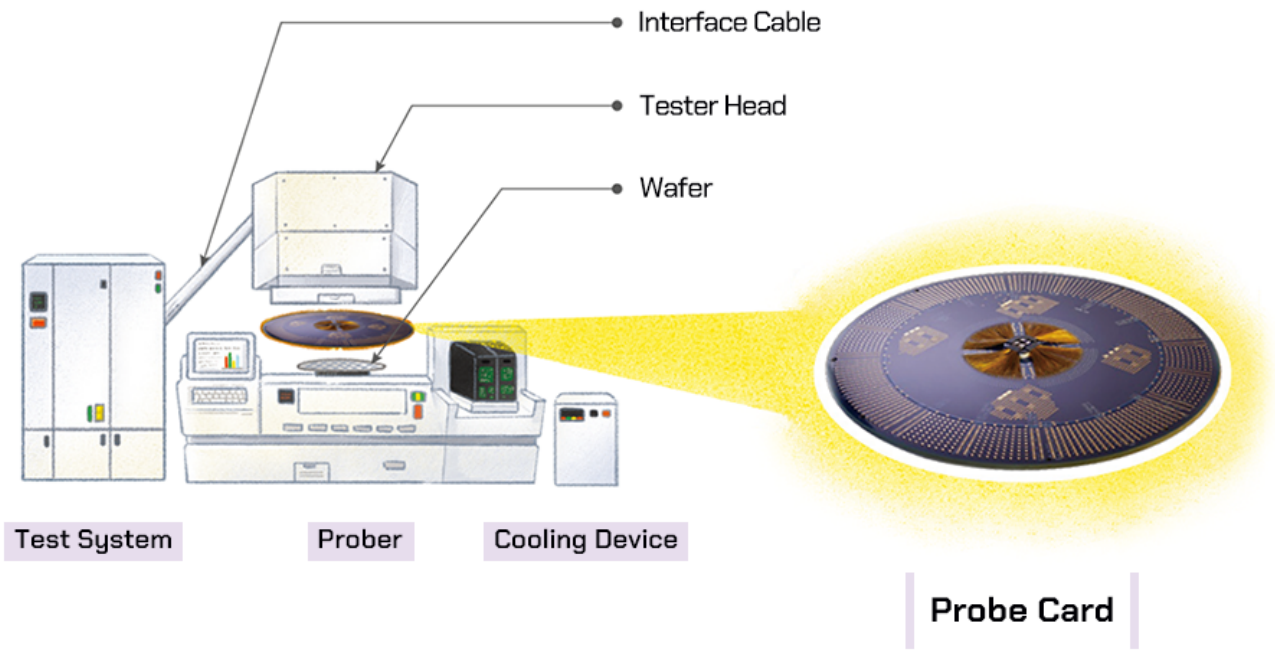
Speed tests are divided into core tests and speed tests. Core tests evaluate whether the core operation, or the main purpose, of a semiconductor performs properly. In the case of semiconductor memories that store data, testing looks at whether data is properly stored in the cell area. Speed tests measure the operating speed, so products are evaluated on whether they can operate at the desired speed.

Operation tests can be divided into three categories: DC tests, AC tests, and function tests. DC tests allow currents to pass into DC so electrical measurements are shown in the form of currents or voltage. Function tests turn on each function of a product to check if they operate properly.

The Process of the Wafer Test

Wafer tests inspect the properties and qualities of the numerous chips that are on a wafer. For the test, the testing equipment and the chips need to be connected to send

electrical connection with the test equipment is relatively easy. However, in the case of wafers, a probe card is required.



▲ Figure 2. Infographic of wafer testing system (Source: Hanol Publishing)

As shown in Figure 2, many probes[2] are built on the top of the card to make physical contact with the pad of the wafer. The wiring that connects the probe and the test equipment is built into the card. These probe cards are mounted on the tester head so they can make contact with the wafer on the prober where they are loaded.

[2]***Probe**: A needle that makes physical and electrical contact with the wafer pad on the probe card.*

When a wafer is loaded with the front side facing up, the probe card on the right is turned over. Then, a probe is mounted on a tester head so that the wafer and probe

system applies the current and signal through the probe card and then rea

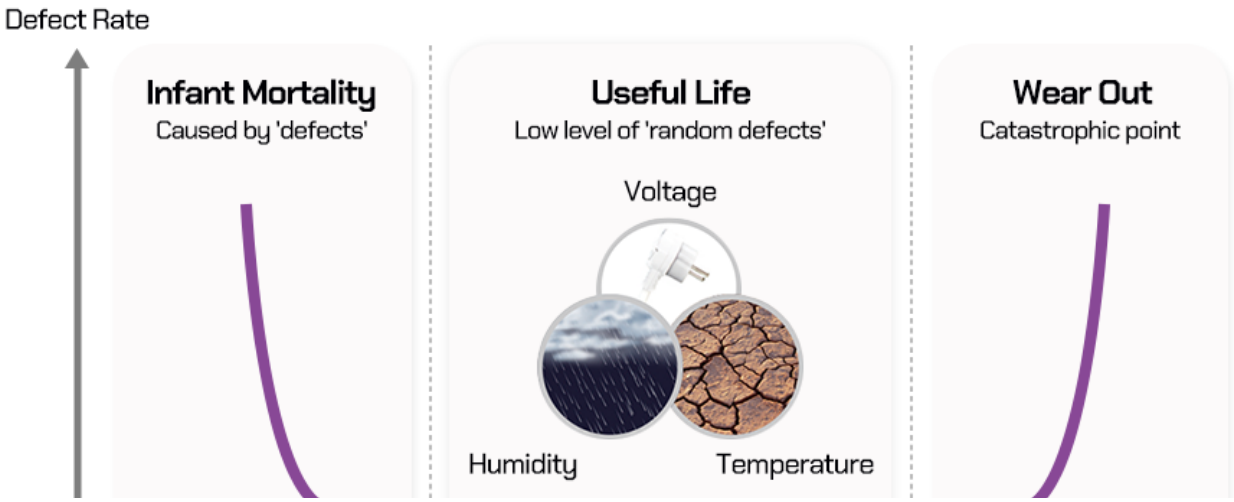
results from it.

Wafer testing usually follows the following process: EPM (Electrical Parameter Monitoring) → Wafer Burn-in → Test → Repair → Test. These steps are described below.

EPM (Electrical Parameter Monitoring)

The purpose of testing is to filter out defective products, but it also has the goal of improving products that are under development or being mass-produced by providing feedback on their deficiencies. The main purpose of EPM is to give feedback on the wafer manufacturing process by evaluating and analyzing the electrical characteristics of the product's unit devices. This is a process of measuring transistor characteristics and contact resistance using electrical methods before actual testing to verify whether the manufactured wafer satisfies the basic properties suggested by the design and device departments.

Wafer Burn-in



▲ Figure 3. Defect rate according to product usage time (Source: Hanol Publishing)

Figure 3 shows the defect rate during product life as a function of time. As it resembles the shape of a bathtub, it's also called a bathtub graph. In the early stages of its lifecycle, there are many early failures, or failures caused by manufacturing defects. When defects from manufacturing are resolved, random failures, or the defect rate during the service life of the product, happen less often. Moreover, when the product wears out, defect rates rise again.

Burn-in is carried out to detect early defects in advance by prompting potential product defects on purpose. Wafer burn-in applies temperature and voltage to stress the wafer product, so any defects that may appear in the initial failure period are exposed.

Wafer Test

Wafers that went through early failure tests via wafer burn-in are then tested with a probe card for a wafer test. Wafer testing is the process of examining the electrical characteristics of a chip at the wafer level. The test serves several purposes including pre-detection of defective chips, giving device and design feedback through wafer-level verification, and sorting out defects that will occur during packaging/mounting[3] ahead of time. This last procedure ensures that the cause of defects at the wafer level can be analyzed and feedback on the manufacturing process can be provided. If defects are sorted in the wafer test, some of the defective cells[4] can be replaced with redundancy cells through a process called repair.

consists of one transistor and one capacitor.

Repair

Mainly performed with semiconductor memories, the process of repair replaces defective cells with surplus cells by applying the repair algorithm. For example, if 1 bit is defective as a result of a wafer test consisting of a DRAM 256-bit memory, the product will have 255 functioning bits. However, if a surplus cell replaces the defective cell, the chip becomes a quality product that satisfies the 256-bit spec again and can be sold to customers. Through repair, yields eventually increase. For this reason, semiconductor memories create surplus cells during design so they can make substitutes according to test results.

Packaging Test

A chip determined to be a quality product in the wafer test undergoes a packaging process, and the completed package undergoes a packaging test again. Even if the wafer is found to be a quality product during the wafer test, defects may occur during the packaging process. Therefore, the packaging test is essential.

For the packaging test, the package pin (the solder ball in #3 of Figure 4) should be faced down and put into the socket so that it can come into contact with the pins in the socket. Then, the packaging test socket is mounted on a package test board to perform a packaging test.

Package Test Board Package Test Socket

▲ Figure 4. Packaging test system (Source: Hanol Publishing)

TDBI (Test During Burn-in)

Burn-in is a test that stresses a product with voltage and temperature in order to eliminate potential defects in the product at an early stage. Burn-in performed after packaging is called TDBI. Burn-in can be performed on the wafer or on the package, but most semiconductor manufacturers burn-in the wafer and the package simultaneously.

Test

This is the process of determining whether a semiconductor operates normally in the user's environment as defined in the datasheet[5]. A temperature corner test is performed to verify that the product meets the specifications for AC/DC factor weakness and operations requested by the customer in the Cell & Peripherals areas.

[5]***Datasheet**: A regulation document that defines the properties that can be found in a semiconductor product.*

Visual Test

When testing is completed, the test results must be recorded on the exterior of the package and, consequently, laser marking is required. After the package test has been completed and marked, the quality package is placed in the package tray. Now, the only remaining step is to ship the product to the customer. Therefore, it is necessary

manufacturers sort out pressed balls, missing balls, and other defects.

<Other articles from this series>

Semiconductor Front-End Process Episode 1: The Birth of Computers, Transistors, and Semiconductors

Semiconductor Front-End Process Episode 2: Protecting Key Components Through Oxidation

Semiconductor Front-end Process Episode 3: Forming Patterns on Wafers Through Photolithography

Semiconductor Front-End Process Episode 4: Etching Fine and Identical Wafer Patterns

Semiconductor Front-End Process Episode 5: Supporting Wafer Miniaturization Through Deposition

Semiconductor Front-End Process Episode 6: Metallization Provides the Connections That Bring Semiconductors to Life

Semiconductor Back-End Process, Episode 2: The Roles, Process, and Evolution of Semiconductor Packaging

Semiconductor Back-End Process Episode 3: Understanding the Different Types of Semiconductor Packages

Semiconductor Back-End Process Episode 4: Understanding the Different Types of Semiconductor Packages, Part 2

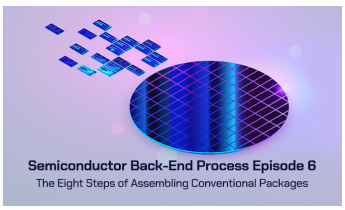
Semiconductor Back-End Process Episode 5: Package Design and Analysis

By **Suh Min-suk**

Technical Leader of PKG Development, SK hynix

TAG #semiconductor #Wafer #back-end process #testing

RELATED POSTS



Semiconductor Back-End Process Episode 6: The Eight Steps of Assembling

Open Communication, Creative Research, and Agile Problem-Solving: The Keys

The Story Behind SK hynix's AAA-Rated Global Compliance Program

[Tech Pathfinder] Small Size, Big Impact: Unveiling the Latest Advances in

SK hynix NEWSROOM

ENG