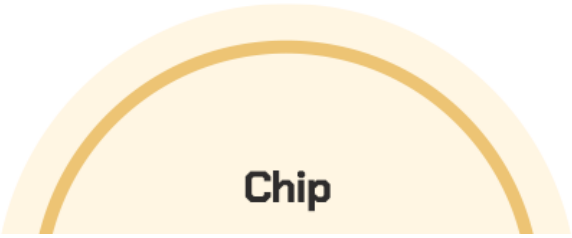
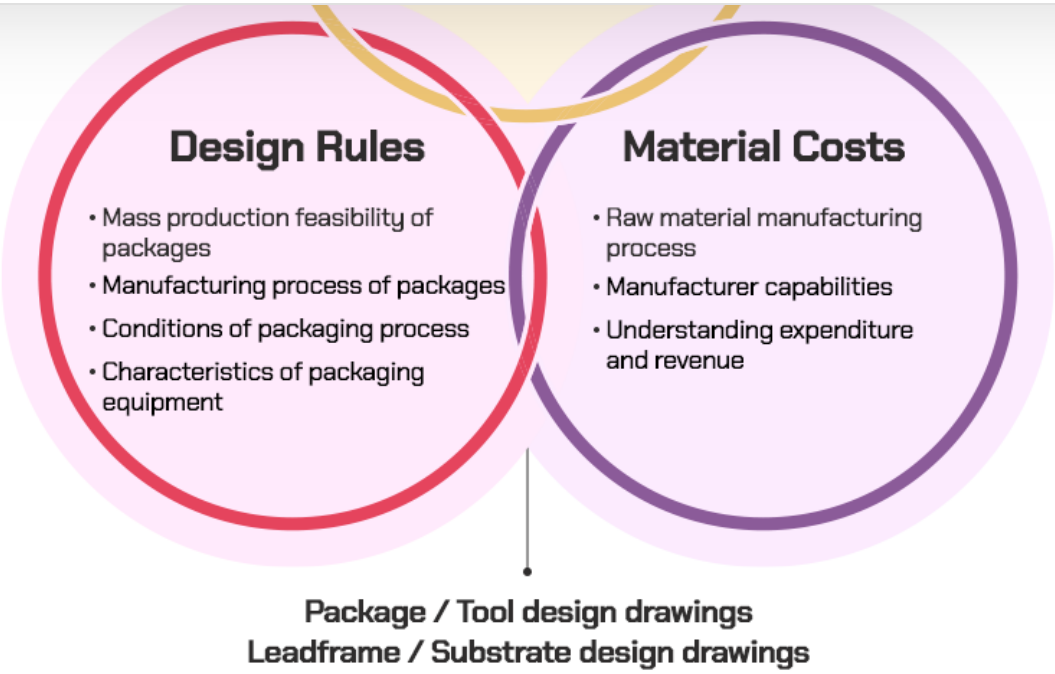
Semiconductor Back-End Process Episode 5: Package Design and Analysis

July 25, 2023

In recent years, semiconductor packages have become increasingly complex which has led to a growing emphasis on design. The semiconductor package design process involves various engineers and industry players sharing information about materials, conducting feasibility tests, and optimizing characteristics of the package. Having explored the different types of packages in the previous episode, this article will explain the stages of the semiconductor design process in detail and introduce the different analyses that ensure the packages act as high-quality interconnection platforms for semiconductors.

The Process of Semiconductor Package Design





▲Figure 1. Aspects of semiconductor package design (Source: Hanol Publishing)

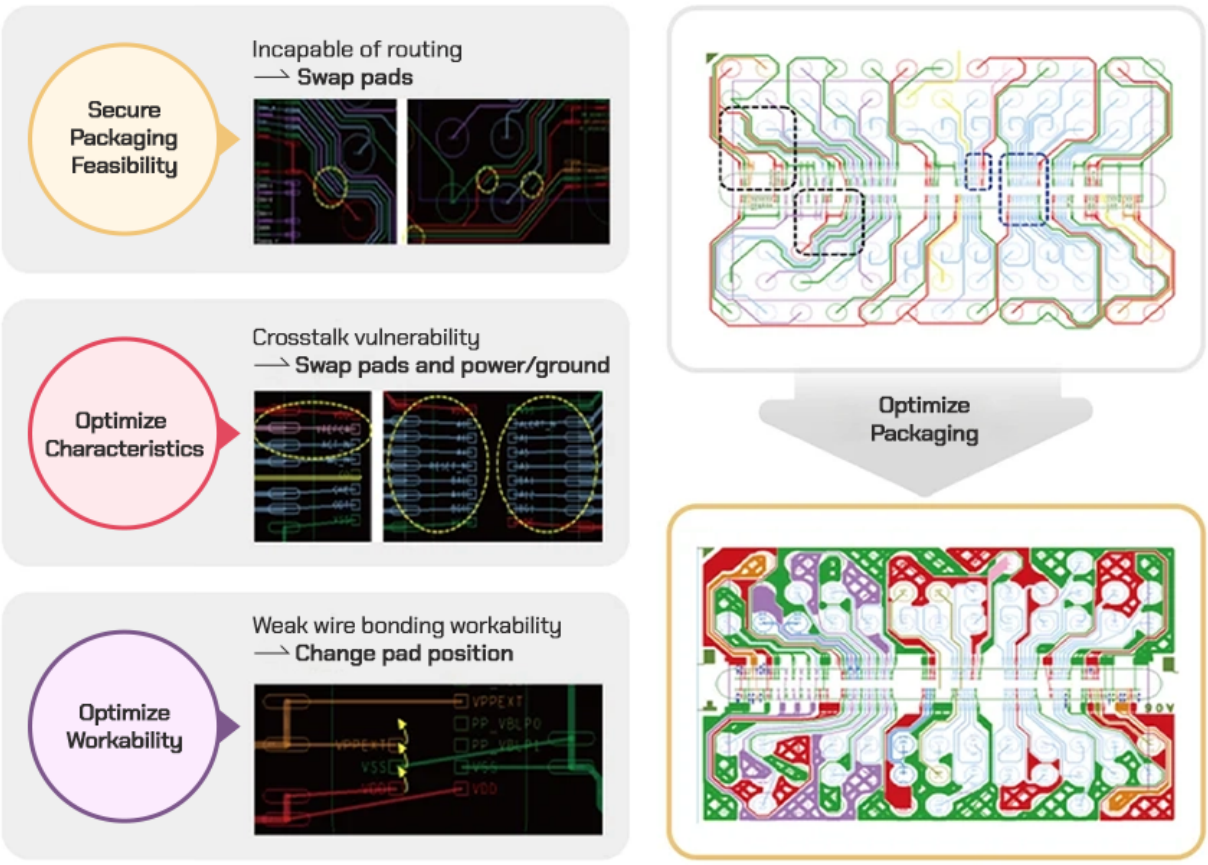
Figure 1 displays the various aspects of semiconductor package design. The design process begins with the department responsible for the chip design providing key information, including the chip pad coordinates, chip layout, and package interconnection data. Then, based on the packaging material, the team designs the structure of the semiconductor package which consists of the substrate and the leadframe. This process involves applying design rules that consider the package's mass production, manufacturing process, process condition, and required equipment.

The package's feasibility should be reviewed at the beginning of development and, afterwards, given to chip and product designers for feedback. Once the feasibility study is completed, orders must be placed to system semiconductor manufacturers with design drawings of the package, tools, leadframe, and substrate. While the

connections must be shared in advance with package process and manufacturing engineers.

When these design drawings are shared, package design engineers conduct a feasibility test by connecting the package solder ball layout and the chip's pad sequence to check whether wiring is possible. Through the pre-feasibility phase, the engineers propose the package solder ball arrangement, package size, and specifications to improve the characteristics and process of the semiconductor chip and device.

Optimizing the Characteristics of the Package



The package design optimization process is shown in Figure 2. The optimal pad placement is proposed in the initial stage of the package feasibility review before work is made on securing the possibility for wiring and optimizing characteristics as well as the workability of packages. To optimize these features, analyses of the structural, thermal, and electrical characteristics are performed.

Today, it is imperative to enhance all of these characteristics to meet the semiconductor industry's increasing demands for improvements in speed, integration, and performance. In the case of electrical characteristics, solder balls are created in the package to increase the number of pins connecting the package to the PCB board and more wiring is added. As a result, the designs of board substrates, leadframes, and PCBs are becoming finer and more complex. However, there are limits when manufacturing these devices related to the process capabilities of the packaging company and the manufacturers that produce components such as the substrate. In package design, therefore, design rules concerning materials, processes, and equipment are created, reviewed periodically, and shared between chip designers and manufacturers of substrates and packages in order to prevent quality issues.

By sharing the design rules, package process engineers and process engineers from substrate manufacturers may work together to reduce the size and pitch of package solder balls in addition to the width and spacing of the signal wiring. Likewise, design rules are used to specify items that range from process capabilities to electrical specifications. Additionally, the methods of managing the tolerance[1] of the package and substrate—as well as the package's process capabilities—are detailed in the design rules.

areas in order: each high-speed signal line, the dielectric[2] thickness to mana[illegible] impedance[3] coherency of each signal line, and the via size[4] for an optimal low-power design. On the other hand, to improve the efficiency and mass production during the package process, the standard marking pattern is taken into account when designing devices like substrates and managed as a design rule.

[1] ***Tolerance****: The range of errors in space or values created from the difference of work capabilities.*

[2] ***Dielectric****: An electrical insulator that can be polarized by applying an electric field.*

[3] ***Impedance****: A measure of the extent to which a circuit opposes the flow of electricity.*

[4] ***Via size****: The size of holes used for electrical connection between different layers of a printed circuit board.*

Analyzing the Packaging Structures

Computer simulation is used to analyze semiconductor packaging structures. Typically, analysis through computer simulation involves applying the derived general equations to specific conditions in order to understand a certain phenomenon. There are four steps involved in the standard computer simulation process.

First, factors that govern a natural phenomenon and the relationship between the factors are placed in mathematical expressions such as the governing equation[5], and then the phenomenon that is the subject of analysis is modeled so that it can undergo computer simulation. Next, the governing equation is applied to the model to calculate it mathematically, and, finally, the result is applied to the phenomenon to analyze it. The methods of analysis through computer simulation are mainly divided into the finite difference method, finite element method (FEM), and finite volume method. FEM is most widely used to analyze semiconductor structures. The engineering aspect of FEM refers to its ability to convert infinite number of points and

[5] ***Governing equation***: *The mathematical formulae that form the basis of a computational code. computational modeling, they govern the predicted behavior of fluids in the subsurface provided by the code.*

[6] ***Degrees of freedom***: *The number of values in the final calculation of a statistic that are free to vary.*

FEM is composed of a finite number of building blocks called elements. Each element has a finite number of points and a governing equation, while a value is obtained by solving the equation. To understand structural analysis, it is essential to understand three key properties of materials that are required for such analysis: coefficient of thermal expansion (CTE), Poisson's ratio, and stress.

CTE is a property which describes the extent a material changes in length due to fluctuations in temperature. In general, a material expands as the temperature increases and it contracts as the temperature decreases. CTE is therefore defined as the fractional increase in the length of a material per unit rise in temperature. Meanwhile, Poisson's ratio is the expansion or contraction of a material in directions perpendicular to the specific direction of loading. To understand this ratio, it is helpful to consider the effect of pushing and pulling on an object. If you pull on an object lengthwise from both ends and apply a tensile force, it stretches in the direction of its length and contracts in the direction of its width. However, if you push it from both ends lengthwise and apply a compressive force, it will shrink in the direction of the force and stretch in the direction of its width. Lastly, stress is the internal force created within an object to resist an external force while maintaining its shape. It is measured in units of pressure.

These material properties are applied to the three main areas of structural analysis utilized in semiconductor packages: package warpage, solder joint reliability, and package strength.

Warpage Analysis

package to warp and create defects. Therefore, structurally analyzing the package based on the product structure, the material's elastic modulus[7], the CTE, the process temperature, and time, makes it possible to predict warpage and prevent defects from occurring.

[7] ***Elastic modulus**: A value that represents the stiffness of a material in solid mechanics. It is defined as the ratio of stress and strain.*

Solder Joint Reliability

Solders serve as mechanical and electrical connections between the semiconductor package and the PCB substrate. As the reliability of solder joints is very important, the joints should undergo structural analysis before a package is made in order to improve the package structure and materials.

Failure mechanisms in solders are primarily a combination of shear cracking caused by in-plane shrinkage and tensile cracking caused by axial tension. Therefore, structural analysis of solder joints is performed by analyzing the amount of stress applied to the solder joint under various process or usage conditions.

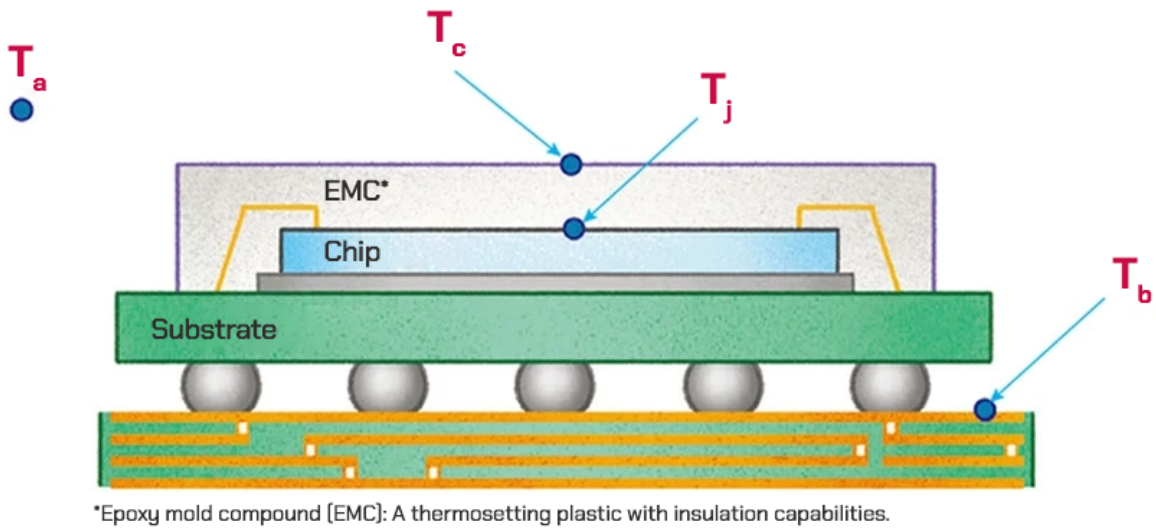
Strength Analysis

As the package serves to protect the chip from external forces, the chip's robustness to external impacts is represented by the package strength. To determine the robustness of a package, a universal testing machine (UTM)[8] is used to perform three-point bending or four-point bending which calculate the breaking strength. Structural analysis simulates these UTM tests to deduce the stress levels in each area of the package and uses the breaking strength of a specific material as a reference to predict the breaking strength of the whole product.

Heat Interpretation

Electronic devices consume power and generate heat as they operate. This heat raises the temperature of components that include semiconductor products, which can compromise the functionality, reliability, and safety of electronic equipment. Therefore, electronic equipment must have proper cooling systems to keep the temperature of components below a certain level in any environment.

Thermal analysis, thus, becomes an essential test as heat dissipation is one of the crucial roles of semiconductor packages. Therefore, generated heat, the heat dissipation effect of the package material and structure, and the temperature effect when the semiconductor package is applied to the system must be accurately understood in advance to be reflected in the package design.



▲Figure 3. Key temperature points of the package (Source: Hanol Publishing)

temperature (Tj), case temperature (Tc), and board temperature (Tb). The temperature for package specifications is usually either Tj max. or Tc max., terms which refer to the maximum temperature that ensures the semiconductor device operates normally. Figure 3 shows each temperature point in the schematic diagram of a package.

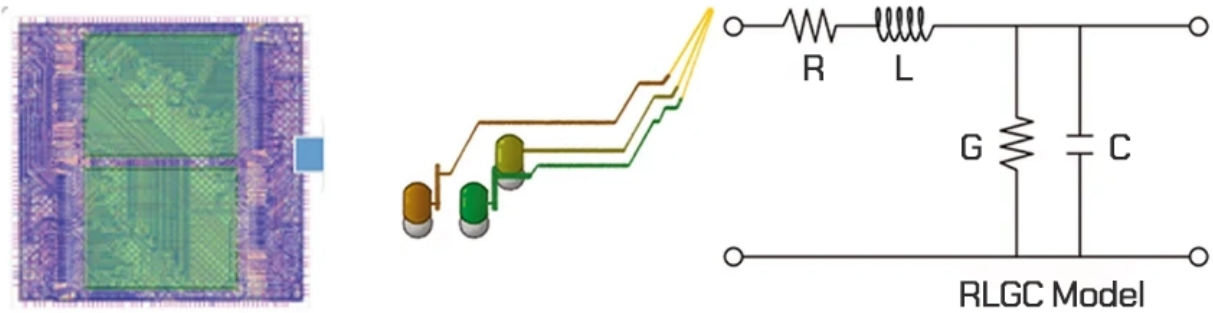
Symbol	Name	Formula
Ja	Junction-to-ambient thermal resistance	(Tj-Ta) / P
Jc	Junction-to-case thermal resistance	(Tj-Tc) / P
Jb	Junction-to-board thermal resistance	(Tj-Tb) / P

P = Power consumption (W)

▲Figure 4. Types of heat characteristics in packages (Source: Hanol Publishing)

By using the main temperature points of the package, it becomes possible to calculate thermal resistance—the most important characteristic for heat protection. Package thermal resistance is an index expressed in units of ℃/W which identifies the temperature increase of a semiconductor product in relation to the surrounding temperature when 1 watt of heat is generated by the chip. This ratio changes according to each product and the environmental conditions. Common types of

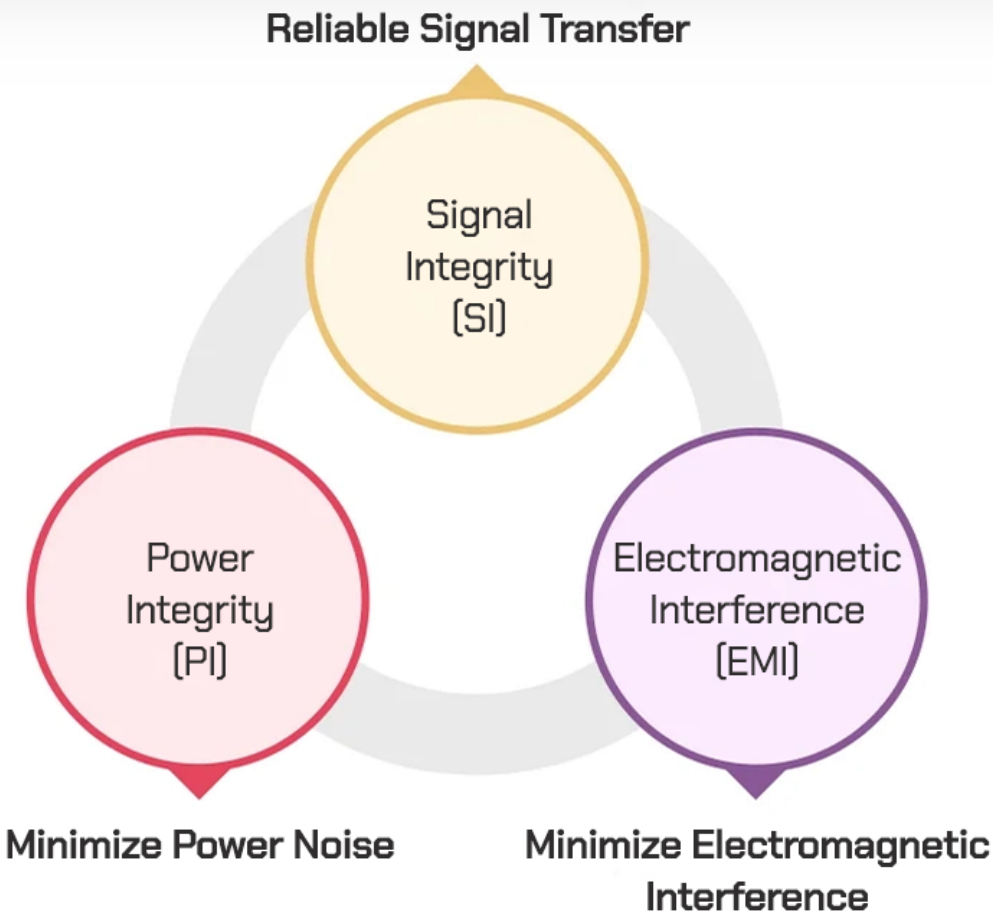
Electrical Simulation



▲Figure 5. An example of a packaged RLGC model (Source: Hanol Publishing)

As semiconductor chips become faster and denser, packages also have a significant impact on the characteristics of semiconductor products. In particular, when a high-performance semiconductor chip is packaged, accurate electrical simulation of the package state is essential. To predict the electrical problems arising from the complex wiring of high-performance semiconductor chips, modeling such as RLGC is used. Thus, electrical simulation creates models and uses them to predict the timing of data transmission, the signal quality, and the shape accuracy in high-speed digital systems.

The basic elements of an electrical model for the electrical analysis of a package are resistance, inductance, and capacitance. Just strong enough to obstruct the flow of a current, resistance is inversely proportional to the unit current flowing on an object. Inductance is the ratio of counter electromotive force that forms from electromagnetic induction caused by a change in the current flowing in a circuit.



▲Figure 6. Areas of electrical analysis (Source: Hanol Publishing)

Using modeling such as RLGC, it becomes possible to predict the most important characteristics, namely signal integrity (SI), power integrity (PI) and electromagnetic interference (EMI) as shown in Figure 5. SI is the measure of an electrical signal's quality, while PI measures the power transmission's quality. Lastly, EMI is an electromagnetic disturbance where radiated or conducted electromagnetic waves interfere with the functioning of other devices. Thus, noise problems should be checked in advance to minimize the developing period and ensure that the integrity and power delivery system can support the creation of a reliable board. SI, PI, and

Supporting the Advancement of Semiconductors

No matter how much individual chip performances improve, the overall system performance cannot be guaranteed unless the electromagnetic characteristics of the pathways connecting the chips on the package and the power supply grid are properly managed. The package design process and related analyses are therefore vital to ensuring the operation and continued advancement of chips. By following certain design rules, it is possible to create the blueprint for semiconductor packages with optimal characteristics. This optimization of a package's characteristics is then realized through structural, thermal and electrical analyses. Ultimately, these stages of design and analysis make it possible to meet the increasing demands for improvements in semiconductors' speed, integration, and performance.

<Other articles from this series>

Semiconductor Front-End Process Episode 1: The Birth of Computers, Transistors, and Semiconductors

Semiconductor Front-End Process Episode 2: Protecting Key Components Through Oxidation

Semiconductor Front-end Process Episode 3: Forming Patterns on Wafers Through Photolithography

Semiconductor Front-End Process Episode 4: Etching Fine and Identical Wafer Patterns

That Bring Semiconductors to Life

Semiconductor Back-End Process Episode 1: Understanding Semiconductor Testing

Semiconductor Back-End Process Episode 2: The Roles, Process, and Evolution of Semiconductor Packaging

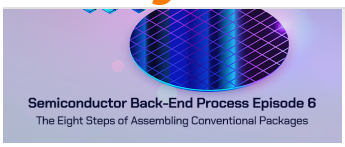
Semiconductor Back-End Process Episode 3: Understanding the Different Types of Semiconductor Packages

Semiconductor Back-End Process Episode 4: Understanding the Different Types of Semiconductor Packages, Part 2

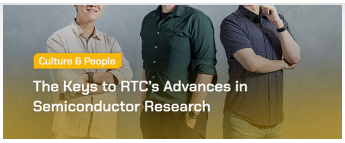
TAG #semiconductor #back-end process #packages #package design

SK hynix NEWSROOM

ENG

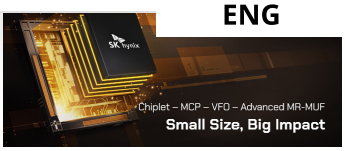


Semiconductor Back-End Process Episode 6: The Eight Steps of Assembling Conventional Packages



Open Communication, Creative Research, and Agile Problem-Solving: The Keys to RTC's Advances in Semiconductor Research

The Story Behind SK hynix's AAA-Rated Global Compliance Program



[Tech Pathfinder] Small Size, Big Impact: Unveiling the Latest Advances in Semiconductor Packaging and Miniaturization