MENU

Whitepaper: Semiconductor Industry from 2015 to 2025

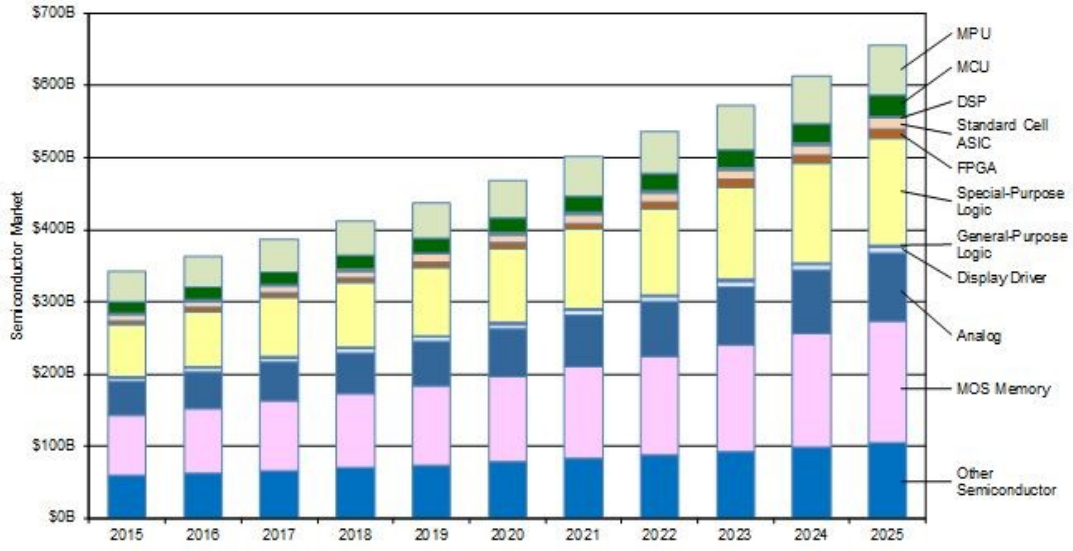
By Dr. Handel Jones, International Business Strategies (IBS)

1. Top-Level Semiconductor Perspective

The global semiconductor market from 2015 through 2025 is shown in the following figure.

FIGURE 1

Global Semiconductor Market

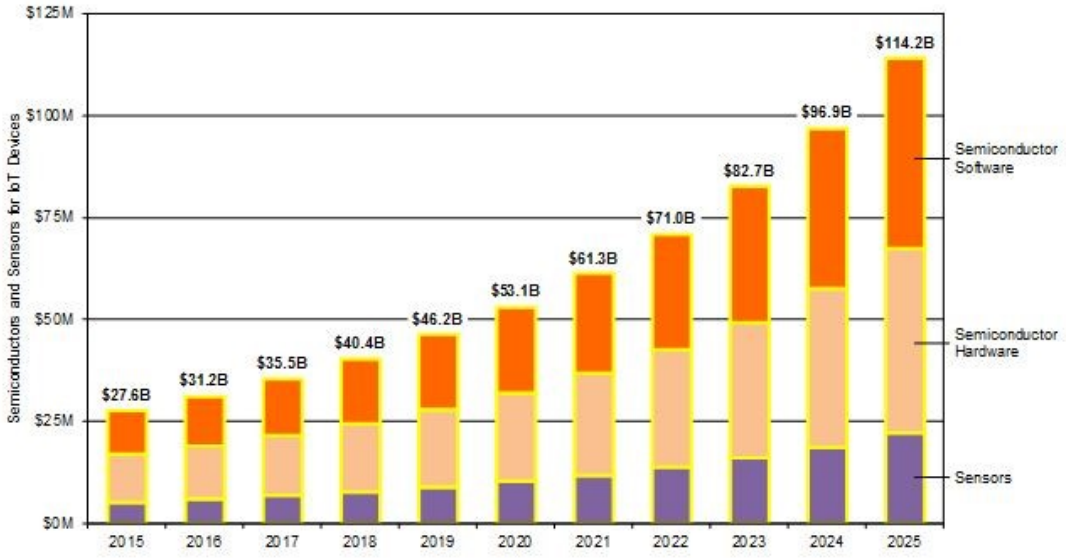


The global semiconductor market will be $655.6B in 2025 compared to $342.7B in 2015 with CAGR of 6.7%.

While the overall growth of the semiconductor market will be lower than in the past, several areas will have significantly higher growth than the overall semiconductor market. One example is the growth of IoT, and the semiconductor and sensor markets for IoT are shown in the following figure.

FIGURE 2

IoT Semiconductor and Sensor Markets



The semiconductor and sensor markets for IoT are projected to be $114.2B in 2025 compared to $27.6B in 2015, with a CAGR of 15.3%. The key semiconductors in IoT applications include controllers, wireless connectivity, and embedded nonvolatile memory. The strong growth of semiconductors in IoT devices is driven by the need for more data, but it is important that the generated data provides value to users.

A critical requirement in the IoT semiconductor market is ultra-low power (ULP), which can require using specialty wafer processes. TSMC is addressing these opportunities with its ULP wafer processes, and Globalfoundries is supporting FD SOI technology.

The IoT market consists of many segments, including consumer, automotive, medical, logistics, and home, that have high growth potential, but with the need for very low power consumption for mobile devices. While new applications will continue to emerge, which will drive the need for new semiconductor products, it will take several years before semiconductor consumption becomes comparable to IoT.

The U.S. and Europe drive the consumption pattern for IoT in the short term, but China will be the large market in 2020 to 2025.

Automotive electronics is going through some major changes with advanced driver assistance systems (ADAS) having good growth

potential. In the future, many of the buying decisions on automobiles will be made based on the electronics content and the services that can be supported. Approximately 90M automobiles are produced annually, with the expectation for a higher volume of automobiles manufactured worldwide as well as increased content of semiconductors per automobile. The process technology for semiconductors in automobiles is also mainly n-1 or n-2.

From another perspective, the smartphone volume will be approximately 1.3B units in 2015, with semiconductor content per phone in excess of $100.00 giving a market of $130B. Smartphones primarily include 4G capability in 2015, and the production volume of 5G smartphones will begin in 2019 or 2020. These 5G phones will support a peak download rate of 1Gbps, which can support multiple streams of 8K video. There will be the need for very high performance processing and very low power consumption. While high performance was the key driver for the adoption of new-generation semiconductors in the past, low power consumption combined with low cost will be the key driver in the future.

It is significant that China lagged the communications leaders by two to three years in the 3G protocol and closed the gap to one year for 4G. Now, China is planning to be the global leader in the 5G protocol, which includes infrastructures such as base stations, networking and transmission equipment, and smartphones. The result is that the demand for advanced semiconductors will grow rapidly in China in the 2020 to 2025 time frame. The semiconductor products consumed within the 5G ecosystem will need to be leadership in performance and ***power consumption*** on a global basis, which can be supported by 10/7nm.

A high percentage of semiconductors manufactured in 10/7nm, consequently, will be consumed in China in 2020 to 2025, which is a different pattern from the past. The supply chain for semiconductors will need to address this radical change in the

industry demand profile.

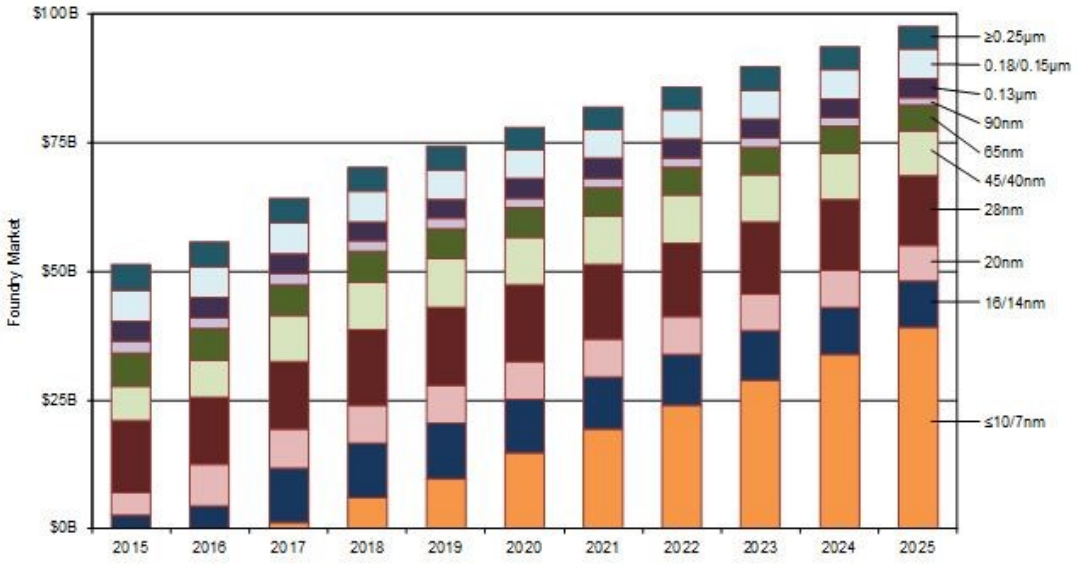
Memory supply and consumption will also primarily be in Asia, with modules that include memory chips and controller functionality. In addition, memory component vendors will become memory solution vendors, where there will be the need for supporting software in the various types of application being addressed, such as cloud computing. The result is that the composition of the semiconductor market will be significantly different in 2020 to 2025 than is the case at the present time.

2. Feature Dimension Trend

The foundry market by feature dimension is shown in the following figure.

FIGURE 3

Foundry Market by Feature Dimension



The foundry market is projected to be $78.0B in 2020, and even with a CAGR of 4.6% from 2020 to 2025, the market is projected to be $97.5B in 2025. It is not expected that large capacity will be added to 16/14nm and larger process technologies after 2020, and as a result, 10/7nm and smaller process technologies will grow from $14.8B in 2020 to $39.0B in 2025.

In 2025, the combination of 16/14nm with 10/7nm and smaller

process technologies (3-D structures) will represent 49.3% of the foundry market, assuming there will be no major penetration of the market by 14nm and 10/7nm FD SOI. With the addition of Intel and Samsung Electronics' internal consumption to the nonmemory wafer supply, 3-D structures will account for more than 50% of the wafer supply in 2025.

The analysis of the foundry market by feature dimension shows that 28nm and shrinks, which include 20nm FD SOI, will also have high revenues through 2025. Most of the wafer capacity required for the 28nm generation of technology has been established, but additional capacity could be added in China, and UMC is supporting this by participating in a facility in Xiamen (China).

The continuously large revenues for 28nm technology are being supported by the development of specialty wafer processes that can give low power consumption such as the ULP version from TSMC that will be used for IoT applications. The 20nm FD SOI process of Globalfoundries will also be extensively used for IoT because of low power consumption.

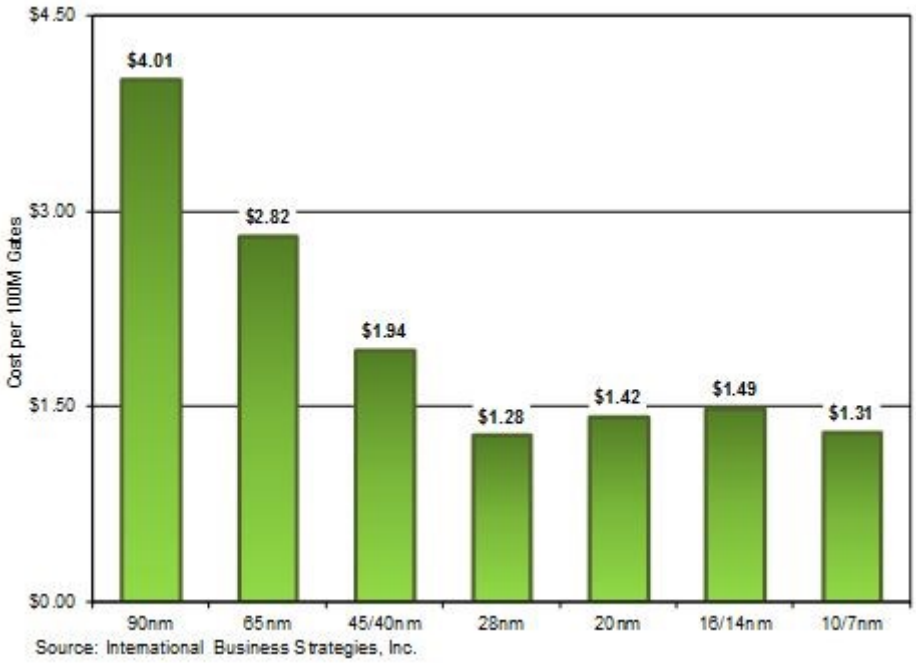
An massive IP portfolio has been developed for 28nm, and strong design expertise has been established for RF, mixed-signal, and digital products.

The 20nm HKMG bulk CMOS technology node is not expected to be large due to high leakage compared to 28nm technology. It is, however, possible that a shrink of 28nm HKMG planar to the 20nm level is possible, which will not require the use of double patterning.

The 16/14nm technology node is not projected to have high revenues due to the high gate cost compared to other technology options, including 10/7nm. A projection of gate costs, including the migration to 10/7nm, is shown in the following figure.

FIGURE 4

Gate Cost



The gate cost projection for 10/7nm is based on the ability to obtain high parametric and systemic yields. The 10/7nm technology is also projected to have a long lifetime similar to that of 28nm.

While there will be continued demand for 16/14nm through 2025, foundry wafer values will be lower than for 28nm wafers in 2025. Another issue is that 20nm can be considered a shrink of 28nm, and the combined 20nm and 28nm technologies will have a consumption value of $20.5B in 2025. Planar technology is considered to be complementary to 3-D structures due to the ability to have greater flexibility in design. An example is that FD SOI supports back and forward biasing.

The technology at 10/7nm will have multiple versions, with Intel and TSMC's versions being mainstream. A perspective on the CAPEX level for 10/7nm and smaller technologies is shown in the following table.

TABLE 1

Market and CAPEX for ≤10/7nm

	2020	2025
Revenues ($M)	14,834	39,047
Wafer price ($K)	9.50	12.90
Wafer volume (MU)	1,561	3,027
Wafer volume (M WPM)	130	252
CAPEX 10K WPM ($K)	2.20	2.93
CAPEX ($M)	28,627	73,906

With the revenues of $14.8B in 2020, the CAPEX for 10/7nm and smaller technologies will be $28.6B. For the revenues of $39.0B in 2025, the cumulative CAPEX for 10/7nm and smaller technologies will be $73.9B (accumulation).

The wafer revenues for 5nm (expected to be last technology node for FinFETs) are projected to be large in 2025 unless more efficient design methodologies are developed. While 5nm will be used for high performance processors for data center applications, 5nm technology is not expected to be widely used in smartphones unless there is a large reduction in wafer costs through 2025. Extreme ultraviolet (EUV) will be used at 5nm for multiple layers, and while there will be high cost per layer, parametric yields can be positively impacted by the use of EUV. The value of using EUV has not been fully understood by the semiconductor industry because of the emphasis on wafer manufacturing cost rather than on final product cost.

The high revenues at 28nm and shrinks to 20nm are a key indicator of the changes in the wafer supply chain with the reduction in feature dimensions. The low revenues of 20nm compared to 28nm are an indicator that gate cost does not necessarily decline with the reduction in feature dimensions as was the case in the past. Gate density, however, will continue to increase, which is consistent with Moore's law.

The high value of 10/7nm, however, is a key indicator of the continued scaling within the 3-D domain, with the primary demand

driver being the lower power consumption within the smartphone and IoT applications. The growth of the foundry market is expected to slow down because the growth rate of the foundry market cannot be higher than that of the semiconductor market in the longer term. Otherwise, the cost of goods will become a high percentage of revenues, and the gross profit margins of semiconductor vendors will decline. A number of foundry vendors, however, disagree with this assumption and project that the growth of the foundry market can be in the double-digit level through 2020.

The cost of participation in advanced technology is rapidly increasing, and only a small number of companies globally will be able to support these investment levels. ***The role of China will, consequently, become important within the wafer supply ecosystem because of the large market potential in China and the ability to obtain large funding sources.***

New device structures will be in initial volume production in 2020 to 2025, with nanowires being a potential option for the next generation of structure after FinFETs. The reality is that it can take 10 years between high volume products and the initial demonstration of a viable product. Furthermore, no device structure has demonstrated a high probability of production volume for microprocessors to date. As a result, FinFET structures are expected to be the mainstream approach for advanced feature technology through 2025. Another expectation is that there will be continued enhancements to 3-D structures, and the 7nm design structures of IBM have some significant technology enhancements. IBM, however, is unlikely ahead of Intel in 3-D structures, especially in the ability to support high volume manufacturing.

Manufacturing and inspection equipment vendors should expect increased requirements on the capabilities of their products, but there will likely be some cyclical demand.

If TSMC and Samsung are closing the gap with Intel for advanced technology nodes, this is good for tooling vendors because of larger orders for new-generation tools.

With the increasing cost of wafers with the reduction in feature dimensions, there are clear benefits to ramping 450mm wafers. ***While the progress has not been as rapid as expected, it is projected that two or three 450mm wafer fabs will be in initial volume production in 2022 of 2023, and one of these 450mm wafer fabs will be in China.*** The technology node will be 10/7nm, and the wafer fab in China will be established through a joint venture.

In addition to the 450mm wafer fab, the wafer capacity for nonmemory products in China will likely be more than 100K WPM in 2020 to 2025. The result will be a CAPEX of $30B or more for the wafer capacity of nonmemory products in China in the future.

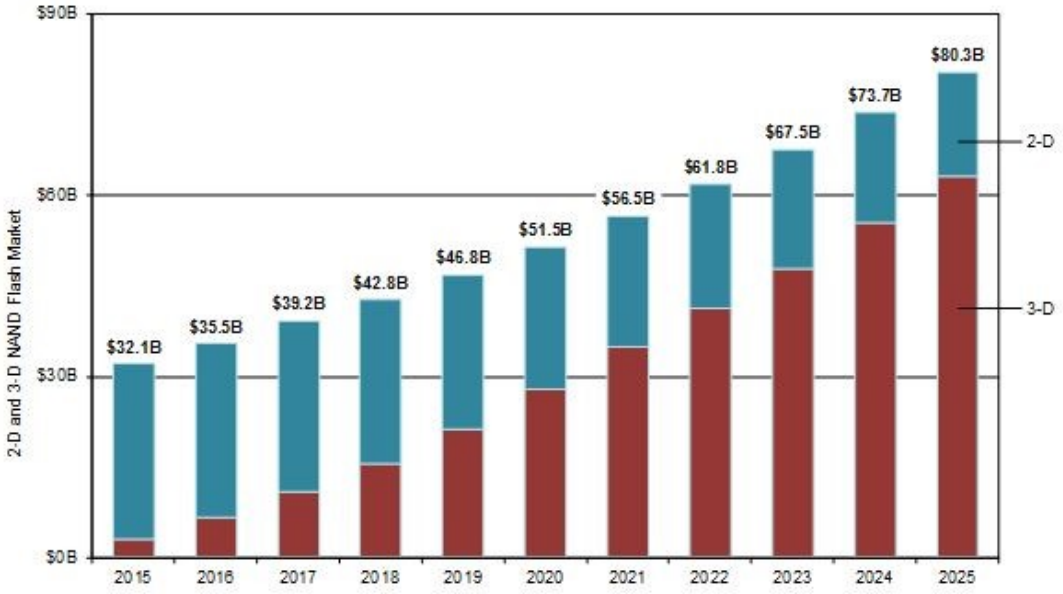
The wafer supply base in China is expected to go through major changes in the next decade and will be a key factor in providing funding support for the migration to smaller feature dimensions.

3. NAND Flash

The NAND Flash market is shown in the following figure.

FIGURE 5

NAND Flash Market



The NAND Flash market is split into 2-D and 3-D structures. Approximately 90.2% of the market in 2015 will be 2-D products, but 3-D products will represent 78.7% of the market in 2025. It is projected that the crossover in revenues between 3-D and 2-D will occur in 2020. The 3-D projections shown are for Samsung's VNAND structures, Toshiba's BiCS structures, and the 3D XPoint structures of Intel and Micron Technology (Intel-Micron).

Samsung has been highly innovative in promoting VNAND products. While high volume production is at 32 layers in 2015, high volume production will be at 96 layers in 2019 or 2020 and 128 layers in 2025. With a depreciated wafer fab, the cost per gigabyte of 3-D NAND will be under $0.10 with 64 layers and $0.06 with 128 layers. The cost for 1TB of 3-D NAND will be $60.00, with a selling price of $95.00. With 1TB 3-D NAND priced at under $100.00 and with its high endurance, NAND Flash products will be mainstream memory capabilities for low latency data center applications as well as for automotive and other applications.

The Intel-Micron 3D XPoint memory products can be used within legacy NAND applications, but new architectures will likely emerge in data centers and mobile platforms.

Large wafer fab capacity will be established for 3-D NAND, which will involve the high growth of etching, deposition, and inspection

tooling. A further trend is that 50% of the 3-D NAND wafer fab capacity will be in China by 2025. In addition to being a large market, China has access to large funding support.

Cross-point resistive random-access memory (RRAM) structures are being developed, and if this technology gives high endurance as well as low cost, it could impact the 3-D NAND Flash market. While RRAM device structures are attractive from a concept perspective, manufacturability in high volume has not been proven.

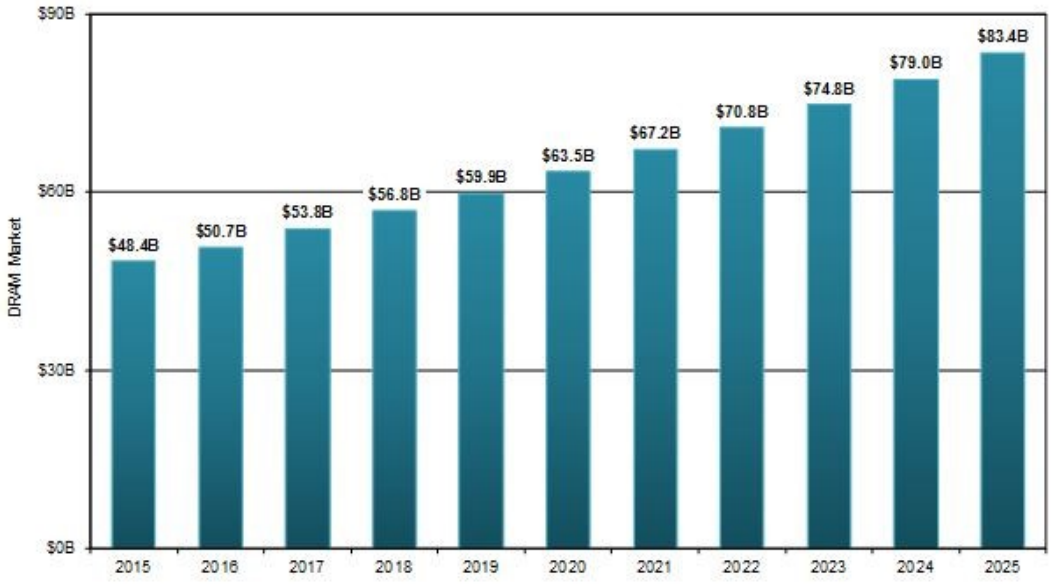
Based on the visibility into advanced nonvolatile memory, 3-D NAND are expected to be mainstream products in 2020 to 2025.

4. DRAM

The DRAM market will continue to experience growth, and a perspective is shown in the following figure.

FIGURE 6

DRAM Market



Enhancements in DRAM technology have saturated, and while there are incremental enhancements, new device structures need to be developed in order to have a disruptive impact on the market.

Spin transfer torque (STT) will be in volume production for niche segments of the market in 2020 to 2025 but will not be a

mainstream capability.

Phase shift memory structures are being developed, but it is early in the ramp-up phase. The new Intel-Micron memory technology can displace DRAMs within systems that are designed to optimize the benefits of new device structures. The provided DRAM market data takes into account the impact of 3D XPoint memory products.

The bit growth of DRAMs is being constrained by the reduction in memory requirements for the latest generation of operating systems. Also, the high price for DRAMs in the recent past has lowered the average memory content for personal computers, tablet computers, and smartphones. The recent decline in prices due to some overcapacity is expected to have a short-term impact only, and the DRAM business is mature and will generate high profits.

The use of multichip packaging will result in changes to DRAM interfaces and the use of new concepts. Additionally, the use of virtual memory concepts will lead to changes in the memory hierarchy and the increased use of nonvolatile 3-D structures as part of the memory ecosystem.

DRAM capacity will increase, but with a low probability of a disruptive technology being widely adopted before 2020.

5. Areas of New Opportunity

The areas of new opportunity in 2015 to 2025 include the following:

- Graphene is expected to start being used for interconnect structures in the next 5 to 10 years. While device structures are also expected to continue being fine-tuned, a vital part of any major improvement is the availability of new materials. Key advances in graphene are expected to be made by Samsung and IBM, but Intel is likely also active.
- Photonics will be widely used for high performance processors

and the supporting function for both on-chip and chip-to-chip interconnects. The technology is close to maturity in 2015 and will need access to specialty wafer processing equipment as well as better inspection tooling.

- The adoption of 5G cellular technology will require very high performance multicore processors, which will be a driver for the 10/7nm and smaller process nodes. A key challenge is the need to have adequate bandwidth through the use of many multiple-input multiple-output (MIMO) antennas on smartphones. New materials will also need to be developed in order for these antennas to support the required bandwidth.

  Integrated antennas and sensors will become a major opportunity for tooling in the deposition of new materials. The support of vertical structures will be complementary to scaling and, in many cases, will be lower cost than scaling.

  RF is an area that needs major enhancements in throughput, where new materials and device structures will need to be developed. Another example of a new and high growth opportunity in RF is the 80GHz devices for ADAS applications.

- The FD SOI wafer volume will be more than 1M wafers in 2020 to 2025 and will require specialty oxide transfer processes and inspection tooling. FD SOI is projected to be scaled to 14nm and 10/7nm, but with some uncertainty regarding the timing.

Technology enhancements in the semiconductor industry will be rapid over the next few years, and innovation is not slowing even though the semiconductor industry is maturing.

Author Biography

Dr. Handel Jones is the founder and CEO of International Business Strategies, Inc. (IBS), which is based in Los Gatos (California) and has been in business for over 25 years. IBS is active in quantifying

the cost of implementing and manufacturing IC products and financial metrics related to market positioning. IBS provides support to many global leaders in key areas of technologies, markets, and business strategies for the semiconductor and electronics industries.

Dr. Jones is the author of *Chinamerica*, which was published by McGraw-Hill and provides insight into the drivers for the economy of the U.S. and China. As a follow-on to *Chinamerica*, Dr. Jones has recently written a new book called *China's Globalization: How China Can Become No. 1*. In addition, Dr. Jones has contributed to a number of publications, including Forbes, China Daily, Global Times, Nikkei Weekly, and others.

Global Update

SEMI

www.semi.org

August 4, 2015

673 South Milpitas Blvd.
Milpitas, CA 95035, USA

semihq@semi.org