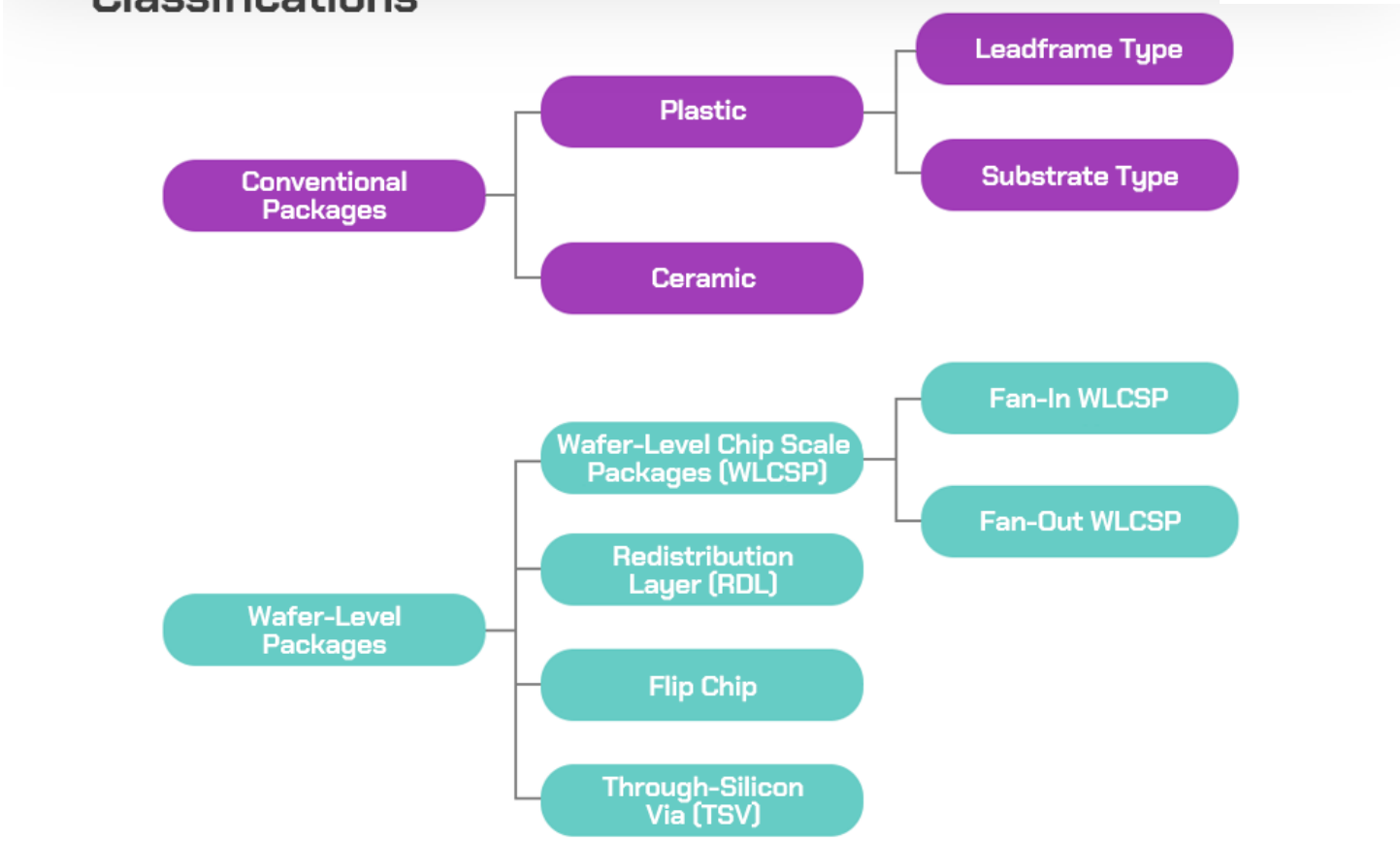
Semiconductor Back-End Process Episode 3: Understanding the Different Types of Semiconductor Packages

June 1, 2023

In the previous episode, it was established that semiconductors require packaging for protection. These packages come in all different shapes and sizes while using different methods to protect and connect delicate integrated circuits. This episode will explore the various categorizations of semiconductor packages, including the types of materials used to make them, their distinct manufacturing techniques, and their application cases.

Classification of Semiconductor Packages

Figure 1 shows the various types of semiconductor packages broken down into two main categories: conventional and wafer-level packaging. In conventional packaging, the wafer is sawed before the chip is packaged, while wafer-level packaging involves a part, or all, of the packaging process being performed at the wafer level before proceeding with wafer sawing



▲ Figure 1. Types of semiconductor packages (Source: Hanol Publishing)

Based on the materials being packaged, conventional packages can be divided into ceramic and plastic packaging. Plastic packages can be further categorized into leadframe or substrate packages depending on the medium of the package.

As for wafer-level packages, they can be categorized into four different types: 1) wafer-level chip scale packages (WLCSP) in which wiring and solder balls are formed on top of the wafer without a substrate 2) redistribution layers (RDL) that use a wafer-level process to rearrange the pads[1] on the chip that are electrically connected to the outside 3) flip chip packages in which solder bumps[2] are formed on the wafer to

For WLCSP, it is divided into fan-in and fan-out WLCSP. The process for fan-in WLCSP involves attaching wiring and solder balls on top of the wafer, while fan-out WLSCP involves rearranging the chips into a molding[3] wafer. This is done to form wiring through a wafer-level process and to attach solder balls onto a package larger than the chip.

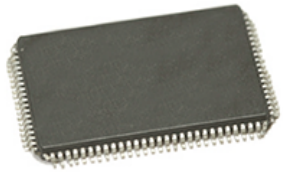
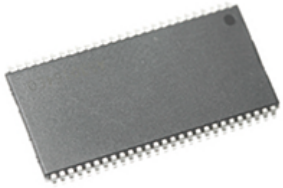
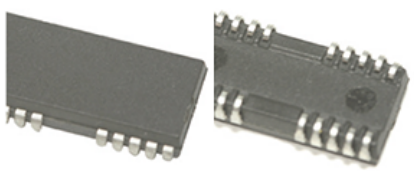
*[1]**Pad**: A passageway that electrically connects to other mediums. On a chip, pads are made to electrically connect with the outside through wires or flip chip bumps. On a substrate, pads are made to connect the chips to each other.*

*[2]**Solder bump**: A conductive bump that connects a chip to a substrate through flip chip bonding. It also connects ball grid arrays (BGA) or chip scale packages (CSP) to a circuit board.*

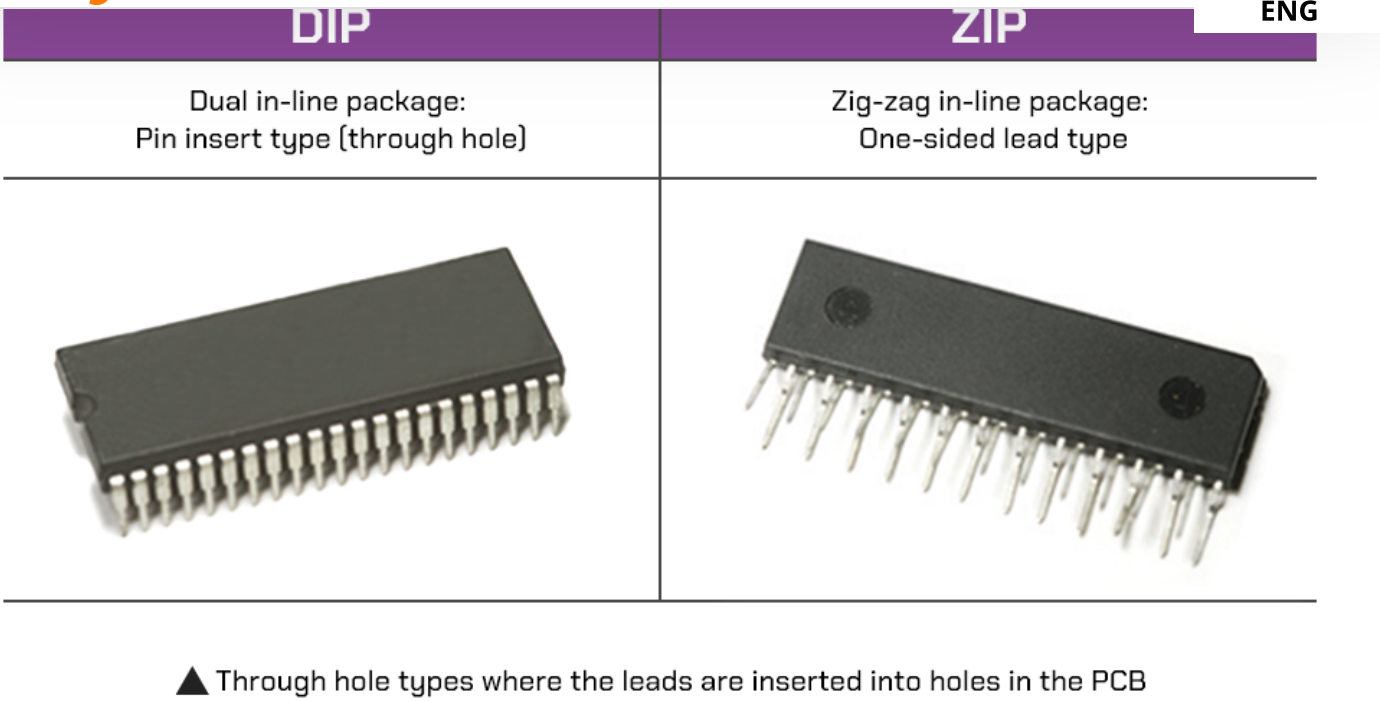
*[3]**Molding**: The process of sealing wire-bonded or flip chip bonded semiconductor products with an epoxy molding compound (EMC).*

Conventional Packages

Plastic Packages: Leadframe

QFP/TQFP	TSOP	SOJ
(Thin) Quad flat package: Four-sided lead type	Thin small outline package: Two-sided, gull-form lead Surface mounting type	Small outline J-leaded package: J-form lead Surface mounting type
		

▲ Surface mounting types where the leads are attached to the surface



▲ Figure 2. Types of leadframe packages (Source: Hanol Publishing)

In a plastic package, the chip is covered in plastic materials such as epoxy mold compound (EMC)[4]. A leadframe package is a type of plastic package that uses a metal lead called a leadframe as its substrate. The leadframe uses an etching method to form wiring on thin metal plates.

[4]***Epoxy mold compound (EMC)****: A thermosetting plastic with excellent mechanical and electrical insulation in addition to temperature resistance properties. It is a resin with relatively small molecular weight capable of three-dimensional curing in the presence of a curing agent or catalyst.*

Figure 2 shows the different types of leadframe packages. In the 1970s, through hole types like dual in-line packages (DIP) or zig-zag in-line packages (ZIP) in which leads are inserted into holes in the printed circuit board (PCB) were commonly used. Later, as the number of pins increased and the design of PCBs became more complex,

products that require a large number of I/O pins like logic chips, packages like QFP in which leads are attached on all four sides are applied. Packages such as thin QFP (TQFP) and TSOP were also developed as system environments required thinner packages.

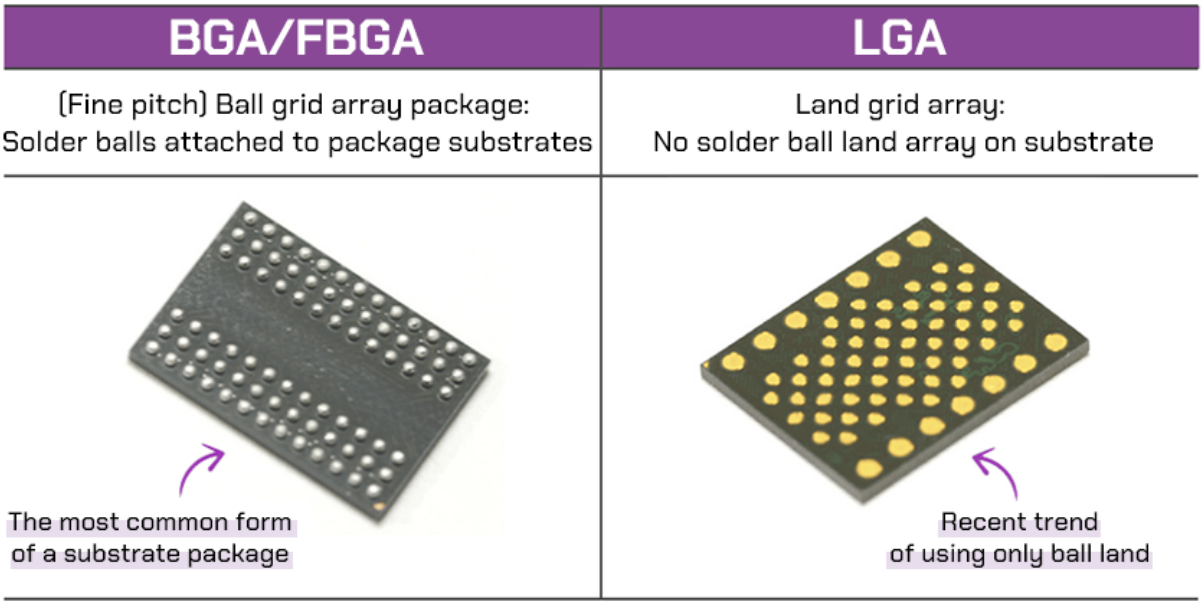
As higher speeds became more important for semiconductor products, substrate packages which can support multi-layer wiring designs became the mainstream packaging technology. Nevertheless, leadframe packages such as TSOP are still widely used because of their low manufacturing costs. Since leadframes are made by stamping or etching wiring shapes on metal plates, they are cheaper than substrates that have a relatively complex manufacturing process. Therefore, leadframe packages are still the preferred choice for the production of semiconductor products that do not require high-speed electrical characteristics.

Plastic Packages: Substrate

As the name suggests, substrate packages use a substrate as the medium. They are sometimes referred to as laminated packages because the substrate is made using multiple layers of film. Unlike leadframe packages which only have one metal layer in the wiring as they are made with a leadframe—a metal plate unable to form more than two metal layers—substrate packages can feature several layers of wiring. This leads to better electrical characteristics and a smaller package size. Another key difference between leadframe and substrate packages is the wiring connection process. The wiring connecting the chip and the system must be separately implemented on the leadframe and the substrate. If the wiring needs to cross each other, a substrate can make a wire cross to another metal layer while a leadframe is unable to do this as it only has one metal layer.

As shown in Figure 2, substrate packages can also feature a large number of pins by

side. This also improves the electrical characteristics of substrate packages process. As for the size of the packages, leadframe packages are generally larger as they consist of the main frame and the space taken up by the lead on the sides. However, substrate packages are smaller as the pins are on the bottom of the package to save space.



▲ Figure 3. Comparison of BGA and LGA (Source: Hanol Publishing)

Due to these advantages, most semiconductor packages today are substrate types. The most common type of substrate package is the ball grid array (BGA) package, but land grid array (LGA) packages, which feature a ball land structure consisting of flat contacts instead of balls as seen in Figure 3, have also been used in recent times.

Ceramic Packages

are mainly used for logic semiconductors that require high reliability as well as for verifying packages made for CMOS image sensors (CIS).

Wafer-Level Packages

Fan-In WLCSP

WLCSP is a prime example of a wafer-level package as most of the manufacturing process takes place at the wafer level. In a broader sense, however, any package that is even partially processed at the wafer level is considered a wafer-level package. Examples include packages that use RDL, flip chip technology, and TSV. In regards to fan-in WLCSP and fan-out WLCSP, the term “fan” refers to the chip’s size. A fan-in WLCSP has package wiring, an insulation layer, and solder balls directly on top of the wafer, contributing to various advantages and disadvantages when compared to conventional packages.

As the size of the package is equal to the size of the chip in fan-in WLCSP packages, they can be manufactured to the smallest dimensions. Furthermore, as the solder balls are directly attached to the chip without a medium such as a substrate, the electrical transmission path is relatively short and, thus, improves electrical characteristics. Lastly, these packages can be processed at a low cost as there is no need for package materials such as substrates and wires. As the package is processed all at once at the wafer level, it can further save costs if there is a large number of net dies—the chips on the wafer—and a high yield.

As for the downsides, fan-in WLCSP packages have weak physical and chemical protection capabilities due to the silicon (Si) chip acting as the package itself. For this same reason, these packages’ coefficient of thermal expansion[5] is vastly different to the PCB substrate to which they will be attached. This puts more stress on the solder

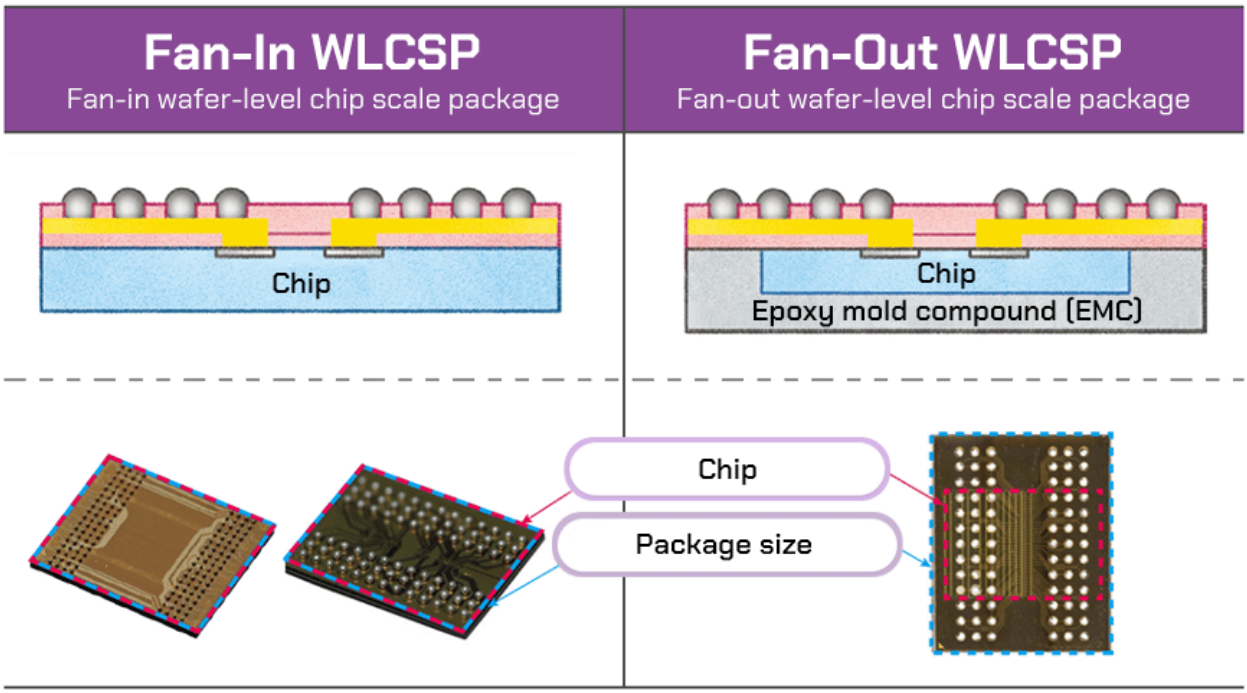
decrease in temperature.

[6]***Solder joint reliability**: The quality that ensures the joint can conduct its intended purpose of making a mechanical and electrical connection during the life of the package when it is connected to a PCB with soldering.*

Another disadvantage of fan-in WLCSP packages is the inability to use existing infrastructure for package testing. And if the package ball layout is larger than the chip size, packaging is not possible at all as the solder ball layout cannot be made on a package. Finally, the packaging costs for fan-in WLCSP can be higher than conventional packaging if the number of chips on the wafer is small and the yield is low.

Fan-Out WLCSP

Fan-out WLCSP possesses the advantages of fan-in WLCSP while overcoming its disadvantages. Figure 4 shows this comparison between fan-in and fan-out WLCSP.

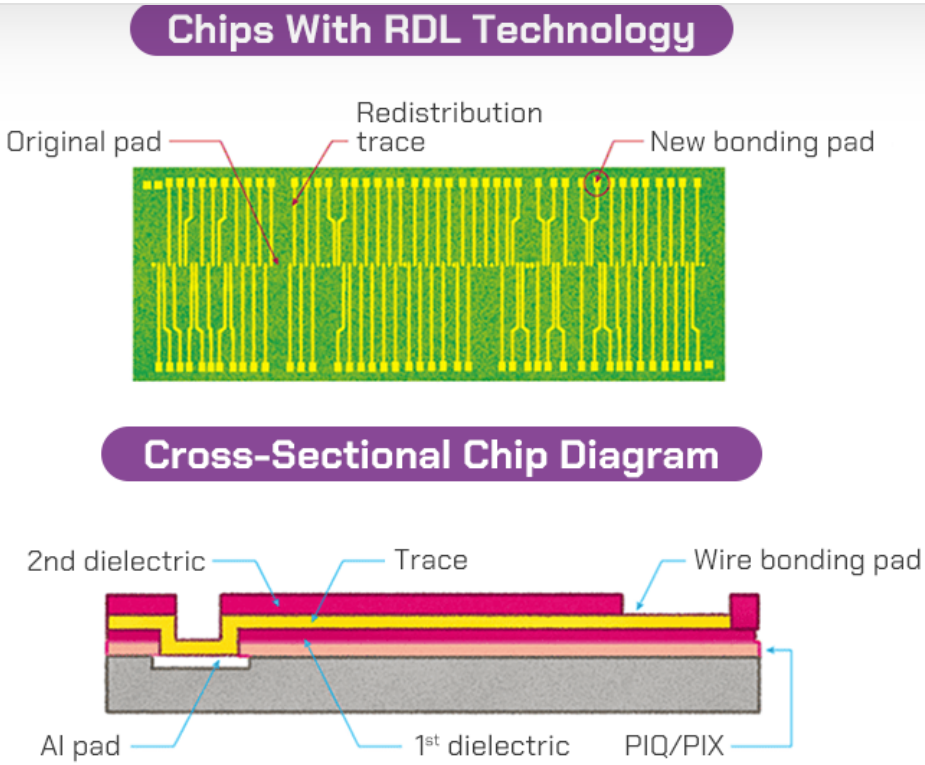


In a fan-in WLCSP, all of the solder balls for the package are on the chip's surface, while a fan-out WLCSP features solder balls for the package which can be "fanned out" away from the chip. For fan-in WLCSP, the wafer is sawed after the packaging process is complete rather than in the middle of the process. Consequently, the size of the chip and the package must be the same, and the solder balls must be within the chip's size. Fan-out WLCSP, on the other hand, involves sawing the chips before the packaging process and arranging the sawed chips on a carrier to reshape the wafer. During this time, the space between the chips is filled with EMC to form a wafer. The wafers are then removed from the carrier, subjected to wafer-level processing, and sawed to make a unit of fan-out WLCSP.

In addition to offering good electrical characteristics just like fan-in WLCSP, fan-out WLCSP overcomes several disadvantages of fan-in WLCSP. These include the inability to use existing infrastructure for package testing, the inability to package products when the ball layout is larger than the chip's size, and increased processing costs arising from the need to package defective chips all together. Due to these advantages of fan-out WLCSP, the application of these packages has been growing in recent years.

RDL

RDL technology refers to the act of rewiring. The purpose of this technology is to rearrange the bonding pads that are already formed on the wafer by adding additional metal layers. Figure 5 shows a diagram and a cross-sectional structure of a center pad chip in which the pads have been redistributed to the edges using RDL technology. RDL technology is a wafer-level process that only reconfigures the pads, and the wafers that have gone through RDL undergo a conventional packaging



▲ Figure 5. A cross-sectional view of a chip with RDL technology (Source: Hanol Publishing)

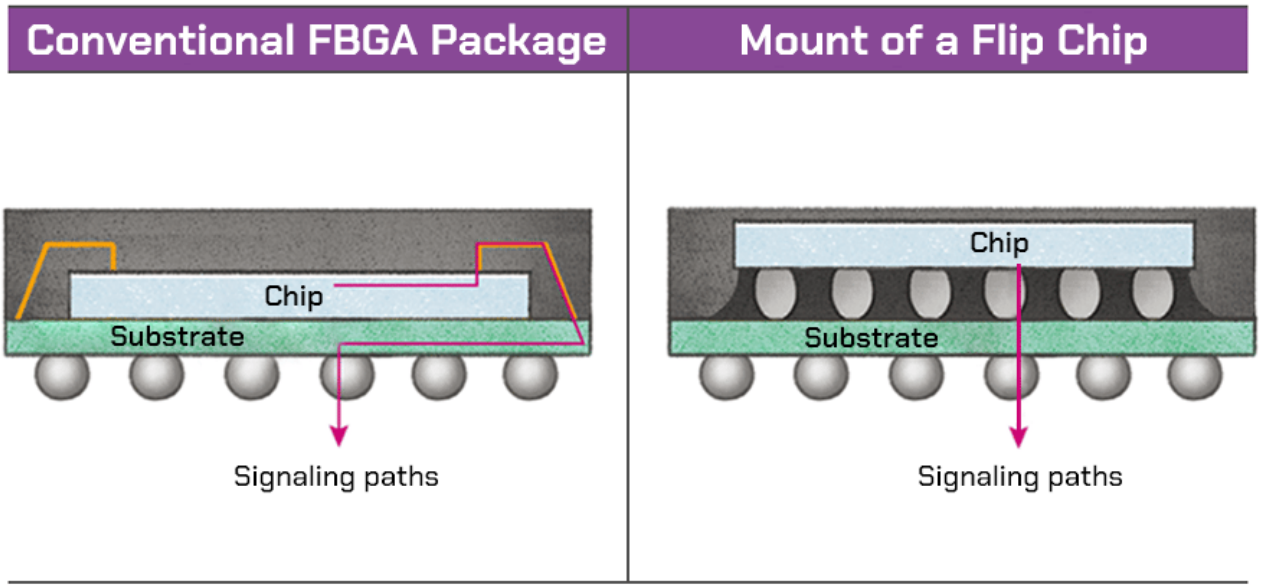
When a customer requests a unique pad arrangement on a wafer, it is more efficient to rearrange the pads on an existing wafer using RDL technology during its packaging rather than going through a new wafer fabrication process. Additionally, RDL technology is also used for chip stacking of center pad chips.

Flip Chip

Flip chip technology gets its name because the bumps formed on the chip are flipped and attached to the package body such as a substrate. It is an interconnection method that electrically connects chips and boards such as substrates, just like traditional wire bonding.

electrical signal transmission path is also shorter compared to wire bonding.

The placement of metal pads on top of a chip used in wire bonding is one-dimensional, limiting their placement to the edges or center of a chip. Flip chip bonding, on the other hand, has no process constraints when it is bonded to the substrate and when the solder bumps are formed. So, the metal pad can be arranged in a two-dimensional manner by using a whole entire side of the chip, which increases the number of metal pads by the power of two. In addition, the pads that will form the bumps can be placed anywhere on top of the chip. Moreover, pads that supply power can be placed near areas where power is required, further enhancing the electrical characteristics. As Figure 6 shows, the signal path for flip chip bonding becomes much shorter compared to wire bonding when exporting information from the chip to the same package ball. It further boosts the electrical characteristics.



▲ Figure 6. Comparison of signal transmission paths for wire bonding and flip chip bonding

As explained, WLCSP and flip chip both form solder balls on top of a wafer. Although both technologies can be mounted directly on a PCB board, there is a fundamental difference between the two—the size of the solder.

With WLCSP, the diameter of its solder balls is typically a few hundred micrometers (μm), but the solders formed on the flip chip are only a couple dozens of μm. Due to its small size, the solder formed on the flip chip is often referred to as a solder bump rather than a solder ball and it is difficult to ensure solder joint reliability with this solder alone. WLCSP solder balls can handle the stress from the difference in the coefficient of thermal expansion between the substrate and the chip. Flip chip solder bumps, on the other hand, cannot. Therefore, to ensure solder joint reliability, a polymer-type underfill material must be used to fill between the flip chip bumps. The underfill material disperses the stress on the bumps and ensures solder joint reliability.

As there are a wide variety of semiconductor package types in addition to the ones explained in this article, the next episode will put a special focus on stack packages and system-in-packages, while subcategories such as wire bonding and TSV will also be explained.

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