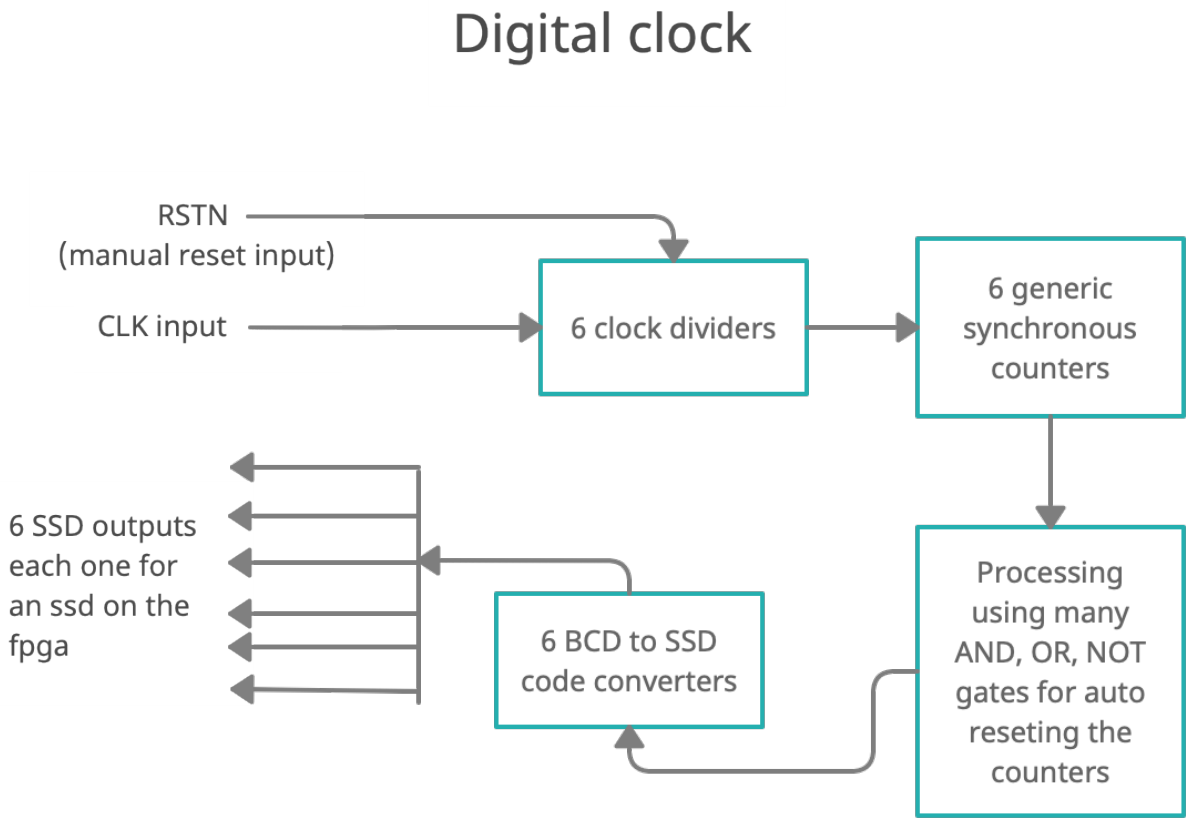
EE232 Project Report

A concerted effort by:
1.Akhil Singh (2004203)
2.Tejas Lolage (2004220)
3.Prateek Singhal (2004227)
4.Dhanvin Prajapati (2004225)
Guidance by Dr. Nandakumar Nambath

Introduction:

We have created a framework of a digital clock with the help of the VHDL language which can be implemented on an fpga board. A digital clock has a number of uses. From being placed inside children's fancy watches to multi-function clocks that have various features. We can also link the clock to another entity to feed the clock output and make the entity work on daily time basis (for example an animated wallpaper which automatically changes its colour to dark in the evening and bright in the morning again).

Block diagram:



Objective of the Project:

The main objective of this project is to make a 24h digital clock which is similar to those which one can see on digital watches, or digital clocks. We aim to use an fpga board for the implementation of this project. The six seven segment displays on the fpga board will be used for the output of the device. There is also a plan of implementation of an active-low manual reset

button which will force reset the clock to 00:00:00 time and the clock will start working from this time once the reset signal is unasserted.

Overview of the System:

This clock follows the 24 hour clock system.
The ones place in second will reset after every ten (i.e. 0 to 9) cycles and tenth place in second will reset after every six (i.e. 0 to 5) cycles. And the same goes for the digits of minute.
In hour, when tenth place is 0 and 1, the ones place will reset after every ten (i.e. 0 to 9) cycles but when tenth place is 2, the once place will reset after four (i.e. 0 to 3) cycles.

Implementation details:

Clock signal and Reset signal were given as input to get the hexadecimal output on the 7-segment display.

Clock signal of 50 MHz was given which was used to generate 6 clock signals with the help of clock divider. These clock signals will be fed to the 6 generic counters that would generate six different outputs according to the format of HH: MM: SS (Hours: Minutes: Seconds).

Now the challenge is to reset the unit place of seconds, minutes and hour to 0 once it crosses nine and simultaneously increasing the value of the tens place of the corresponding number. For ex, once the time is 00:00:09, it should show 00:00:10th next second, similarly with the minute and the hour place too. This was achieved by giving the active low load signal to generic counters, which would be low whenever the Boolean expression generated by and, or and not gates give the output LDN as 0. Four the hour hand, we have to reset the clock to 00:00:00 once it crosses 23:59:59 which was again achieved by the help of these gates.

Once the correct binary output signal is generated, we converted it to SSD format with the help of Binary code to SSD converter so that it can display time on the 7-segment display on the FPGA. A reset button was also there which could reset the time to 00:00:00.

Results:

After coding the requirements of the project and debugging a lot of the bugs in the code, we finally were able to achieve an output of our preference. We also checked the reset signal and it was working just as expected. The code is now ready to be cross checked using the fpga board by programming the DE10 lite kit.

Conclusion:

- VHDL is a very powerful language which can help us make our own projects with the help of an fpga board.
- Using simple components such as AND, OR, NOT gate, we can build seemingly complex architectures which are useful to man in reality.

Google Drive link:

Click me

References:

We took insight from one of the sites for project ideas using vhdl. There was code readily available on the website but we have not touched the website code or even looked at it for any inspiration. The coding and methodology is solely an effort from our side.
Website link: Click me