K Sri Phani Tejaswi

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Education

NIT Rourkela **2023 – 2026**
M.Tech, ECE (CGPA: 8.00) *Rourkela, Odisha*

GRIET, Hyderabad **2017 – 2022**
B.Tech, Electrical and Electronics Engineering (CGPA: 7.5) *Hyderabad, Telangana*

Sasi Educational Institutes **2015 – 2017**
Intermediate (MPC Stream) (96.6%) *Velivennu, AP*

Montessori High School **2015**
SSC (CGPA: 9.5) *Tanuku, AP*

Skills

- **Programming Languages:** C, C++, Python, Verilog Hardware Description Language (HDL)
- **EDA Tools:** Cadence Virtuoso, MATLAB, Ansys Electromagnetic Suite, Keysight Advanced Design System (ADS), Cadence Tools, Ansys High Frequency Structure Simulator (HFSS)
- **Familiar Tools:** Simulink, LabVIEW, Multisim, LTspice,AMD Vivado
- **Languages:** English, Telugu, Hindi

Relevant Courses

- Analog and Mixed-Signal IC Design (**Cadence Virtuoso**)
- Digital VLSI Design (**AMD Vivado**)
- Phase-Locked Loops (PLL) (**NPTEL**)
- Reconfigurable System Design (**Verilog HDL**, FPGA)
- Microwave & RF Circuit Design (**Keysight ADS**, **HFSS**)
- Radar Systems & Signal Processing (**MATLAB**)
- Advanced Digital Signal Processing & Optimization
- Instrumentation & Signal Conditioning
- MEMS Design and Fabrication

Projects

Analog IC Design & Simulation (July 2025 - present)

Cadence Virtuoso

- Designed and implemented a 2-stage Operational Transconductance Amplifier (OTA) and a Bandgap Reference (BGR) circuit using **Cadence Virtuoso** with the **SCL and UMC 180nm technology nodes**, gaining hands-on experience in schematic design, simulation, and layout.
- Designed a Rail-to-Rail (gm compensated over input common mode range)Input differential-ended folded cascode Operational Transconductance Amplifier (OTA), achieving above 70 dB gain and 60deg Phase Margin. Implemented a Common Mode Feedback (CMFB) method to maintain the output common-mode voltage.
- Designed a Gilbert Cell and Working towards PLL system level design.
- Mtech Project around building Delta Sigma ADC block for Capacitive Sensing.

Capacitive Change Sensing System with Arduino Acquisition (July 2025)

- Developed a hardware project utilizing a 556 timer and Sallen-Key filter to sense capacitive changes, where the 556 timer generated a time period inversely proportional to capacitance, enabling precise measurement. Incorporated Arduino for data acquisition and analysis.
- Designed and fabricated a custom **PCB** for the sensing circuitry.

Low-Noise Amplifier (LNA) Design

- Designed and simulated an LNA for RF front-end applications in Keysight ADS to design and optimize High-Frequency Low Noise Amplifiers (LNAs) ensuring unconditional stability and achieved sub-2 dB Noise Figure with 15-20 dB gain (2023-2024).

Designing of 3-Tap FIR Filter

- Mini Project in Reconfigurable System Design CourseWork_2023: Designed and implemented a finite impulse response (FIR) filter using Verilog HDL and Xilinx Vivado software.

FMCW Radar Signal Processing Algorithm

- Developed and implemented an FMCW radar signal processing algorithm using MATLAB (2023-2024).

Smart Wireless Charging with Charge Monitoring

- In this project the battery is charged wirelessly by using transmitting and receiving coils. The battery percentage is monitored and displayed on LCD. The setup will turn on automatically with the presence of the vehicle and get charged. Used the following: Arduino Uno, IR Transmitters & Receivers, Li-on Battery, Bridge Rectifier, Voltage Regulator, Ultrasonic Sensor.

Balancing Robot Using Arduino

- Used Arduino Nano R3, Stepper Motors & Sensors, Arduino IDE.

Internships

BHEL Hyderabad **2019**

Intern *Hyderabad, Telangana*

- Gained practical exposure in the design and fabrication processes involved in Electrical Machines during a hands-on training program.

SkillVertex, Bangalore **2021**

Training and Internship *Bangalore, Karnataka*

- Completed specialized training on Hybrid and Electric Vehicles, covering their evolution, design, and future trends.
- Worked on documentation for Battery Management Systems and presented a detailed analysis on Advanced Driver Assistance Systems (ADAS).

Teaching Experience

Analog Electronics Lab Instructor **Jul 2025**

Teaching Assistant (Undergraduate Lab) *NIT Rourkela*

- Conducted laboratory sessions for undergraduate students on key analog design topics including MOS characterization, Single-Stage Amplifiers, Current Mirrors, Differential Amplifiers, Two-Stage Operational Amplifiers, and Analog Layout Design.
- Provided hands-on guidance and support for Cadence-based circuit design, simulation, and analysis.

Ignore this section this is for ATS

Analog IC Designer, Mixed-Signal Designer, RFIC Designer, RF Engineer. LNA, VCO, PLL, Mixer, ADC (sigma delta), op-amp, OTA, bandgap reference (BGR), impedance matching, differential design, switched-capacitor, CMFB, current mirrors. Cadence Virtuoso ADE/AMS, Keysight ADS, Ansys HFSS, MATLAB, LTspice. VNA, spectrum analyzer, oscilloscope, NF (noise figure), IIP3, P1dB, phase noise, S-parameters (S11/S21), ENOB, gain, bandwidth, phase margin, jitter. CMOS, RF CMOS, BiCMOS, 180nm. Layout, parasitic extraction, DRC/LVS, tapeout, post-layout simulation, schematic design.