ASSIGNMENT-3

AIM AND OBJECTIVE

- The topic of assignment is to do the full ASIC flow of one bit adder,4-bit and 16-bit carrylook-ahead adder and ripple adder.

INTRODUCTION

- This report consists of areas , powers and other statistics and comparisions of adder,4-bit and 16-bit carrylook-ahead adder and ripple adder.
- This report uses data from softwares like XILINX(to generate timing diagrams and RTL schematics,area,delay.power),CADENCE tools like GENUS(to generate area,power,netlist files etc)and INNOVUS(to have physical design along with other statistics like timing reports ,area, optimized power etc;)

PROCEDURE(XILINX)

- The first part of the assignment is to write verilog codes with test benches using XILINX ISE.
- After writing the codes,we can use behavioral simulation to get the gate diagram in XILINX
- Then we use the feature of Schematics in which we have an option called RTL schematics to generate the same.
- We can use power analyzer to get the power reports using XILINX
- We can get delay and area in Design summary after setting current file as top module

PROCEDURE(GENUS)

- In GENUS as it has been written before,we generate timing diagrams using a file named rc_script.tcl.
- In that file we give the respective verilog file as an input for generation of timing diagrams,power,area,netlist files etc;
- We run “genus -f rc_script.tcl -gui” command in the terminal to generate the above mentioned files

PROCEDURE(INNOVUS)

- After generating the netlist files from genus,we give them as an input for a file named Default.globals as a first step in INNOVUS.
- Now we source this Default.global file to get a rough layout on the INNOVUS gui.
- After that we go to Floor plan to select “specify floorplan” to give the appropriate values of width and height of the layout.

PROCEDURE(INNOVUS contd)

- Then we go to Power and select “connect global nets”to give the connection to VDD and VSS mentioned in the Default.globals file. (Generally VSS=0;VDD=0.9V)
- Then we add rings(top,bottom:Metal(9);left,right:Metal(8),offset:0)and stripes(num of sets:3 and layer:Metal(1)) to the layout.
- Then we route the layout by selecting “Special Route” and adding the net.

PROCEDURE(INNOVUS contd)

- After we have routed the layout we choose tools as to set the layout in “analysis mode” for calculation of area,power and other statistical analysis.
- Then we place the standard cell with input/output pins and jtag.
- Then we nano-route the layout for more optimization
- We then see area and power by “report_area” and “report_power” respectively .
- We then generate timing diagrams in different situations like pre-cts,post-cts.post-route etc;
- We can also optimize the circuit in these situations and observe the statistics
- We can get whole summary report using “ report” option in “file” menu.

FOLLOWING SLIDES WILL HAVE VARIOUS OBSERVATIONS FROM ALL SOFTWARES(XILINX,CADENCE(GENUS, INNOVUS))

OBSERVATIONS : DIGITAL BLOCK	POWER		AREA		DELAY	
	GENUS (nW)	INNOVUS (mW)	GENUS (um^2)	INNOVUS (um^2)	GENUS(ps)	XILINX(ns) gate+net
ONE_BIT RIPPLE	691.602	0.0003928	19.679	19.6794	356	5.776+4.887
4_BIT RIPPLE	3777.270	0.002176	78.718	78.7176	1109	8.959+6.723
4_BIT_LOOKAHEAD	4338.693	0.003049	92.342	92.3418	999	8.920+6.723
16_BIT_RIPPLE	13971.304	0.01069	314.870	314.8704	4108	21.690+14.067
16_BIT_LOOKAHEAD	17406.160	0.01367	369.367	369.3672	3587	21.378+14.067

TYPE OF ADDER	AREA		POWER		DELAY	
	RIPPLE	LOOKAHEAD	RIPPLE	LOOKAHEAD	RIPPLE	LOOKAHEAD
4_BIT ADDER	78.7186	92.3418	0.002176	0.003049	1109	999
16_BIT ADDER	314.8704	369.3672	0.01069	0.01367	4108	3587

DISSCUSSIONS

- There are differences between the statistics generated by GENUS and INNOVUS.
- The values of area generated by INNOVUS are rounded off to get the area values generated by GENUS.
- The values of leakage power are very close and similar in case of GENUS & INNOVUS
- This difference is because , INNOVUS gives more optimized and better values than GENUS which only gives a rough approximation of the values of power and area

CONCLUSIONS

- This assignment gives us the different practical statistics of area ,power etc and also gives the oppurtunity to compare the statistics and observe/learn from them
- It also gives us the ideaology of practical manufacturing of the gates/MUX etc;
- We can practically see the values of area,power,timing diagram and physical layout of gates/circuits learnt in the class.

SPECIFIC CONCLUSIONS

- Ripple adder and Look ahead adder have their own pros and cons.
- Their usage entirely depends upon the requirement of the situation
- In look ahead adder, delay time is less though power is more as there are more nets and gates.
- So it depends upon us where we want to optimize.

REFRENCES

- https://drive.google.com/drive/folders/1DkpjyA1jlUY42pv-zL3H0AUn_PxH4NKe
- https://youtu.be/jEsLRqFlW8k?list=PLWE6HLkxLyyJezx1YaFTgoNtrSiIE0dx
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