Tejaswini Panchadarla

Contact Information

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Education

Year	Degree	Institution	CGPA
2025	M.Tech, Embedded Controls & Software	**IIT Kharagpur**	9.53 / 10
2020	B.Tech, Electronics & Communication Engineering	Andhra University	8.65 / 10

Professional Experience

Lead AI Engineer, Tektronix India Pvt Ltd, Bangalore — May 2024 – Present

- Led **AI enablement** for MSO 5/6-Series oscilloscopes: deployed PyTorch→ONNX→TensorRT pipeline for real-time waveform anomaly tagging (4.3× faster, $< 10\,\mu$s acquisition stall).
- Architected Linux 5.15 RT BSP on quad-core Cortex-A72 + dual Cortex-M7 SoC; cold-boot cut by 28 %, DMA underruns eliminated at 2 Gs/s via lock-free ring buffers.
- Designed C++17 **plug-in SDK** exposing quantization, pruning, and live model hot-swap to Python; feature prototyping time down by 40 % for FW teams.
- Authored 80-page "Oscilloscope AI SDK" and produced tutorial videos adopted by 20+ internal and customer engineering groups.
- Cross-functional debug with FPGA, analog and SI teams using ftrace, perf and VTune to resolve DDR4 timing and cache-miss hotspots, unblocking release two weeks early.

Senior Software Engineer, Wipro Technologies Ltd — Sep 2020 – Jul 2023

- Optimised multi-modal CV demo on **Snapdragon Compute Dev Kit**: WinML graph rewrites + FP16 quantisation cut end-to-end latency by **45 %** while preserving accuracy.
- Implemented Bayesian autotuner sweeping GPUNPU tile sizes; ResNet50 throughput improved **2.1**× and methodology incorporated into internal optimisation toolkit.
- Refactored SM8250 camera, IMU and CSI-2 drivers to reduce DMA bandwidth **30 %**; enabled sustained 800 fps capture with zero frame drops.
- Deployed Jenkins + Azure CI with latencyaccuracy trend dashboards; regression triage time shrank from 3 days to **4 hours**.

Instrumentation Intern, *NTPC*, Visakhapatnam — **Jan 2019**

- Automated Modbus historian migration to ARM-based edge controllers, reducing turbine downtime analysis by 60 %.

Key Projects

Edge SHM & Defect Detection Platform (M.Tech Thesis) — *2023 – 2025*

- Pipeline: sensor fusion (Kalman) → PCA → Isolation Forest; **YOLOv8 + SAHI** crack localiser.
- Ported to **Windows on Snapdragon** dev kit; optimized with `SNPE` FP16 and WinML graph transforms (6 ms/frame, 95 % mAP@0.5).
- Implemented power-aware scheduler switching between CPU bigLITTLE cores and NPU based on thermal budget, extending on-device operation by 20 %.

Technical Skills

Languages: C (11 yrs), C++20 (6 yrs), Python 3 (7 yrs), BatchPowerShell, Bash
AI Toolchains: Qualcomm SNPE, Windows WinMLDirectML, ONNX Runtime, PyTorch, TensorFlow-Lite
Optimization: Hexagon DSP intrinsics, NEONSVE, CUDA, Vulkan Compute, ETWWPA, VTune
Platforms: Windows 11 on ARM, Linux 5.x, Yocto, RT-PREEMPT
Dev Tools: Visual Studio, gdbkgdb, perf, Git, Gerrit, Azure DevOps, Jenkins, Docker
Concepts: Quantization, pruning, tensor sparsity, memory tiling, heterogeneous scheduling, KPI dashboarding

Achievements

- Department Topper (M.Tech, IIT Kharagpur).
- Grand Prize — Intel AI Hackathon @ IEEE INDICON 2025.
- Silver — IIT Kharagpur General Championship Chess Tournament.