Probing HDL based on Java + Scala + Polyglot Compiler System/s JLANG/LLVM/JikesRVM/KVM/Metascala VM-Scala VM/JI Prolog/JHDL/Interactive State Machine + HOL-Isabelle Theorem Prover [ITP]/Coq Theorem Prover [CTP] + Scallina/Scala Code Generator Tool.

[JVM Languages → HDL Important Tools → Driving Next Generation IoT Revolution]

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[I] Main Idea + Inspiration + Introduction :

Towards Advanced Testing of Complex FPGAs & Related Informatics in Space + Medicine + Telecoms + HPC Systems R&D Applications → A Simple Suggestion.

[II] R&D Informatics Framework to TEST Complex FPGAs - > Different S&T Domains

IT is very EASY to derive your own JVM based FPGA Testing Frameworks Using Java & Scala with an excellent basis for IoT Heterogeneous Environment/s. Please follow our Notes.
Do you need more information ? - Just our TITLE is enough.

[III] Useful + Important References :

[a] https://github.com/tejdnk-2019-ShortNotes

[IV] Acknowledgment/s : Sincere Thanks + Non-Profit R&D +Inspire Others Always.

[THE END]