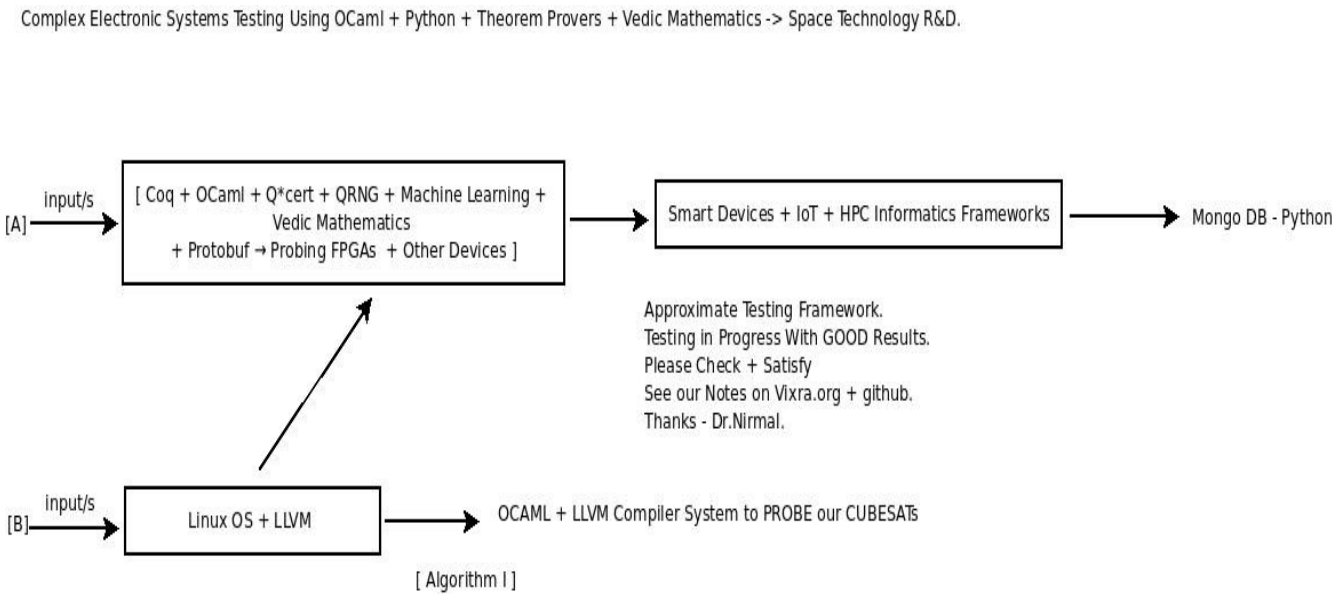
"RTL Hardware Design in OCaml/HardCaml" Using Vedic Mathematics + Theorem Proving + QRNG-Python + Python-HDL + Python Tools → Advancing Space Technology Multi-Disciplinary Informatics R&D w.r.t Next Generation CUBESATs.

[Coq + OCaml + Q*cert + QRNG + Machine Learning + Mathematics + Protobuf → Probing FPGAs + Other Devices]

Nirmal – Informatics R&D – USA/UK/Israel/France/BRICS Group of Nations.
Current Member – ante INST UTD Dallas TX USA.
Contact_info – hmfg2014@gmail.com

[I] Main Idea + Inspiration + Introduction :

"Hardcaml is an embedded DSL for designing and simulating hardware in OCaml. Generic hardware designs are easily expressed using features such as higher order functions, lists, maps etc. A built in simulator allows designs to be simulated within Hardcaml. Designs are converted to either Verilog or VHDL to interact with standard back end tooling." → **[Testing + Verification of Algorithms]**



[Figure I – Simple Algorithm I – CUBESATs Testing Using OCaml + Python]

[II] Useful + Important References :

[a] https://github.com/tejdnk-2019-ShortNotes

[III] Acknowledgment/s : Sincere Thanks & Non-Profit R&D. Inspiring Others is GOOD.

[THE END]