Monitoring Experimental Tool Chain for Migen-RubyRTL IP interchange Using Ruby + Python + Dr.Racket/Redex -> A Novel Algorithm to Verify FPGA based Computing & Abstracting Abstract Machines - A Simple Idea to Generate Next Generation Semiconductor R&D Design Platforms.

Nirmal - Current Member - ante Inst UTD Dallas TX USA.
Contact_info - hmfg2014@gmail.com

[I] Main Idea + Inspiration + Introduction :

Towards a Hardware DSL Ecosystem: RubyRTL and Friends -> [arXiv : 2004.09858v1]

[II] R&D Algorithm I w.r.t Ruby + Python + Dr.Racket :

Dr.Racker/Redex - AAM -> Python -> FPGA Devices & Computing -> to generate NEXT GENERATION R&D ideas.

Please refer to Figure 2 in the above mentioned reference : arXiv:2004.09858v1 -> & try to monitor the FPGA Devices for more informatics.

[III] Acknowledgment/s: Sincere Thanks to all WHO made this happen in my LIFE.Non-Profit R&D.Inspire others always.

[IV] Conclusion/s + Future Perspectives : Dr.Racket/Redex based Novel Algorithm to Probe FPGAs Using AAM.

[V] https://github.com/tejdnk-2019-ShortNotes -> Plenty of Examples for your use - Thanks for your time - Dr.Nirmal.

Results : We are seeing some promising results by re-designing the Algorithms presented in the above mentioned publication.
Rigorous Testing in Progress @ the TIME of Submission.

[THE END]