

To Explore & Test [JI Prolog+ JLang + [jxos/mjvmk]] Usage w.r.t Next Generation Intelligent Embedded Systems [ES] Co-Design involving : [Hardware + Software + Firmware] based on [Smart Devices + IoT + HPC Systems] → To run Space + Medicine + Telecoms Heterogeneous Systems.

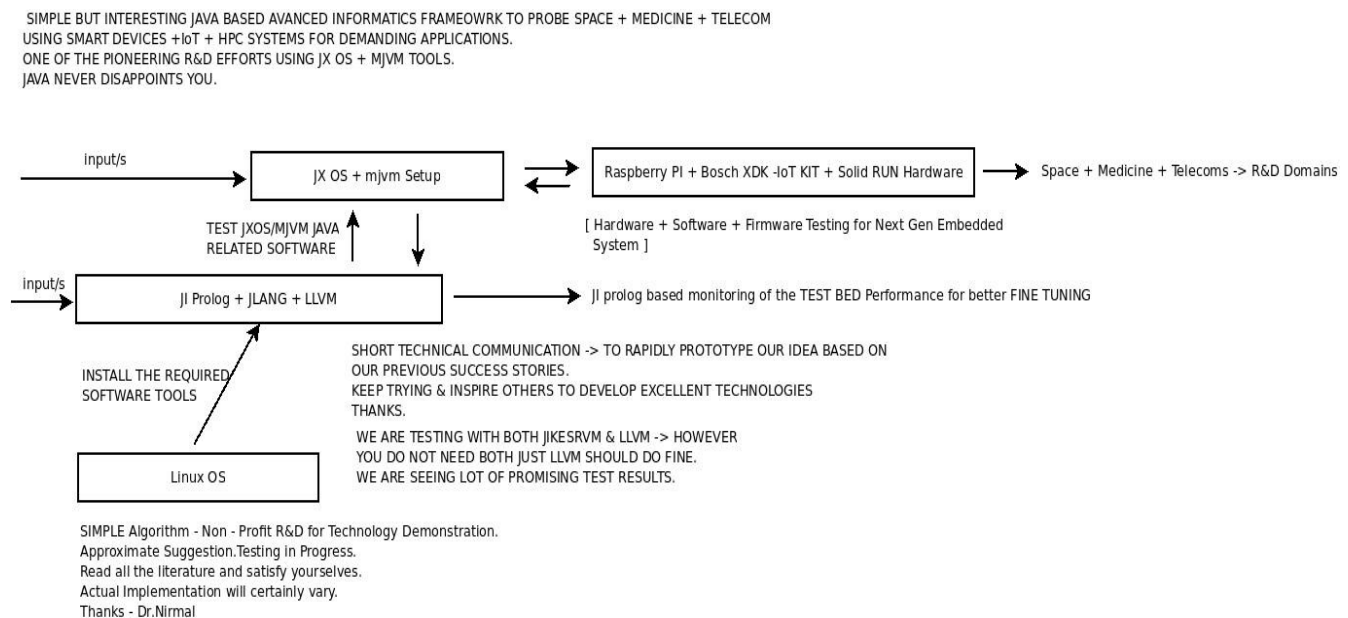
[Exploring Java based TEST BED Architecture for Embedded Systems]

Nirmal – Informatics R&D – USA/UK/Israel/BRICS Group of Nations.

Current Member – ante Inst UTD Dallas TX USA.

Contact_info – hmfg2014@gmail.com

[I] Main Idea + Inspiration + Introduction :



[Figure I – Algorithm I – Our Simple Informatics TEST BED]

JX OS + mjvmk → Seem to be promsing tools in our exploration of ES + Prolog.

[II] References : <https://github.com/tejdnc-2019-ShortNotes> <https://www.cs.cornell.edu/~dzag/other>

[III] Acknowledgment/s : Thanks to all. Non-Profit R&D. Inspiring Others Always is GOOD.

[THE END]