Homework 7

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Part 1: Single stage operational Amplifier

**Objective**:

Design a simple common source amplifier schematic and layout in cadence and run playout and post layout simulation for DC, AC, Noise and Transient response.

**Environment setup:**

1. Connected to server tuxedo.egr.uh.edu
2. Copied the library files from blackboard using winscp
3. Created a new liobrary and attached to an existing technology library NCSU\_TechLib\_ami06

**Schematic Design:**

1. Created schematic design of simple common source amplifier with the given specification in cadence tutorial.

Size of transistors:

M0: width = 19.95u, Length = 600n

M2: width = 9u , Length = 600n

M4: width = 9u, Length = 600n

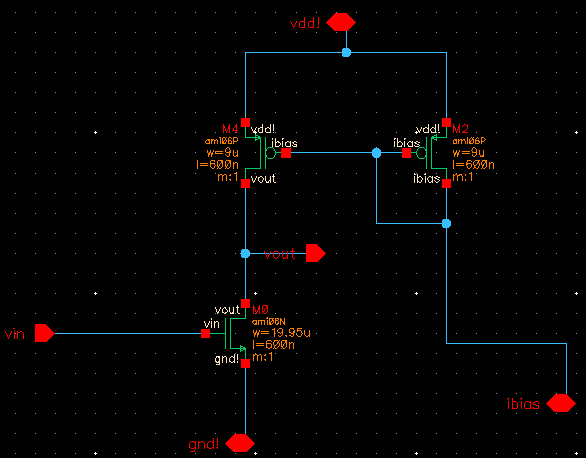


Figure1: schematic of CS amplifier

1. Created symbol from the schematic just created and arranged the pin positions.

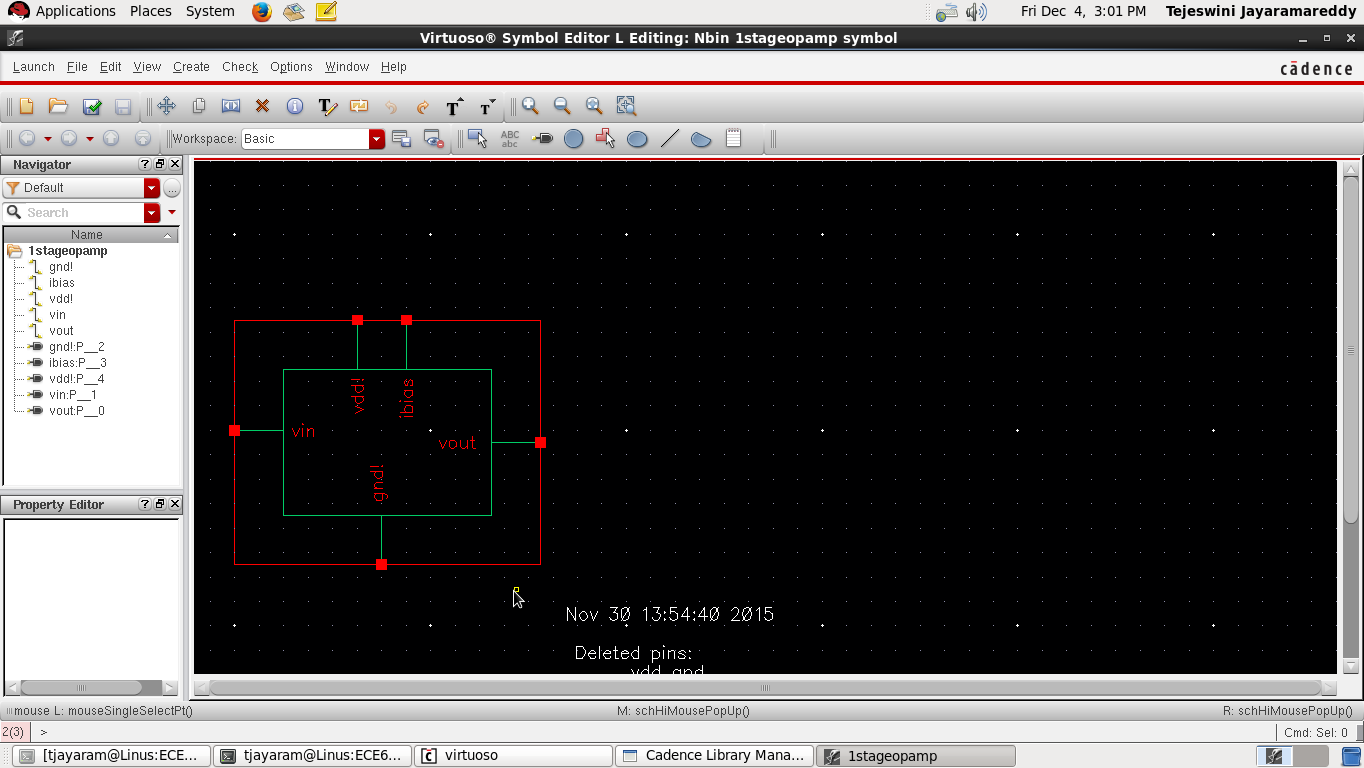


Figure2: symbol of CS amplifier

1. Created a new library and attached to NCSU\_TechLib\_ami06 library. Imported the symbol we created in step b and added additional voltage sources. Final Schematic is as shown below.

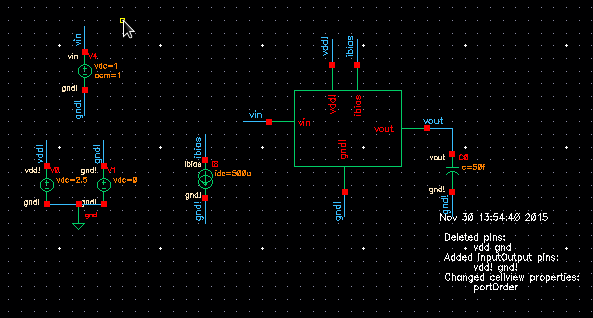


Figure3: Testbench schematic of CS amplifier

1. Launched ADE L and chosen “Simulation/Directory/Host” from setup menu. “ami06N\_flicker.m” and “ami0PN\_flicker.m” are chosen for noise simulation. Simulated Circuit and observed that the simulation is successful.

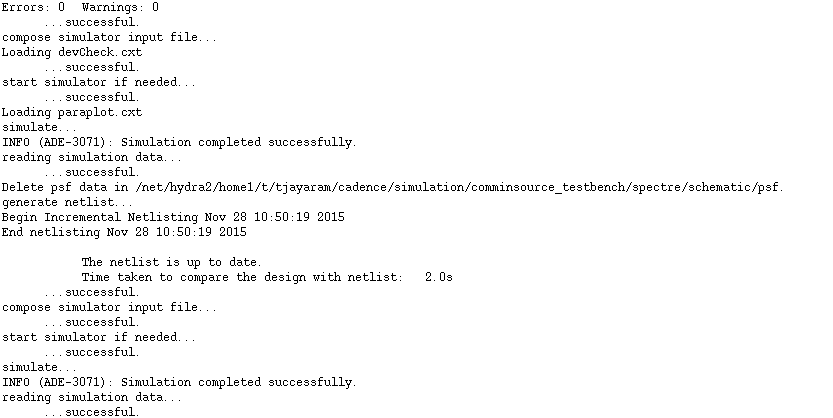


Figure4: Simulation output of CS amplifier

1. Ran DC Analysis and printed DC operating points and node voltages on schematic.

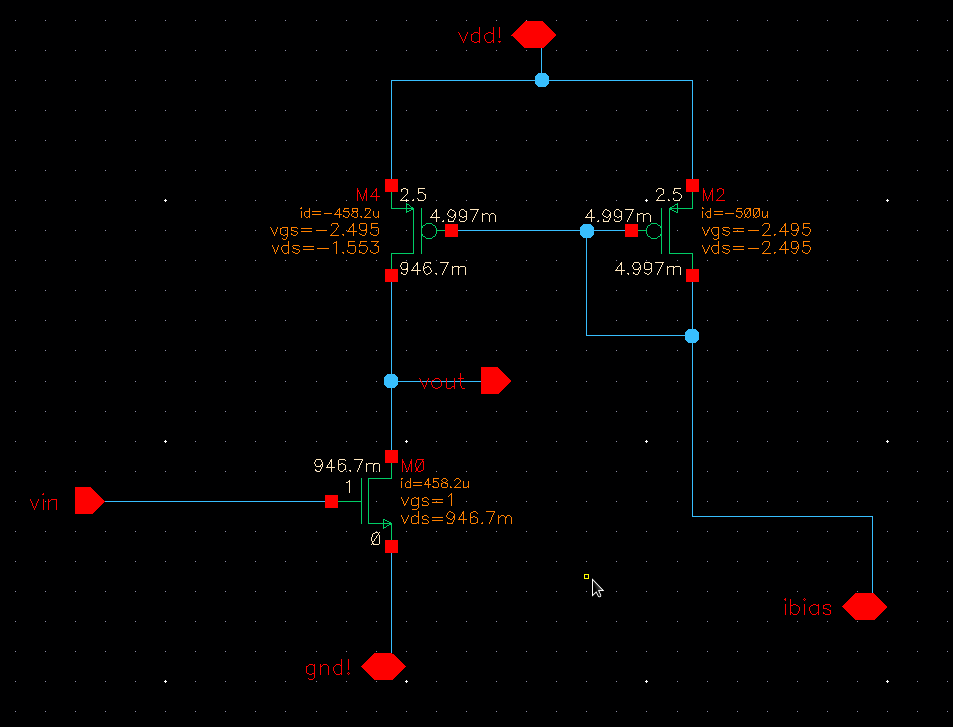


Figure5: CS amplifier schematic with node voltages and DC operating points printed

1. Ran AC analysis and AC Magnitude and Phase.



Figure 6: AC Magnitude Plot of CS amplifier

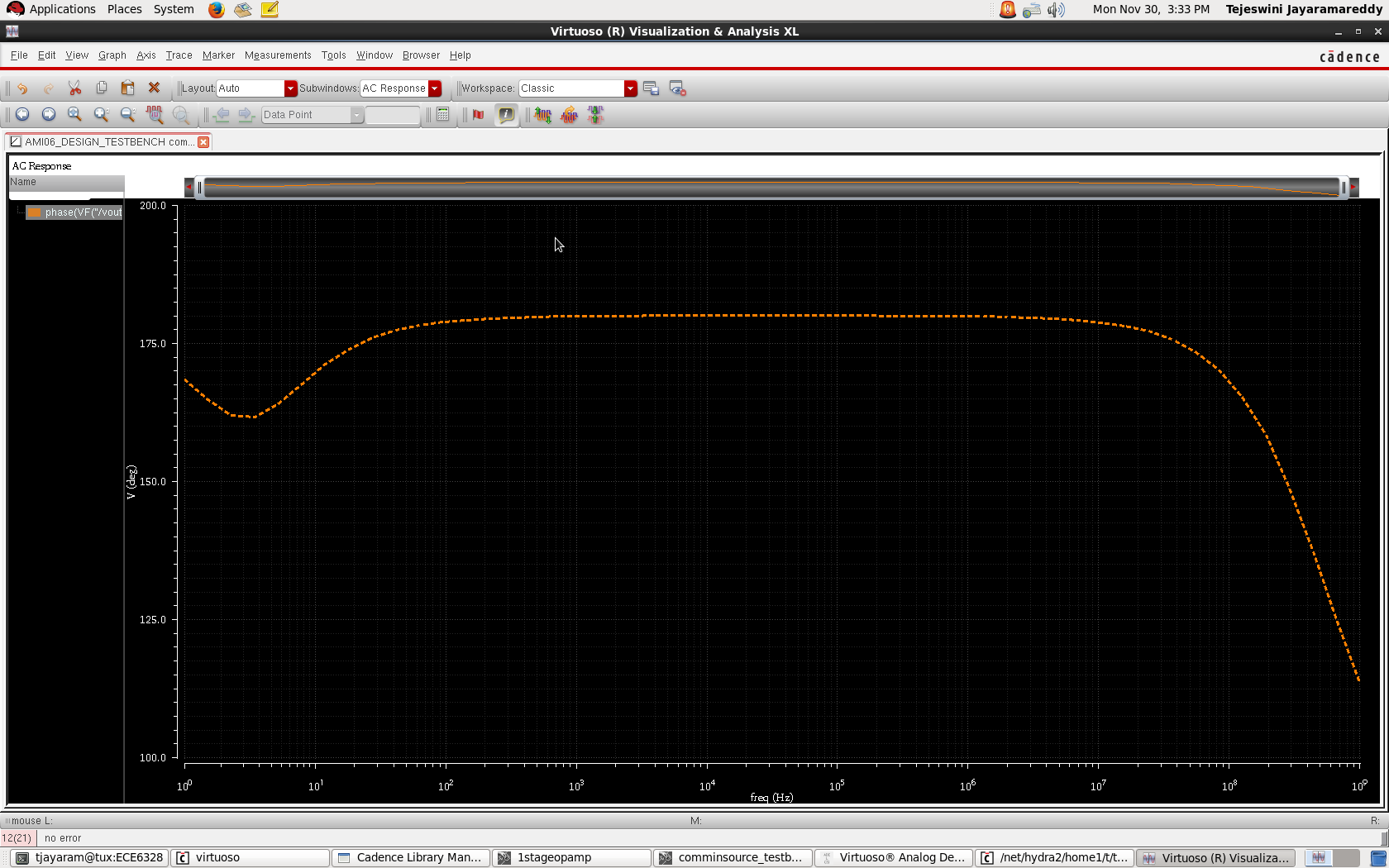


Figure 7: AC phase plot of CS amplifier

1. Plotted Noise response.

Input noise

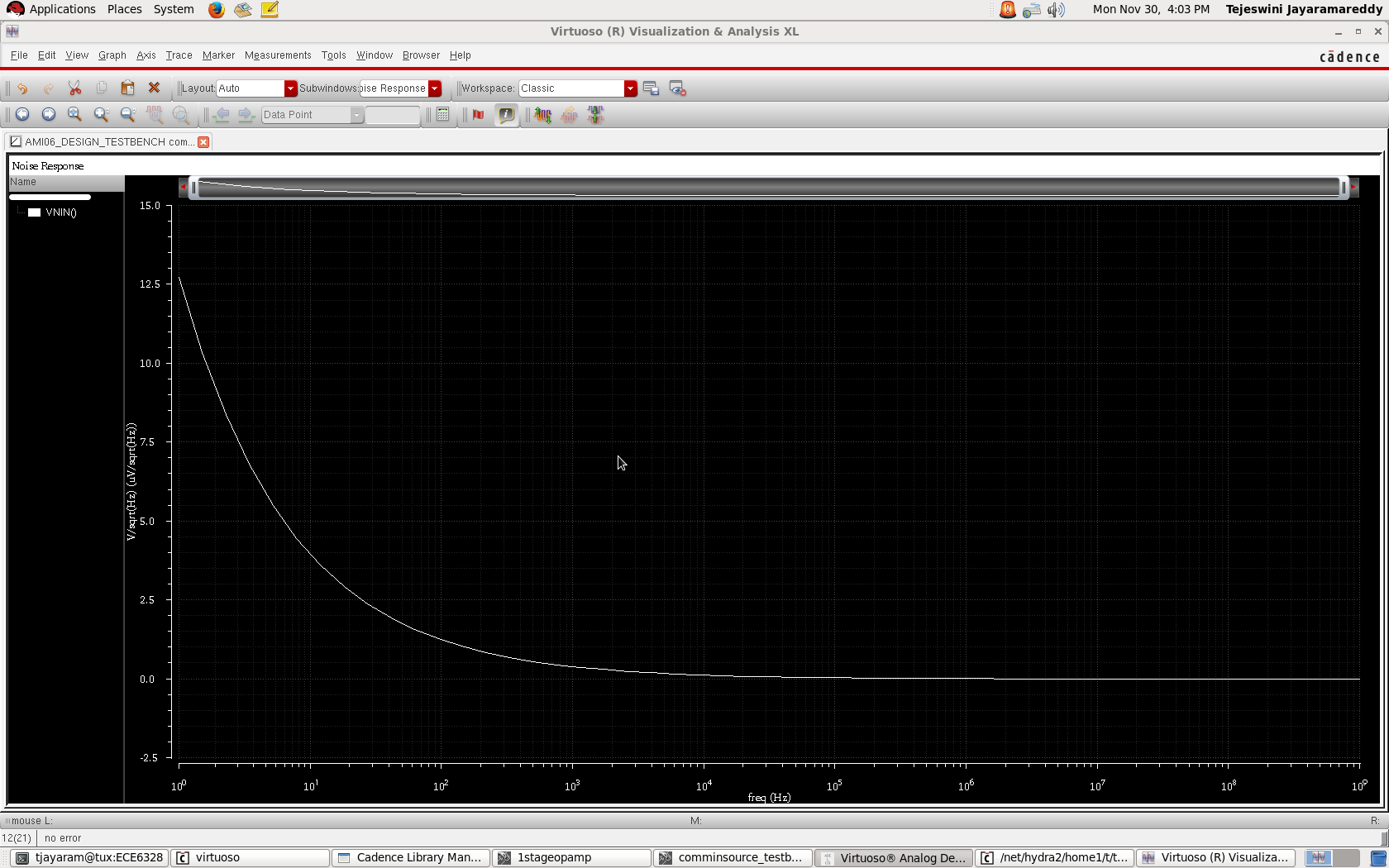


Figure 8: Input noise response plot of CS amplifier

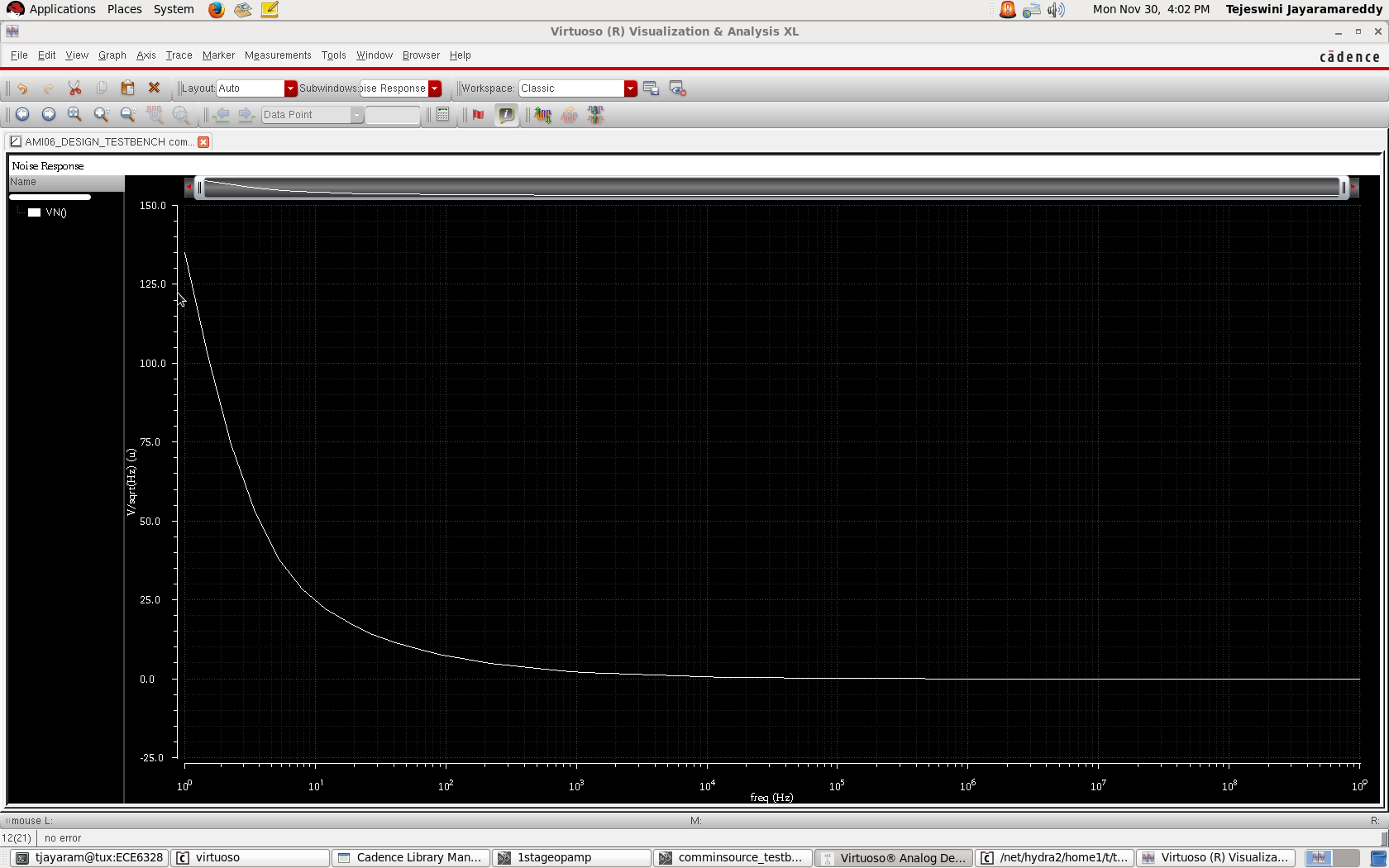


Figure 9: Equivalent output noise response plot of CS amplifier

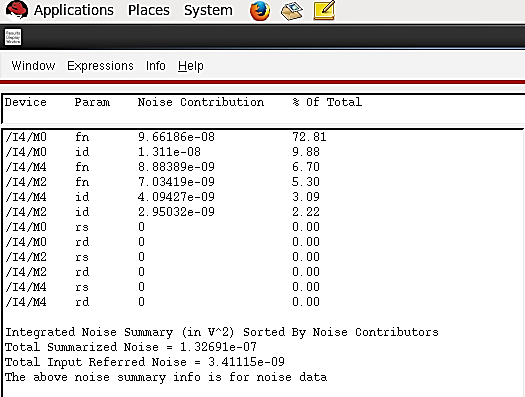
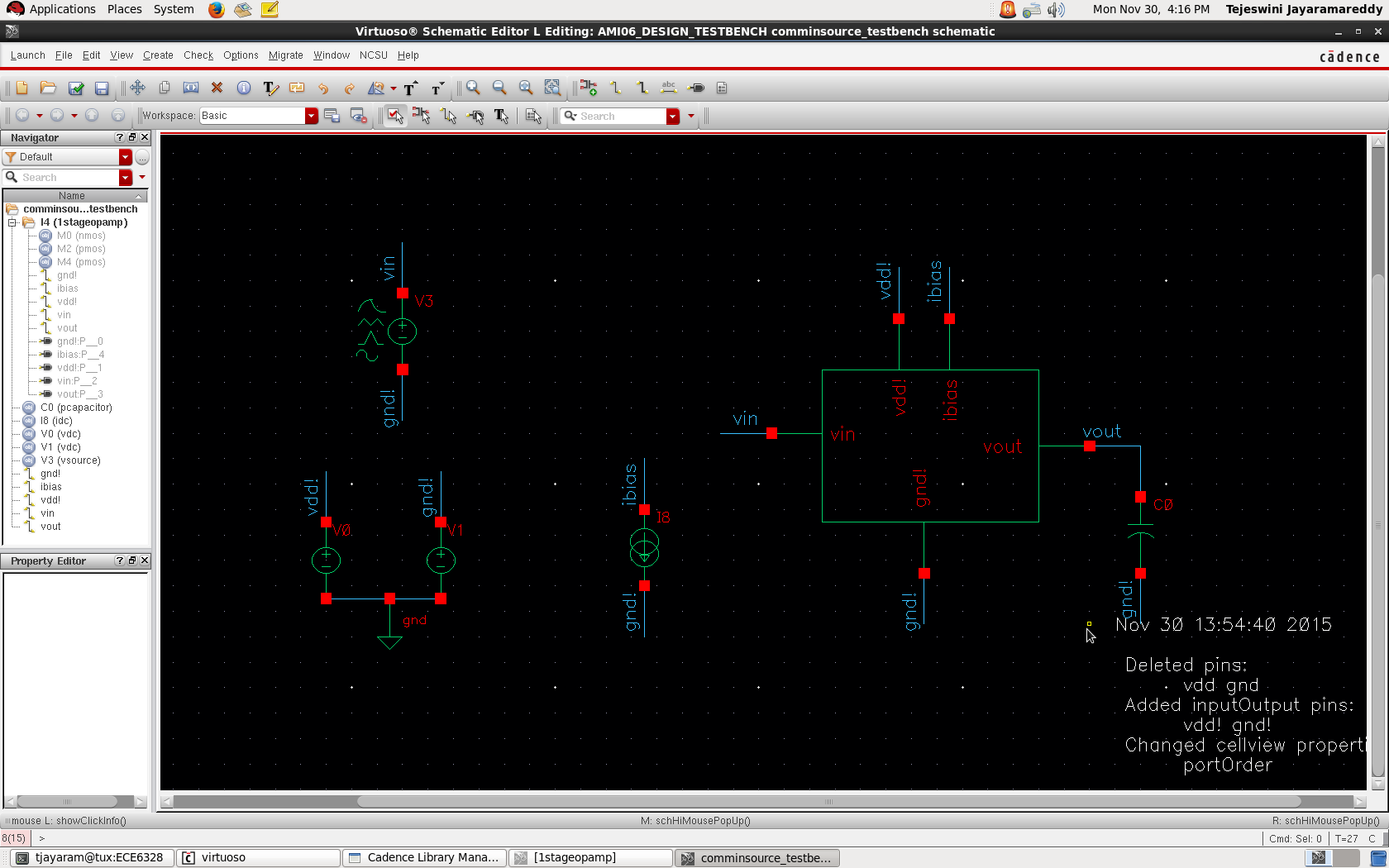


Figure 10. Integrated noise summary of CS amplifier

1. DC voltage is replaced with sinusoidal input signal in testbench schematic and plotted transient response at the input and output signal

Figure 11. Testbench schematic for Transient response

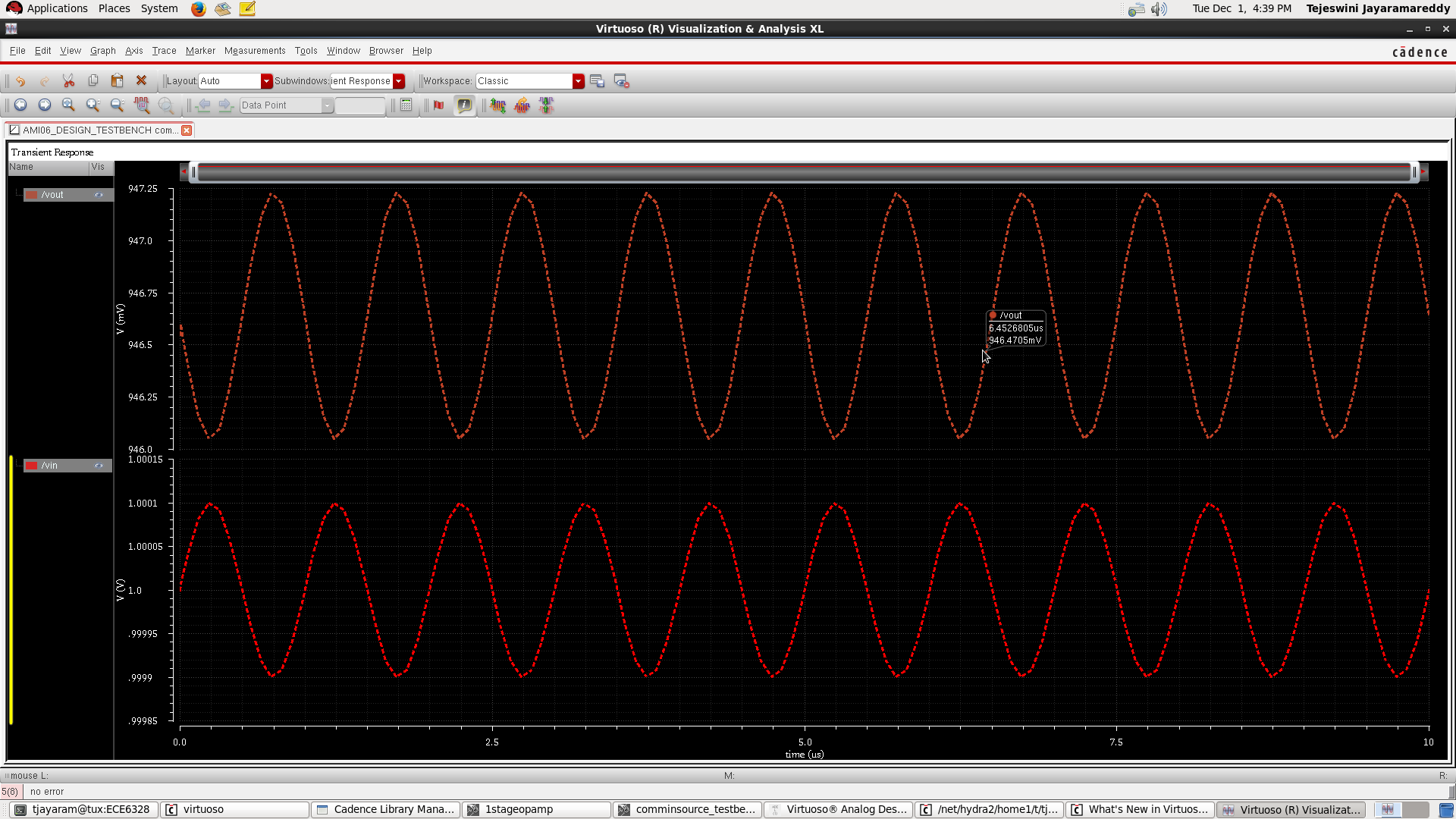


Figure 12. Transient response plot for CS amplifier

**Layout Design:**

1. Layout is designed for CS amplifier with one nmos and 2 pmos transistors.

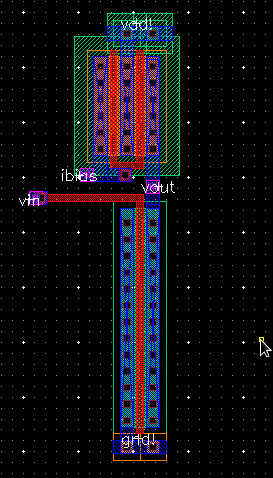


Figure 13: Layout design of CS amplifier

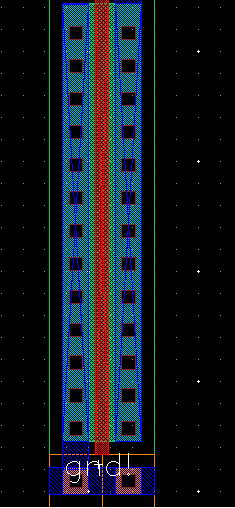


Figure 14: nmos portion of CS amplifier layout

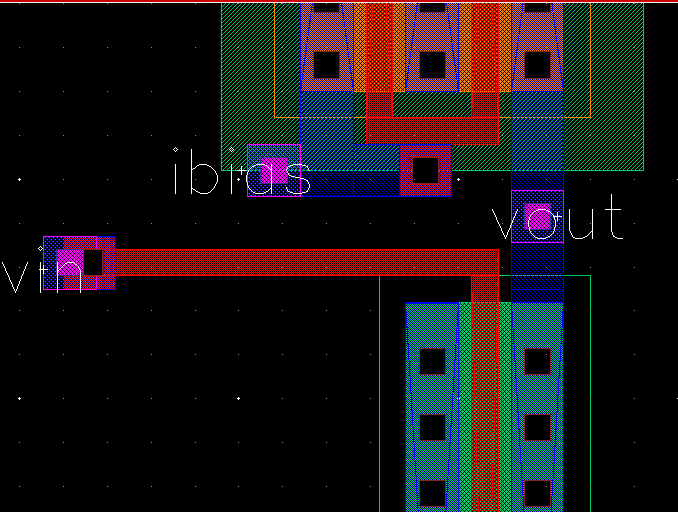


Figure 15. Portion of CS amplifier layout showing contacts.

In figure 15, four contacts are observed.

Poly-metal1 and metal1-metal2 contacts are used for vin.

Metal1-metal2 contact is used for vout.

Ploy-metal1 and metal1-metal2 contacts are used for ibias.

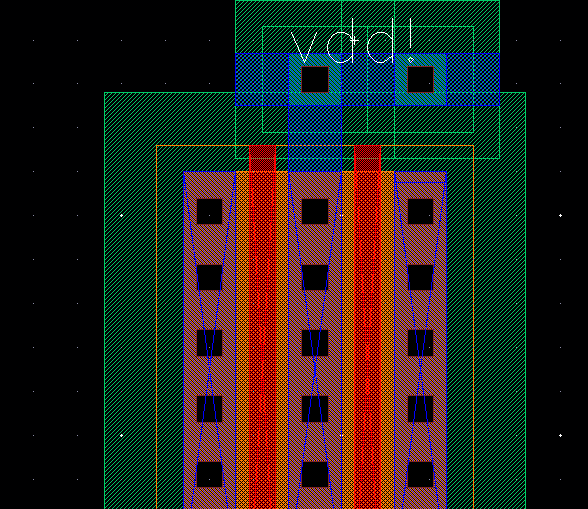


Figure 16. Portion of layout showing vdd and ntap connections

1. Performed Design rule check and found no errors and warnings

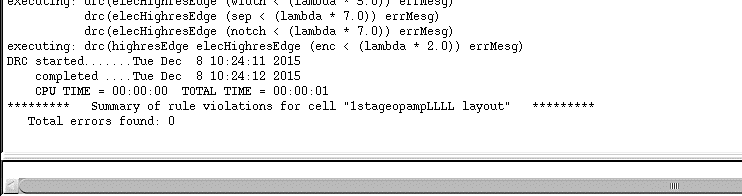


Figure 17. DRC output

1. Extracted layout from the schematic and is as below.

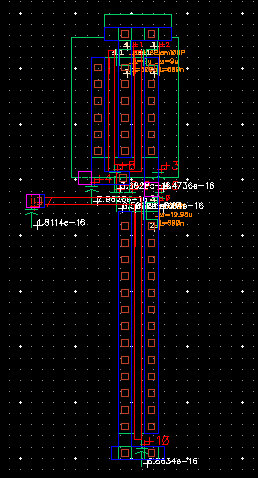


Figure. 18 CS amplifier layout extracted

1. Performed layout verses schematic check comparing extracted schematic in step c and analog schematic created in part a. Found match and LVS success message is shown below.

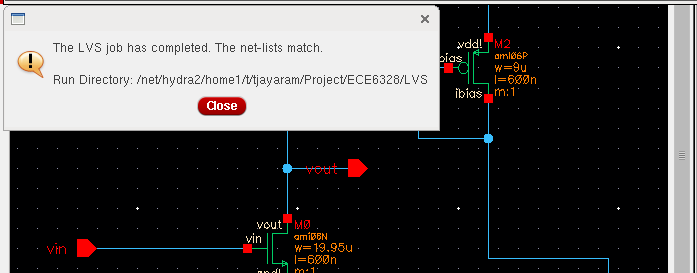
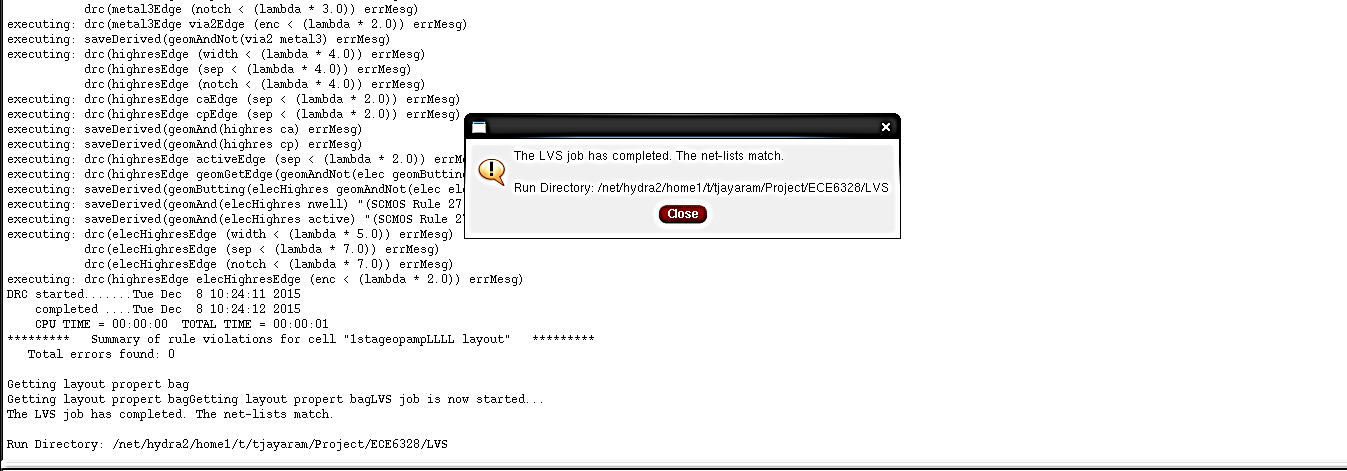


Figure 19. LVS check of CS amplifier



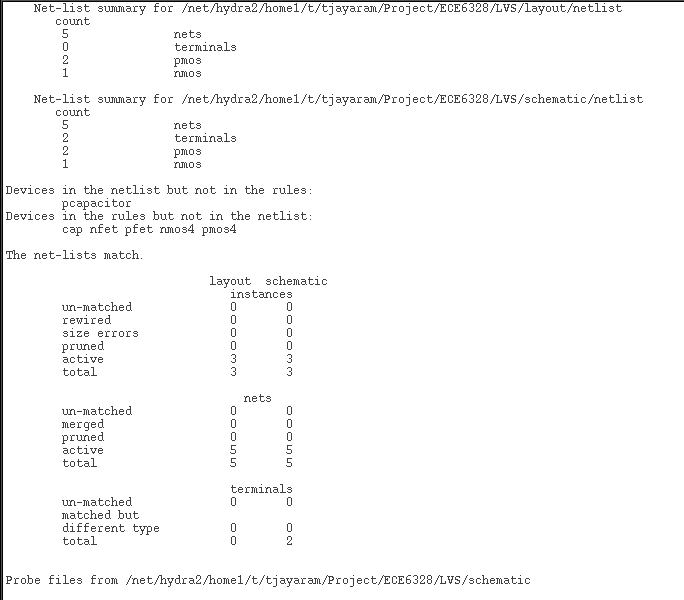


Figure 20. LVS output of CS amplifier

Summary LVS summary is shown above in figure 20.

1. AC Magnitude and Phase are plotted post layout and are found as below in figure 23 and figure 24

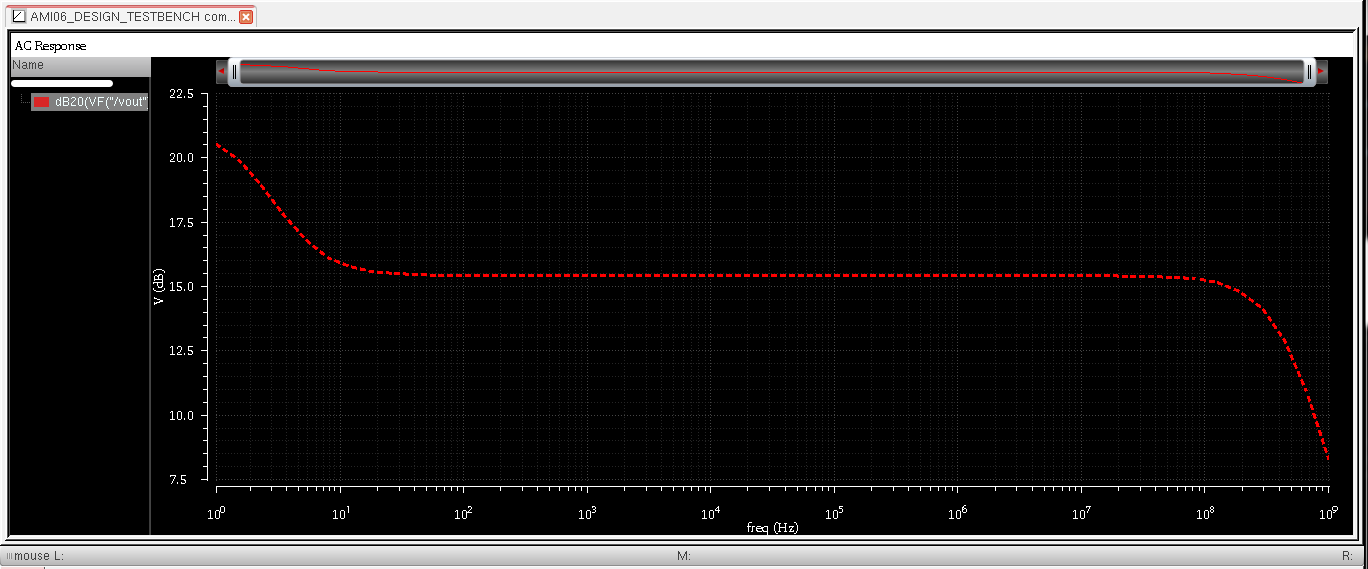


Figure 23. Post layout AC magnitude plot

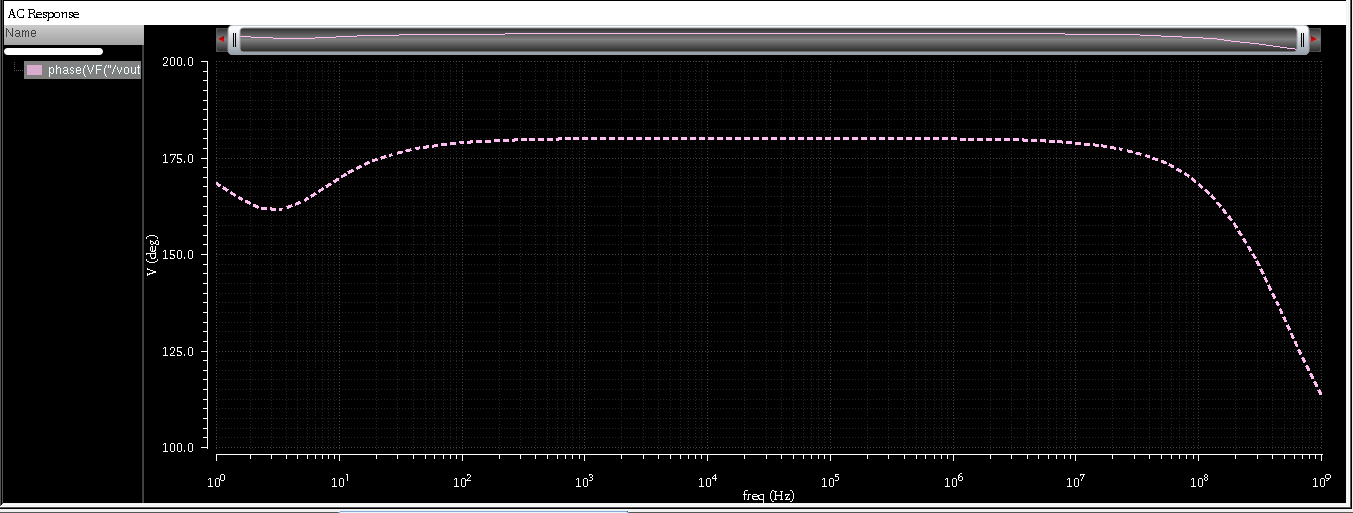


Figure 24. Post layout AC phase plot

1. Post layout, Transient response is plotted and is as shown below in Figure. 25

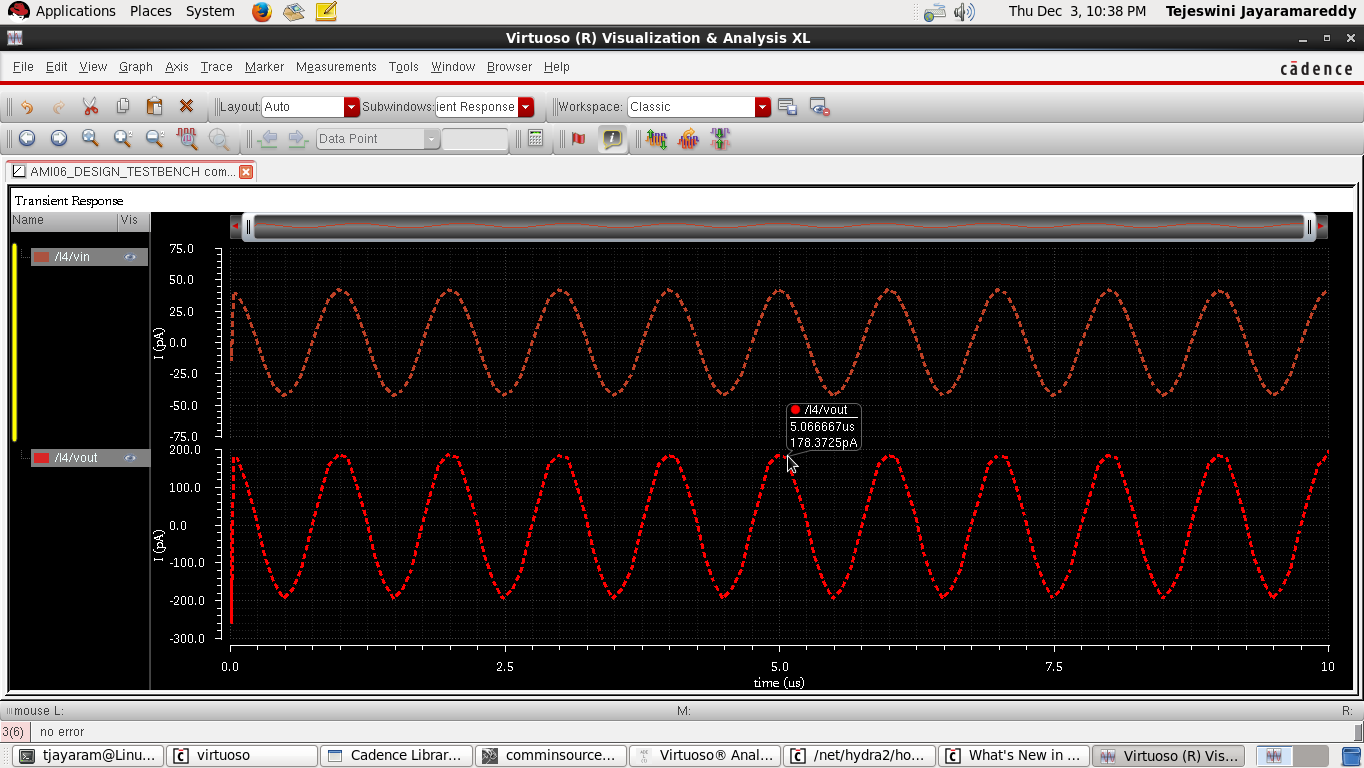


Figure 25. Post layout simulation transient response