**<div id="q4">**

**<p>**

**<strong>- What is cross talk?**

**</strong> <br /> Due to cross coupling capacitance, the switching of the signal in one wire can affect neighbouring wire. This affect is known as cross talk. Cross talk is an important issue because it may lead setup or hold violation. <br />-----**

**</p>**

**</div>**

**<div id="q5">**

**<p>**

**<strong>- How can we avoid cross talk?**

**</strong> <br /> Double spacing => more spacing => less capacitance => less cross talk**

**<br /> Multiple vias => less resistance => less RC delay**

**<br /> Shielding => constant cross coupling capacitance => known value of crosstalk**

**<br /> Buffer insertion => boost the victim strength <br />-----**

**</p>**

**</div>**

**<div id="q6">**

**<p>**

**<strong>- Explain how shielding avoids crosstalk problem?**

**</strong> <br /> High frequency noise (or glitch) is coupled to VSS (or VDD) since shielded layers are connected to either VDD or VSS. Coupling capacitance remains constant with VDD or VSS. <br />-----**

**</p>**

**</div>**

**<div id="q7">**

**<p>**

**<strong>- How buffer can be used in victim line to avoid crosstalk?**

**</strong> <br /> Buffers increase victim signal strength. Buffers break the net length, and therefore victims are more tolerant to coupled signal from aggressor.<br />-----**

**</p>**

**</div>**

**<div id="q8">**

**<p>**

**<strong>- What is skin effect?**

**</strong> <br /> On high frequency current tend to flow on the surface of wire. This phenomenon is called skin effect. <br />-----**

**</p>**

**</div>**

**<div id="q5">**

**<p>**

**<strong>Transfer characteristics of an inverter</strong>**

**</p>**

**</div>**

**<div id="q5-fig1">**

**<img src="AnalogIntegratedCircuits\_CMOSBasics\_fig5.png" alt="Transfer characteristics of an inverter" style="width:475px;height:250px" >**

**</div>**

**</div>**

**<div id="q5-table1">**

**<table>**

**<tr>**

**<th>Region A</th> <th>0 < Vin < Vtn</th> <th>NMOS: off, PMOS: Linear mode</th>**

**</tr>**

**<tr>**

**<th>Region B</th> <th>Vtn < Vin < VDD</th> <th>Blue</th>**

**</tr>**

**<tr>**

**<th>Region C</th> <th>00002</th> <th>Red</th>**

**</tr>**

**<tr>**

**<th>Region D</th> <th>00003</th> <th>Green</th>**

**</tr>**

**<tr>**

**<th>Region E</th> <th>00003</th> <th>Green</th>**

**</tr>**

**</table>**

**</div>**

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**top:74em; }**

**#q5-table1{**

**border-collapse: collapse;**

**border: solid 3px black }**

**#q5-table1 table th {**

**border: solid 1px black;**

**padding: 0rem;**

**text-align: left;**

**font-family: "Times New Roman";**

**font-size: 18px; }**

**<div id="q9">**

**<p>**

**<strong>In CMOS technology, in digital design, why do we design the size of PMOS to be higher than the NMOS? </strong> <br />**

**In PMOS the carriers are holes whose mobility is less than the electrons, the carriers in NMOS. That means PMOS is slower than an NMOS. In CMOS technology, NMOS helps in pulling down the output to ground and PMOS helps in pulling up the output to Vdd. If the sizes of PMOS and NMOS are the same, then PMOS takes long time to charge up the output node. If we use a larger PMOS then there will be more carriers to charge the node and overcome the slow nature of PMOS. Basically we do all this to get equal rise and fall times for the output node.**

**</p>**

**</div>**

**<div id="q10">**

**<p>**

**<strong>Why PMOS and NMOS are sized equally in a Transmission Gates? </strong> <br />**

**In Transmission Gate, PMOS and NMOS aid each other rather competing with each other. That's the reason why we need not size them like in CMOS. In CMOS design we have NMOS and PMOS competing which is the reason we try to size them proportional to their mobility.**

**</p>**

**</div>**

**<div id="q11">**

**<p>**

**<strong>All of us know how an inverter works. What happens when the PMOS and NMOS are interchanged with one another in an inverter? </strong> <br />**

**If the source and drain are also connected properly. It will act as a buffer. But suppose input is logic 1 output will be degraded 1 similarly degraded 0;**

**</p>**

**</div>**

**Give 5 important design techniques you would follow when doing a Layout for digital circuits?**   
a) In digital design, decide the height of standard cells you want to layout. It depends upon how big your transistors will be. Have reasonable width for VDD and GND metal paths. Maintaining uniform height for all the cell is very important since this will help you use place route tool easily and also increase you want to do manual connection of all the blocks it saves on lot of area.  
b) Use one metal in one direction only. This does not apply for metal 1. Say you are using metal 2 to do horizontal connections, and then use metal 3 for vertical connections, metal4 for horizontal, metal 5 vertical etc...  
c) Place as many substrate contacts as possible in the empty spaces of the layout.  
d) Do not use poly over long distances as it has huge resistances unless you have no other choice.  
e) Use fingered transistors as and when you feel necessary.  
f) Try maintaining symmetry in your design. Try to get the design in BIT Sliced manner.

**Why power stripes routed in the top metal layers?**

The resistivity of top metal layers is less and hence less IR drop is seen in power distribution network. If power stripes are routed in lower metal layers this will use good amount of lower routing resources and therefore it can create routing congestion.

**Why do you use alternate routing approach HVH/VHV (Horizontal-Vertical-Horizontal/ Vertical-Horizontal-Vertical)?**

This approach allows routability of the design and better usage of routing resources.

**How delays are characterized using WLM (Wire Load Model)?**

A wire load model attempts to predict the capacitance and resistance of nets in the absence of placement and routing information. The estimated net capacitance and resistance are used for delay calculation. Technology library vendors supply statistical wire load models to support estimation of wire loads based on the number of fan out pins on a net. You can set wire load models manually or automatically. Wire loading models contain all the information required by compiler to estimate interconnect wiring delays.

**Let’s say enough routing resources available, timing is fine, can you increase clock buffers in clock network? If so will there be any impact on other parameters?**

No. You should not increase clock buffers in the clock network. Any increase in clock buffers can increase area, and power. When everything is fine why you want to touch clock tree?

**What are pros/cons of latch/FF (Flip Flop)?**

always @(d) begin

If (clk == 1’b1) begin q <= d;

end

end

D-Flip-flop:

always @(posedge clk) begin

q <= d;

end

Pros and cons of latch and Flip-Flop:

Latch takes less area, consume less power, and facilitate time borrowing or cycle stealing, not friendly with DFT tools

Latches are used in asynchronous systems.

Flip-flop takes more area, consumes more power, allow synchronous logic, friendly with DFT tools

**Tell me some of applications of buffer?**

1) They are used to introduce small delays

2) They are used to eliminate cross talk

3) They are used to support high fan out, e.g.: bufg

**Can you explain what struck at zero means?**These stuck-at problems will appear in ASIC. Sometimes, the nodes will permanently tie to 1 or 0 because of some fault. To avoid that, we need to provide testability in RTL. If it is permanently 1 it is called stuck-at-1. If it is permanently 0 it is called stuck-at-0.

**What is tie-high and tie-low cells and where it is used?**

Tie-high and Tie-Low cells are used to connect the gate of the transistor to either power or ground. In deep sub-micron processes, if the gate is connected to power/ground the transistor might be turned on/off due to power or ground bounce. The suggestion from foundry is to use tie cells for this purpose. These cells are part of standard-cell library.

Ground bounce is usually seen on high density [VLSI](http://en.wikipedia.org/wiki/VLSI) where insufficient precautions have been taken to supply a logic gate with a sufficiently low resistance connection (or sufficiently high [capacitance](http://en.wikipedia.org/wiki/Capacitance)) to ground. In this phenomenon, when the gate is turned on, enough current flows through the [emitter](http://en.wikipedia.org/wiki/Emitter)-collector circuit that the silicon in the immediate vicinity of the emitter is pulled high, sometimes by several volts, thus raising the local ground, as perceived by the transistor, to a value significantly above true ground.

The cells which require Vdd, comes and connect to Tie high... (so tie high is a power supply cell)...while the cells which wants Vss connects itself to Tie-low.

**What are High-Vt and Low-Vt cells?**

Hvt cells are MOS devices with less leakage due to high Vt but they have higher delay than low Vt, whereas the low Vt cells are devices which have less delay but leakage is high. The threshold voltage dictates the transistor switching speed, it matters how much minimum threshold voltage applied can make the transistor switching to active state which results to how fast we can switch the transistor.

**CMOS transistor sizing**

1- If you have N MOSFET in series multiply each transistor by N (ignore transistors in parallel)

2- Scale pull up network by 3